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**Customer: DELL**

**Product Specification**

**Rev. 0**

**(DELL DPN : YRJJ7)**

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**B8: Chongqing BOE Optoelectronics CO., LTD**

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## 1.0 GENERAL DESCRIPTION

### 1.1 Introduction

NV160WUM-N45 is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 16.0 inch diagonally measured active area with WUXGA resolutions (1920 horizontal by 1200 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.7M(round down) (true 8bit) colors and color gamut sRGB100%. The TFT-LCD panel used for this module is a low reflection and higher color type. Therefore, this module is suitable for Notebook PC. The LED driver for back-light driving is built in this model. All input signals are eDP1.4 interface compatible.

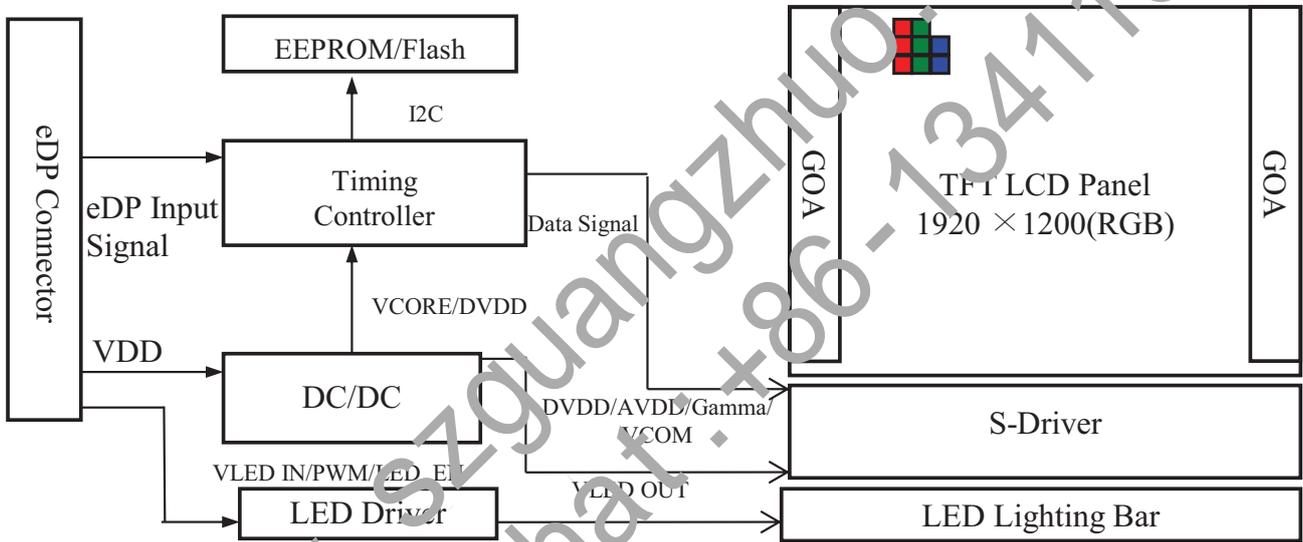


Figure 1. Drive Architecture

### 1.2 Features

- 2 lane eDP interface with 2.7Gbps link rates
- Thin and light weight, Low Power Light
- 16.7M(round down) (true 8bit) color depth, color gamut sRGB100%
- Single LED lighting bar (Bottom side/Horizontal Direction)
- Data enable signal mode
- Green product (RoHS & Halogen free product)
- On board LED driving circuit
- Low driving voltage and low power consumption
- On board EDID chip
- DPCD Version 1.4
- Function : **DBC/BIST/PSR1**
- Adjust backlight brightness with DC

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**1.3 Application**

- Notebook PC (Wide type)

**1.4 General Specification**

The followings are general specifications at the model NV160WUM-N45. (listed in Table 1)

&lt;Table 1. General Specifications&gt;

Parameter	Specification	Unit	Remarks
Active area	344.6784(H) × 215.424(V)	mm	
Number of pixels	1920 (H) × 1200(V)	pixels	
Pixel pitch	179.52(H) × 179.52(V)	um	
Pixel arrangement	RGB Vertical stripe		
Display colors	16.7M(round down) (true 8bit)		
Color gamut	95%min, 100% typ		sRGB
Display mode	Normally Black		
Dimensional outline	349.68±0.1(H)*255.32±0.5(V) (W/PCB)*3.0(Max.), 349.78±0.3 (H) × 255.32±0.5 (V)(W/O PCB) × 5.0 (Max.)	mm	
Weight	460(Max.)	g	
Surface treatment	Fine AG		
Surface hardness	2H		
Back-light	Bottom edge side, 1-LED lighting bar type		Note 1
Power consumption	P <sub>D</sub> : 1.2(Max.)	W	@Mosaic
	P <sub>BL</sub> : 3.2(Max.)	W	@VLED=12V
	P <sub>Total</sub> : 4.4(Max.)	W	@Mosaic

Notes : 1. LED Lighting Bar (66\*LED Array)

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## 2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Absolute Maximum Ratings >

Ta=25+/-2°C

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V <sub>DD</sub>	-0.3	4.0	V	Note 1
eDP input Voltage	V <sub>eDP</sub>	0	2.0	V	
Logic Supply Voltage	V <sub>IN</sub>	V <sub>SS</sub> -0.3	V <sub>DD</sub> +0.3	V	Note 2
Operating Temperature	T <sub>OP</sub>	0	+50	°C	
Storage Temperature	T <sub>ST</sub>	-20	+60	°C	

Notes :

1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.
2. Temperature and relative humidity range are shown in the figure below.  
95 % RH Max. ( 40 °C ≥ Ta) Maximum wet-bulb temperature at 39°C or less.(Ta >40°C)No condensation.

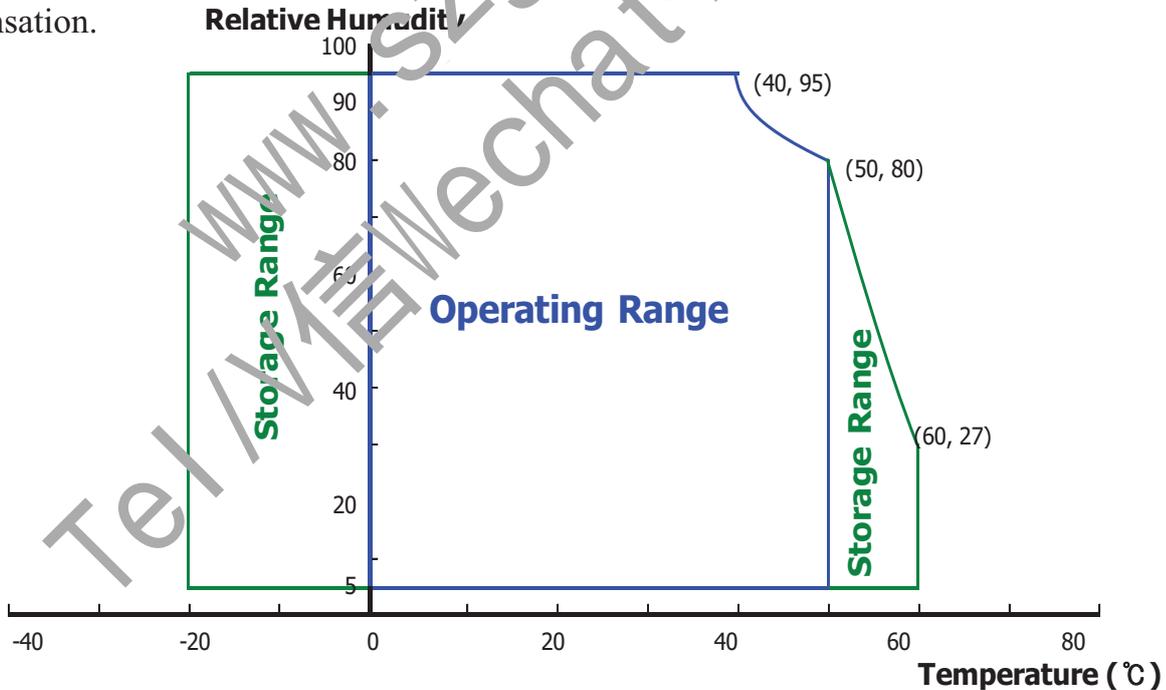


Figure 2. Temperature and Relative Humidity Range

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**3.0 ELECTRICAL SPECIFICATIONS****3.1 Electrical Specifications**

&lt; Table 3. Electrical Specifications &gt;

Ta=25+/-2°C

Parameter		Min.	Typ.	Max.	Unit	Remarks	
Power Supply Voltage	V <sub>DD</sub>	3.0	3.3	3.6	V	Note 1	
Permissible Input Ripple Voltage	V <sub>RF</sub>	-10% VDD	-	+10% VDD	V	@ V <sub>DD</sub> = 3.3V, note4	
CABC Control Level	High Level	0.8 VDDIO	-	3.6	V	@V <sub>DDIO</sub> =1.8 Note 5	
	Low Level	0	-	0.15 VDDIO	V		
BIST Control Level	High Level	0.8 VDDIO	-	3.6	V		
	Low Level	0	-	0.15 VDDIO	V		
Power Supply Inrush Current	Inrush	-	-	2	A	Note3	
Power Supply Current	Mosaic	I <sub>DD</sub>	-	-	400	mA	
	Red		-	-	400	mA	
	Green		-	-	400	mA	
	Blue		-	-	400	mA	
Power Consumption	Mosaic	P <sub>M</sub>	-	-	1.2	W	
	Red	P <sub>R</sub>	-	-	1.2	W	
	Green	P <sub>G</sub>	-	-	1.2	W	
	Blue	P <sub>B</sub>	-	-	1.2	W	
	BLU	P <sub>BL</sub>	-	3.1	3.2	W	Note 2
	Total	P <sub>Total</sub>	-	3.1	4.4	W	Note 1

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### 3.0 ELECTRICAL SPECIFICATIONS

#### 3.1 Electrical Specifications

Notes :

- The supply voltage is measured and specified at the interface connector of LCM.  
The current draw and power consumption specified is for 3.3V at 25 °C.(Typ. value for reference)
  - Mosaic pattern 8\*8
  - R/G/B patterns



(a) (b)  
Figure 3. Power Measure Patterns

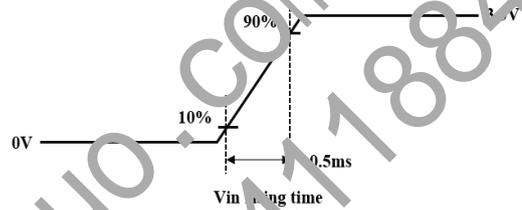


Figure 4. Inrush Measure Condition

- Calculated value for reference ( $V_{LED} \times I_{LED}$ ) , The power consumption with LED Driver are under the  $V_{LED} = 12.0V$  , 25°C, PWM Duty 100% .
- Measure condition (Figure 4)
- Input voltage range:3.0~3.6V.Test condition: Oscilloscope bandwidth 20MHz, AC coupling
- CABC&BIST setting

Pin No	Define	Enable	Disable
1	DBC	Pull High	Pull Low/Floating
14	BIST	Pull High	Pull Low/Floating

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**3.2 Backlight Unit**

&lt; Table 4. LED Driving Guideline Specifications &gt;

Ta=25+/-2°C

Parameter		Min.	Typ.	Max.	Unit	Remarks
LED Forward Voltage		$V_F$	-	-	2.9	V
LED Forward Current		$I_F$	-	14.0	-	mA
LED Power Input Voltage		$V_{LED}$	5	12	21	V
LED Power Input Current		$I_{LED}$	-	-	267	mA
LED Power Consumption		$P_{LED}$	-	-	3.2	W
Power Supply Voltage for LED Driver Inrush		$I_{LED}$ inrush	-	-	1.5	A
LED Life-Time		N/A	15,000	-	-	Hour $I_F = 14.0mA$ Note 2
EN Control Level	Backlight On	$V_{BL\_EN}$	2.5	-	5.0	V
	Backlight Off		0	-	0.3	V
PWM Control Level	High Level	$V_{BL\_PWM}$	2.5	-	3.6	V
	Low Level		0	-	0.3	V
PWM Control Frequency		$F_{PWM}$	200	-	2,000	Hz
Duty Ratio			5	-	100	%

Notes :

1. The current and power consumption with LED Driver are under the  $V_{LED} = 12.0V$ ,  $25^\circ C$ , PWM Duty 100%.
2. The LED life-time define as the estimated time to 50% degradation of initial luminous.
3. Measure condition (Figure 5).
4. LED\_EN&PWM setting

Pin No	Define	Enable	Disable
22	LED_EN	Pull High	Pull Low/Floating
23	PWM	Pull High	Pull Low/Floating

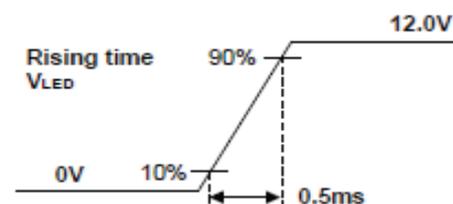


Figure 5. Inrush Measure Condition

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### 3.3 LED Structure

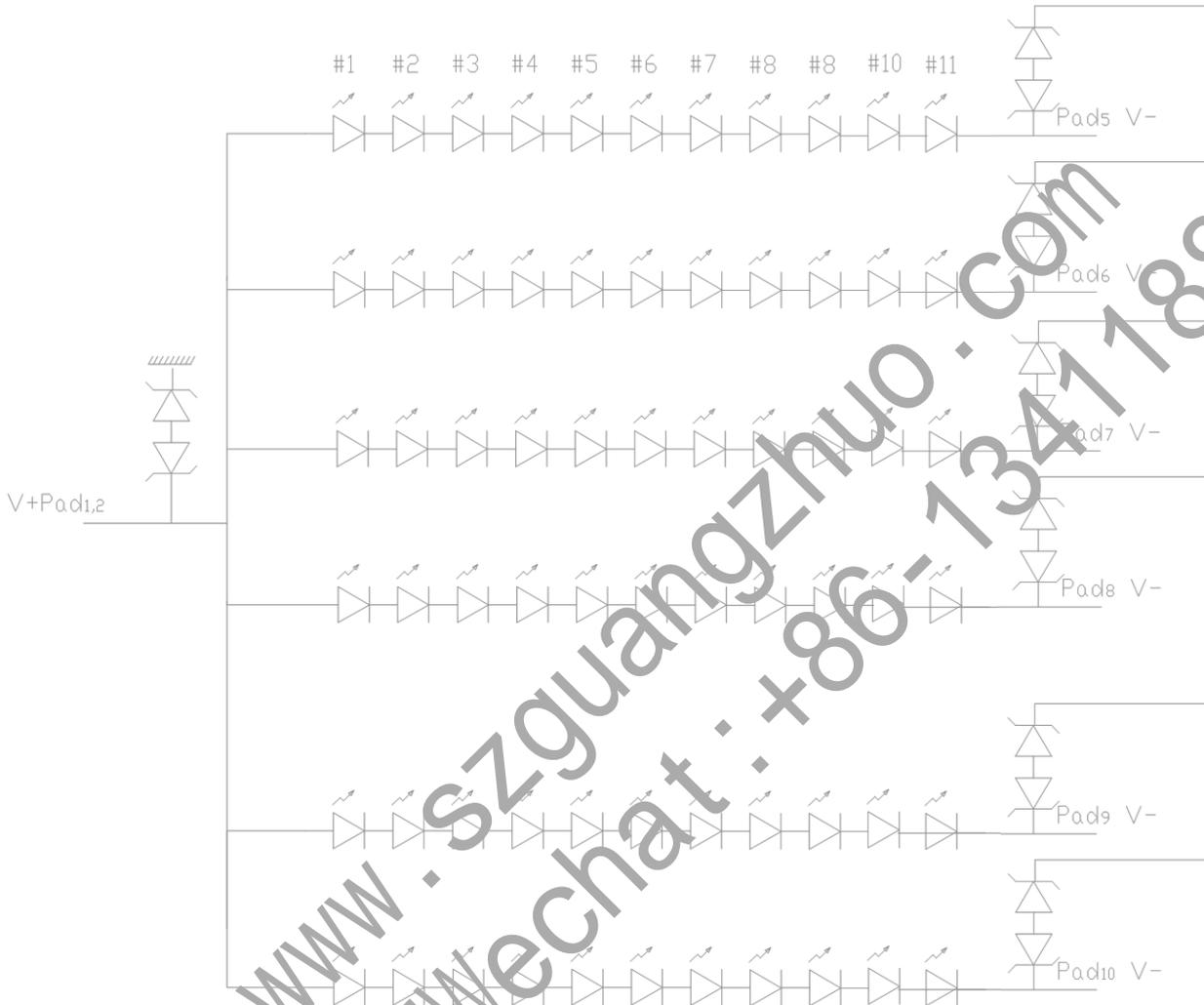


Figure 6. LED Structure

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## 4.0 OPTICAL SPECIFICATION

### 4.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance  $\leq 1$  lux and temperature =  $25 \pm 2^\circ\text{C}$ ) with the equipment of luminance meter system (PR730&PR810) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of  $\theta$  and  $\phi$  equal to  $0^\circ$ . We refer to  $\theta\phi=0$  ( $=\theta_3$ ) as the 3 o'clock direction (the "right"),  $\theta\phi=90$  ( $=\theta_{12}$ ) as the 12 o'clock direction ("upward"),  $\theta\phi=180$  ( $=\theta_9$ ) as the 9 o'clock direction ("left") and  $\theta\phi=270$  ( $=\theta_6$ ) as the 6 o'clock direction ("bottom"). While scanning  $\theta$  and/or  $\phi$ , the center of the measuring spot on the display surface shall stay fixed. The backlight should be operating for 30 minutes prior to measurement. VDD shall be  $3.3 \pm 0.3\text{V}$  at  $25^\circ\text{C}$ . Optimum viewing angle direction is 0'clock.

### 4.2 Optical Specifications

&lt;Table 5. Optical Specifications&gt;

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	$\theta_3$	CR > 10 $\theta = 0^\circ$	80	85	-	Deg.	Note 1
		$\theta_9$		80	85	-	Deg.	
	Vertical	$\theta_{12}$		80	85	-	Deg.	
		$\theta_6$		80	85	-	Deg.	
Luminance Contrast Ratio		CR	$\theta = 0^\circ$	1000	1200	-		Note 2
Luminance of White	5 Points	Y	$\theta = 0^\circ$ ILED = 14.0mA	255	300	-	cd/m <sup>2</sup>	Note 3
White Luminance Uniformity	5 Points	$\Delta Y_5$		80	-	-		Note 4
	13 Points	$\Delta Y_{13}$	65	-	-			
White Chromaticity		$W_x$	$\theta = 0^\circ$	0.283	0.313	0.343		Note 5
		$W_y$		0.299	0.329	0.359		
Reproduction of Color	Red	$R_x$	$\theta = 0^\circ$	Typ.-0.03	0.646	Typ.+0.03		
		$R_y$			0.333			
	Green	$G_x$			0.294			
		$G_y$			0.606			
	Blue	$B_x$			0.144			
		$B_y$			0.058			
Color Gamut				95%	100	-	%	SRGB
Response Time (Rising + Falling)		$T_{RT}$	$T_a = 25^\circ\text{C}$ $\theta = 0^\circ$	-	16	25	ms	Note 6
Cross Talk		CT	$\theta = 0^\circ$	-	-	2.0	%	Note 7
Gamma		-	-	1.7	2.2	2.7		

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## Notes :

- Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 7).
- Contrast measurements shall be made at viewing angle of  $\Theta = 0$  and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (see Figure 7) Luminance Contrast Ratio (CR) is defined mathematically.
 
$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$
- Center Luminance of white is defined as luminance values of 5 point average across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 8 for a total of the measurements per display.
- The White luminance uniformity on LCD surface is then expressed as :  $\Delta Y = \text{Minimum Luminance of 5(or 13) points} / \text{Maximum Luminance of 5(or 13) points}$ . (see Figure 8 and Figure 9).
- The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
- The electro-optical response time measurements shall be made as Figure 10 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is  $T_r$ , and 90% to 10% is  $T_f$ .
- Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark. (See Figure 11).

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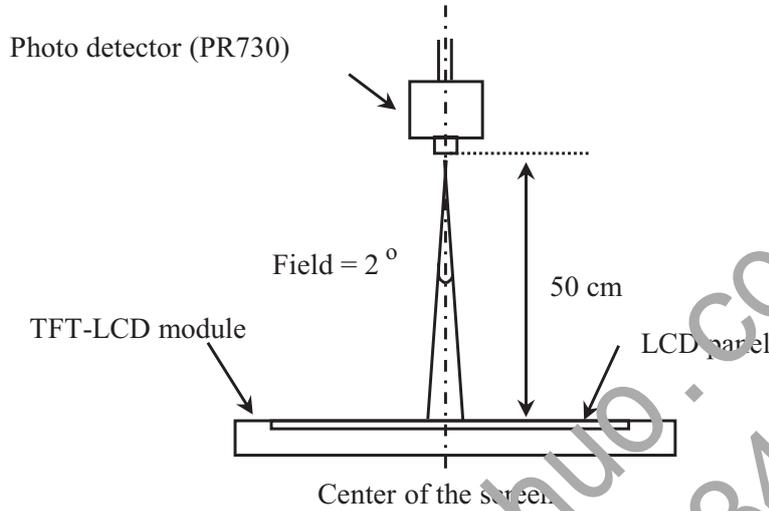
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### 4.3 Optical Measurements



Optical characteristics measurement setup

Figure 7. Measurement Set Up

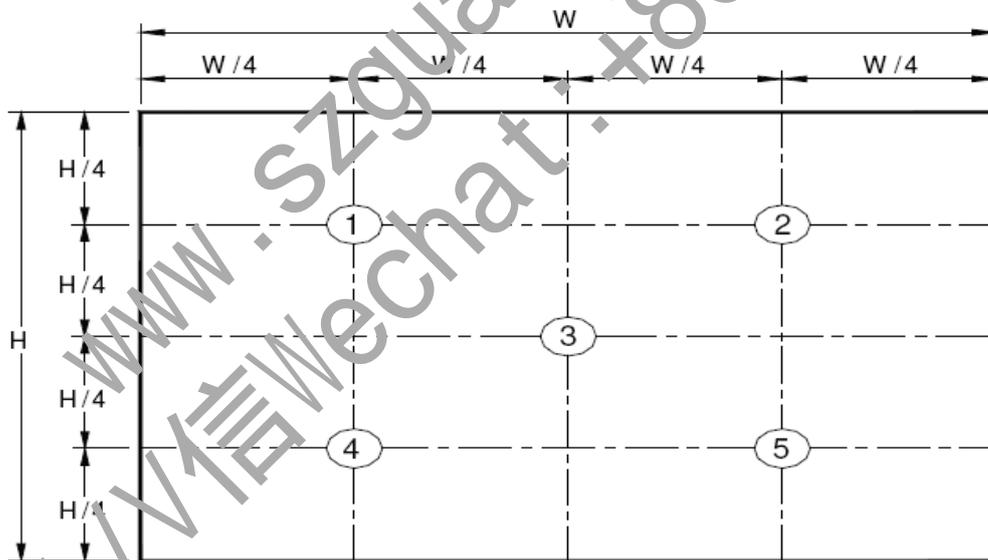


Figure 8. White Luminance and Uniformity Measurement Locations (5 points)

Center Luminance of white is defined as luminance values of center 5 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 7 for a total of the measurements per display.

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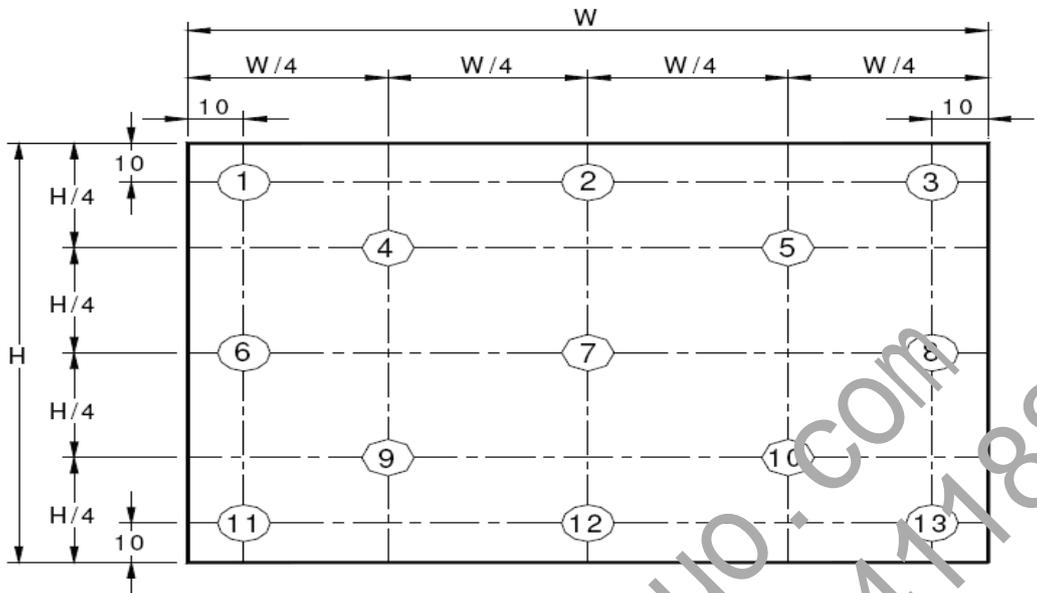


Figure 9. Uniformity Measurement Locations (13 points)

The White luminance uniformity on LCD surface is then expressed as:  $\Delta Y5$  = Minimum Luminance of five points / Maximum Luminance of five points (see Figure 8)  $\Delta Y13$  = Minimum Luminance of 13 points / Maximum Luminance of 13 points (see Figure 9).

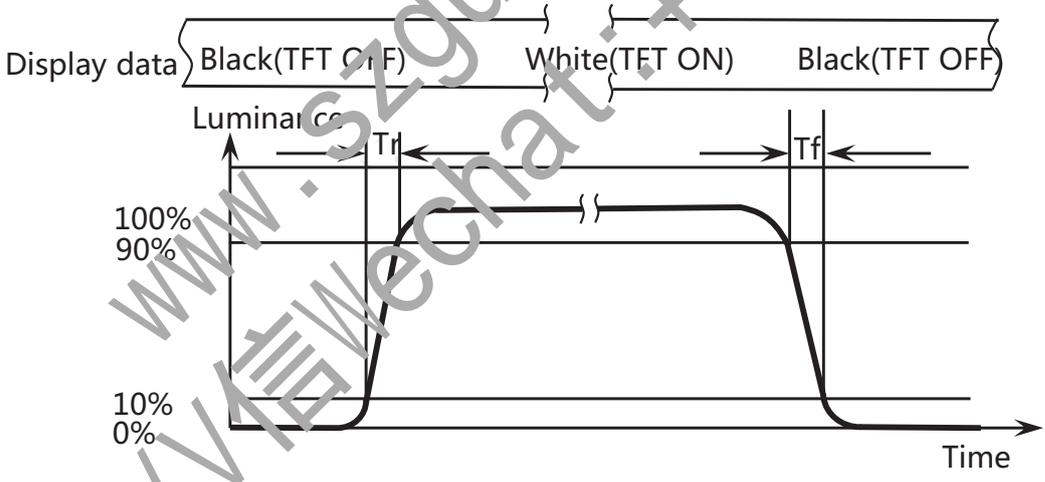


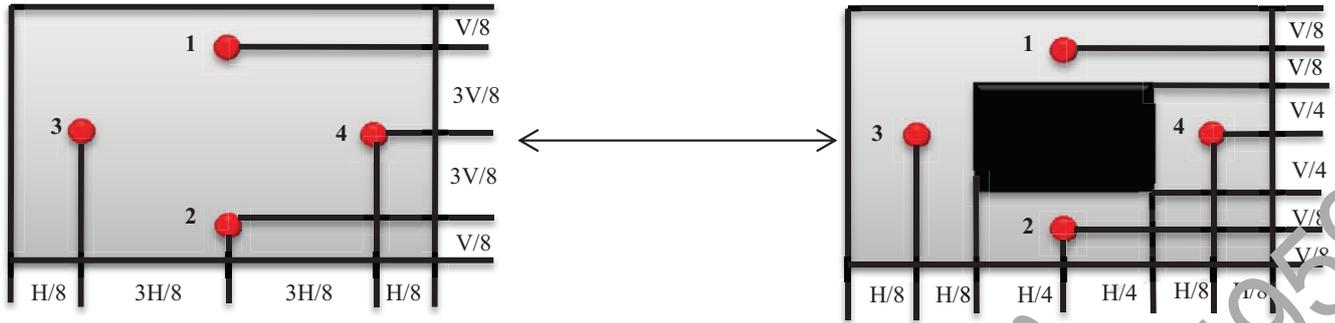
Figure 10. Response Time Testing

The electro-optical response time measurements shall be made as shown in Figure 10 by switching the “data” input signal ON and OFF. Tr: The luminance to change from 10% to 90% ,Tf: The luminance to change from 90% to 10% .

The test system : LMS PR810

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$$\text{Cross Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_A} \right| \times 100$$

Figure 11. Cross Talk Modulation Test Description

Where:

$Y_A$  = Initial luminance of measured area (cd/m<sup>2</sup>)

$Y_B$  = Subsequent luminance of measured area (cd/m<sup>2</sup>)

The location 1/2/3/4 measured will be exactly the same in both patterns. The test background gray is from L64 to L192. Take the largest data as the result.

Cross Talk of one area of the LCD surface by another shall be measured by comparing the luminance ( $Y_A$ ) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance ( $Y_B$ ) of that same area when any adjacent area is driven dark. (Refer to Figure 11)

The test system: PR730

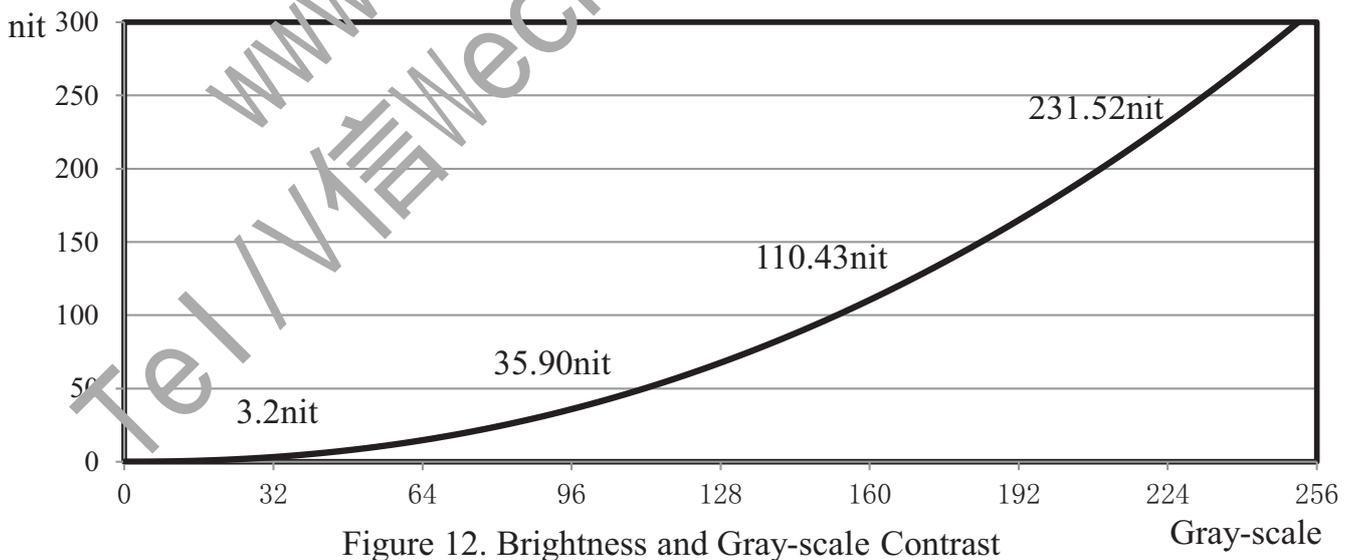


Figure 12. Brightness and Gray-scale Contrast

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## 5.0 INTERFACE CONNECTION

### 5.1 Electrical Interface Connection

The electronics interface connector is I-PEX 20696-030E or Compatible.

The connector interface pin assignments are listed in Table 6.

<Table 6. Pin Assignments for the Interface Connector>

Pin No.	Symbol	Description
1	DBC_EN	DBC_Function Reserved
2	H_GND	Ground
3	LANE1_N	eDP RX Channel 1 Negative
4	LANE1_P	eDP RX Channel 1 Positive
5	H_GND	Ground
6	LANE0_N	eDP RX Channel 0 Negative
7	LANE0_P	eDP RX Channel 0 Positive
8	H_GND	Ground
9	AUX_CH_P	eDP AUX CH Positive
10	AUX_CH_N	eDP AUX CH Negative
11	H_GND	Ground
12	LCD_VCC	Power Supply, 3.3V (typ.)
13	LCD_VCC	Power Supply, 3.3V (typ.)
14	BTST	Panel Self Test Enable
15	H_GND	Ground
16	H_GND	Ground
17	HPD	Hot Plug Detect Output
18	BL_GND	LED Ground
19	BL_GND	LED Ground
20	BL_GND	LED Ground
21	BL_GND	LED Ground
22	BL_ENABLE	LED Enable Pin(+3.3V Input)
23	BL_PWM	System PWM Signal Input
24	NC	No Connection
25	NC	No Connection
26	BL_POWER	LED Power Supply 5V-21V
27	BL_POWER	LED Power Supply 5V-21V
28	BL_POWER	LED Power Supply 5V-21V
29	BL_POWER	LED Power Supply 5V-21V
30	NC	No Connection

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### 5.2 eDP Interface

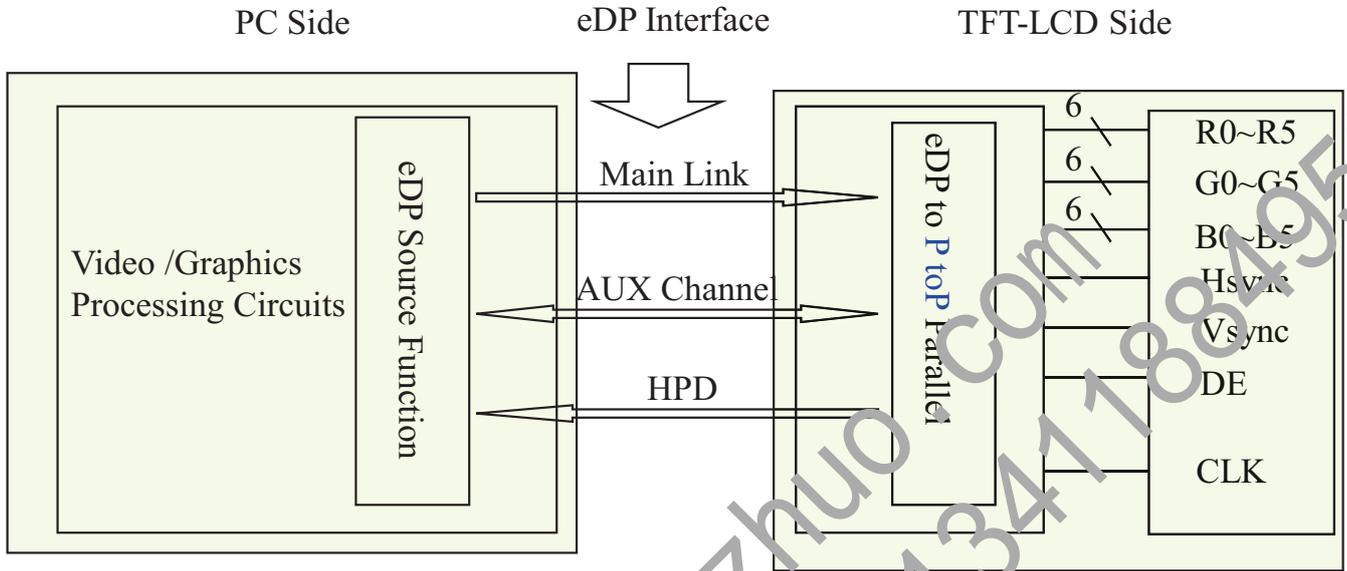
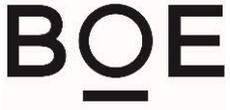


Figure 13. eDP Interface Architecture

Note:

Transmitter : Parade DP501 or equivalent.  
 Transmitter is not contained in module.

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### 5.3 Data Input Format

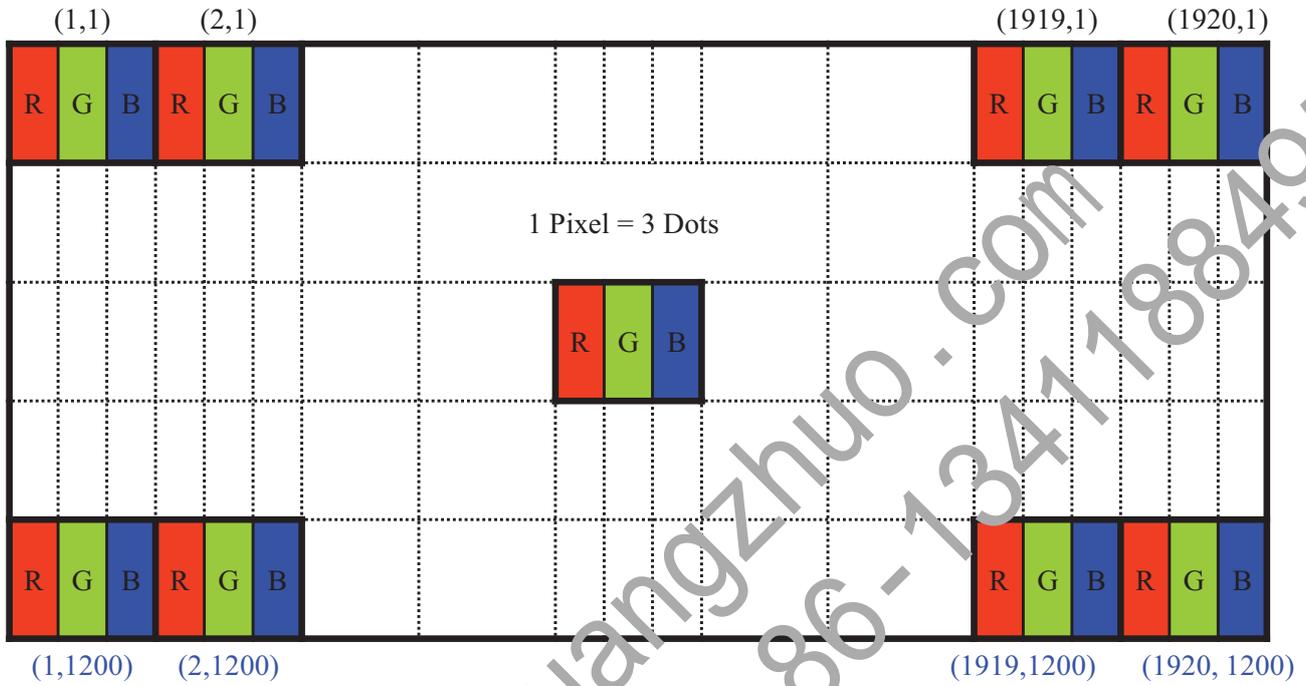


Figure 14. Display Position of Input Data (V-H)

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**5.4 Back-light & LCM Interface Connection**

BLU Interface Connector: UJU PF040-B10B-C09 or Compatible.

&lt;Table 7. Pin Assignments for the BLU Connector&gt;

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vout	LED anode connection	6	LED	LED cathode connection
2	Vout	LED anode connection	7	LED	LED cathode connection
3	NC	No Connection	8	LED	LED cathode connection
4	GND	Ground	9	LED	LED cathode connection
5	LED	LED cathode connection	10	LED	LED cathode connection

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**6.0 SIGNAL TIMING SPECIFICATION****6.1 The NV160WUM-N45 Is Operated By The DE Only**

&lt; Table 8. Signal Timing Specification &gt;

Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	-	158.49	-	MHz
Frame Period		Tv	-	1246	-	lines
			-	60	-	Hz
			-	16.67	-	ms
Vertical Display Period		Tvd	-	1200	-	lines
One line Scanning Period		Th	-	2120	-	clocks
Horizontal Display Period		Thd	-	1920	-	clocks

Note : The above is as optimized setting.

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### 6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 9.

<Table 9. eDP Main-Link RX TP4 Package Pin Parameters>

Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock (Link clock down-spreading)	SSC	-	-	0.5	%	
Differential peak-to-peak input voltage at package pins	$V_{RX-DIFFp-p}$	120	-	200	mV	
Rx input DC common mode voltage	$V_{RX-DC-CM}$	0	-	2	V	
Differential termination resistance	$R_{RX-DIFF}$	80	-	100	$\Omega$	
Single-ended termination resistance	$R_{RX-SE}$	40	-	60	$\Omega$	
Rx short circuit current limit	$I_{RX-SHORT}$	-	-	20	mA	
Intra-pair skew at Rx package pins (HBR) RX intra-pair skew tolerance at HBR	$L_{RX-SKEW-INTRA-PAIR}$	-	-	60	ps	
AC Coupling Capacitor	$C_{SOURCE-ML}$	75	-	200	nF	Source side

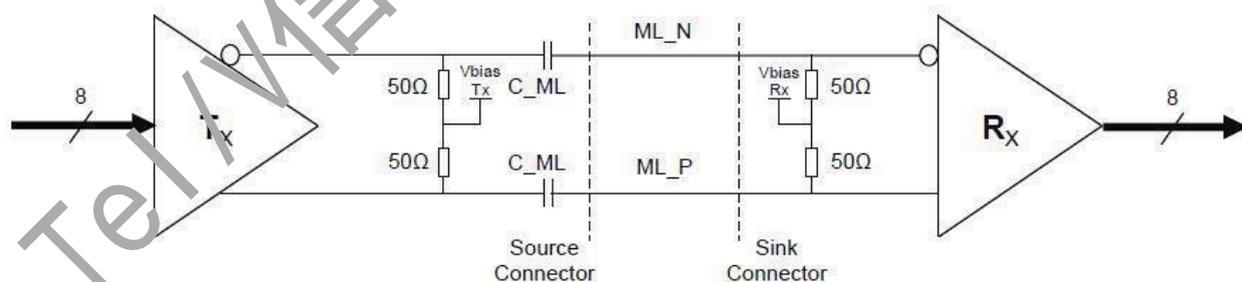


Figure 15. Main link differential pair

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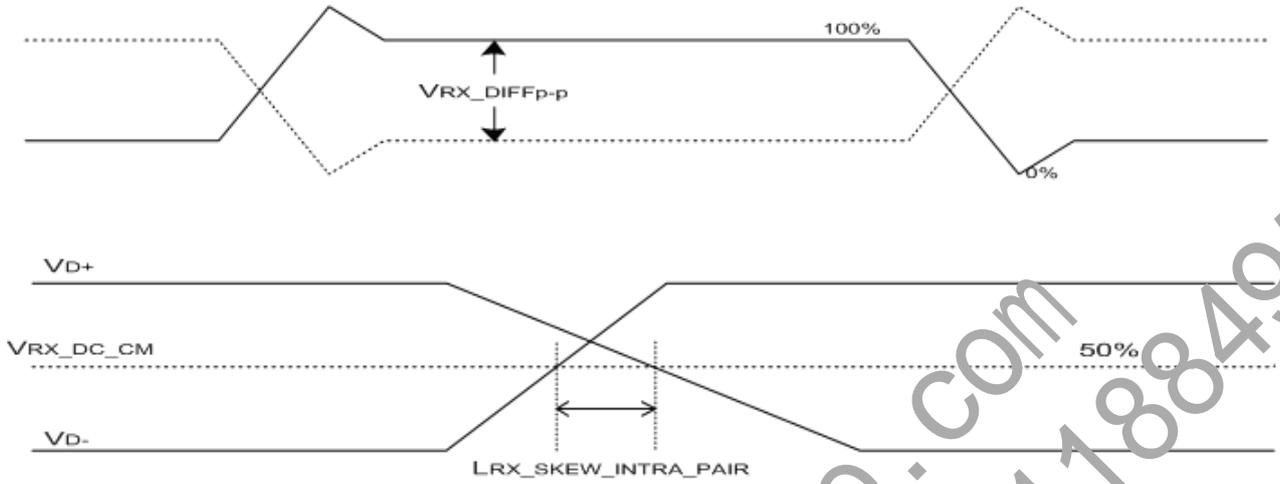


Figure 16. VRX-DIFFp-p & LRX\_SKEW\_INTRA\_PAIR

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<Table 10. HPD Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
HPD voltage	V <sub>HPD</sub>	2.25	-	3.6	V	Sink side
Hot Plug Detection Threshold	-	2.0	-	-	V	Source side
Hot Unplug Detection Threshold	-	-	-	0.8V	V	
HPD_IRQ Pulse Width	HPD_IRQ	0.5	-	1	ms	
HPD_TimeOut	-	2.0	-	-	ms	

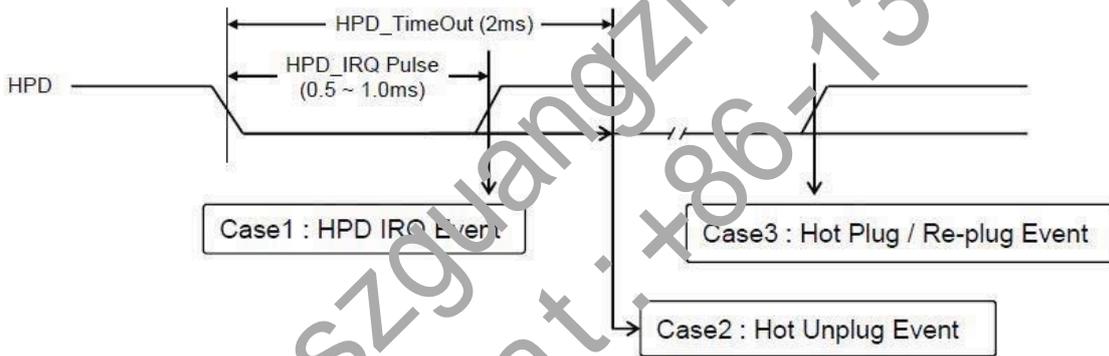


Figure 17. HPD Events

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<Table 11. AUX Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
AUX unit interval	$U_{IAUX}$	0.4	0.5	0.6	Us	
AUX peak-to-peak input differential voltage	$V_{AUX-RX-DIFFp-p}$	0.29	-	1.38	V	Sink Side Connector Pin
AUX CH termination DC resistance	$R_{AUX-TERM}$	80	100	120	Ohm	
AUX DC common mode voltage	$V_{AUX-DC-CM}$	0	-	2	V	
AUX turn around common mode voltage	$V_{AUX-TURN-CM}$			0.3	V	
AUX short circuit current limit	$I_{AUX-SHORT}$	-	-	90	mA	
AUX AC Coupling Capacitor	$C_{SOURCE-AUX}$	75		200	nF	Source side

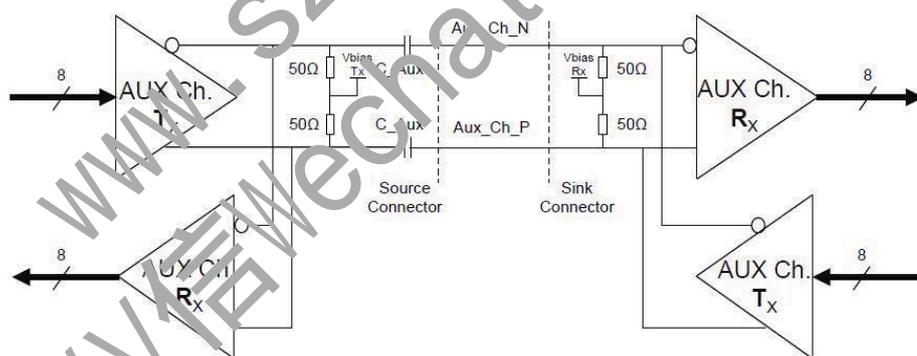


Figure 18. AUX differential pair

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## 7.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

<Table 12. Input Signal & Basic Display Colors & Gray Scale of Colors >

	Colors & Gray scale	Data signal																							
		R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Light Blue	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Purple	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	△	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Darker	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	△				↑								↑								↑				
	▽				↓								↓								↓				
	Brighter	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	▽	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Gray scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	△	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Darker	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	△				↑								↑							↑					
	▽				↓								↓							↓					
	Brighter	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
	▽	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Gray scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	
	△				↑								↑							↑					
	▽				↓								↓							↓					
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	
Gray scale of White& Black	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	△	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	
	Darker	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	
	△				↑								↑							↑					
	▽				↓								↓							↓					
	Brighter	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	
	▽	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	
White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		

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### 8.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below.

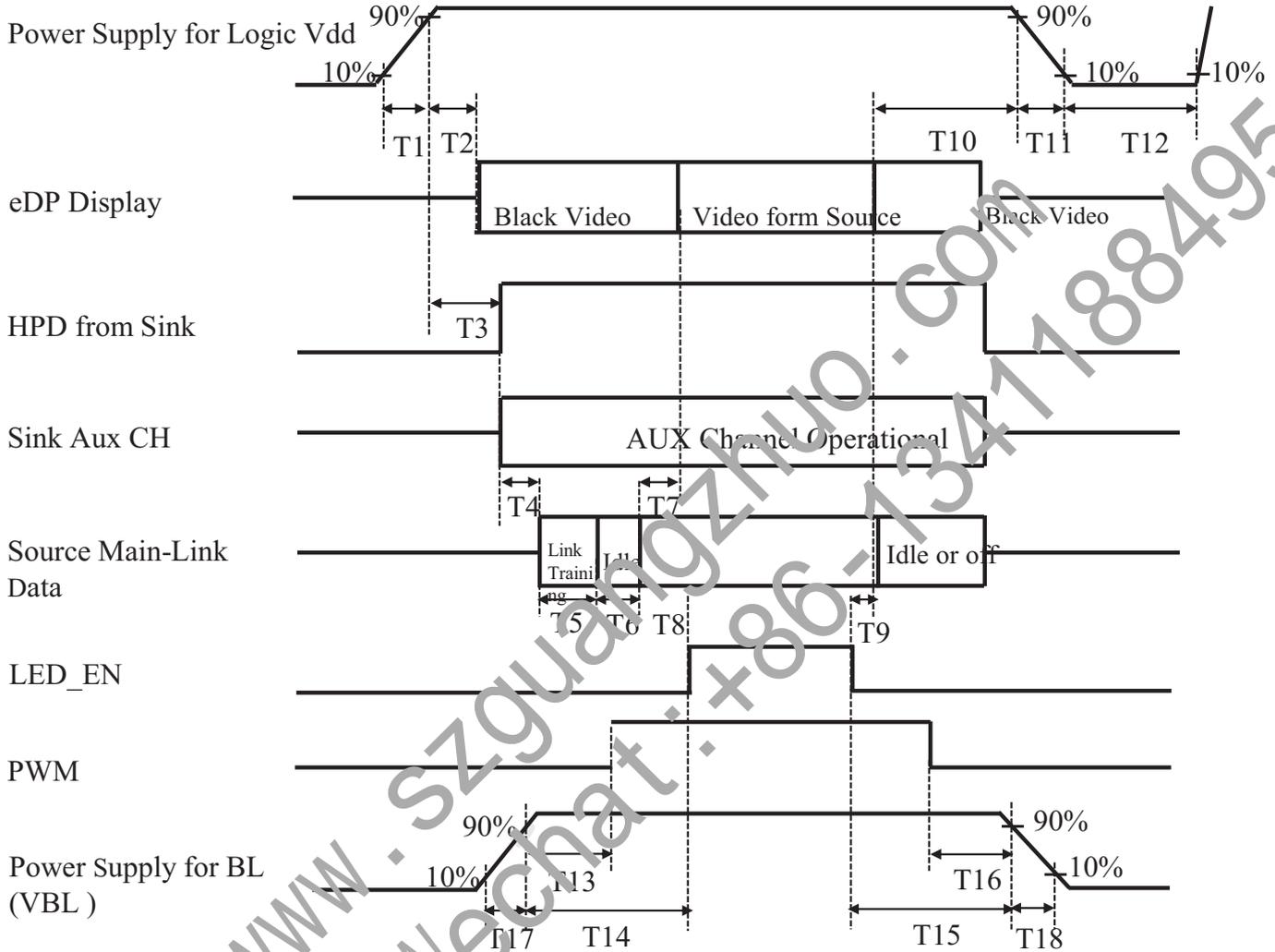


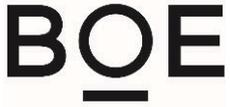
Figure 19. Power Sequence

- 0.5ms ≤ T1 ≤ 10 ms
- 0ms < T2 ≤ 200 ns
- 0ms < T3 ≤ 200 ms
- T4+T5+T6+T8>80ms
- 0ms < T7 ≤ 50ms
- 50ms ≤ T8
- 0ms < T9
- 40ms < T10 < 500 ms
- 0.5ms ≤ T11 ≤ 10 ms
- 500ms ≤ T12
- 0ms < T13
- 0ms < T14
- 0ms < T15
- 0ms < T16
- 0.5ms ≤ T17
- 0.5ms ≤ T18

**Notes:**

1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal are valid.

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## 9.0 Connector Description

Physical interface is described as for the connector on LCM.

These connectors are capable of accommodating the following signals and will be following components.

### 9.1 TFT LCD Module

< Table 13. Signal Connector >

Connector Name /Description	For Signal Connector
Manufacturer	STM or Compatible
Type/ Part Number	I-PEX 20696-030E or Compatible
Mating Housing/ Part Number	I-PEX 20454-030T or Compatible

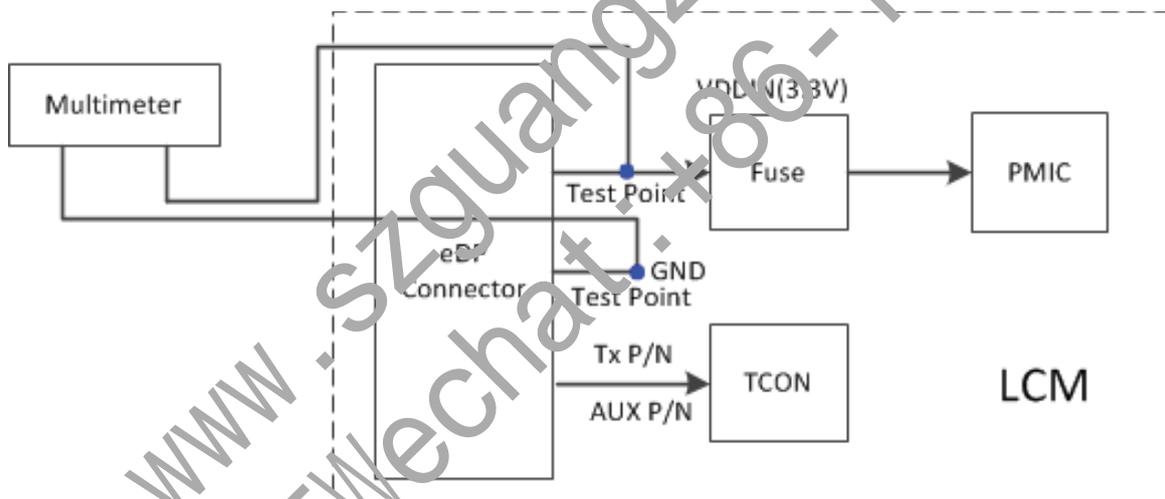
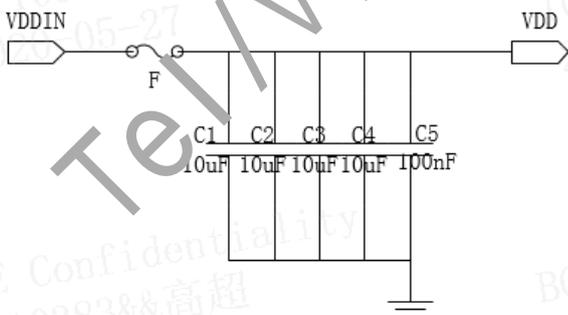


Figure 20. RC Loading Test Schematic Diagram



Item	RC Loading	
	R	C
FNXCXY	1.29MΩ	38.5uF

Figure 21. VCC Loop R/C Loading Parameter

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## 10.0 MECHANICAL CHARACTERISTICS

### 10.1 Dimensional Requirements

Figure 26 shows mechanical outlines for the model NV160WUM-N45.  
Other parameters are shown in Table 14.

&lt;Table 14. Dimensional Parameters&gt;

Parameter	Specification	Unit
Active Area	344.6784(H) × 215.424(V)	mm
Number of pixels	1920 (H) × 1200(V)	pixels
Pixel pitch	179.52(H) × 179.52(V)	um
Pixel arrangement	RGB Vertical stripe	
Display colors	16.7M(round down) (true 8bit)	
Display mode	Normally Black	
Dimensional outline	349.68±0.3(H)*255.32±0.5(V) (W/PCB)*3.0(Max.), 349.68±0.3 (H) × 255.32±0.5 (V) (W/O PCB) × 5.0 (Max.)	mm
Weight	400(Max.)	g

### 10.2 Mounting

See Figure 26.

### 10.3 Anti-Glare and Polarizer Hardness.

The surface of the LCD has an Anti-Glare coating to minimize reflection and a 3H hardness coating to reduce scratching

### 10.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 350lux.

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**11.0 RELIABILITY TEST**

The reliability test items and its conditions are shown in below.

&lt;Table 15. Reliability Test&gt;

No	Test Items	Conditions	Remark
1	High temperature storage test	Ta = 60°C , 60%RH, 240 hrs	
2	Low temperature storage test	Ta = -20°C , 240 hrs	
3	High temperature & high humidity operation test	Ta = 50°C , 80%RH, 240 hrs	
4	High temperature operation test	Ta = 50°C , 60%RH, 240 hrs	
5	Low temperature operation test	Ta = 0°C , 240 hrs	
6	Thermal shock	Ta = -20°C ↔ 60°C (0.5 hr), 60% ± 3%RH, 100 cycle	
7	Vibration test (non-operating)	Ta = 25°C , 60%RH 1.5G, 10~500Hz, Sine X,Y,Z / Sweep rate : 1 hour	Note 1
8	Shock test (non-operating)	Ta = 25°C , 60%RH, 220G, Half Sine Wave 2msec ± X ± Y, ± Z Once for each direction	Note 1
9	Electro-static discharge test (operating)	Air : 150 pF, 330Ω, ± 15 KV Contact : 150 pF, 330Ω, ± 8 KV Ta = 25°C , 60%RH,	Note 2

Notes :

1. The fixture must be hard enough , so that the module would not be twisted or bent.
2. Self- recovery and restart recovery is allowed. No hardware failures.

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## 12.0 HANDLING & CAUTIONS

### (1) Cautions when taking out the module

- Pick the pouch only, when taking out module from a shipping package.

### (2) Cautions for handling the module

- As the electrostatic discharges may break the LCD module, handle the LCD module with care.
- Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

### (3) Cautions for the operation

- When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

### (4) Cautions for the atmosphere

- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

### (5) Cautions for the module characteristic

- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

### (6) Other cautions

- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc. Please pack the module not to be broken. We recommend to use the original shipping packages.

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### 13.0 LABEL

#### (1) Product Label

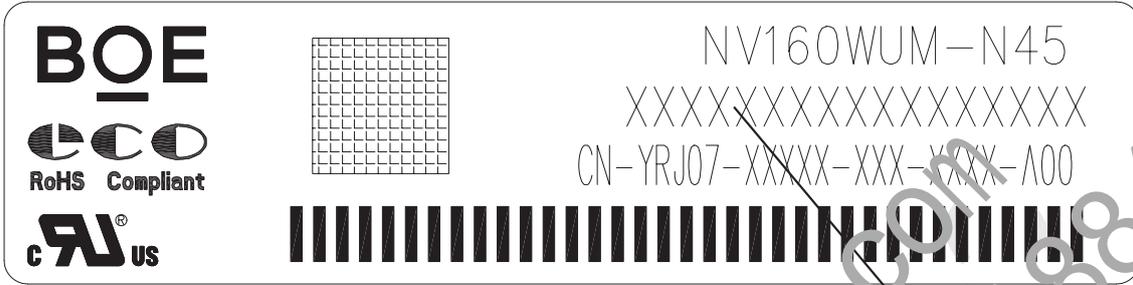


Figure 22. Product Label

Module ID Naming Rule:

<Table 16. Module ID Naming Rule>

Digit Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Code	B	9	A	F	1	7	8	8	D	3	1	0	0	0	0	6	8
Description	Product Name		Product Grade	B8	Year	Month	Model Extension Code (Last 4 Digits of FG CODE)				Serial No. 00001-ZZZZZZ						

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(2) High voltage caution label

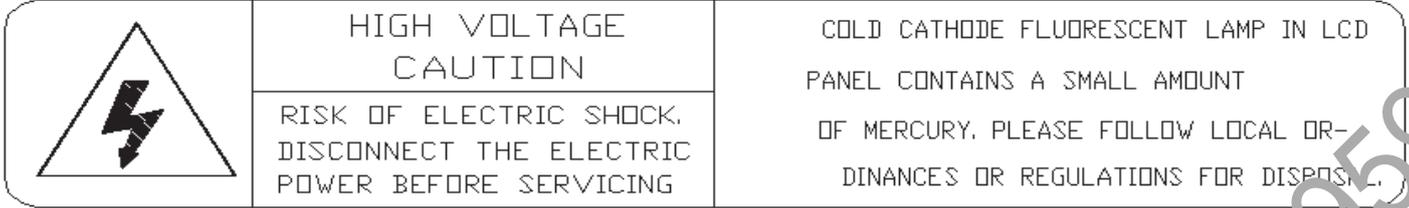


Figure 23. High Voltage Caution Label

(3) Box label

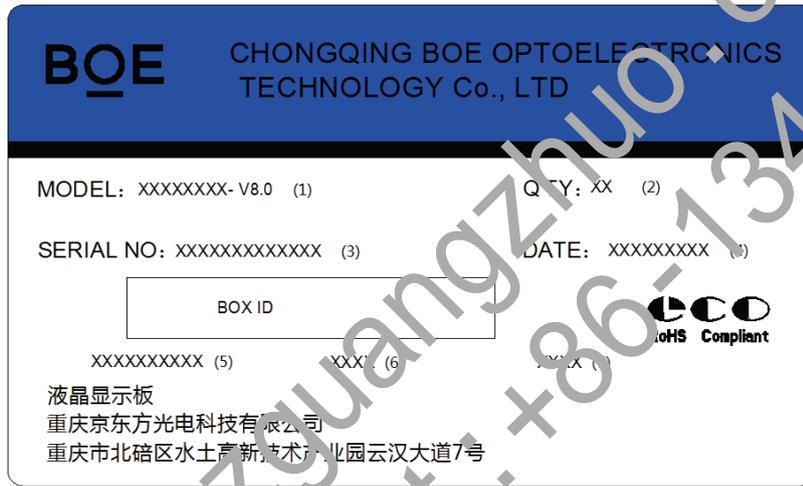


Figure 24. Box Label

Serial number marked part needs to print, show as follows:

1. FG-CODE(Before 12 bit)
2. Product quantity
3. Box ID
4. Date
5. The client section material number(The client)
6. FG-Code After four
7. The supplier code

Total Size:100×50mm

<Table 17. Box Label Naming Rule >

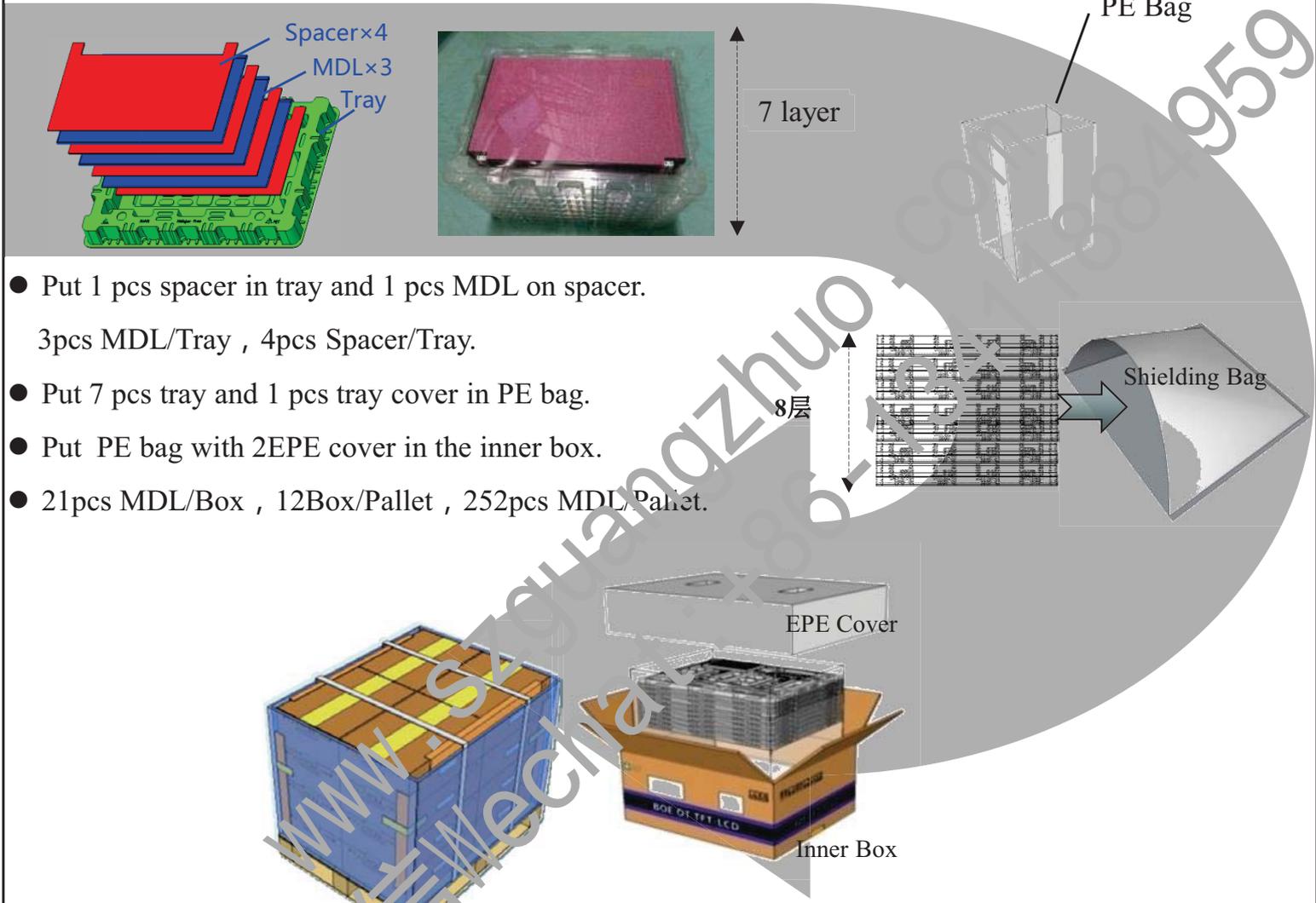
Digit Code	1	2	3	4	5	6	7	8	9	10	11	12	13
Code	B	9	A	F	1	7	8	N	0	0	3	2	7
Description	Product Name		Product Grade	B8	Year		Month	Revision	BOX Serial Number				

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## 14.0 PACKING INFORMATION

### 14.1 Packing Order



- Put 1 pcs spacer in tray and 1 pcs MDL on spacer.  
3pcs MDL/Tray , 4pcs Spacer/Tray.
- Put 7 pcs tray and 1 pcs tray cover in PE bag.
- Put PE bag with 2EPE cover in the inner box.
- 21pcs MDL/Box , 12Box/Pallet , 252pcs MDL/Pallet.

Figure 25. Packing Order

### 14.2 Note

- Box dimension: 522mm×392mm×294mm
- Package quantity in one box: 21pcs
- Total weight: 11kg

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### 15.0 MECHANICAL OUTLINE DIMENSION



Figure 26. TFT-LCD Module Outline Dimension (Front View)

**NOTES:**

1. WARPAGE AND DEFORMATION SPEC.: 0.5mm MAX.
2. THE eDP CONNECTOR IS MEASURED AT PIN 1 AND MATING LINE
3. UNSPECIFIED TOLERANCE REFER TO ` 0.3 mm
4. THE MEASUREMENT METHOD FOR THE DIMENSION OF MODULE, PLEASE REFRE TO PRODUCT SPEC.
5. TOP POLARIZER IS THE HIGHEST PORTION.
6. "( )" MEANS REFERENCE DIMENSIONS.
7. CRITICAL DIMENSION: ①~⑩  
CPK: ①~③

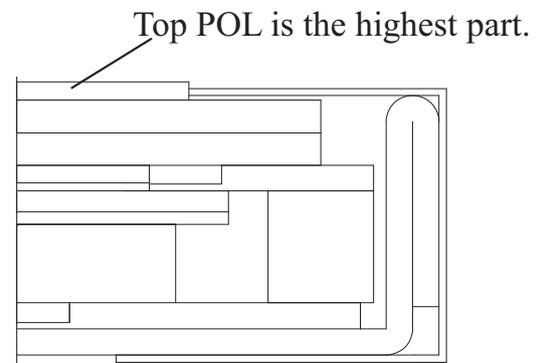


Figure 27. Highest Point Position

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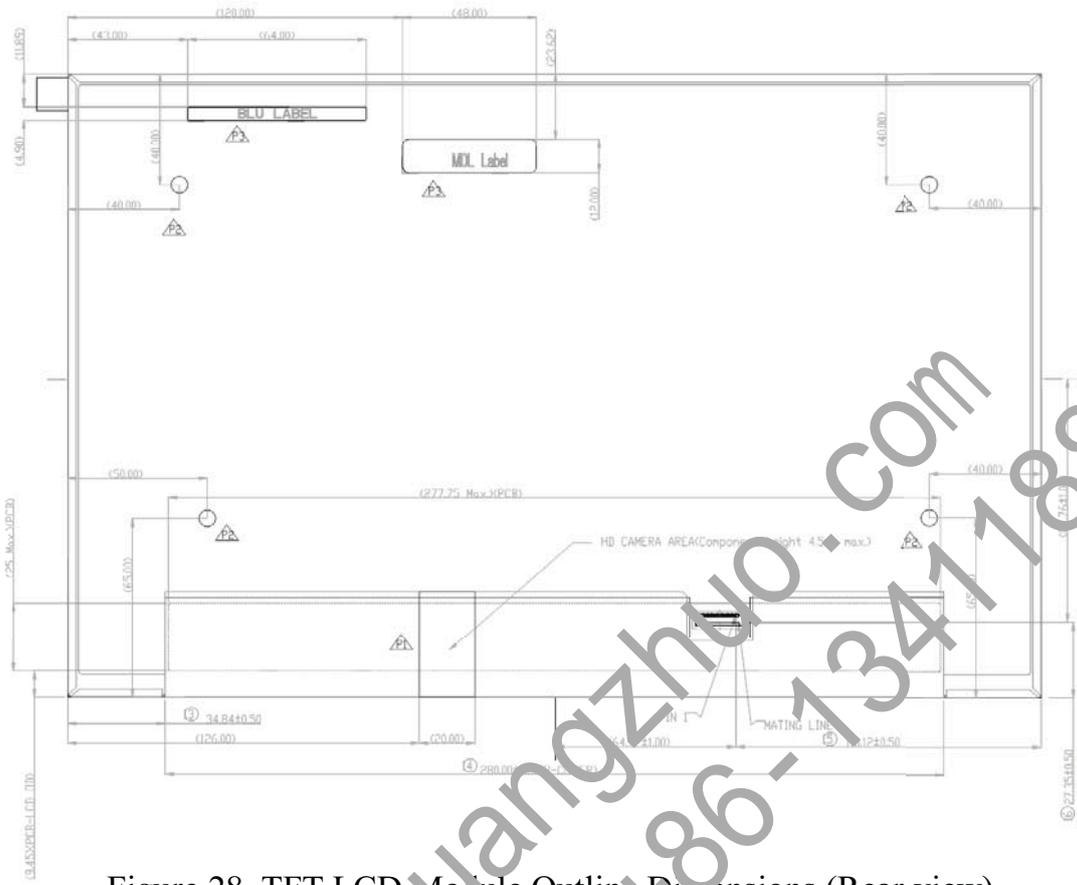


Figure 28. TFT-LCD Module Outline Dimensions (Rear view)

**NOTES:**

1. WARPAGE AND DEFORMATION SPEC.: 0.5mm MAX.
2. THE eDP CONNECTOR IS MEASURED AT PIN 1 AND MATING LINE
3. UNSPECIFIED TOLERANCE REFER TO ` 0.3 mm
4. THE MEASUREMENT METHOD FOR THE DIMENSION OF MODULE, PLEASE REFRE TO PRODUCT SPEC.
5. TOP POLARIZER IS THE HIGHEST PORTION.
6. "()" MEANS REFERENCE DIMENSIONS.
7. CRITICAL DIMENSION: ①~⑩  
CPK: ①~③

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### 16.0 EDID Table

00	Header	00	0		0	EDID Header
01		FF	255		255	
02		FF	255		255	
03		FF	255		255	
04		FF	255		255	
05		FF	255		255	
06		FF	255		255	
07		00	0		0	
08	ID Manufacturer Name	09	9		BOE	ID = BOE
09		E5	229			
0A	ID Product Code	59	89		2649	ID = 2649
0B		0A	10			
0C	32-bit serial No.	00	0		0	
0D		00	0		0	
0E		00	0		0	
0F		00	0		0	
10	Week of manufacture	14	20		20	
11	Year of Manufacture	1F	31		2021	Manufactured in 2021
12	EDID Structure Ver.	01	1		1	EDID Ver 1.0
13	EDID revision #	04	4		4	EDID Rev. 0.4
14	Video input definition	A5	165		-	Refer to right table
15	Max H image size	22	34		34	34.468 cm (Approx)
16	Max V image size	16	22		22	21.542 cm (Approx)
17	Display Gamma	78	120		2.2	Gamma curve = 2.2
18	Feature support	07	7		-	Refer to right table
19	Red/Green low bits	95	149		-	Red / Green Low Bits
1A	Blue/White low bits	EF	245		-	Blue / White Low Bits
1B	Red x high bits	45	165	662	0.646	Red (x) = 10100101 (0.646)
1C	Red y high bits	55	85	341	0.333	Red (y) = 01010101 (0.333)
1D	Green x high bits	4B	75	301	0.294	Green (x) = 01001011 (0.294)
1E	Green y high bits	9B	155	621	0.606	Green (y) = 10011011 (0.606)
1F	Blue x high bits	24	36	147	0.144	Blue (x) = 00100100 (0.144)
20	Blue y high bits	0E	14	59	0.058	Blue (y) = 00001110 (0.058)
21	White x high bits	50	80	321	0.313	White (x) = 01010000 (0.313)
22	White y high bits	54	84	337	0.329	White (y) = 01010100 (0.329)
23	Established timing 1	00	0		-	Refer to right table
24	Established timing 2	00	0		-	
25	Established timing 3	00	0		-	

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26	Standard timing #1	01	1			Not Used
27		01	1			
28	Standard timing #2	01	1			Not Used
29		01	1			
2A	Standard timing #3	01	1			Not Used
2B		01	1			
2C	Standard timing #4	01	1			Not Used
2D		01	1			
2E	Standard timing #5	01	1			Not Used
2F		01	1			
30	Standard timing #6	01	1			Not Used
31		01	1			
32	Standard timing #7	01	1			Not Used
33		01	1			
34	Standard timing #8	01	1			Not Used
35		01	1			
36	Detailed timing/monitor descriptor #1	EA	234		158.40	158.4912MHz Main clock
37		3D	61			
38		80	128		1920	Hor Active = 1920
39		C8	200		200	Hor Blanking = 200
3A		70	112		-	4 bits of Hor. Active + 4 bits of Hor. Blanking
3B		B0	176		1200	Ver Active = 1200
3C		2E	46		46	Ver Blanking = 46
3D		40	6		-	4 bits of Ver. Active + 4 bits of Ver. Blanking
3E		30	48		48	Hor Sync Offset = 48
3F		20	32		32	H Sync Pulse Width = 32
40		56	54		3	V sync Offset = 3 line
41		00	0		6	V Sync Pulse width : 6 line
42		59	89		345	Horizontal Image Size = 344.68 mm (Low 8 bits)
43		D7	215		215	Vertical Image Size = 215.42 mm (Low 8 bits)
44		10	16		-	4 bits of Hor Image Size + 4 bits of Ver Image Size
45		00	0		0	Hor Border (pixels)
46		00	0		0	Vertical Border (Lines)
47	1A	26		-	Refer to right table	

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48	Detailed timing/monitor descriptor #2	88	136		126.8	126.79296MHz Main clock	
49		31	49				
4A		80	128		1920	Hor Active = 1920	
4B		C8	200		200	Hor Blanking = 200	
4C		70	112			4 bits of Hor. Active + 4 bits of Hor. Blanking	
4D		B0	176		1200	Ver Active = 1200	
4E		2E	46		46	Ver Blanking = 46	
4F		40	64			4 bits of Ver. Active + 4 bits of Ver. Blanking	
50		30	48		48	Hor Sync Offset = 48	
51		20	32		32	H Sync Pulse Width = 32	
52		36	54		3	V sync Offset = 3 line	
53		00	0		6	V Sync Pulse width = 6 line	
54		59	89		345	Horizontal Image Size = 344.68 mm (Low 8 bits)	
55		D7	215		215	Vertical Image Size = 215.42 mm (Low 8 bits)	
56		10	16			4 bits of Hor Image Size + 4 bits of Ver Image Size	
57		00	0		0	Hor Border (pixels)	
58		00	0		0	Vertical Border (Lines)	
59		1A	26			Refer to right above table	
5A		Detailed timing/monitor descriptor #3	00	0			Dell P/N:YRJ07
5B			00	0			
5C	00		0				
5D	FE		254				
5E	00		0				
5F	59		89		Y		
60	52		82		R		
61	4A		74		J		
62	20		48		0		
63	17		55		7		
64	80	128		10000000	EDID Revision:A00		
65	4E	78		N	BOE PN		
66	56	86		V			
67	31	49		1			
68	36	54		6			
69	4E	78		N			
6A	34	52		4			
6B	35	53		5			

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6C		00	0			Flag
6D		00	0			
6E		00	0			
6F		00	0		Data Type Tag: Manufacturer Specified Data 00	
70		00	0			Flag
71		03	3		-	6-bit Color Depth With 2FRC
72		41	65		-	WLED & singal light bar & one light bar
73		21	33		-	Frame rate 40Hz~65Hz
74	Detailed timing/monitor descriptor #4	9E	158		-	Light Controller:PWM & Max. Luminance300
75		00	0		-	Front Surface:Anti-Glare & RGB v-stripe
76		11	17		-	with DBC
77		00	0		-	no Motion Blur & no Active Gamma
78		00	0		-	no Wireless Enhancement & no In-Screen
79		0A	10		-	2 lane edp
7A		41	65		-	Built-In Self Test
7B		0A	10			Format :
7C	20	32			terminate with ASCII code 0Ah	
7D	20	32			and pad field with ASCII code 20h	
7E	Extension flag	00	0		1	0 : 1个EDID; N-1: N个EDID
7F	Checksum	40	64		64	

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## 17.0 GENERAL PRECAUTIONS

### 17.1 HANDLING

(1) When the module is assembled, It should be attached to the system firmly using every mounting holes.

Be careful not to twist or bend the modules.

(2) Refrain from strong mechanical shock or any force to the module. Otherwise, it may cause improper operation or damage to the module.

(3) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than 1 HB pencil lead.

(4) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use Ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static, it may cause damage to the module.

(9) Use fingerstalls with soft gloves to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Do not pull or fold the LED FPC.

(12) Do not touch any component which is located on the back side.

(13) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(14) Pins of connector shall not be touched directly with bare hands.

### 17.2 STORAGE

(1) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35°C and relative humidity of less than 70%.

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.

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### 17.3 OPERATION

- (1) Do not connect, disconnect the module in the “ Power On” condition.
- (2) Power supply should always be turned on/off by following item 8.0 “ Power on/off sequence “.
- (3) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
- (4) The standard limited warranty is only applicable when the module is used for general notebook applications. If used for purposes other than as specified, BOE is not to be held reliable for the defective operations. It is strongly recommended to contact BOE to find out fitness for a particular purpose.

### 17.4 OTHERS

- (1) Avoid condensation of water. It may result in improper operation or disconnection of electrode.
- (2) Do not exceed the absolute maximum rating value. ( the supply voltage variation, input voltage variation, Variation in part contents and environmental temperature, so on) Otherwise the module may be damaged.
- (3) If the module displays the same pattern continuously for a long period of time, it can be the situation when The “ image sticks” to the screen.
- (4) This module has its circuitry PCB’s on the rear or bottom side and should be handled carefully to avoid being stressed.

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Appendix A

The Measurement Methods for the Dimensions of Module

1. Caliper:

Thickness of Outline (Without/With PCB)

2. Coordinate Measuring Machine:

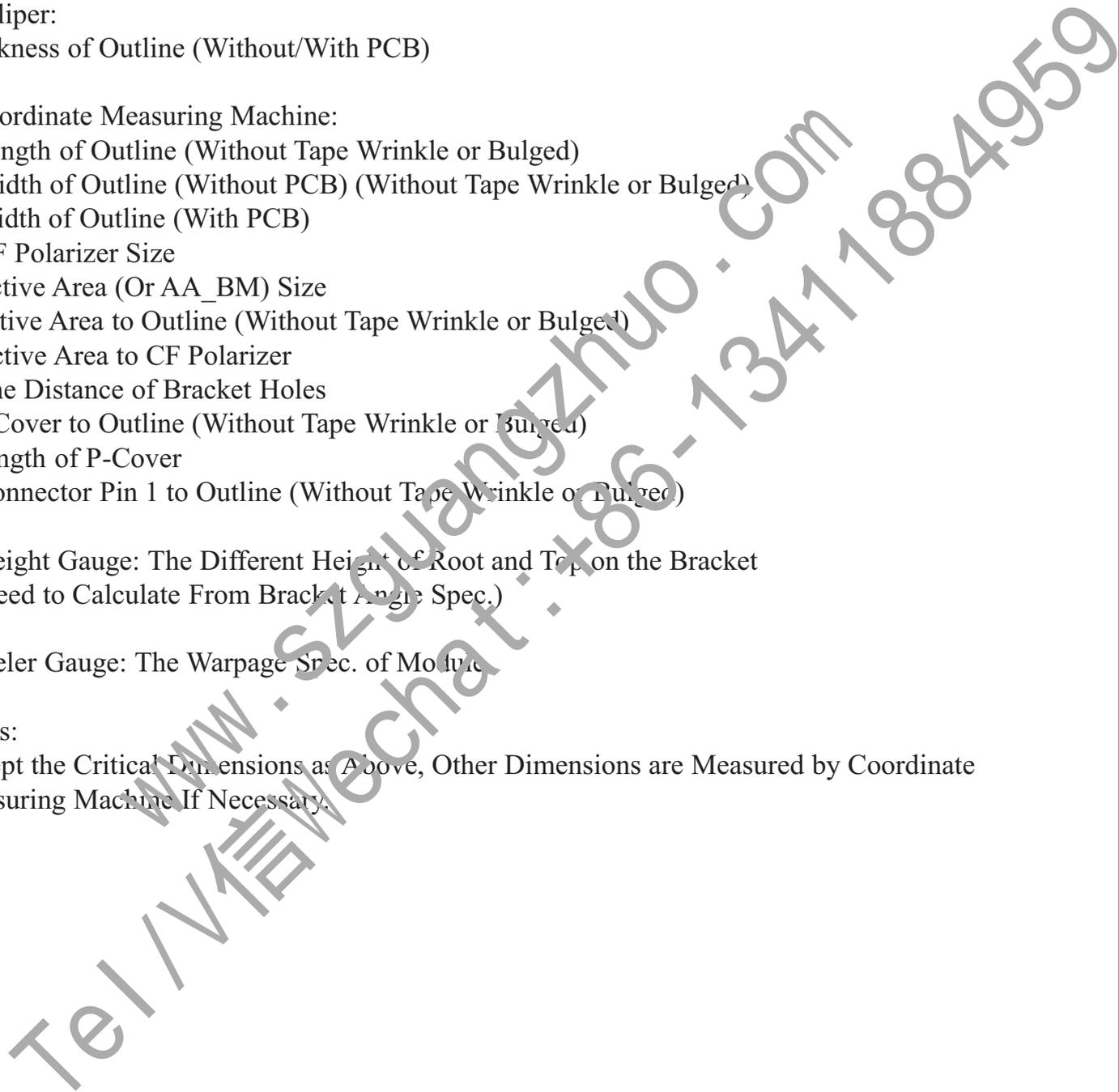
- a. Length of Outline (Without Tape Wrinkle or Bulged)
- b. Width of Outline (Without PCB) (Without Tape Wrinkle or Bulged)
- c. Width of Outline (With PCB)
- d. CF Polarizer Size
- e. Active Area (Or AA\_BM) Size
- f. Active Area to Outline (Without Tape Wrinkle or Bulged)
- g. Active Area to CF Polarizer
- h. The Distance of Bracket Holes
- i. P-Cover to Outline (Without Tape Wrinkle or Bulged)
- j. Length of P-Cover
- k. Connector Pin 1 to Outline (Without Tape Wrinkle or Bulged)

3. Height Gauge: The Different Height of Root and Top on the Bracket  
(Need to Calculate From Bracket Angle Spec.)

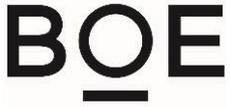
4. Feeler Gauge: The Warpage Spec. of Module

Notes:

Except the Critical Dimensions as Above, Other Dimensions are Measured by Coordinate Measuring Machine If Necessary.



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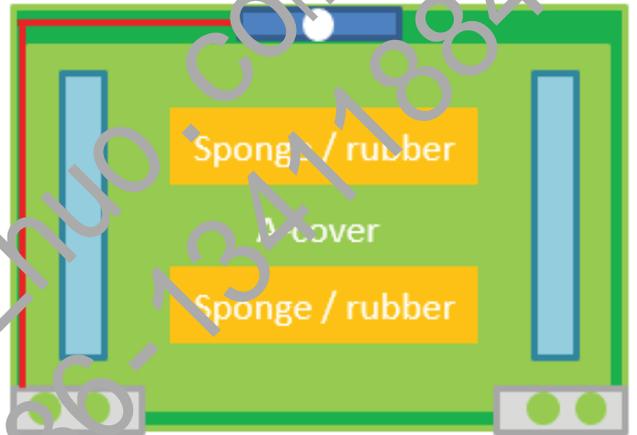
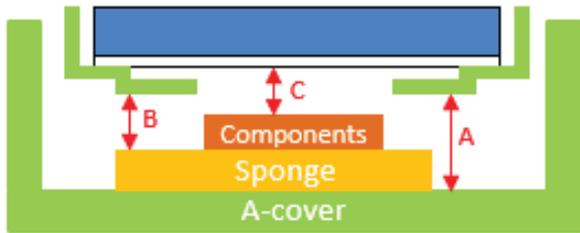
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Appendix B

LCM to A-Cover / sponges Z-gap



	Plastic Cover	Metal Cover
A	≥ 1.0mm	≥ 0.8mm
B	≥ 0mm	
C	> 0.5mm	

Purpose

The reflector area is very sensitive, BOE would suggest that design enough z-gap to decrease the risk of water ripple, white spots and other abnormal display

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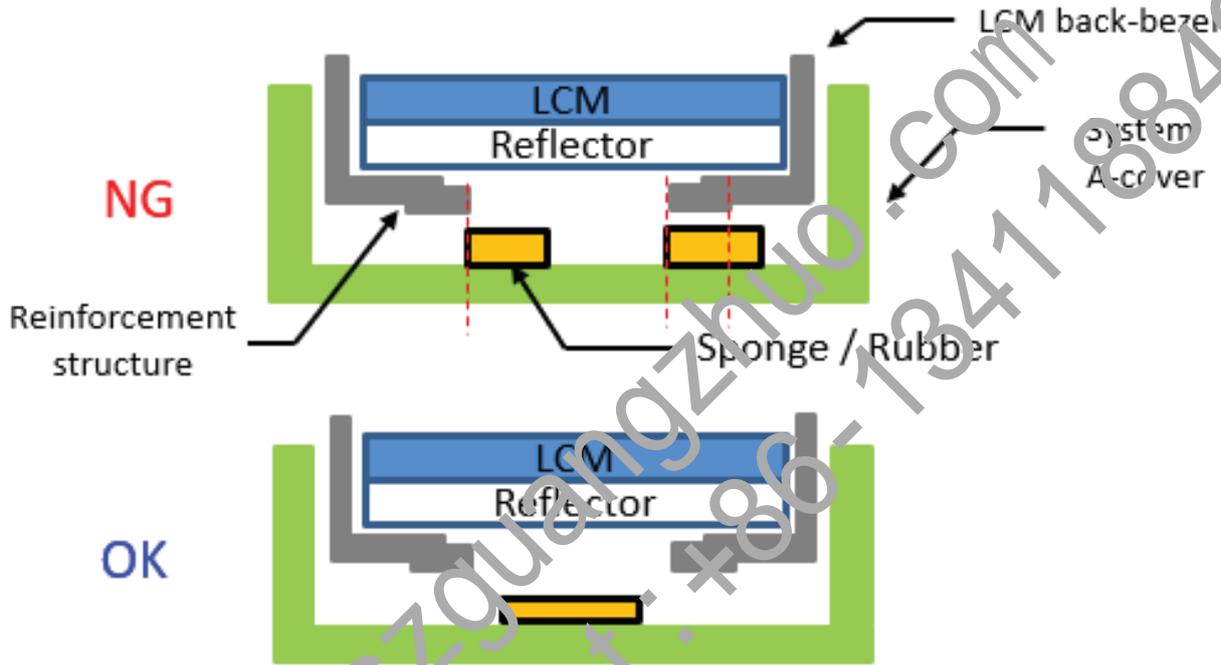
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**LCM to A-Cover / sponges z-gap**



Purpose	<p>If attach sponges or rubbers which correspond to white reflector area, it may cause white spot, pooling or other relative issues. BOE would suggest that attach wide range sponges / rubbers which can cover the LCM back-bezel opening</p>
---------	--

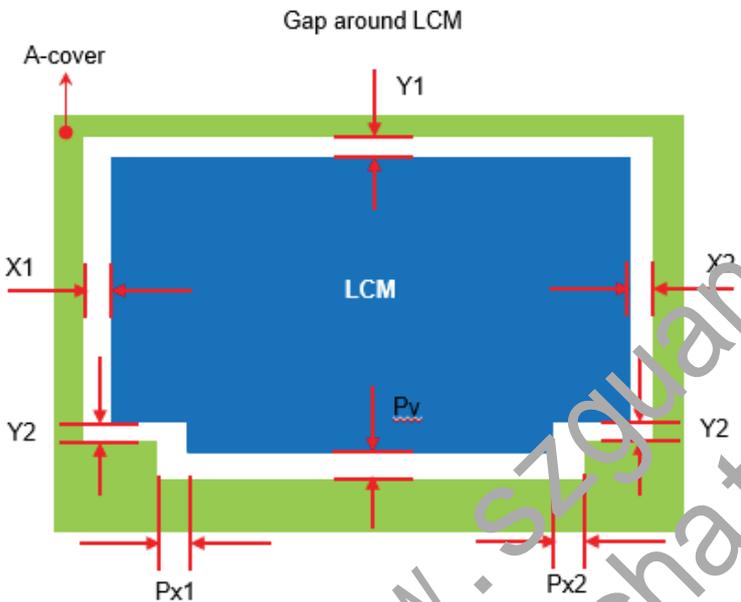
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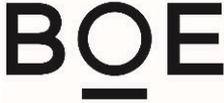
**LCM to side wall / protrusions**



	Normal border (screws)	Narrow border (fix by tapes)
X1 / X2	Min: 0.45mm	Min: 0.35mm
Y1 / Y2	Min: 0.45mm	Min: 0.35mm
Px1 / Px2	Min: 0.55mm	
Pv	Min: 0.55mm	

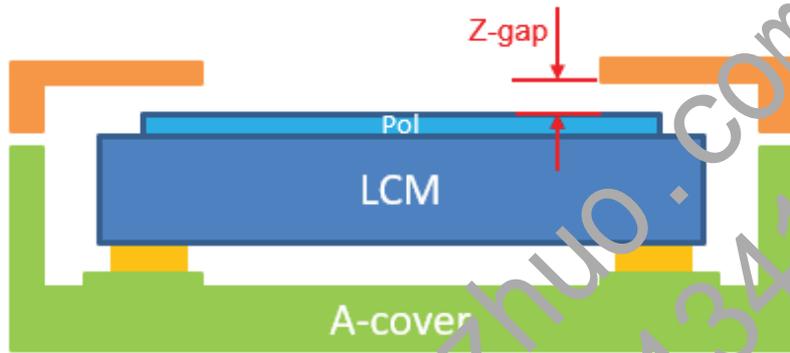
**Purpose** BOE would suggest that design enough gap around LCM to prevent shock test failure, or interference, cell crack, abnormal display...etc. in the reliability test

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**LCM to B-cover z-gap**

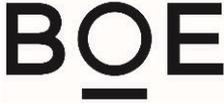


Bezel Tape	Z-Gap
Without	0.15 ~ 0.25mm
With	0.15 ~ 0.20mm

Purpose	Too less z-gap between system B-cover and LCM top pol has high risk that may cause cell crack, pooling, light leakage and other issues
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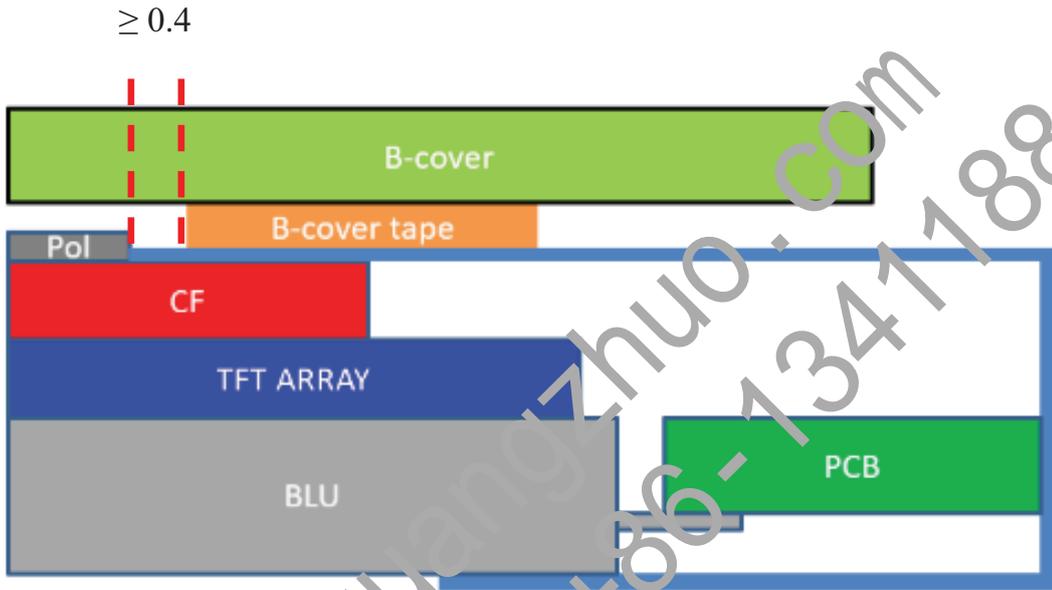
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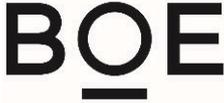
**B-cover tape to top pol edge**



If attach b-cover and LCM with tapes,  
Please let tapes to be located out of top pol edges 0.4mm away on 4 sides

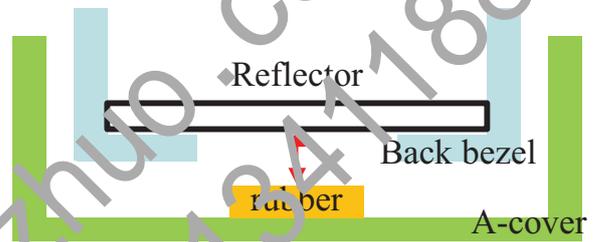
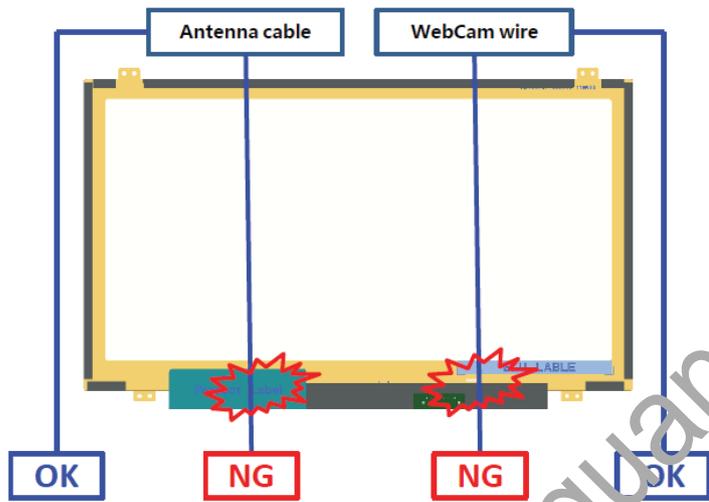
Purpose	To avoid the B-cover tape override top pol then cause pooling or light leakage issue
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**Antenna Cable & Webcam wire**



If sponge within the reflector area is necessary, we suggest that the gap between reflector and sponge is more than 0.5mm

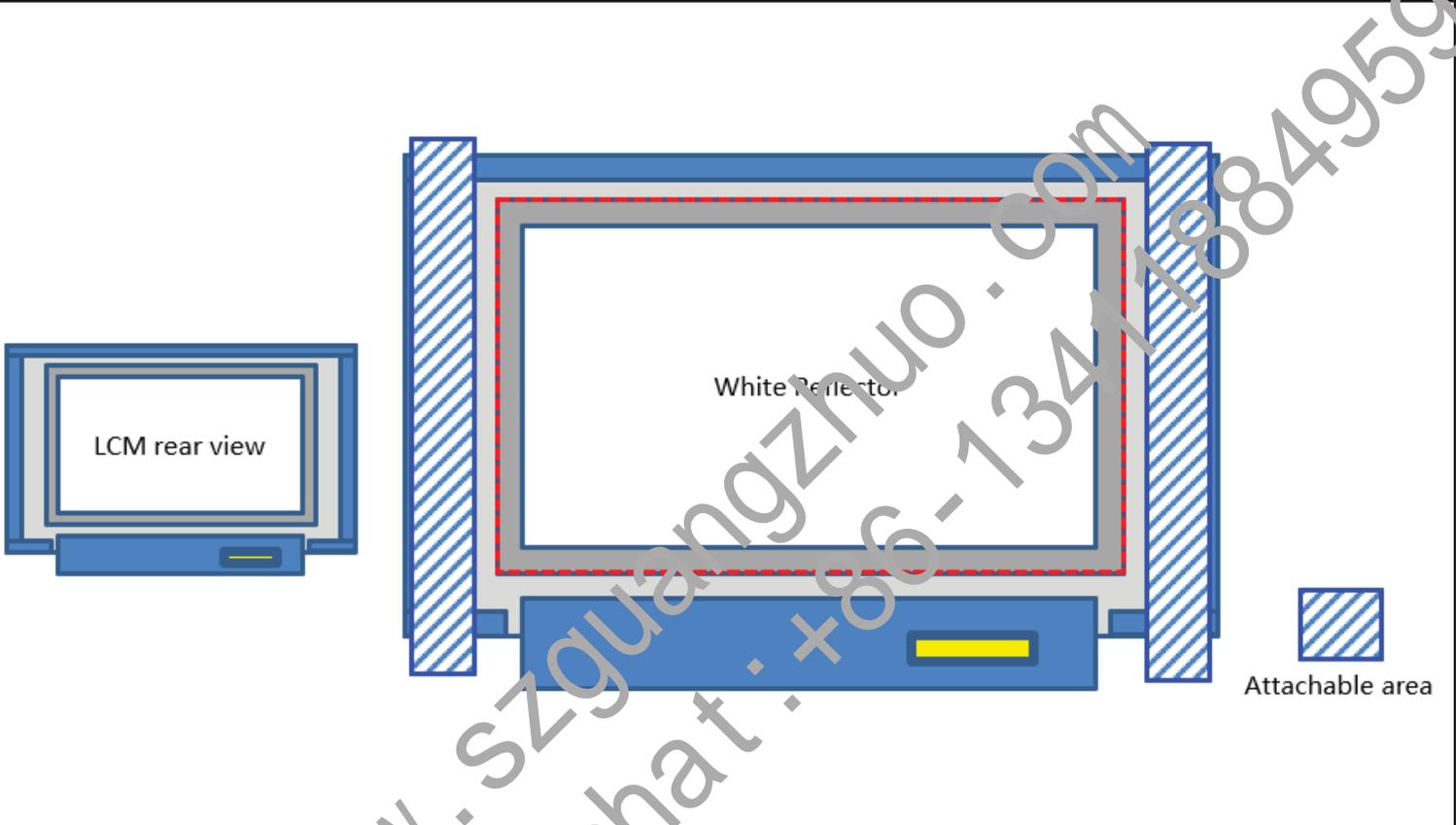
Purpose	<ol style="list-style-type: none"> <li>BOE would suggest that do not set Antenna or WebCam cable / wire go behind LCM to avoid back crack test, hinge test ,twist test or pogo test with abnormal display</li> <li>If the cable / wire is necessary to go behind LCM, please make a groove with rounds of characters to protect the cable / wire, or attach with higher sponges / rubbers adjacent to the cable / wire route</li> <li>Suggest that attach the cable / wire with tapes to A-cover</li> <li>Do not attach anything with LCM reflector area. If attach cable / wire with LCM reflector area, it may cause pooling, white spot, light leakage and other related issues</li> </ol>
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Appendix B

**LCM paste area**



Purpose	If use the stretch remove tapes to fix LCM with A-cover, please set the stretch remove tapes correspond to the LCM back-bezel and do not let the tapes override the back-bezel's level step of opening
---------	--

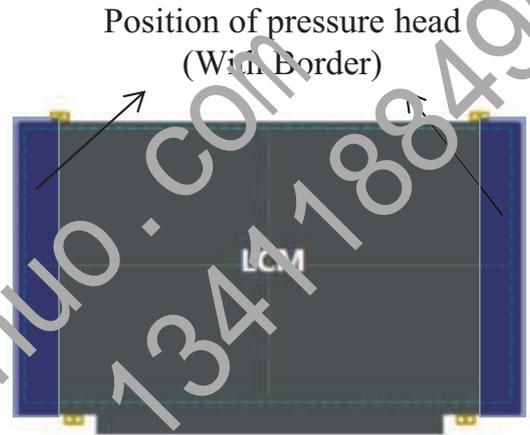
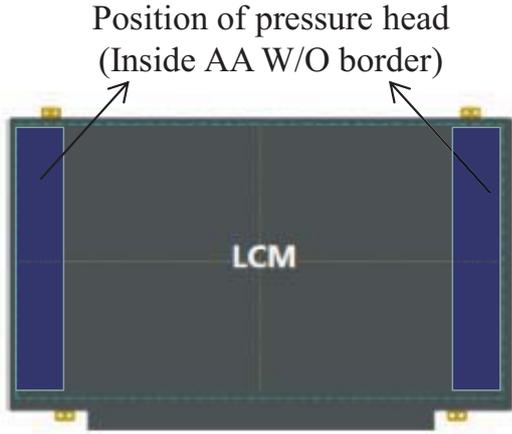
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**LCM pressable area**



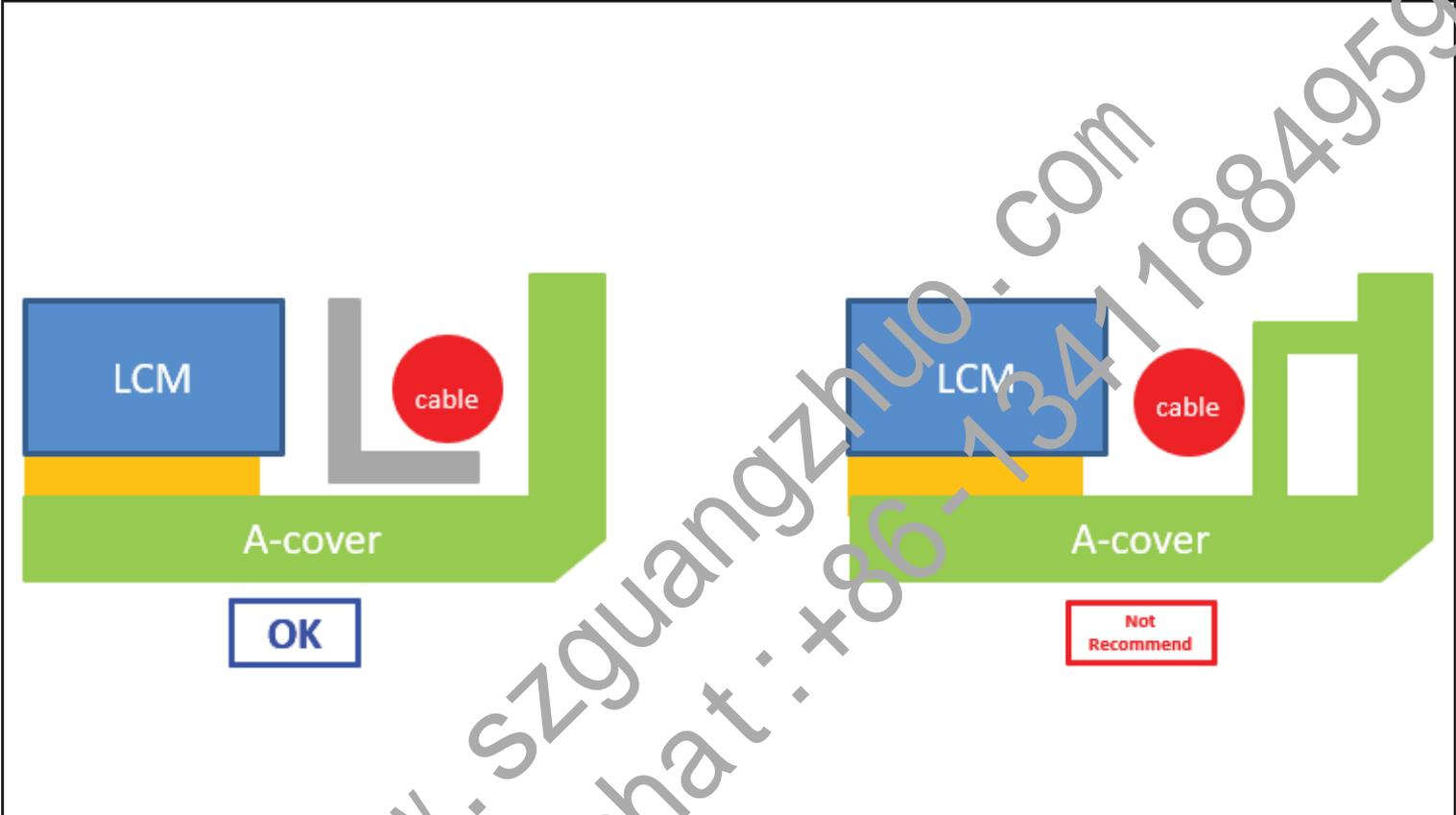
Purpose	<ol style="list-style-type: none"> <li>1. If LCM is fixed on A-cover by using the press jig during assembling.</li> <li>2. To avoid panel broken, the design of pressure head of press jig can not only pin on cell panel. The pressure head needs to pin on the LCM frame, which the LCM frame can share the pressure of the pressing head.</li> </ol>
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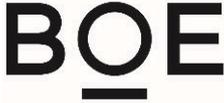
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**Wire setting**



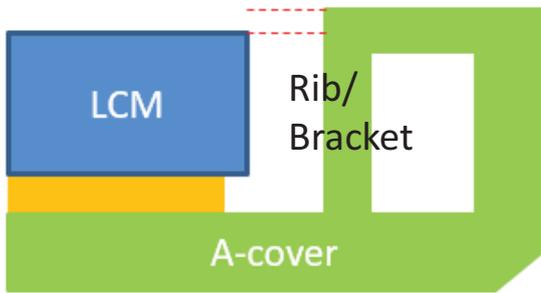
Purpose	Wires should be placed between protrusions/side wall and A-cover. If place the wires between LCM and Protrusions/side wall, it may interfere with LCM when assembling, or even cause LCM broken in reliability test.
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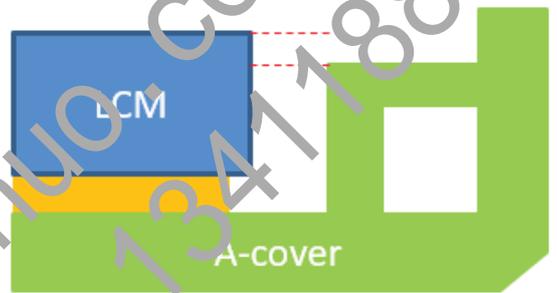
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**A-cover strength**



OK



Not Recommend

Purpose	<ol style="list-style-type: none"> <li>BOE would recommend that structural Rib/Bracket height is higher than LCM, in order to avoiding pressures to LCM.</li> <li>The L-shape Bracket is recommended.</li> </ol>
---------	--

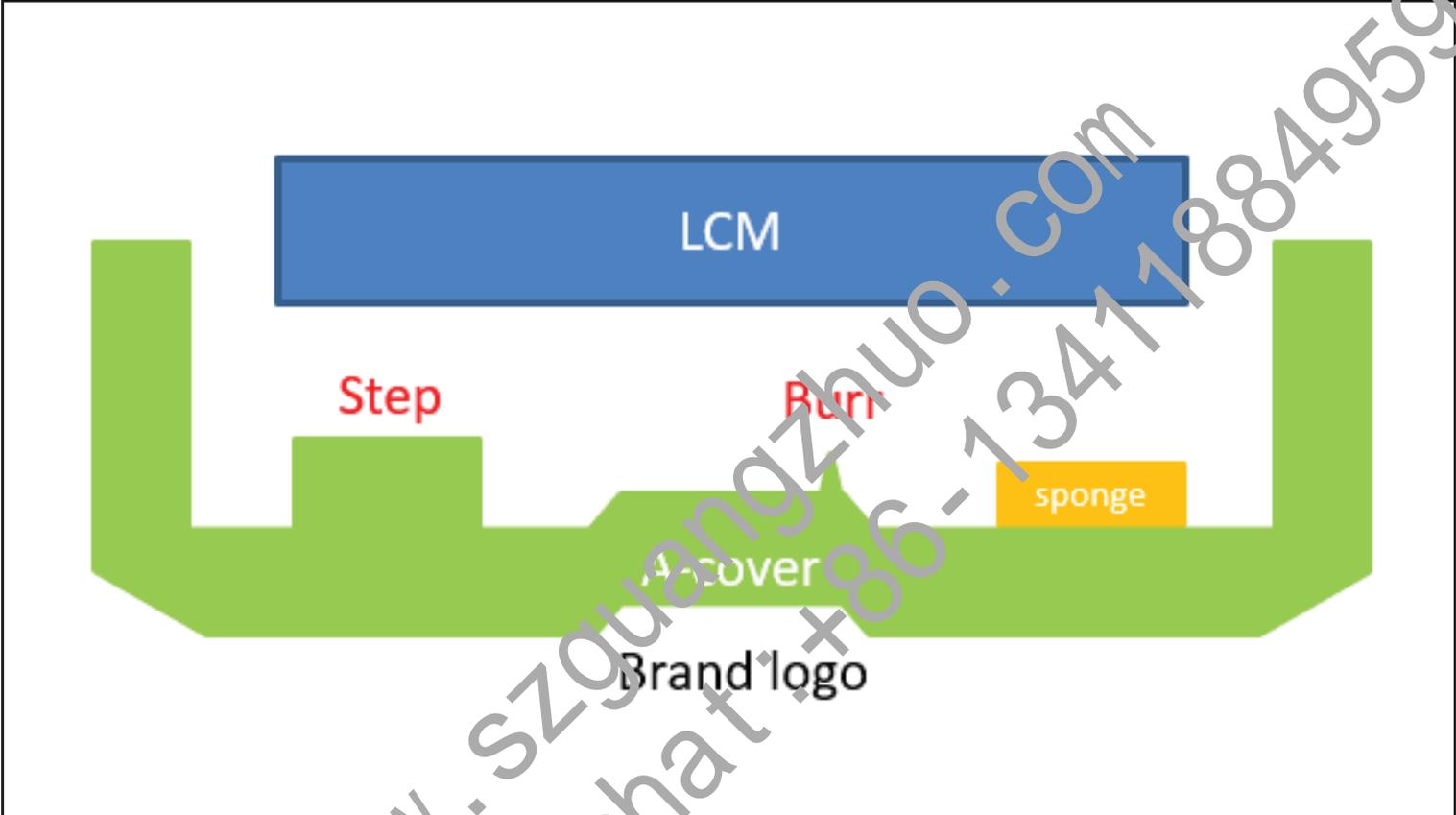
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**System A-cover Inner Surface**



Purpose	There should not exist any burr, segment gap or protrusions beside Logo, which may cause White Spot or Glass Broken by stress concentration.
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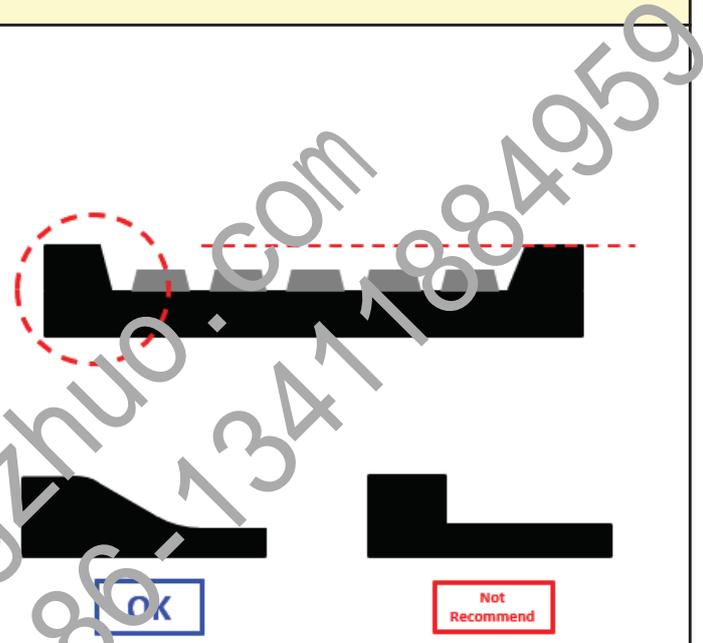
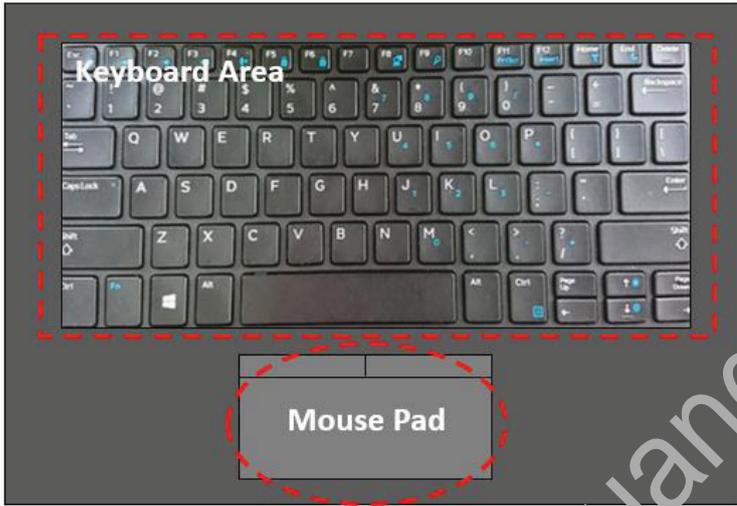
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Appendix B

**Keyboard area & Mouse pad**



**Purpose** The transition surface between keyboard and mouse pad should be smooth and without vertical steps\ too large level steps

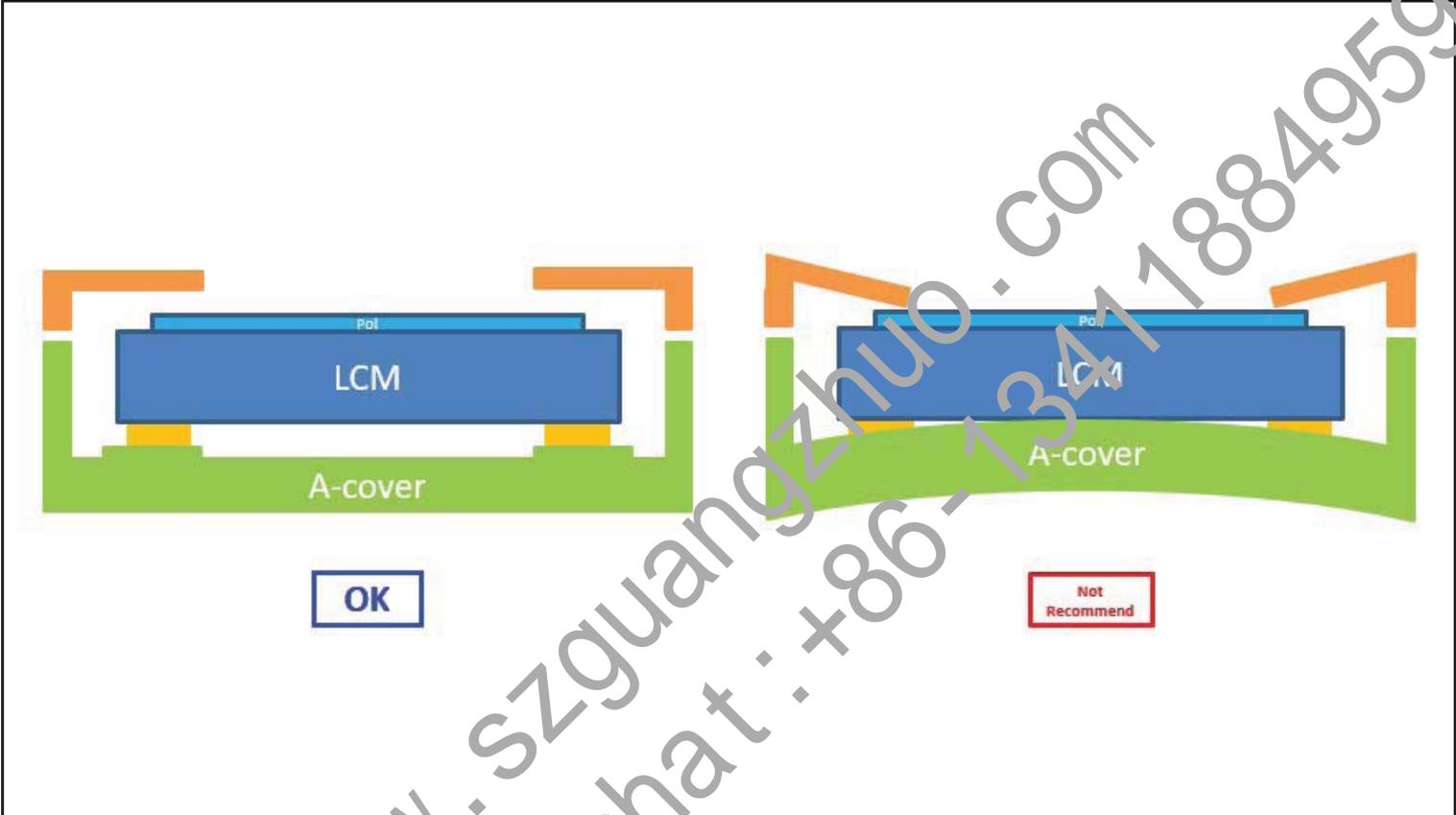
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**System cover reliability**



Purpose	<ol style="list-style-type: none"> <li>1. No interference between system and LCM in assembly process except compressible grounding gaskets</li> <li>2. The permanent deformation which caused by Reliability test is not allowed to contact LCM</li> </ol>
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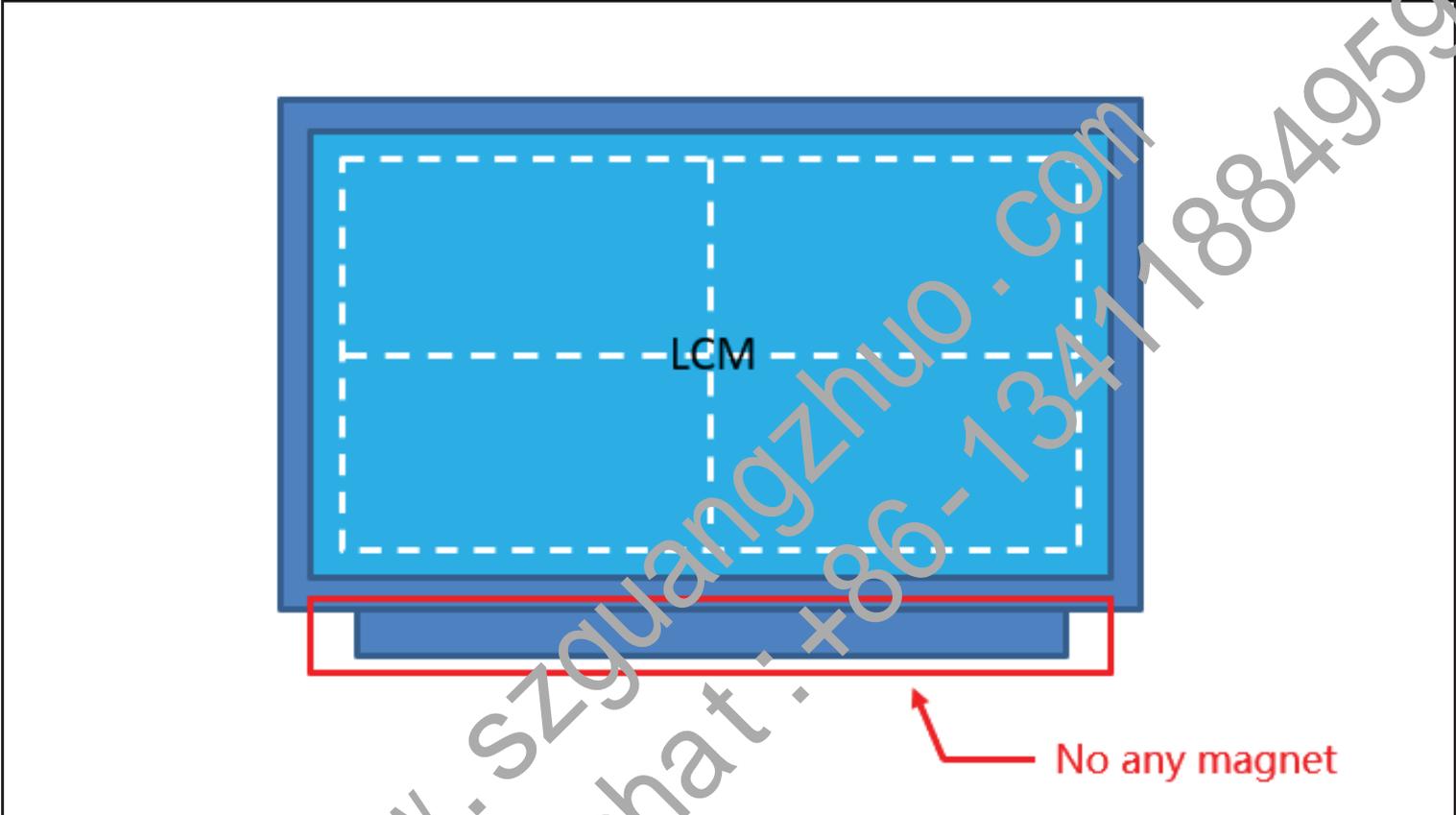
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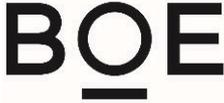
**A/B-cover near LCD PCBA**



Purpose	There should not be any magnet object close to LCM PCBA, it may cause physical or electricity noise issue
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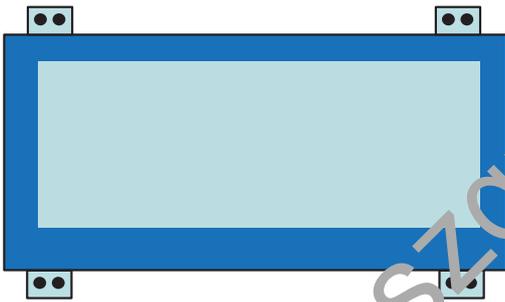
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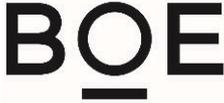
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**A-cover add sponges on Boss side wall**



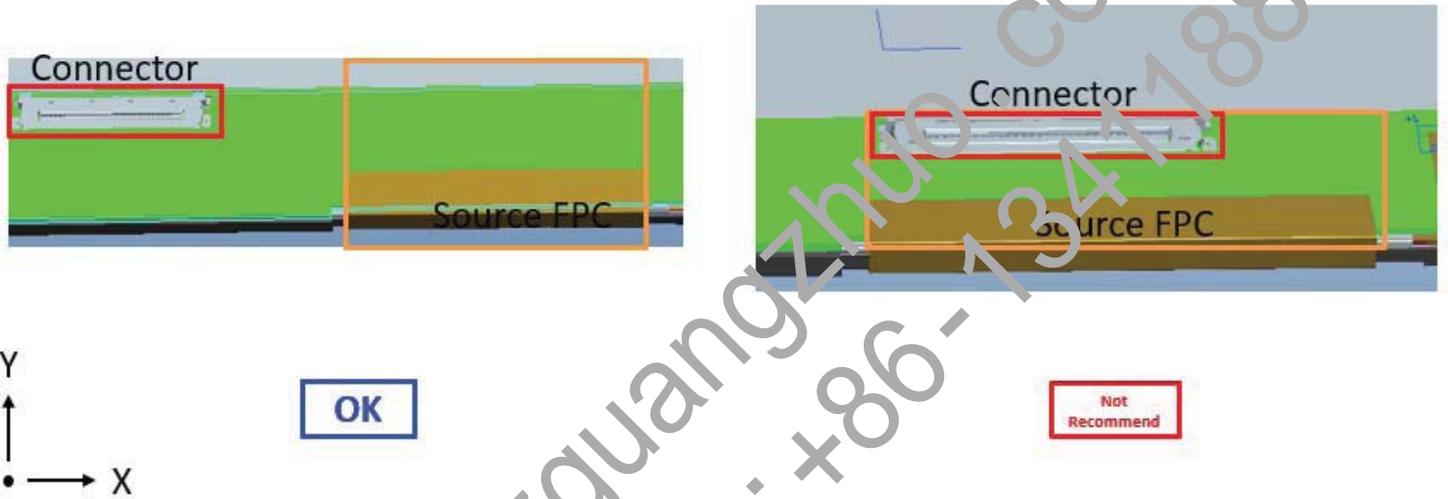
Purpose	BOE would suggest to attach Sponges to the side-wall of the Boss column of A-cover to reduce the risk of panel broken in assembling process.
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**LCM to A-Cover / sponges z-gap**



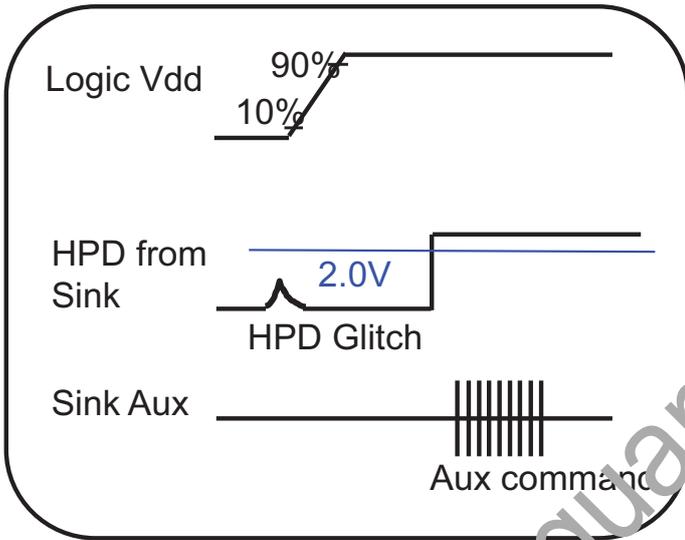
Purpose	Bent type product: The System Connector should not overlap with LCM FPC in X-direction, it may cause FPC lead broken during system connector plug and un-plug process (Panel FPC Bonding location is related to Mask and can not be changed easily)
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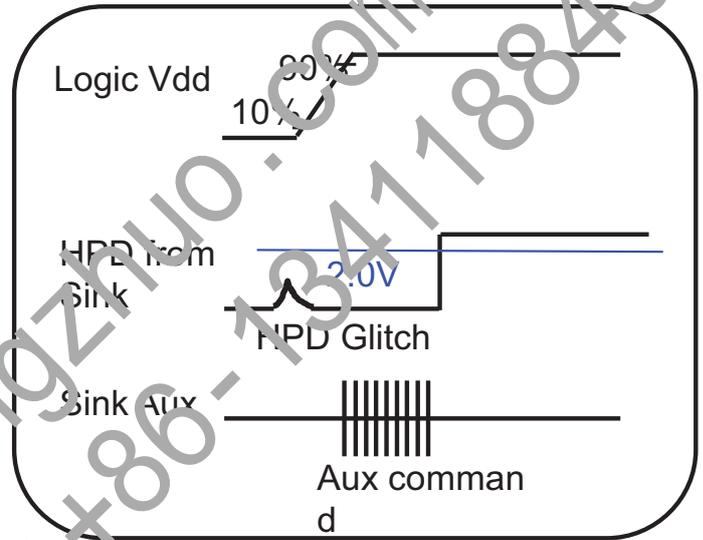
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Appendix C

**HPD Signal recognition**



Normal Signal (Ignore HPD Glitch)



Abnormal Signal

Purpose

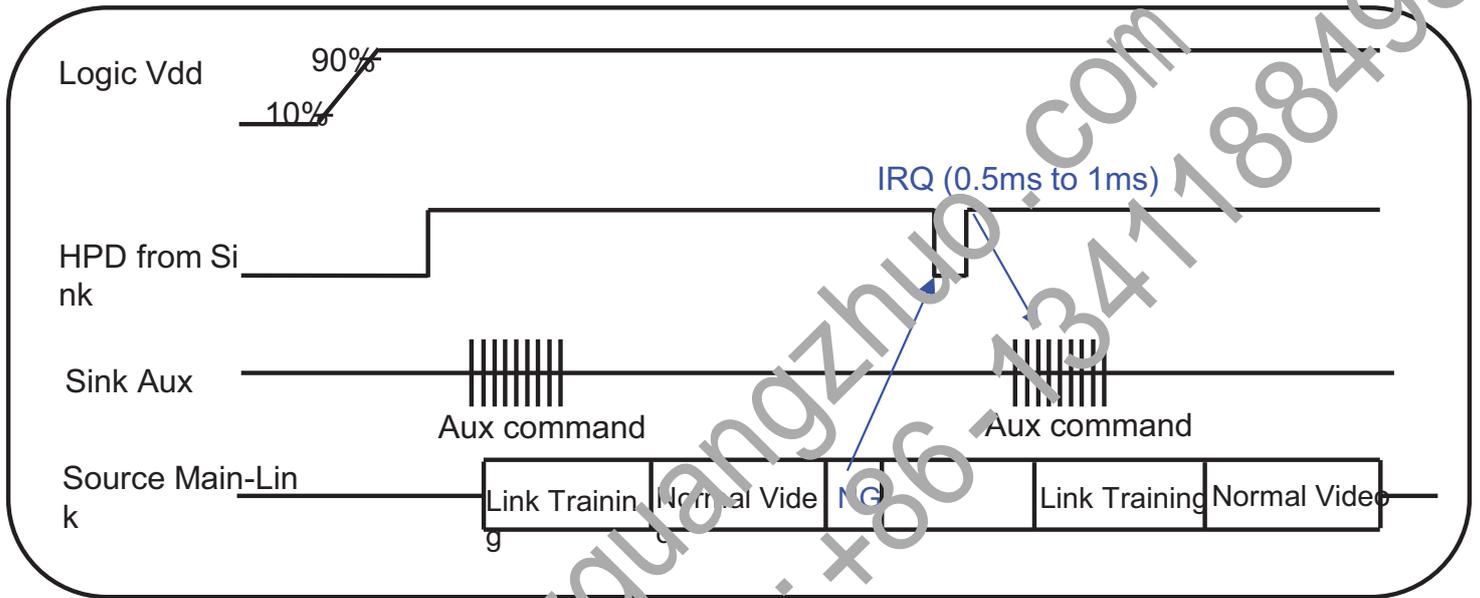
When HPD glitch voltage less than 2.0(V), system signal can't output AUX command data.

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**HPD Signal Definition IRQ (Interrupt Request)**



<b>Purpose</b>	When HPD signal low than 0.5ms to 1ms, the source device should check sink status field from the DPCE and take link training again.
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## Appendix C

### Main link eye diagram of TP3

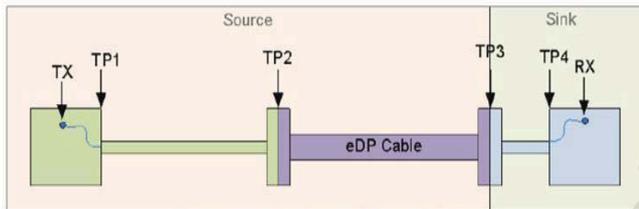
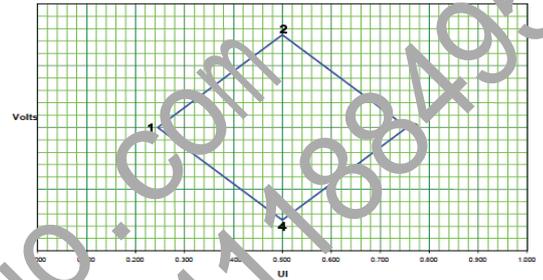


Figure 4-1: Embedded Link Reference Points



Measured TP3 on LCM connector.

Downstream Device Mask at TP3

	UI	Voltage
1	0.246	0
2	0.5	0.075
3	0.755	0
4	0.5	-0.075

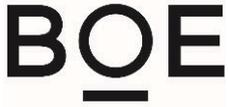
Eye for TP3 at HBR

	UI	Voltage
1	0.375	0
2	0.5	0.023
3	0.625	0
4	0.5	-0.023

Eye for TP3 at RBR

#### Purpose

1. Main Link EYE Diagram should meet TP3 point of VESA.
2. The measure method is through access fixture.



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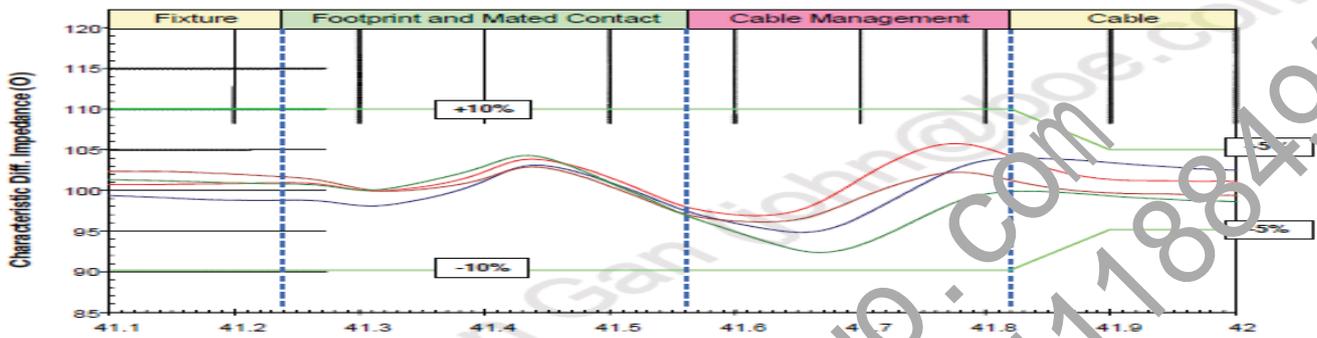
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**Impedance Profile through a DP Connector**



Differential Impedance Profile Measurement Data Example

Segment	Differential Impedance Value	Maximum Tolerance
Fixture	100Ω/VESA	±10%
Connector	100Ω/VESA	±10%
Wire management	100Ω/VESA	±10%
Cable	100Ω/VESA	±5%

Impedance Profile Values for Cable Assembly

Purpose

Cable Impedance Profile 100ohm for Cable Assembly

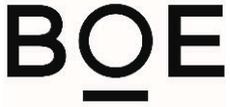
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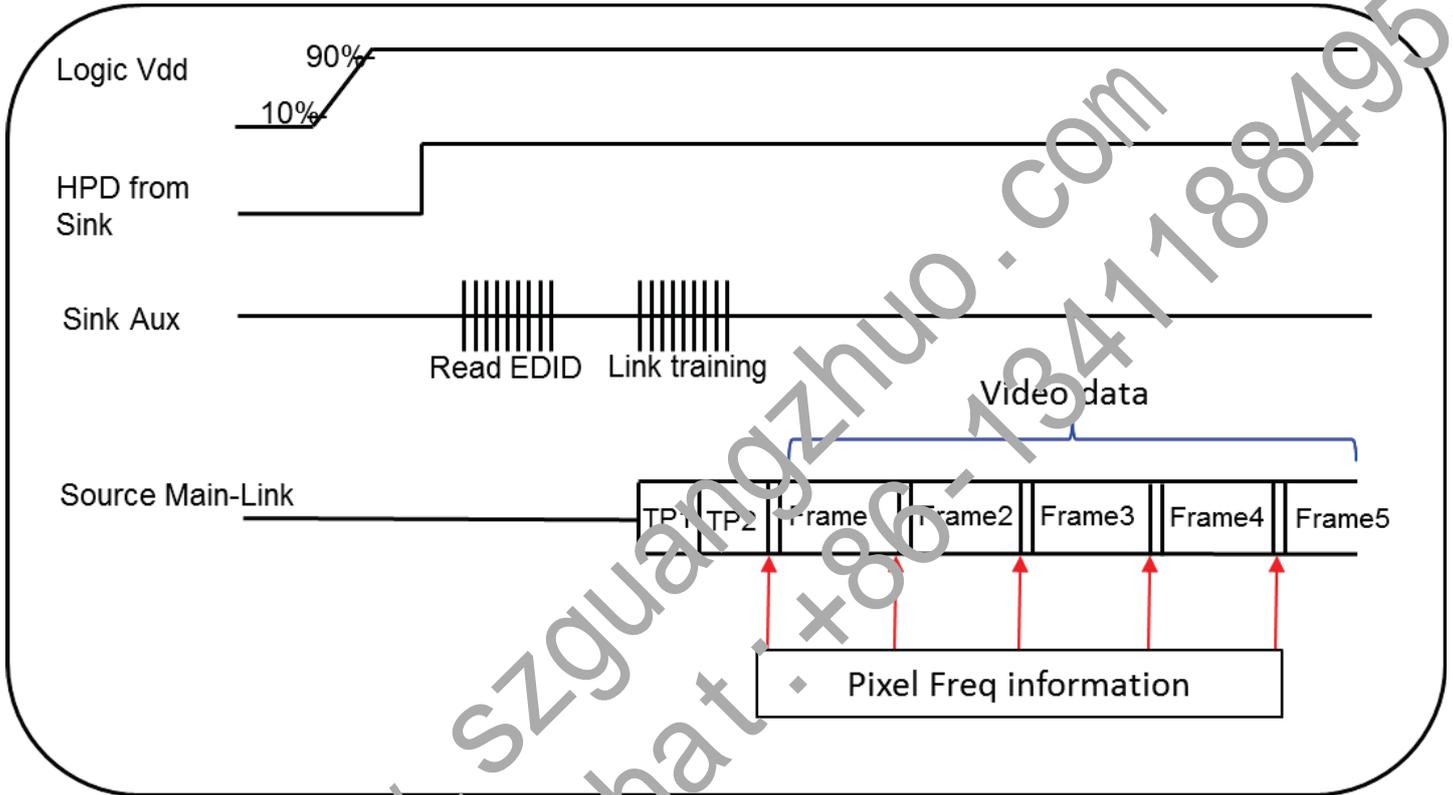
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**Main Link Pixel Freq information value of MSA data**



Purpose

1. It need to fix pixel freq information value of MSA data output to prevent the initial abnormal pixel freq information value from incoming after power on.
2. BOE can read DPCD to check this value. Ex: BIOS is 1.62G , but into windows is 2.7G.

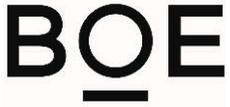
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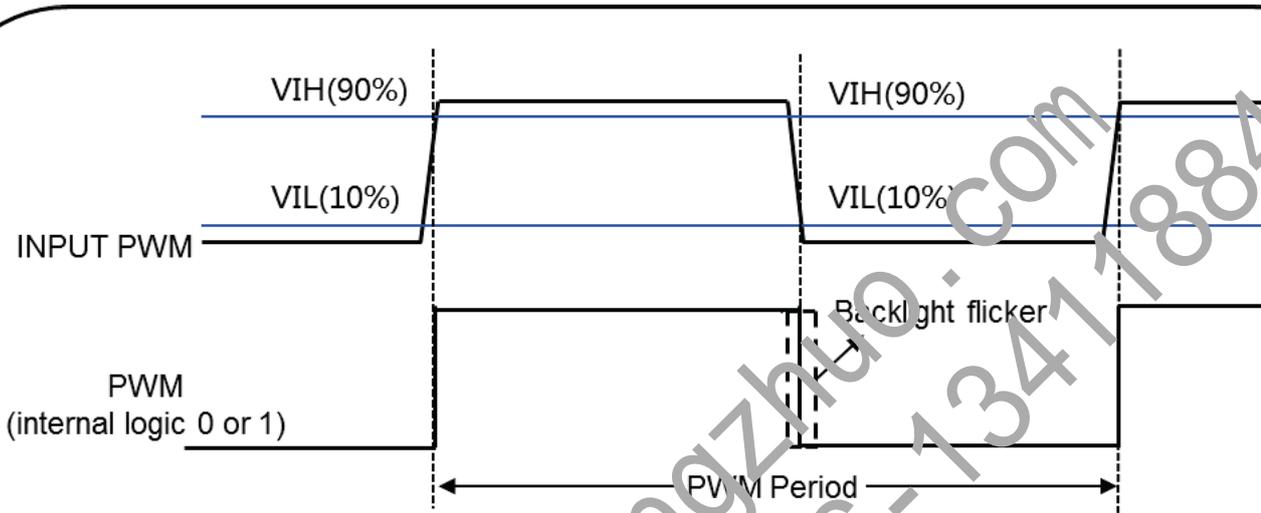
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**System Input PWM Rising/Faling time**



Example:

Freq	Cycle Time	PWM Rising Time	PWM Falling Time
200Hz	5ms	≤1us	≤1us
1KHz	1ms	≤200ns	≤200ns

Purpose

1. LED driver need to calculate the duty cycle of input PWM signal.
2. To avoid backlight flicker visible on LCD, system input PWM suggest :  
PWM rising ≤ 200ppm\*cycle time ; PWM falling ≤ 200ppm\*cycle time.

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