

TITLE : NV140WUM-N6A

Customer: DELL

Product Specification

Rev. 0

(DELL DPN : G9EC5)

HEFEI BOE Optoelectronics Technology CO., LTD

REVISION HISTORY

() Preliminary Specification

(√) Final Specification

Revision No.	Page	Description of Changes	Date	Prepared
P0	63	Initial Release	2022.5.30	Zhou Kun
P1	63	Update X11 Spec & some details	2022.8.25	Zhou Kun
0	63	Update A00 Spec & some details Add LCM_AA to flange hole center dimension	2022.11.25 2023.1.4	Zhou Kun

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1.0 GENERAL DESCRIPTION

1.1 Introduction

NV140WUM-N6A is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 14.0inch diagonally measured active area with Full-HD+ resolutions (1920 horizontal by 1200 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.7M (True 8bit) colors and color gamut 100% sRGB typical. The TFT-LCD panel used for this module is a low reflection and higher color type. Therefore, this module is suitable for Notebook PC. The LED driver for back-light driving is built in this model. All input signals are eDP1.3 interface compatible.

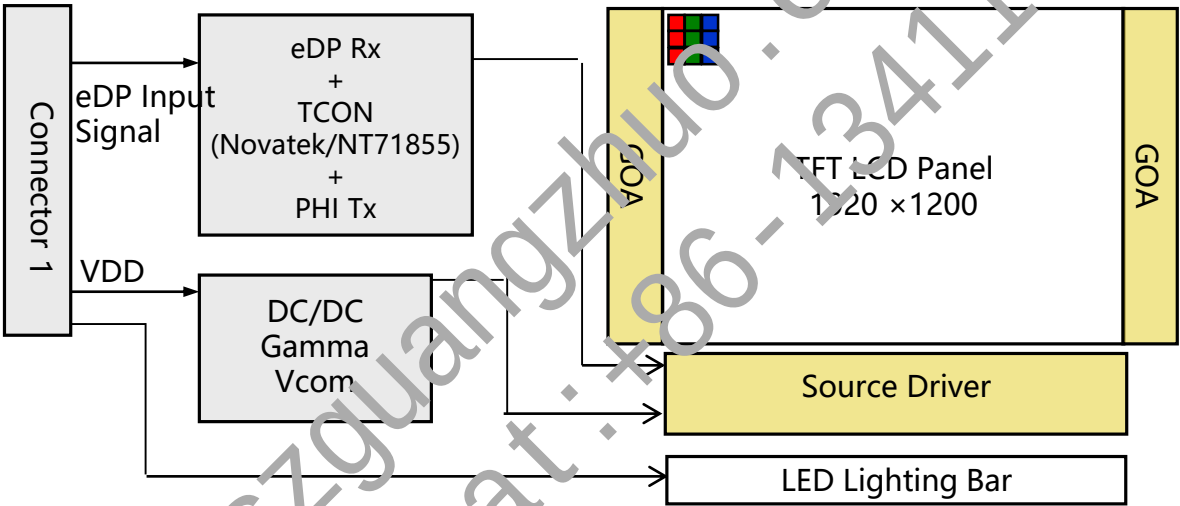


Figure 1. Drive Architecture

1.2 Features

- 2 lane eDP interface with 2.7Gbps link rates
- Thin and light weight, Low Blue Light
- 16.7M (True 8bit) color depth, color gamut 100% sRGB typ.
- Single LED lighting bar (Bottom side/Horizontal Direction)
- Data enable signal mode
- Side mounting frame
- Green product (RoHS & Halogen free product)
- On board LED driving circuit
- Low driving voltage and low power consumption
- On board FID chip
- DPCD Version 1.2
- Function : PSR/SDRRS/BIST
- Adjust backlight brightness with DC mode

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1.3 Application

- Notebook PC (Wide type)

1.4 General Specification

The followings are general specifications at the model NV140WUM-N6A. (listed in Table 1)

<Table 1. General Specifications>

Parameter	Specification	Unit	Remarks
Active area	301.5936(H) x 188.496(V)	mm	
Number of pixels	1920 (H) ×1200 (V)	pixels	
Pixel pitch	157.08(H) ×157.08 (V)	um	
Pixel arrangement	RGB Stripe		
Display colors	16.7M (8bit)		
Color gamut	100% sRGB (typ.)		
Display mode	Normally Black		
Dimensional outline	306.6 typ (H) ± 0.3 195.35 typ (V) ± 0.5 (V/COF bending)	mm	
Weight	240(Max.)	g	
Surface treatment	HC		
Surface hardness	3H		
Back-light	Bottom edge side, 1-LED lighting bar type		Note 1
Power consumption	P _D : 0.5(Max.)	W	@Mosaic
	P _{BL} : 2.33(Max.)	W	@VLED=12V
	P _{Total} : 2.83(Max.)	W	@Mosaic

2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Absolute Maximum Ratings>

Ta=25+/-2°C

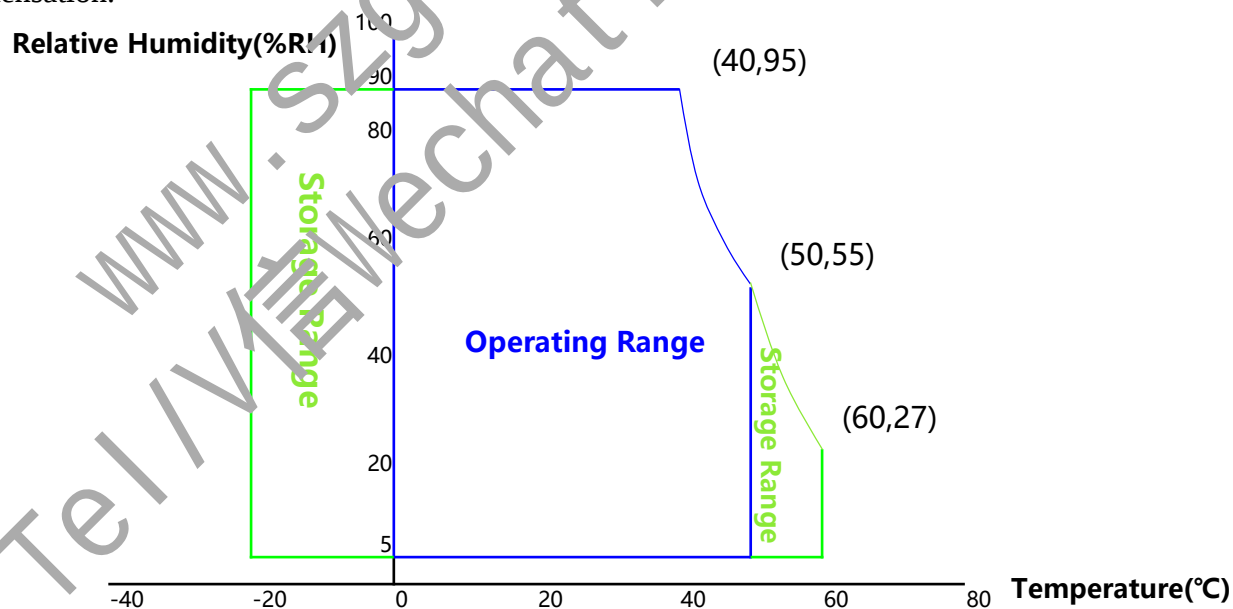
Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V _{DD}	-0.3	4.0	V	Note 1
eDP input Voltage	V _{eDP}	0	2.0	V	
Logic Supply Voltage	V _{IN}	V _{SS} -0.3	V _{DD} +0.3	V	
Operating Temperature	T _{OP}	0	+50	°C	Note 2
Storage Temperature	T _{ST}	-20	+60	C	

Notes :

1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.

2. Temperature and relative humidity range are shown in the figure below.

95 % RH Max. (40 °C ≥ Ta) Maximum wet-bulb temperature at 39°C or less.(Ta >40°C)No condensation.



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3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

< Table 3. Electrical Specifications > Ta=25+/-2°C

Parameter			Min.	Typ.	Max.	Unit	Remarks	
Power Supply Voltage		V _{DD}	3.0	3.3	3.6	V	Note 1	
Permissible Input Ripple Voltage		V _{RF}	-10% VDD	-	+10% VDD	V	@ V _{DD} = 3.3V, note4	
CABC Control Level		High Level	0.8 VDDIO	-	3.6	V	@V _{DDIO} =1.8 or 2.5V(根据实际填写具体数值)	
		Low Level	0	-	0.15 VDDIO	V		
BIST Control Level		High Level	0.8 VDDIO	-	3.6	V		Note 5
		Low Level	0	-	0.15 VDDIO	V		
Power Supply Inrush Current		I _{inrush}	-	-	2	A	Note3	
Power Supply Current	Mosaic	I _{DD}	-	125	151	mA		
	Red		-	123	151	mA		
	Green		-	123	151	mA		
	Blue		-	123	151	mA		
Power Consumption	Mosaic	P _M	-	0.375	0.5	W		
	Red	P _R	-	0.369	0.5	W		
	Green	P _G	-	0.369	0.5	W		
	Blue	P _B	-	0.369	0.5	W		
	BLU	P _{BL}	-	2.218	2.33	W	Note 2	
	Total	P _{Total}	-	2.587	2.85	W	Note 1	

3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

Notes :

- The supply voltage is measured and specified at the interface connector of LCM.
The current draw and power consumption specified is for 3.3V at 25 °C.(Typ. value for reference)
 - Mosaic pattern 8*8
 - R/G/B patterns



(a) (b)
Figure 3. Power Measure Patterns

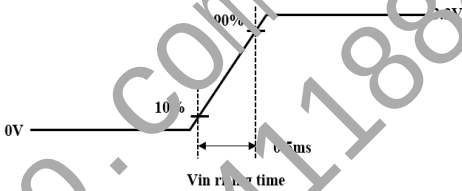


Figure 4. Inrush Measure Condition

- Calculated value for reference ($V_{LED} \times I_{LED}$) , The power consumption with LED Driver are under the $V_{LED} = 12.0V$, $25^{\circ}C$, PWM Duty 100% .
- Measure condition (Figure 4)
- Input voltage range:3.0~3.6V.Test condition: Oscilloscope bandwidth 20MHz, AC coupling
- CABC&BIST setting

Pin No	Define	Enable	Disable
14	BIST	Pull High	Pull Low/Floating

3.2 Backlight Unit

< Table 4. LED Driving Guideline Specifications > Ta=25+/-2°C

Parameter		Min.	Typ.	Max.	Unit	Remarks
LED Forward Voltage	V _F	-	-	5.4	V	
LED Forward Current	I _F	-	10	-	mA	
LED Power Input Voltage	V _{LED}	5	12	21	V	
LED Power Input Current	I _{LED}	-	194.2	-	mA	Note 1
LED Power Consumption	P _{LED}	-	-	2.33	W	
Power Supply Voltage for LED Driver Inrush	I _{led} inrush	-	-	2	A	
LED Life-Time	N/A	10,000	-	-	Hour	I _F = 20mA Note 2
EN Control Level	Backlight On	1.2	-	5.0	V	Note 4
	Backlight Off	0	-	0.6	V	
PWM Control Level	High Level	1.2	-	5.0	V	
	Low Level	0	-	0.6	V	
PWM Control Frequency	F _{PWM}	200	-	10,000	Hz	
Duty Ratio		5	-	100	%	Note 3

- Notes :
- 1. The current and power consumption with LED Driver are under the VLED = 12.0V , 25°C, PWM Duty 100% .
 - 2. The LED life-time define as the estimated time to 50% degradation of initial luminous.
 - 3. Measure condition (Figure 5).
 - 4.LED_EN&PWM setting

Pin No	Define	Enable	Disable
22	LED_EN	Pull High	Pull Low/Floating
23	PWM	Pull High	Pull Low/Floating

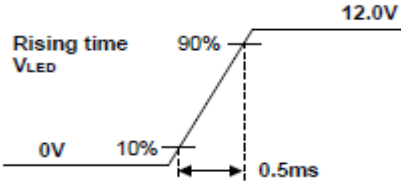


Figure 5. Inrush Measure Condition

3.3 LED Structure



Figure 6. LED Structure

4.0 OPTICAL SPECIFICATION

4.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = $25\pm 2^{\circ}\text{C}$) with the equipment of luminance meter system (PR730&PR810) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and ϕ equal to 0° . We refer to $\theta\phi=0$ ($=03$) as the 3 o'clock direction (the "right"), $\theta\phi=90$ ($=012$) as the 12 o'clock direction ("upward"), $\theta\phi=180$ ($=09$) as the 9 o'clock direction ("left") and $\theta\phi=270$ ($=06$) as the 6 o'clock direction ("bottom"). While scanning θ and/or ϕ , the center of the measuring spot on the display surface shall stay fixed. The backlight should be operating for 30 minutes prior to measurement. VDD shall be $3.3\pm 0.3\text{V}$ at 25°C . Optimum viewing angle direction is 6 o'clock.

4.2 Optical Specifications

<Table 5. Optical Specifications>

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ_3	$CR > 10$	88	-	-	Deg.	Note 1
		Θ_9		88	-	-	Deg.	
	Vertical	Θ_{12}		88	-	-	Deg.	
		Θ_6		88	-	-	Deg.	
Luminance Contrast Ratio		CR	$\Theta = 0^\circ$	1000	1200	-		Note 2
Luminance of White	5 Points	V_w	$\Theta = 0^\circ$ $I_{LED} = 10mA$	255	300	-	cd/m ²	Note 3
White Luminance Uniformity	5 Points	ΔY_5		80	-	-		Note 4
	13 Points	ΔY_{13}		65	-	-		
White Chromaticity		W_x	$\Theta = 0^\circ$	0.283	0.313	0.343		Note 5
		W_y		0.299	0.329	0.359		
Reproduction of Color	Red	R_x	$\Theta = 0^\circ$	Typ.-0.03	0.650	Typ.+0.03		
		R_y			0.329			
	Green	G_x			0.297			
		G_y			0.623			
	Blue	B_x			0.147			
		B_y			0.045			
Color Gamut				95	100	-	%	SRGB
Response Time (Rising + Falling)		T_{RT}	$T_a = 25^\circ C$ $\Theta = 0^\circ$	-	30	35	ms	Note 6
Cross Talk		CT	$\Theta = 0^\circ$	-	-	1.0	%	Note 7
Gamma		-	-	1.7	2.2	2.7		

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Notes :

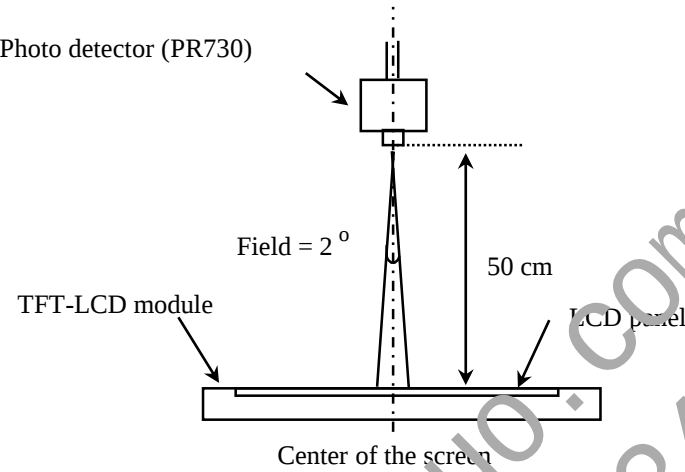
- Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 7).
- Contrast measurements shall be made at viewing angle of $\Theta=0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see Figure 7) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

- Center Luminance of white is defined as luminance values of 5 point average across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 8 for a total of the measurements per display.
- The White luminance uniformity on LCD surface is then expressed as : $\Delta Y = \text{Minimum Luminance of 5(or 13) points} / \text{Maximum Luminance of 5(or 13) points.}$ (see Figure 8 and Figure 9).
- The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels, first in red, green, blue and white. Measurements shall be made at the center of the panel.
- The electro-optical response time measurements shall be made as Figure 10 by switching the “data” input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_r , and 90% to 10% is T_f .
- Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (Y_A) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (Y_B) of that same area when any adjacent area is driven dark. (See Figure 11).

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4.3 Optical Measurements



Optical characteristics measurement setup

Figure 7. Measurement Set Up

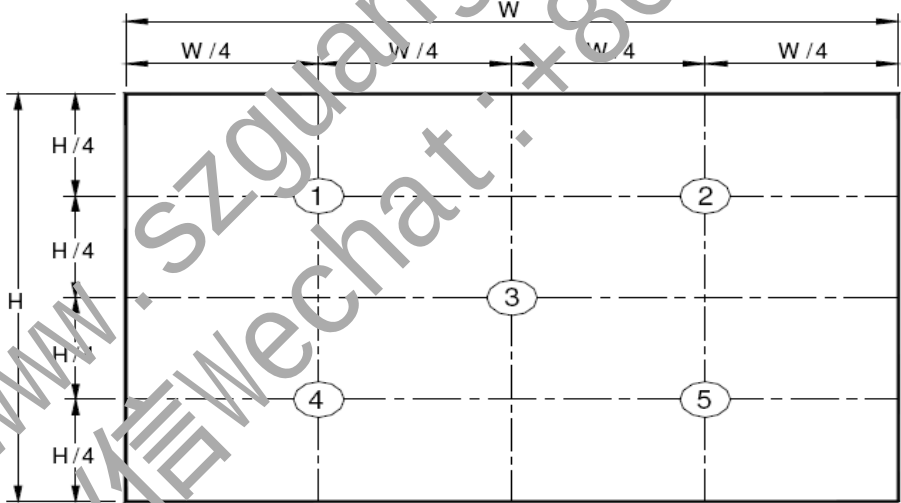
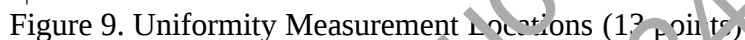


Figure 8. White Luminance and Uniformity Measurement Locations (5 points)

Center Luminance of white is defined as luminance values of center 5 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 7 for a total of the measurements per display.



The White luminance uniformity on LCD surface is then expressed as: $\Delta Y_5 = \text{Minimum Luminance of five points} / \text{Maximum Luminance of five points}$ (see Figure 8), $\Delta Y_{13} = \text{Minimum Luminance of 13 points} / \text{Maximum Luminance of 13 points}$ (see Figure 9).

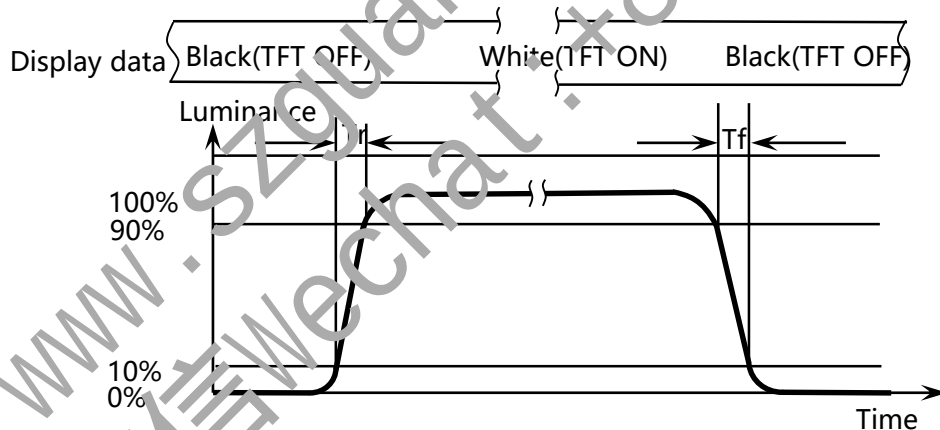
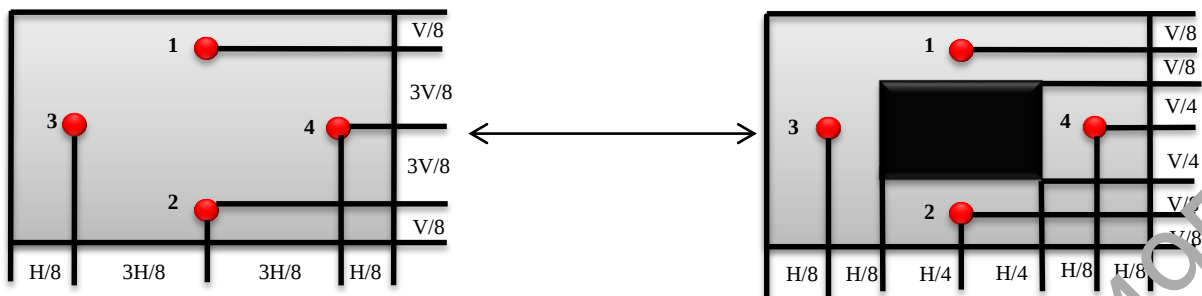


Figure 10. Response Time Testing

The electro-optical response time measurements shall be made as shown in Figure 10 by switching the “data” input signal ON and OFF. Tr: The luminance to change from 10% to 90% ,Tf: The luminance to change from 90% to 10% .

The test system : LMS PR810



$$\text{Cross Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_A} \right| \times 100$$

Figure 11. Cross Talk Modulation Test Description

Where:

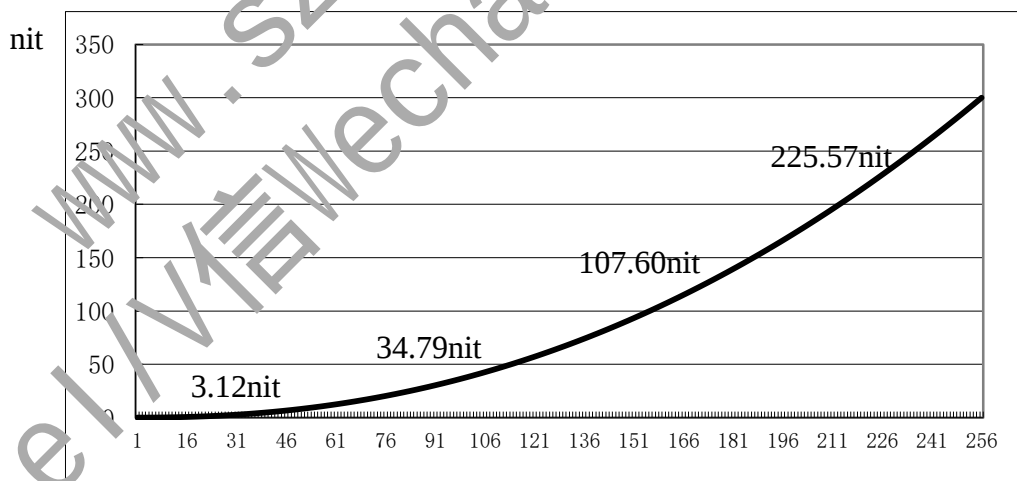
Y_A = Initial luminance of measured area (cd/m^2)

Y_B = Subsequent luminance of measured area (cd/m^2)

The location 1/2/3/4 measured will be exactly the same in both patterns. The test background gray is from L64 to L192. Take the largest data as the result.

Cross Talk of one area of the LCD surface by another shall be measured by comparing the luminance (Y_A) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (Y_B) of that same area when any adjacent area is driven dark. (Refer to Figure 11)

The test system: PR730



Gray-scale

Figure 12. Brightness and Gray-scale Contrast

5.0 INTERFACE CONNECTION

5.1 Electrical Interface Connection

The electronics interface connector is I-PEX 20682-030E-02.
The connector interface pin assignments are listed in Table 6.

<Table 6. Pin Assignments for the Interface Connector>

Terminal	Symbol	Functions
PIN No.	Symbol	Description
1	DBC	DBC control signal
2	H_GND	Ground
3	Lane1_N	eDP RX channel 1 negative
4	Lane1_P	eDP RX channel 1 positive
5	H_GND	Ground
6	Lane0_N	eDP RX channel 0 negative
7	Lane0_P	eDP RX channel 0 positive
8	H_GND	Ground
9	Aux_Ch_P	eDP AUX CH positive
10	Aux_Ch_N	eDP AUX CH negative
11	H_GND	Ground
12	LCD_VCC	LCD Power Supply, 3.3V (typ.)
13	LCD_VCC	LCD Power Supply, 3.3V (typ.)
14	LCD_Self_Test(BIST)	BIST pin(High enable, Low or float disable)
15	LCD_GND	Ground
16	LCD_GND	Ground
17	HPD	HPD signal pin
18	BL_GND	Ground
19	BL_GND	Ground
20	BL_GND	Ground
21	BL_GND	Ground
22	BL_Enable	LED Enable Pin(+3.3V Input)
23	BL_PWM	System PWM signal Input
24	NC	Not connect
25	NC	Not connect
26	BL_PWR	Backlight power
27	BL_PWR	Backlight power
28	BL_PWR	Backlight power
29	BL_PWR	Backlight power
30	NC	Not connect

5.2 eDP Interface

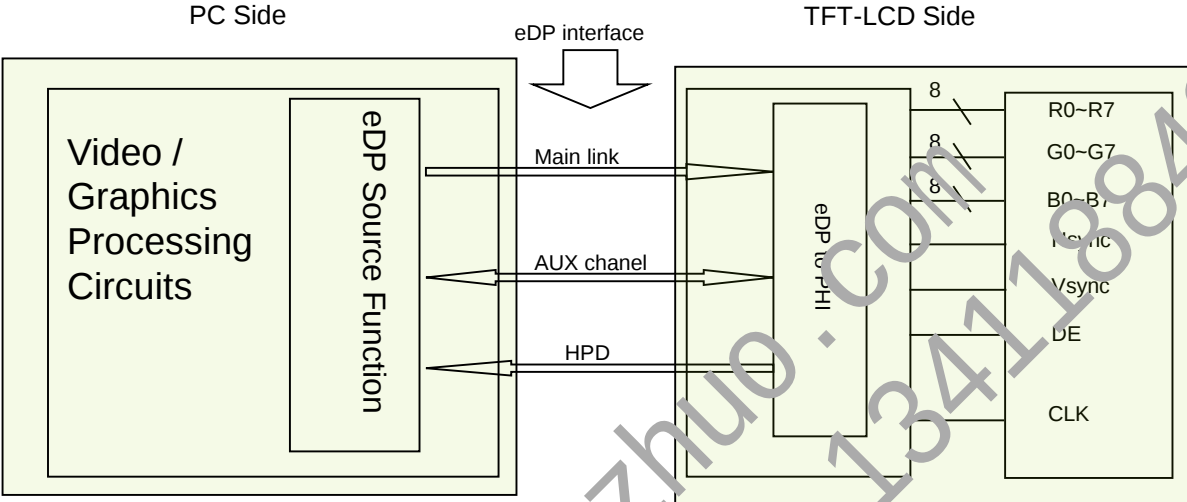


Figure 11. eDP Interface Architecture

Note:
Transmitter NT71855 or equivalent.
Transmitter is not contained in module.

5.3 Data Input Format

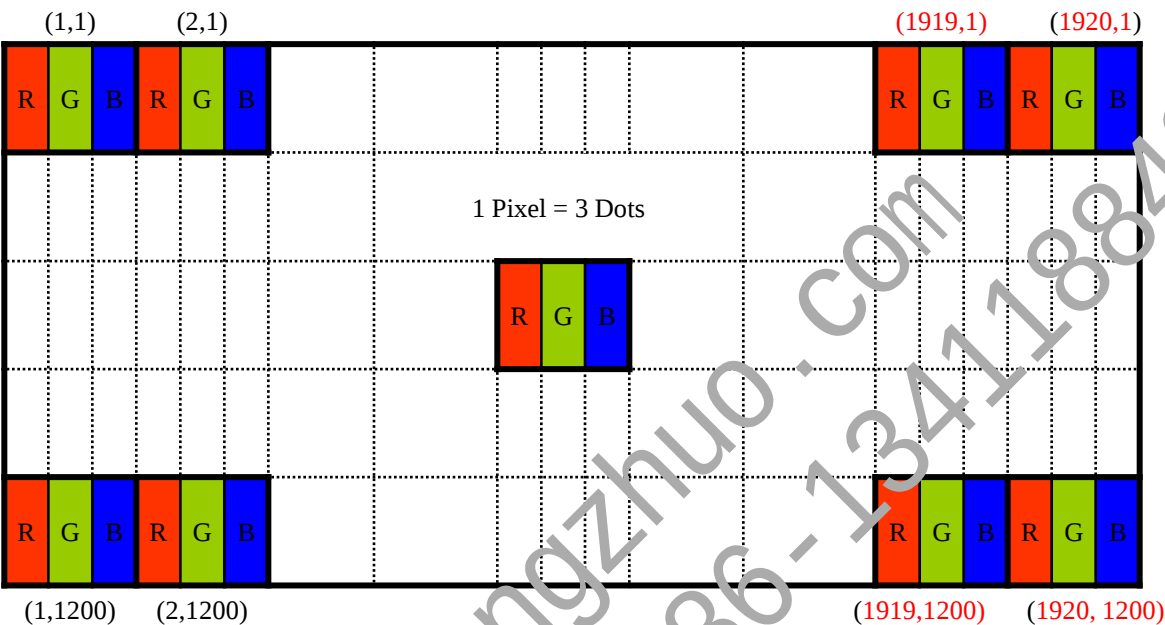


Figure 14. Display Position of Input Data (V-H)

5.4 Back-light & LCM Interface Connection

BLU Interface Connector: MSAK24022P10

<Table 7. Pin Assignments for the BLU Connector>

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	V-	LED cathode connection	6	V-	LED cathode connection
2	V-	LED cathode connection	7	GND	GND
3	V-	LED cathode connection	8	NC	NC
4	V-	LED cathode connection	9	V+	LED anode connection
5	V-	LED cathode connection	10	V+	LED anode connection

6.0 SIGNAL TIMING SPECIFICATION

6.1 The NV140WUM-N6A Is Operated By The DE Only

< Table 8. Signal Timing Specification >

Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	-	154.8	-	MHz
Frame Period		Tv	-	1240	-	lines
			-	60	-	Hz
			-	16.67	-	ms
Vertical Display Period		Tvd	-	1200	-	lines
One line Scanning Period		Th	-	2080	-	clocks
Horizontal Display Period		Tinc	-	1920	-	clocks

Note : The above is as optimized setting.

6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 9.

<Table 9. eDP Main-Link RX TP4 Package Pin Parameters>

Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock (Link clock down-spreading)	SSC	-	-	0.5	%	
Differential peak-to-peak input voltage at package pins	$V_{RX-DIFFp-p}$	120	-	1200	mV	
Rx input DC common mode voltage	$V_{RX_DC_CM}$	0	-	2	V	
Differential termination resistance	$R_{RX-DIFF}$	80	100	120	Ω	
Single-ended termination resistance	R_{RX-SE}	40	-	60	Ω	
Rx short circuit current limit	I_{RX_SHORT}	-	-	50	mA	
Intra-pair skew at Rx package pins (HBR) RX intra-pair skew tolerance at HBR	$L_{RX_SKEW_INTRA_PAIR}$	-	-	60	ps	
AC Coupling Capacitor	C_{SOURCE_ML}	75	100	200	nF	Source side

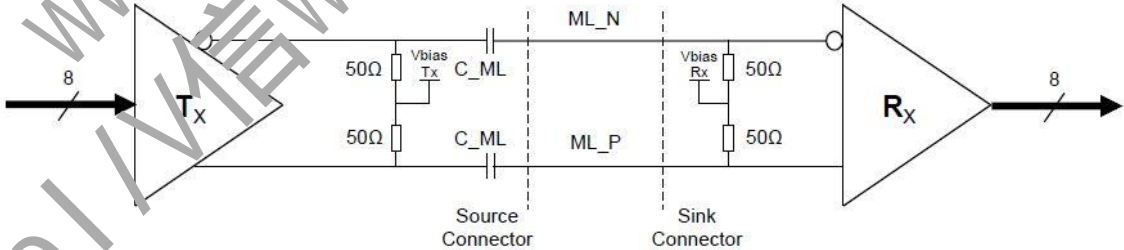


Figure 15. Main link differential pair

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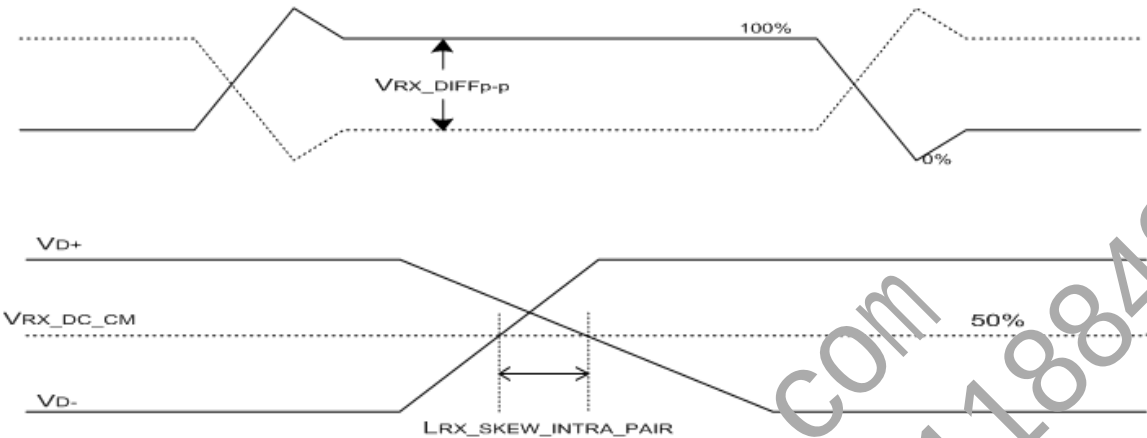


Figure 16. VRX-DIFFp-p & LRX_SKEW_INTRA_PAIR

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<Table 10. HPD Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
HPD voltage	V _{HPD}	2.25	-	3.6	V	Sink side
Hot Plug Detection Threshold	-	2.0	-	-	V	Source side
Hot Unplug Detection Threshold	-	-	-	0.8V	V	
HPD_IRQ Pulse Width	HPD_IRQ	0.5	-	1	ms	
HPD_TimeOut	-	2.0	-	-	ms	

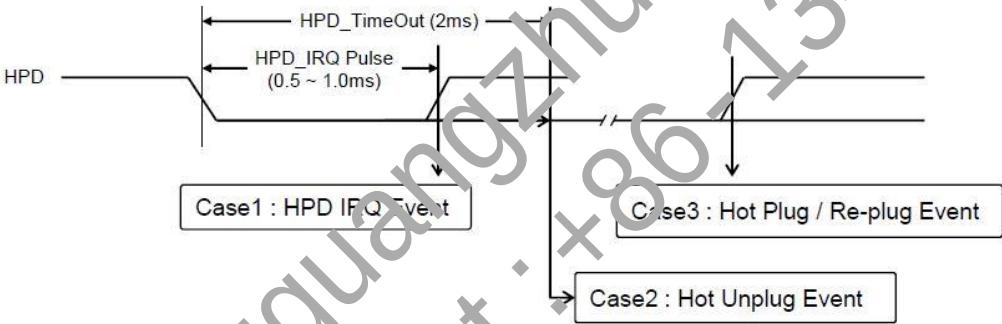


Figure 17. HPD Events

<Table 11. AUX Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
AUX unit interval	U_{IAUX}	0.4	0.5	0.6	Us	
AUX peak-to-peak input differential voltage	$V_{AUX-RX-DIFFp-p}$	0.29	-	1.38	V	Sink Side Connector Pin
AUX CH termination DC resistance	$R_{AUX-TERM}$	80	100	120	Ohm	
AUX DC common mode voltage	$V_{AUX-DC-CM}$	0	-	2	V	
AUX turn around common mode voltage	$V_{AUX-TURN-CM}$			3.3	V	
AUX short circuit current limit	$I_{AUX-SHORT}$	-	-	90	mA	
AUX AC Coupling Capacitor	$C_{SOURCE-AUX}$	75		200	nF	Source side

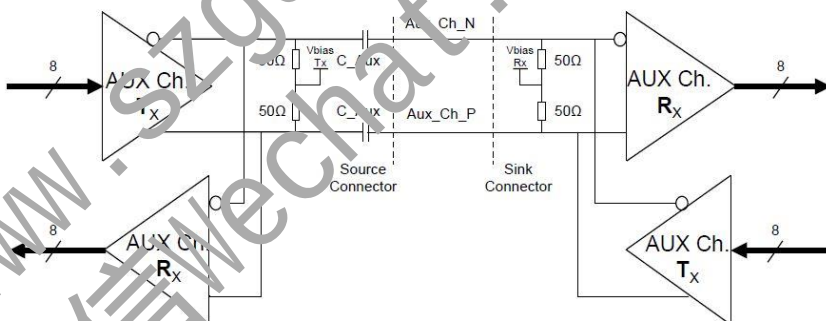


Figure 18. AUX differential pair

7.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

<Table 12. Input Signal & Basic Display Colors & Gray Scale of Colors >

		Colors & Gray scale	Data signal																											
			R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7				
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1			
	Green	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0			
	Light Blue	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1			
	Red	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	Purple	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1			
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0			
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1			
Gray scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	△	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	Darker	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	▽																													
	Brighter	1	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	▽	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	Red	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
Gray scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	△	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	Darker	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	▽																													
	Brighter	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0			
	▽	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0			
	Green	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0			
Gray scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0			
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0			
	▽																													
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1			
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1			
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1			
Gray scale of White & Black	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	△	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
	Darker	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0			
	▽																													
	Brighter	1	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1			
	▽	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1			
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				

8.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below.

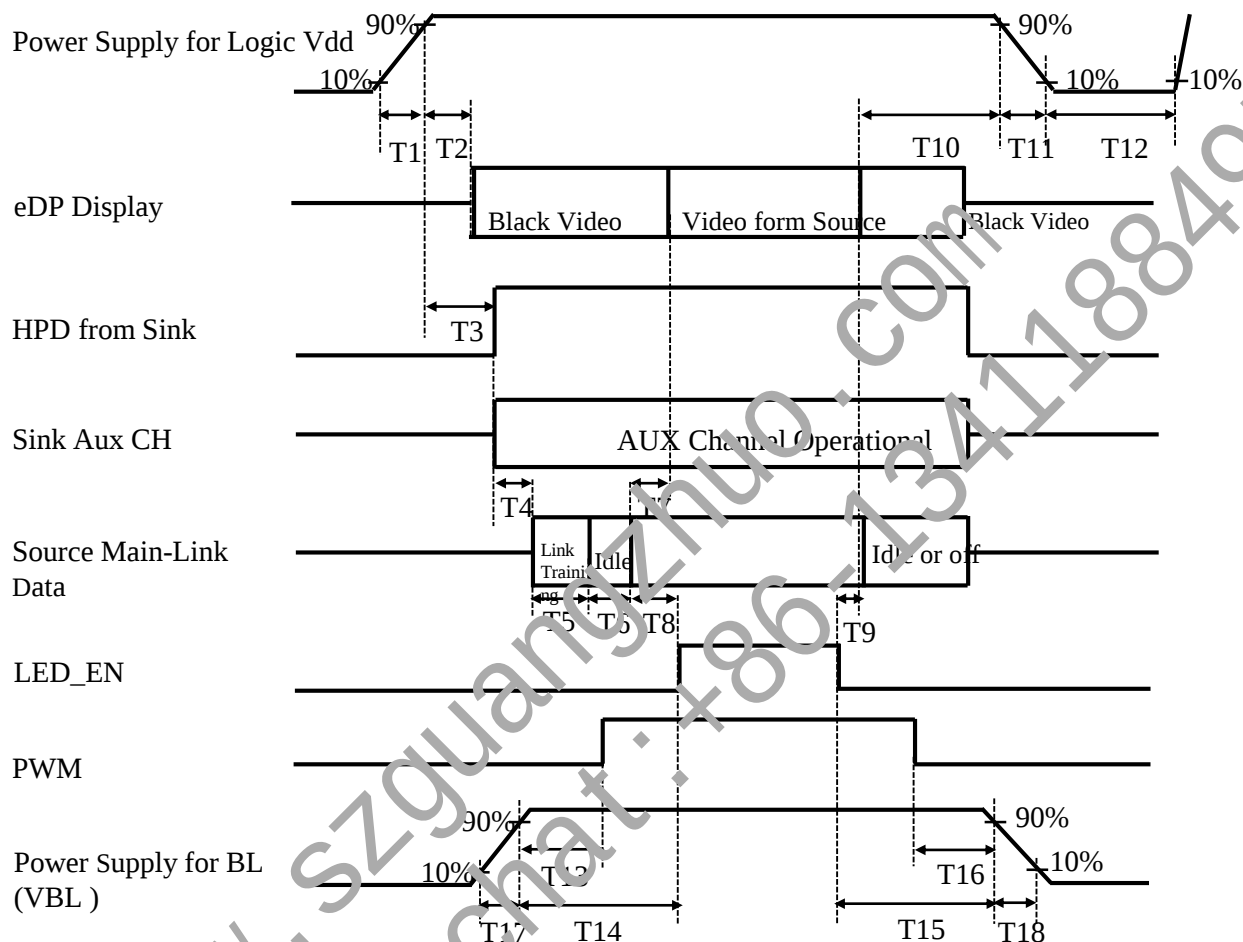


Figure 19. Power Sequence

- $0.5\text{ms} \leq T1 \leq 10\text{ms}$
- $0\text{ms} < T2 \leq 200\text{ms}$
- $0\text{ms} < T3 \leq 20\text{ms}$
- $T4+T5+T6+T8 \leq 80\text{ms}$
- $0\text{ms} < T7 \leq 50\text{ms}$
- $50\text{ms} < T9$
- $0\text{ms} < T1$
- $40\text{ms} < T10 < 500\text{ms}$
- $0.5\text{ms} \leq T11 \leq 10\text{ms}$
- $500\text{ms} \leq T12$
- $0\text{ms} < T13$
- $0\text{ms} < T14$
- $0\text{ms} < T15$
- $0\text{ms} < T16$
- $0.5\text{ms} \leq T17$
- $0.5\text{ms} \leq T18$

Notes

1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal are valid.

10.0 MECHANICAL CHARACTERISTICS

10.1 Dimensional Requirements

Figure 26 shows mechanical outlines for the model NV140WUM-N6A.
Other parameters are shown in Table 14.

<Table 14. Dimensional Parameters>

Parameter	Specification	Unit
Active Area	301.5936(H) x 188.496(V)	mm
Number of pixels	1920 (H) × 1200 (V)	pixels
Pixel pitch	157.08(H) × 157.08 (V)	um
Pixel arrangement	RGB Stripe	
Display colors	16.7M (8bit)	
Display mode	Nominally Black	
Dimensional outline	306.6±0.3/195.35±0.5(W/COF bending)	mm
Weight	240 max	g

10.2 Mounting

See Figure 26.

10.3 Anti-Glare and Polarizer Handress.

The surface of the LCD has an HC coating to minimize reflection and a coating to reduce scratching.

10.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 350lux.

11.0 RELIABILITY TEST

The reliability test items and its conditions are shown in below.
<Table 15. Reliability Test>

No	Test Items	Conditions	Remark
1	High temperature storage test	Ta = 60 °C, 240 hrs	
2	Low temperature storage test	Ta = -20 °C, 240 hrs	
3	High temperature/High humidity Storage	Ta = 50 °C, 80%RH, 240 hrs	
4	High temperature operation test	Ta = 50 °C, 240 hrs	
5	Low temperature operation test	Ta = 0 °C, 240 hrs	
6	Thermal Shock Storage	Ta = -20 °C ↔ 60 °C (0.5 hr), 100 cycle	
7	Package Vibration test (non-operating)	加速度 1.49Grms, 频率 5~300Hz, Z (负载) 1hr, X 1hr, Y 1hr	Note 1
8	Package Drop test (non-operating)	1 corner/3 edges/6 faces	Note 1
9	Electro-static discharge test	Air Discharge: +/-2kV and +/-4kV Criteria A. +/-8kV and +/-12kV Criteria B. +/-15kV Criteria C. Contact Discharge: +/-2kV Criteria A. +/-4kV and +/-6kV Criteria B. +/-8kV Criteria C.	Note 2

- Notes :
- 1. The fixture must be hard enough , so that the module would not be twisted or bent.
 - 2. Self-recovery and restart recovery is allowed. No hardware failures.

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12.0 HANDLING & CAUTIONS

- (1) Cautions when taking out the module

 - Pick the pouch only, when taking out module from a shipping package.
- (2) Cautions for handling the module

 - As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
 - As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
 - As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
 - Do not pull the interface connector in or out while the LCD module is operating.
 - Put the module display side down on a flat horizontal plane.
 - Handle connectors and cables with care.
- (3) Cautions for the operation

 - When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
 - Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.
- (4) Cautions for the atmosphere

 - Dew drop atmosphere should be avoided.
 - Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.
- (5) Cautions for the module characteristic

 - Do not apply fixed pattern data signal to the LCD module at product aging.
 - Applying fixed pattern for a long time may cause image sticking.
- (6) Other cautions

 - Do not disassemble and/or re-assemble LCD module.
 - Do not re-adjust variable resistor or switch etc.
 - When returning the module for repair or etc. Please pack the module not to be broken. We recommend to use the original shipping packages.

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13.0 LABEL

(1) Product Label

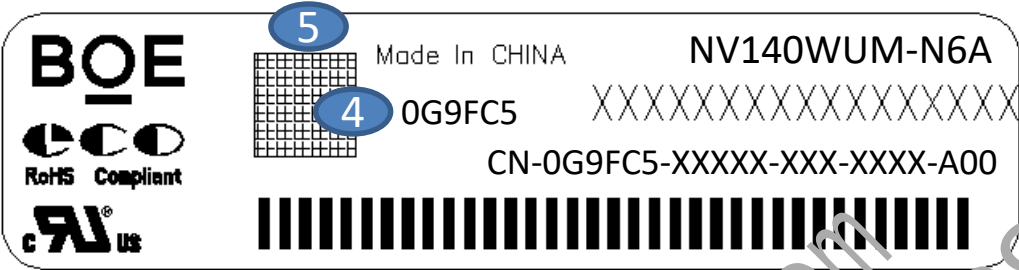


Figure 22. Product Label

- 1 BOE MDL ID(厂内使用)
- 2 PPID码 (客户端使用) , 包括六组 (23码) :
第一组CN: CN=中国
第二组: Dell 的DPN码, dell每个项目都有一个5位的DPN码, 写在PPID中需在第一位补0, DPN码请与FAE确认, 本项目DPN: G9FC5
第三组: 工厂代码, B3工厂BOH00, B5工厂BO500, B8工厂BOC00, B18工厂BON00
第四组: 日期代码 (具体顺序: 年-月-日)
年: 2015=5
月: 1-12月依次为1、 2、 3..... 9、 A、 B、 C
日: 1-31日依次为1、 2、 3..... 9、 A、 B、 C、 U、 V
第五组: 生产顺序代码
第六组: 版本信息代码, 对应不同产品不同送样阶段, 每批样品送样前请与FAE提前确认
- 3 MDL ID 条纹码 (厂内使用)
- 4 Dell DPN编码, dell每个项目都有一个5位的DPN, 需在第一位补0
- 5 PPID对应的二维码, 二维码不采用带方框的QR码格式

	EVT	DVT	DVT1.1	DVT1.2	DVT2	DVT2.1	Pilot build	MP
New model	X00	X10	X11	X12	X20	X21	A00	A00
MP model at previous Dell project	A00	A00	A00	A00	A00	A00	A00	A00

Module ID Naming Rule:

<Table 16. Module ID Naming Rule>

序号号	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
代码	X	X	X	X	X	X	X	D	9	4	0	X	X	X	X	X	X
描述	GBN代码		等级	B3	年份		月	FG Code后四位				序列号					

(2) High voltage caution label

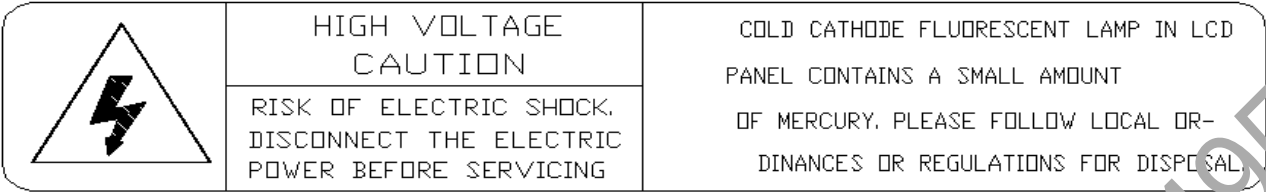
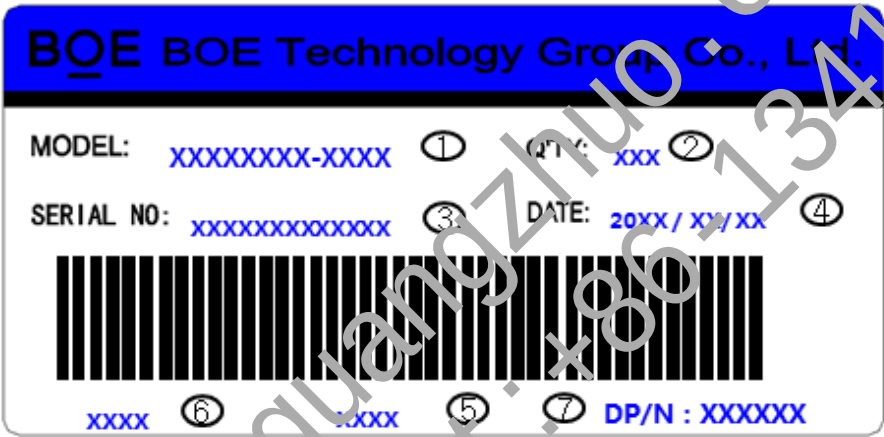


Figure 23. High Voltage Caution Label

(3) Box label



Serial number marked part needs to print, show as follows:

1. FG-CODE(Before 12 bit)
2. Product quantity
3. Box ID
4. Date
5. FG-Code After four
6. The client section material number(The client)
7. The client section material number(The client)

Total Size:100×50mm

<Table 17. Box Label Naming Rule >

序号号	1	2	3	4	5	6	7	8	9	10	11	12	13
代码	X	X	S	3	1	5	B	0	0	0	1	H	D
描述	GBN		Grade	B3	Year		Month	Serial No					

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14.0 PACKING INFORMATION

14.1 Packing Order

1-. Put the Panel in the Tray

- Then put the Spacer on the Panel

- Capacity:2pcs LCM/Tray

2pcs Spacer/Tray

2-. Repeat put the Tray & Panel & Spacer until to 15pcs, At last put 1pcs empty Tray

-Put the 16 pcs Tray in the PE Bag

3-. Put one EPE Board in the Inner Box

-Put the PE Bag with 16 pcs Tray in the EPE Board

-At last put one EPE Board

- Capacity : 30pcs LCM/Box

4-. Put 16EA Box on the Pallet

- Secure with strapping tape, wrap around 11m, paper protection Angle.

-Capacity:4EA Box/Layer,4Layer,480pcs LCM/Pallet

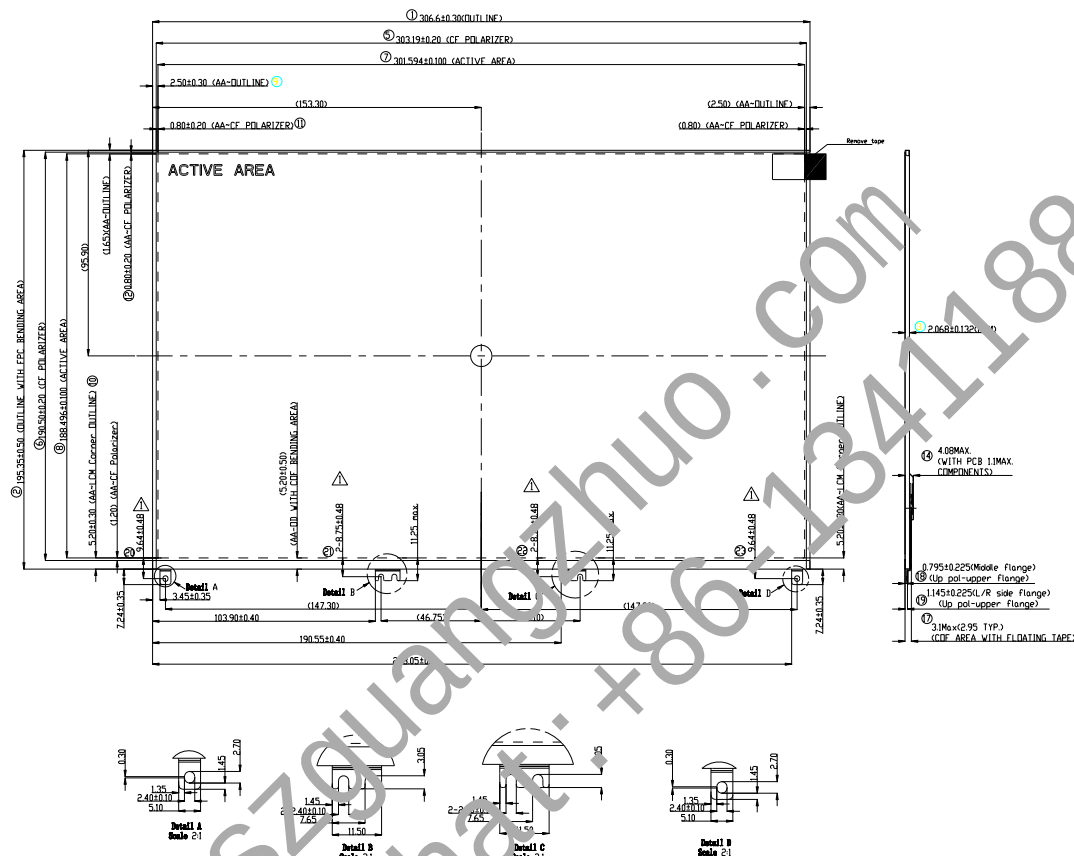
Figure 26. Packing Order

14.2 Note

- Box dimension: :507mm(W) x 507mm(D) x 240mm(H)
- Package quantity in one box: 30pcs

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15.0 MECHANICAL OUTLINE DIMENSION



NOTES:

1. WARPAGE AND DEFORMATION SPEC.: 0.8mm MAX.
2. THE eDP CONNECTOR IS MEASURED AT PIN 1 AND MATING LINE
3. UNSPECIFIED TOLERANCE REFER TO 0.3 mm
4. THE MEASUREMENT METHOD FOR THE DIMENSION OF MODULE, PLEASE REFER TO APPENDIX A.
5. "0" MEANS REFERENCE DIMENSIONS.
6. CRITICAL DIMENSION: ①~②③

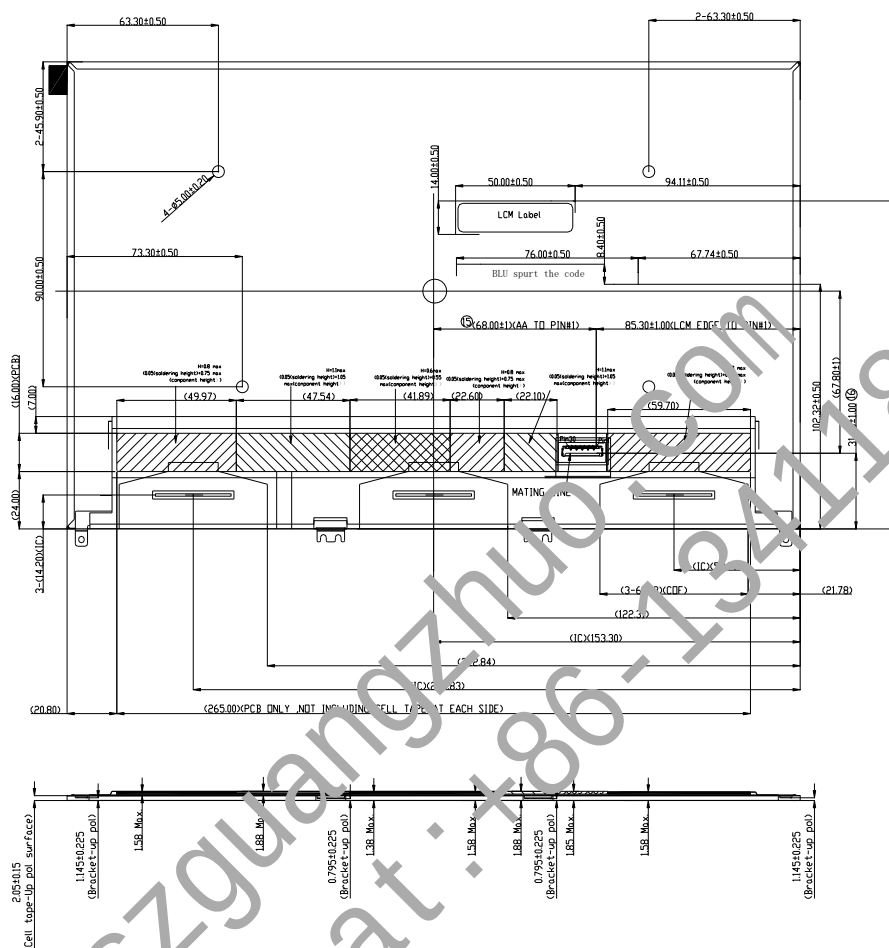


Figure 28. TFT-LCD Module Outline Dimensions (Rear view)

NOTES:

- 1.WARPAGE AND DEFORMATION SPEC.: 0.8mm MAX.
- 2.THE eDP CONNECTOR IS MEASURED AT PIN 1 AND MATING LINE
- 3.UNSPECIFIED TOLERANCE REFER TO ±0.3 mm
- 4.THE MEASUREMENT METHOD FOR THE DIMENSION OF MODULE, PLEASE REFRE TO PRODUCT SPEC..
- 5."()" MEANS REFERENCE DIMENSIONS.
- 6.CRITICAL DIMENSION: ①~②③

16.0 EDID Table

Address (HEX)	Function	Hex	Dec	crc	Input values.	Notes
00	Header	00	0		0	EDID Header
01		FF	255		255	
02		FF	255		255	
03		FF	255		255	
04		FF	255		255	
05		FF	255		255	
06		FF	255		255	
07		00	0		0	
08	ID Manufacturer Name	09	9		BOE	ID = BOE
09		E5	229			
0A	ID Product Code	44	68		2884	ID = 2884
0B		0B	11			
0C	32-bit serial No.	00	0		0	
0D		00	0		0	
0E		00	0		0	
0F		00	0		0	
10	Week of manufacture	14	20		20	
11	Year of Manufacture	20	32		2032	Manufactured in 2022
12	EDID Structure Ver.	01	1		1	EDID Ver 1.0
13	EDID revision #	04	4		4	EDID Rev. 0.4
14	Video input definition	A5	165		-	Refer to right table
15	Max H image size	1F	30		30	30 cm (Approx)
16	Max V image size	13	19		19	19 cm (Approx)
17	Display Gamma	78	120		2.2	Gamma curve = 2.2
18	Feature support	03	3		-	Refer to right table
19	Red/Green low bits	F1	241		-	Red / Green Low Bits
1A	Blue/White low bits	90	144		-	Blue / White Low Bits
1B	Red x high bits	A6	168	671	0.656	Red (x) = 10101000 (0.656)
1C	Red y high bits	54	84	335	0.328	Red (y) = 01010100 (0.328)
1D	Green x high bits	76	76	304	0.297	Green (x) = 01001100 (0.297)
1E	Green y high bits	97	159	637	0.623	Green (y) = 10011111 (0.623)
1F	Blue x high bits	25	37	150	0.147	Blue (x) = 00100101 (0.147)
20	Blue y high bits	0C	12	49	0.048	Blue (y) = 00001100 (0.048)
21	White x high bits	50	80	320	0.313	White (x) = 01010000 (0.313)
22	White y high bits	54	84	336	0.329	White (y) = 01010100 (0.329)
23	Established timing 1	00	0		-	Refer to right table
24	Established timing 2	00	0		-	
25	Established timing 3	00	0		-	

26	Standard timing #1	01	1			Not Used
27		01	1			
28	Standard timing #2	01	1			Not Used
29		01	1			
2A	Standard timing #3	01	1			Not Used
2B		01	1			
2C	Standard timing #4	01	1			Not Used
2D		01	1			
2E	Standard timing #5	01	1			Not Used
2F		01	1			
30	Standard timing #6	01	1			Not Used
31		01	1			
32	Standard timing #7	01	1			Not Used
33		01	1			
34	Standard timing #8	01	1			Not Used
35		01	1			
36	Detailed timing/monitor descriptor #1	74	116		154.76	154.76MHz Main clock
37		3C	60			
38		80	128		1920	Hor Active = 1920
39		A0	160		160	Hor Blanking = 160
3A		70	112		-	4 bits of Hor. Active + 4 bits of Hor. Blanking
3B		20	176		1200	Ver Active = 1200
3C		28	40		40	Ver Blanking = 40
3D		40	64		-	4 bits of Ver. Active + 4 bits of Ver. Blanking
3E		3C	48		48	Hor Sync Offset = 48
3F		20	32		32	H Sync Pulse Width = 32
40		56	54		3	V sync Offset = 3 line
41		70	0		6	V Sync Pulse width : 6 line
42		2E	46		302	Horizontal Image Size = 302 mm (Low 8 bits)
43		BC	188		188	Vertical Image Size = 188 mm (Low 8 bits)
44		10	16		-	4 bits of Hor Image Size + 4 bits of Ver Image Size
45		00	0		0	Hor Border (pixels)
46		00	0		0	Vertical Border (Lines)
47		1A	26		-	Refer to right table

48	Detailed timing/monitor descriptor #2	5D	93		123.81	123.81MHz Main clock
49		30	48			
4A		80	128		1920	Hor Active = 1920
4B		A0	160		160	Hor Blanking = 160
4C		70	112		-	4 bits of Hor. Active + 4 bits of Hor. Blanking
4D		B0	176		1200	Ver Active = 1200
4E		28	40		40	Ver Blanking = 40
4F		40	64		-	4 bits of Ver. Active + 4 bits of Ver. Blanking
50		30	48		48	Hor Sync Offset = 48
51		20	32		32	Hor Sync Pulse Width = 32
52		36	54		3	V sync Offset = 3 line
53		00	0		6	V Sync Pulse width = 6 line
54		2E	46		302	Horizontal Image Size = 302 mm (Low 8 bits)
55		BC	188		188	Vertical Image Size = 188 mm (Low 8 bits)
56		10	16		-	4 bits of Hor Image Size + 4 bits of Ver Image Size
57		00	0		0	Hor Border (pixels)
58		00	0		0	Vertical Border (Lines)
59		1A	26		-	Refer to right above table
5A	Detailed timing/monitor descriptor #3	00	0			Indicates descriptor #3 is a display Descriptor
5B		00	0			
5C		00	0			Reserved
5D		FF	254			Tag : ASCII String
5E		00	0			Reserved
5F		4	71		G	D/PN:G9FC5
60		39	67		9	
61		46	70		F	
62		43	67		C	
63		35	53		5	
64		80	128		10000000	EDID:A00
65		4E	78		N	BOE PN:NV140WUM-N6A-3940
66		56	86		V	
67		31	49		1	
68		34	52		4	
69		30	48		0	
6A		57	87		W	
6B		55	85		U	

6C	Detailed timing/monitor descriptor #4	00	0			Indicates descriptor #4 is a display Descriptor
6D		00	0			
6E		00	0			Reserved
6F		00	0			Tag : ASCII String
70		00	0			Reserved
71		02	2		00000010	8-bit Color Depth & No FRC
72		41	65		01000001	WLED & single light bar & one light bar
73		31	49		00110001	Frame rate 48Hz~60Hz
74		9E	158		10011110	Light Controller: PWM & Max. Luminance 300
75		00	0		00000000	Front Surface: Anti-Reflective & RGB v-stripe
76		01	1		00000001	NTSC, sRGB
77		00	0		00000000	no Motion Blur & no Active Gamma
78		00	0		00000000	no Wireless Enhancement & no In-Cell Scanner
79		0A	10		00001010	2 Lane edp1.3
7A		41	65		01000001	Built-In Self Test
7B		0A	10			
7C		20	32			
7D		20	32			
7E	Extension flag	00				0 : 1个EDID; N-1: N个EDID
7F	Checksum	58	232	232	-	

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17.0 GENERAL PRECAUTIONS

17.1 HANDLING

- (1) When the module is assembled, It should be attached to the system firmly using every mounting holes. Be careful not to twist or bend the modules.
- (2) Refrain from strong mechanical shock or any force to the module. Otherwise, it may cause improper operation or damage to the module.
- (3) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than 1 HB pencil lead.
- (4) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.
- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth .In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static , it may cause damage to the module.
- (9) Use fingerstalls with soft gloves to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Do not pull or fold the LED FPC.
- (12) Do not touch any component which is located on the back side.
- (13) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (14) Pins of connector shall not be touched directly with bare hands.

17.2 STORAGE

- (1) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃ and relative humidity of less than 70%.
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.

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17.3 OPERATION

- (1) Do not connect, disconnect the module in the “ Power On” condition.
- (2) Power supply should always be turned on/off by following item 8.0 “ Power on/off sequence “.
- (3) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
- (4) The standard limited warranty is only applicable when the module is used for general notebook applications. If used for purposes other than as specified, BOE is not to be held reliable for the defective operations. It is strongly recommended to contact BOE to find out fitness for a particular purpose.

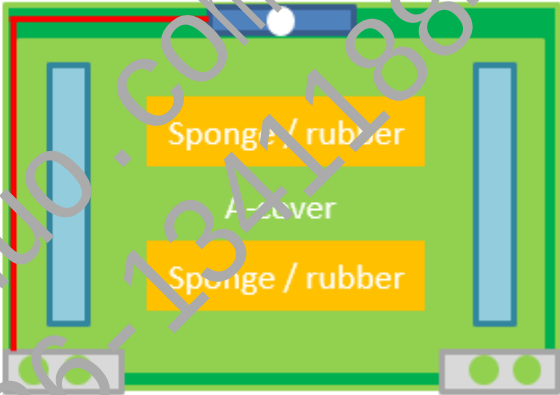
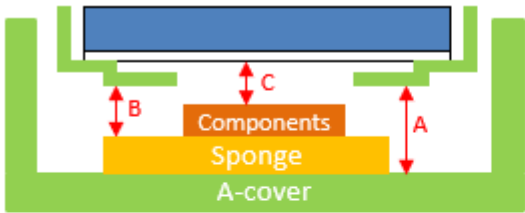
17.4 OTHERS

- (1) Avoid condensation of water. It may result in improper operation or disconnection of electrode.
- (2) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation, Variation in part contents and environmental temperature, etc.) Otherwise the module may be damaged.
- (3) If the module displays the same pattern continuously for a long period of time, it can be the situation when The “ image sticks” to the screen.
- (4) This module has its circuitry PCB’s on the rear or bottom side and should be handled carefully to avoid being stressed.

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Appendix B

LCM to A-Cover / sponges Z-gap



	Plastic Cover	Metal Cover
A	≥ 1.0mm	≥ 0.8mm
B	≥ 0mm	
C	> 0.5mm	

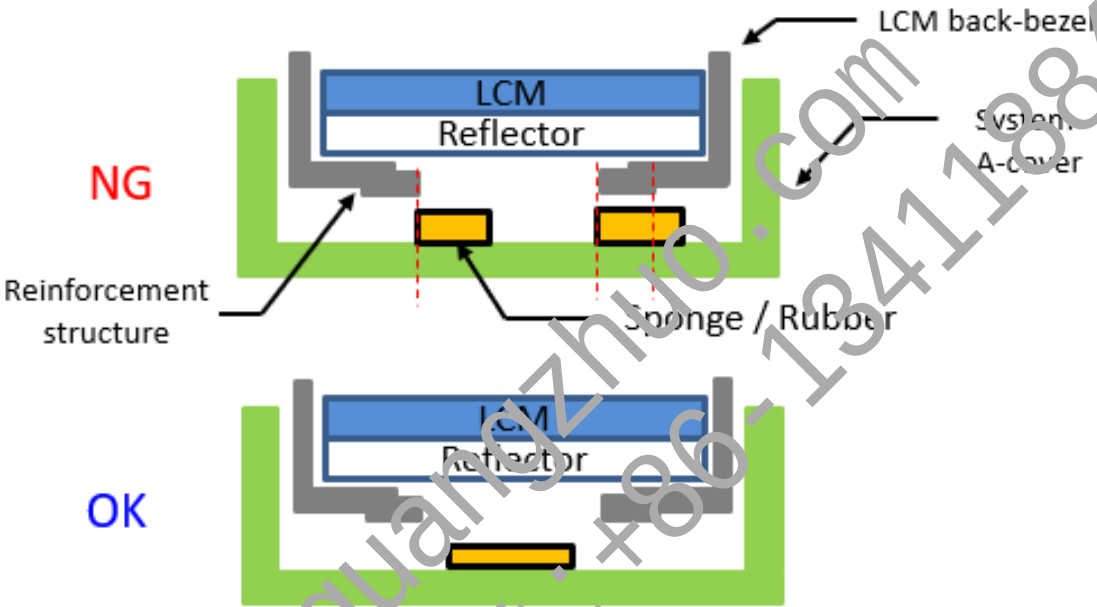
Purpose

The reflector area is very sensitive, BOE would suggest that design enough z-gap to decrease the risk of water ripple, white spots and other abnormal display

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LCM to A-Cover / sponges z-gap

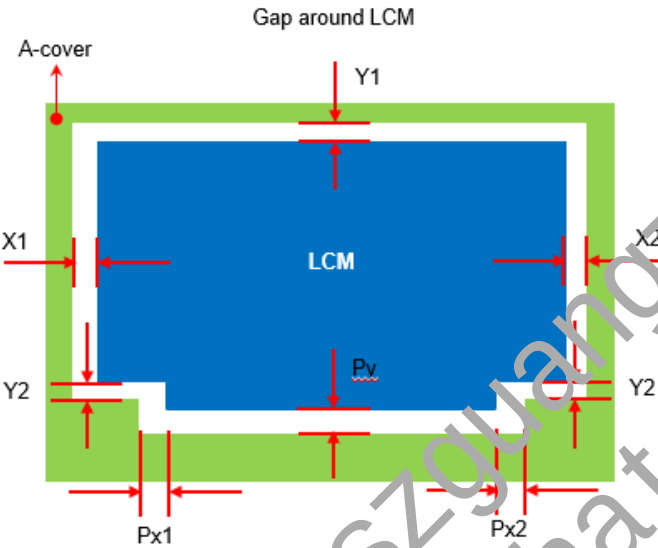


Purpose	If attach sponges or rubbers which correspond to white reflector area, it may cause white spot, pooling or other relative issues. BOE would suggest that attach wide range sponges / rubbers which can cover the LCM back-bezel opening
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Appendix B

LCM to side wall / protrusions



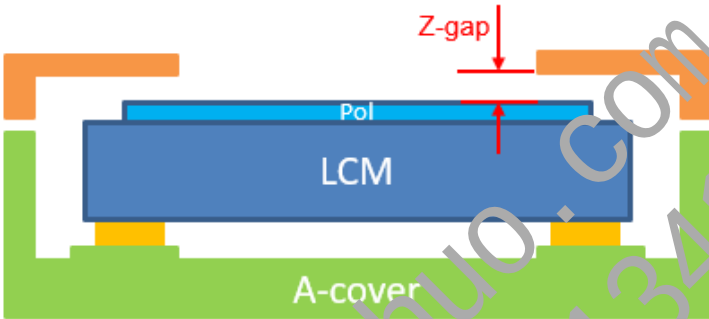
	Normal border (screws)	Narrow border (fix by tapes)
X1 / X2	Min: 0.45mm	Min: 0.35mm
Y1 / Y2	Min: 0.45mm	Min: 0.35mm
Px1 / Px2	Min: 0.55mm	
Py		

Purpose

BCE would suggest that design enough gap around LCM to prevent shock test failure, or interference, cell crack, abnormal display...etc. in the reliability test

Appendix B

LCM to B-cover z-gap

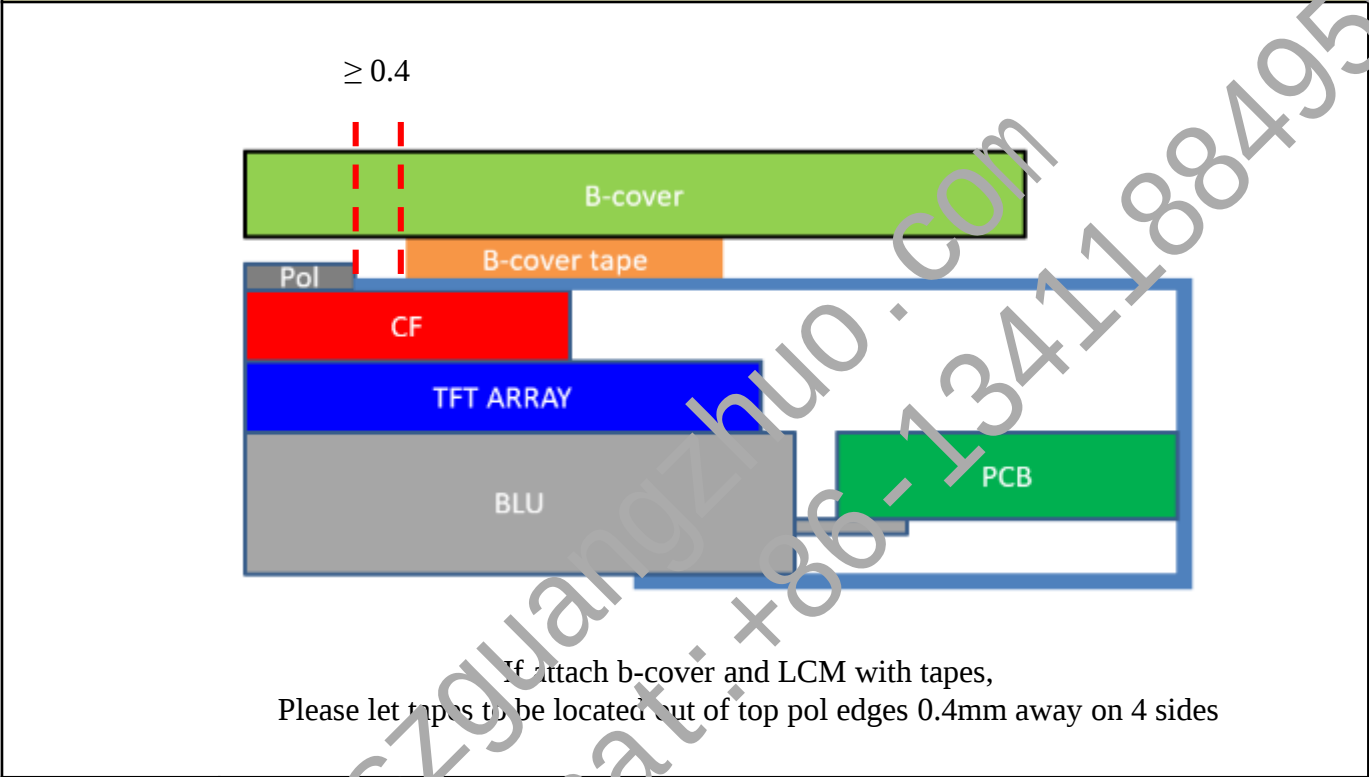


Bezel Tape	Z Gap
Without	0.15 ~ 0.25mm
With	0.15 ~ 0.20mm

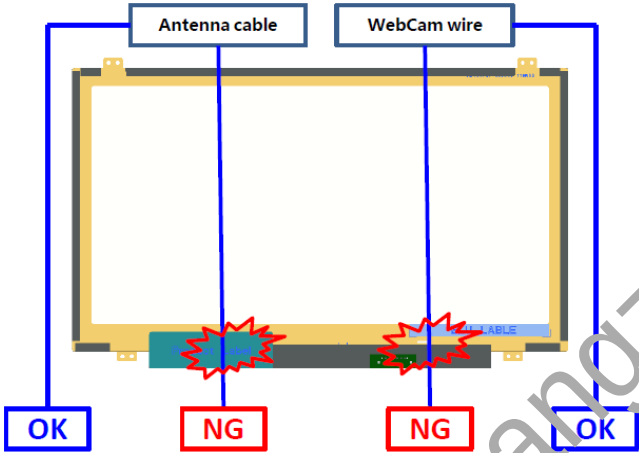
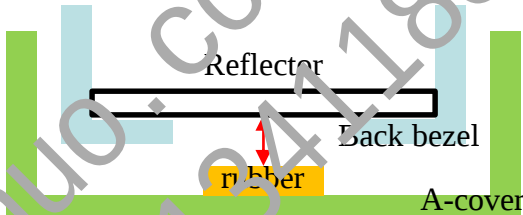
Purpose	Too less z-gap between system B-cover and LCM top pol has high risk that may cause cell crack, pooling, light leakage and other issues
---------	--

Appendix B

B-cover tape to top pol edge



Purpose	To avoid the B-cover tape override top pol then cause pooling or light leakage issue
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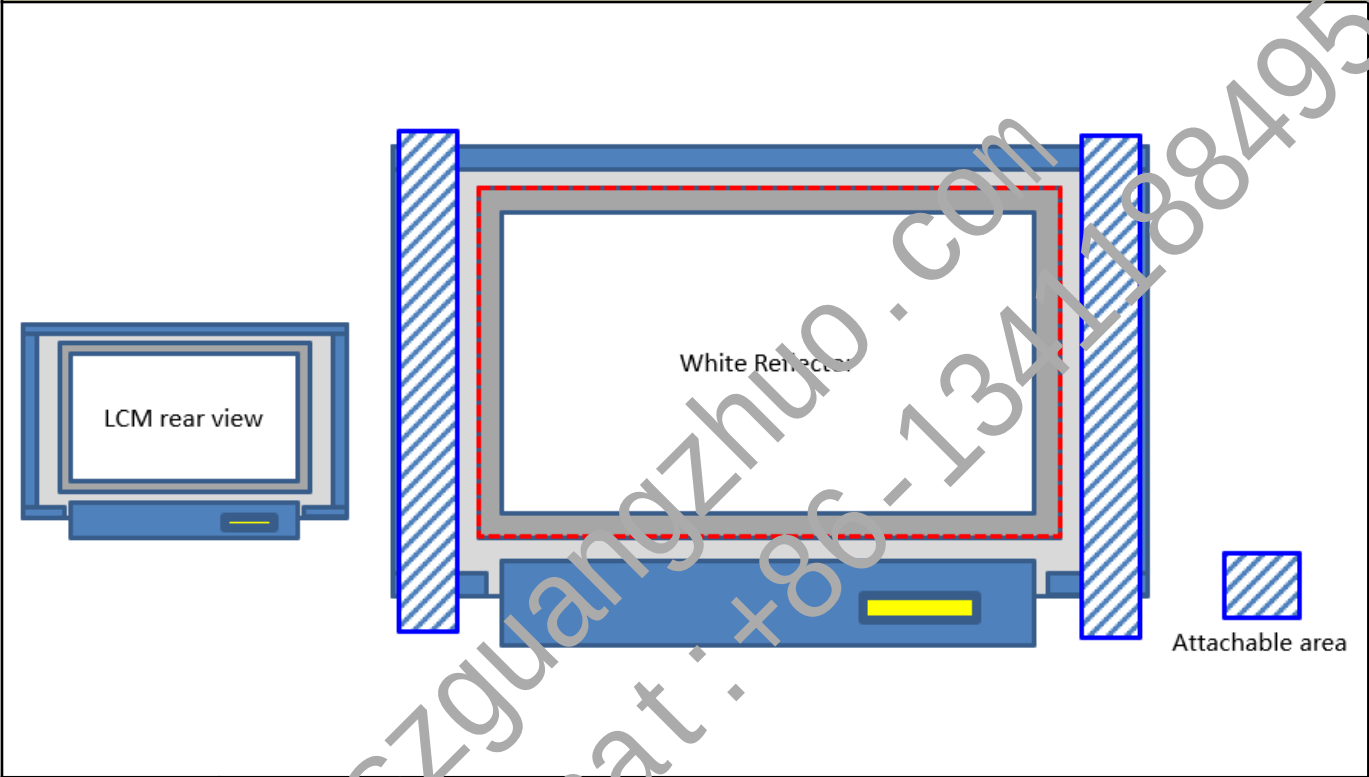
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Antenna Cable & Webcam wire			
  If sponge within the reflector area is necessary, we suggest that the gap between reflector and sponge is more than 0.5mm			
Purpose	1. BOE would suggest that do not set Antenna or WebCam cable / wire go behind LCM to avoid backpack test, hinge test ,twist test or pogo test with abnormal display 2. If the cable / wire is necessary to go behind LCM, please make a groove with round or chamfers to protect the cable / wire, or attach with higher sponges / rubbers adjacent to the cable / wire route 3. Suggest that attach the cable / wire with tapes to A-cover 4. Do not attach anything with LCM reflector area. If attach cable / wire with LCM reflector area, it may cause pooling, white spot, light leakage and other related issues		

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Appendix B

LCM paste area



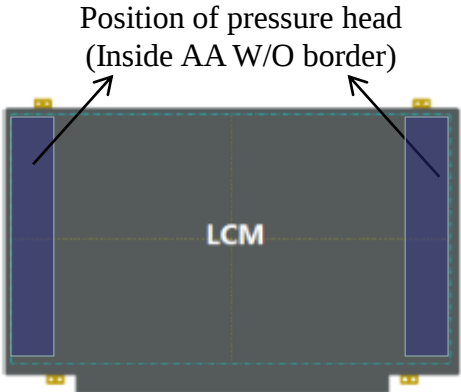
Purpose	If use the stretch remove tapes to fix LCM with A-cover, please set the stretch remove tapes correspond to the LCM back-bezel and do not let the tapes override the back-bezel's level step or opening
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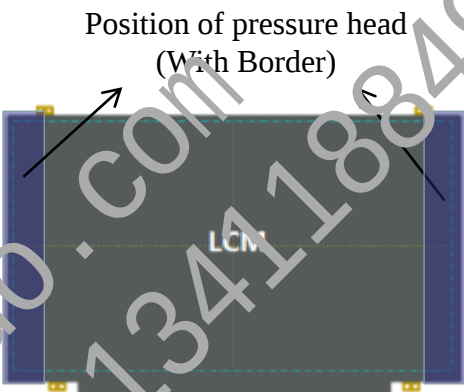
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Appendix B

LCM pressable area



NG



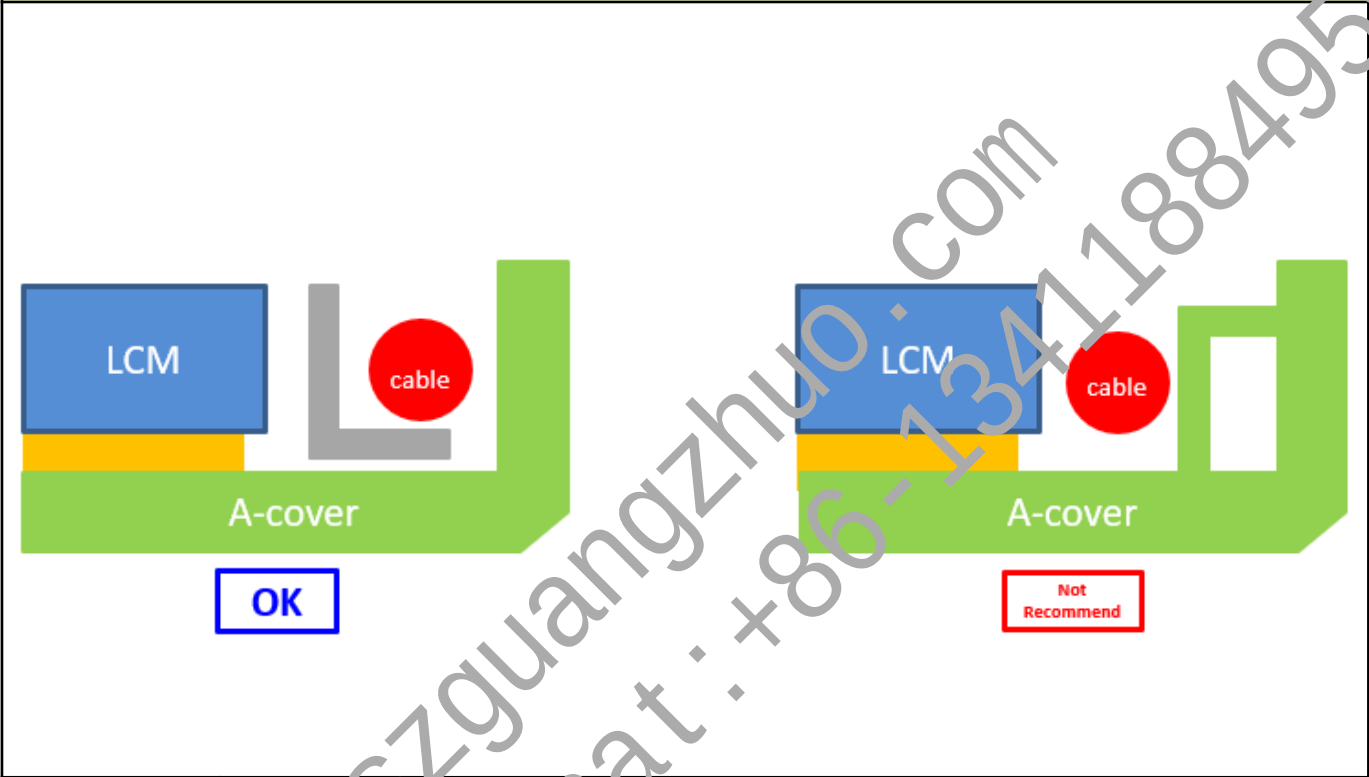
OK

Purpose	1. If LCM is fixed on A-cover by using the press jig during assembling. 2. To avoid panel broken the design of pressure head of press jig can not only pin on cell panel. The pressure head needs to pin on the LCM frame, which the LCM frame can share the pressure of the pressing head.
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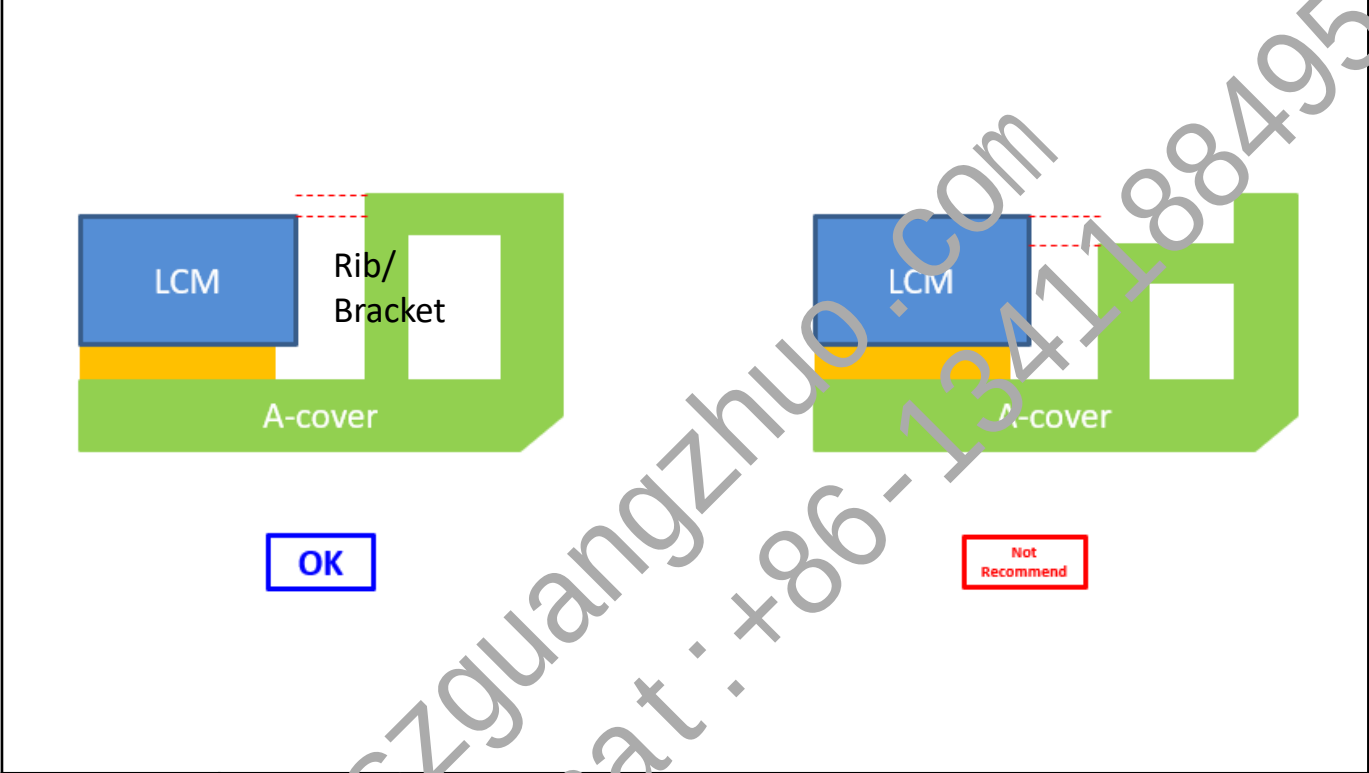
Wire setting



Purpose	Wires should be placed between protrusions/side wall and A-cover. If place the wires between LCM and Protrusions/side wall, it may interfere with LCM when assembling, or even cause LCM broken in reliability test.
---------	--

Appendix B

A-cover strength

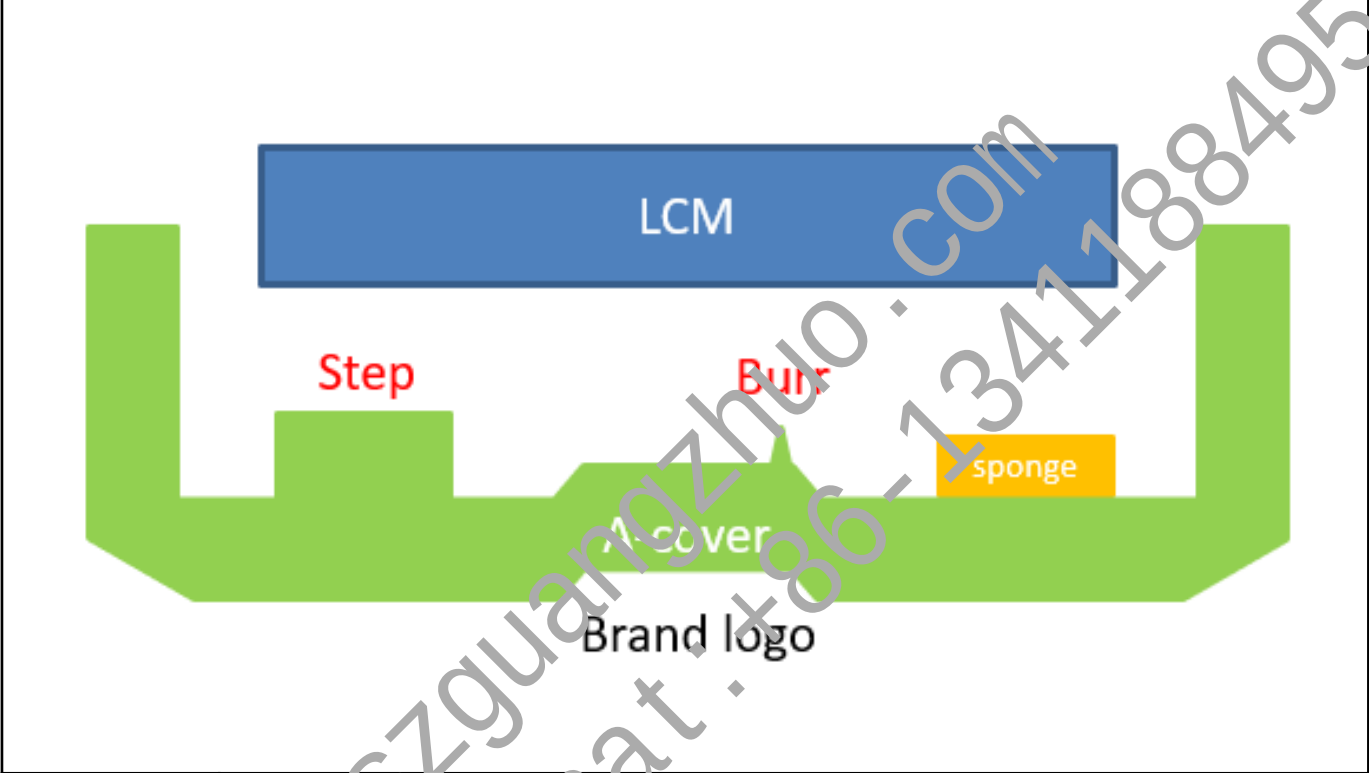


Purpose	1. BOE would recommend that structural Rib/Bracket height is higher than LCM, in order to avoiding pressures to LCM. 2. The L-shape Bracket is recommended.
---------	---

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Appendix B

System A-cover Inner Surface



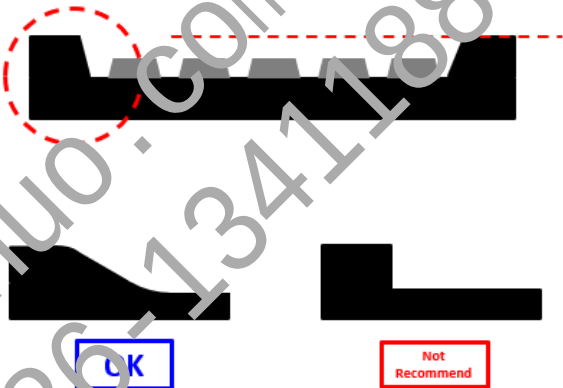
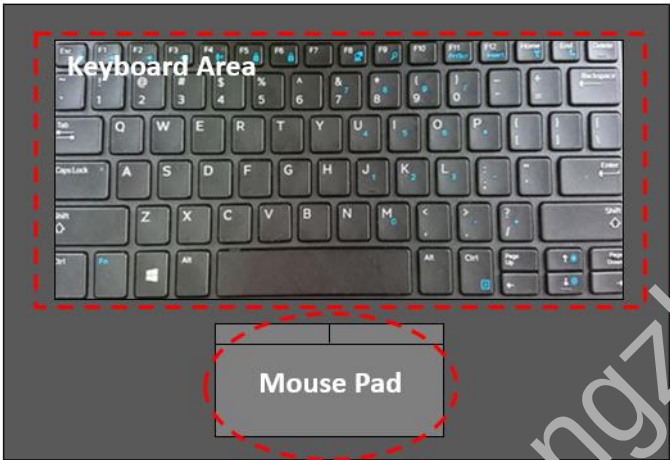
Purpose	There should not exist any burr, segment gap or protrusions beside Logo, which may cause White Spot or Glass Broken by stress concentration.
---------	--

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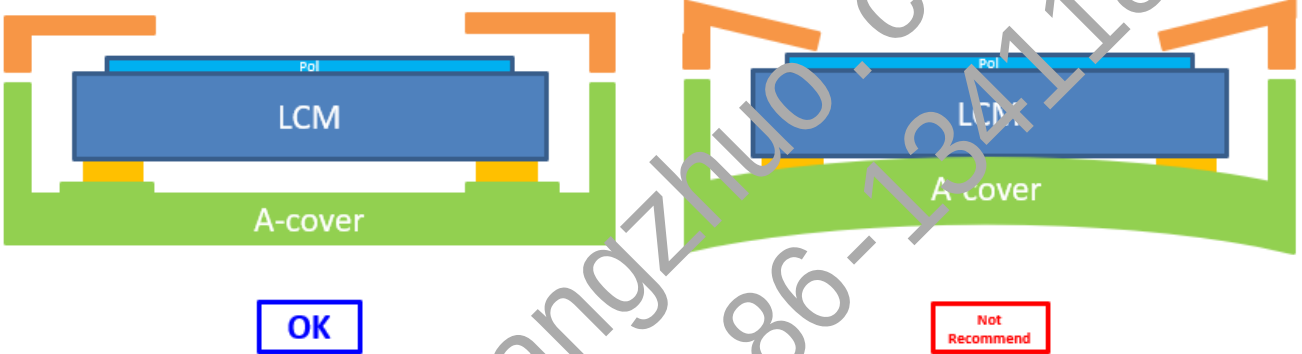
Appendix B

Keyboard area & Mouse pad



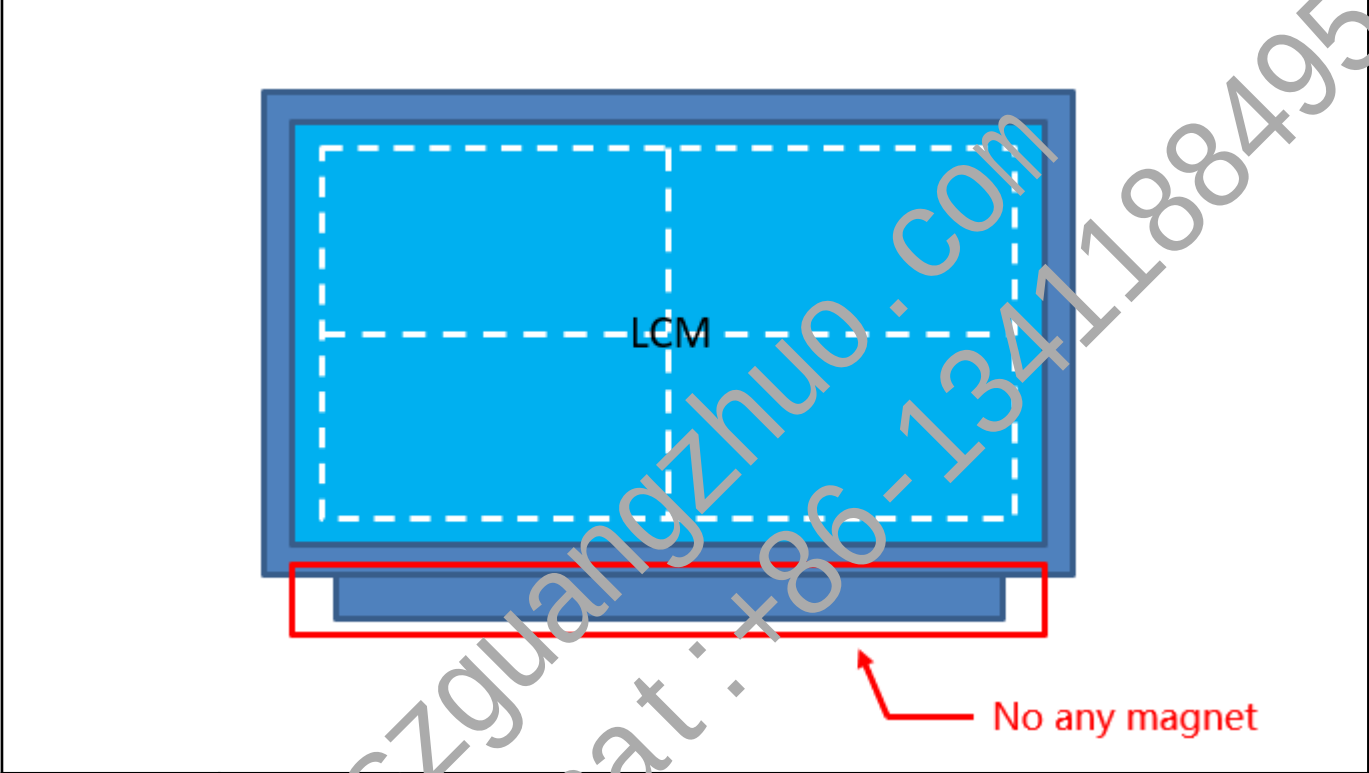
Purpose	The transition surface between keyboard and mouse pad should be smooth and without vertical steps/ too large level steps
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System cover reliability			
			
Purpose	1. No interference between system and LCM in assembly process except compressible grounding gaskets 2. The permanent deformation which caused by Reliability test is not allowed to contact LCM		
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DAS-RD-2019006-C			A4(210 X 297)

Appendix B

A/B-cover near LCD PCBA

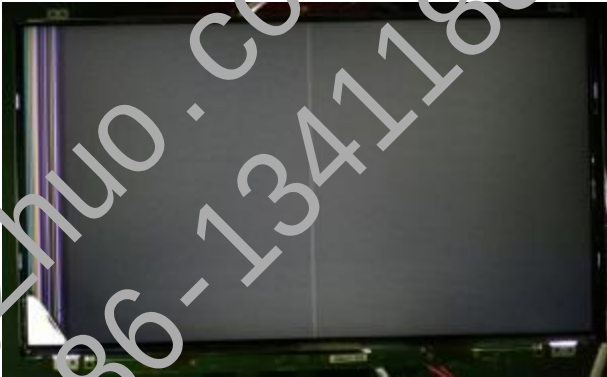


Purpose	There should not be any magnet object close to LCM PCBA, it may cause physical or electricity noise issue
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Appendix B

A-cover add sponges on Boss side wall

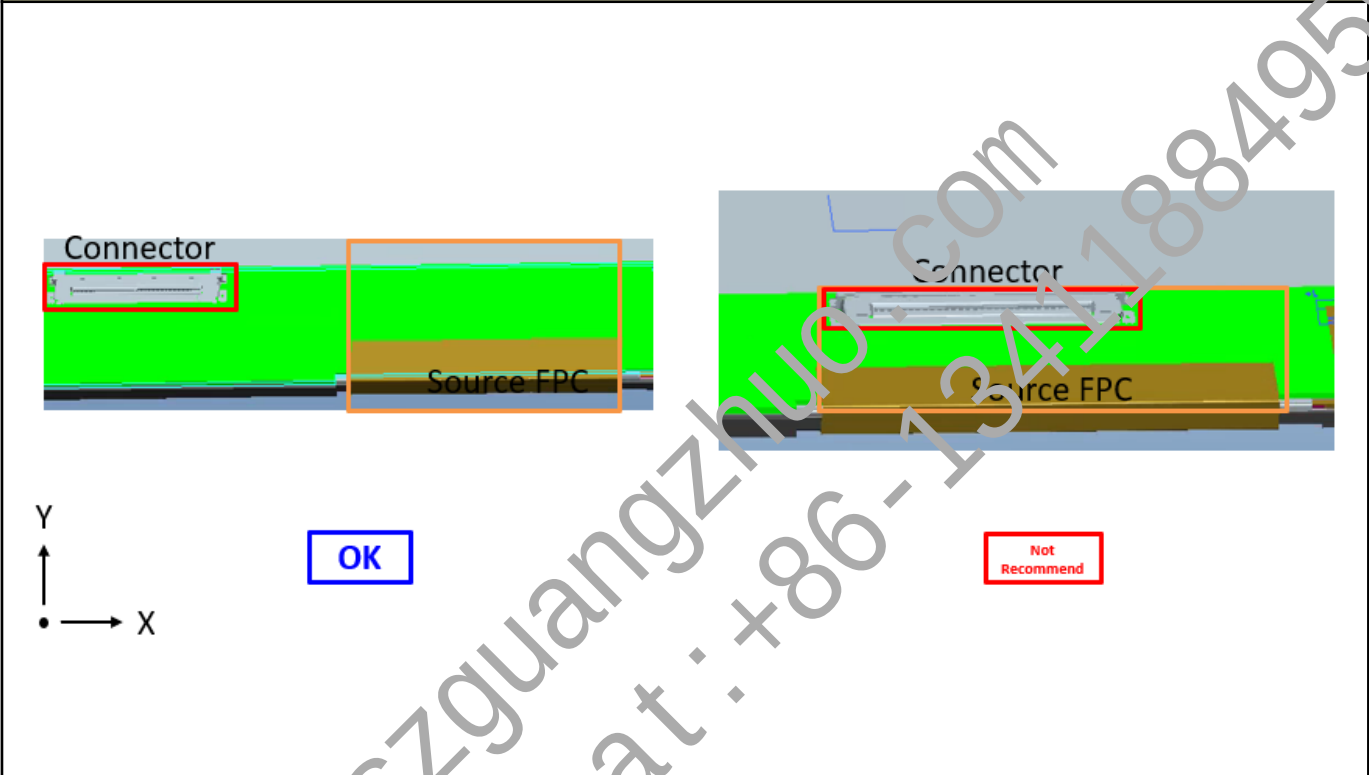

Purpose	BOE would suggest to attach Sponges to the side-wall of the Boss column of A-cover to reduce the risk of panel broken in assembling process.
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Appendix B

LCM to A-Cover / sponges z-gap

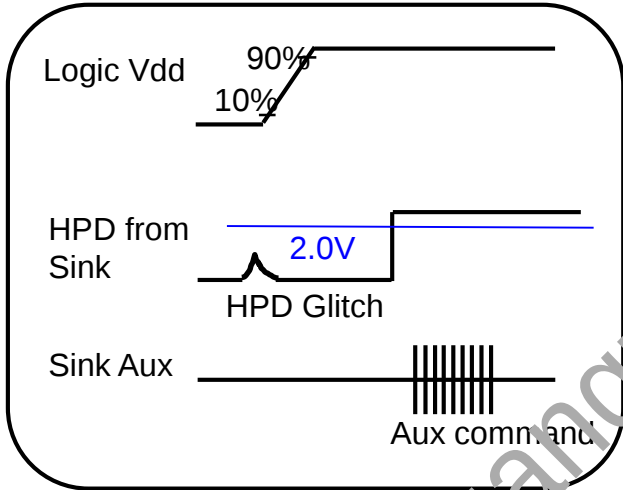


Purpose	Bent type product: The System Connector should not overlap with LCM FPC in X-direction, it may cause FPC lead broken during system connector plug and un-plug process (Panel FPC Bonding location is related to Mask and can not be changed easily)
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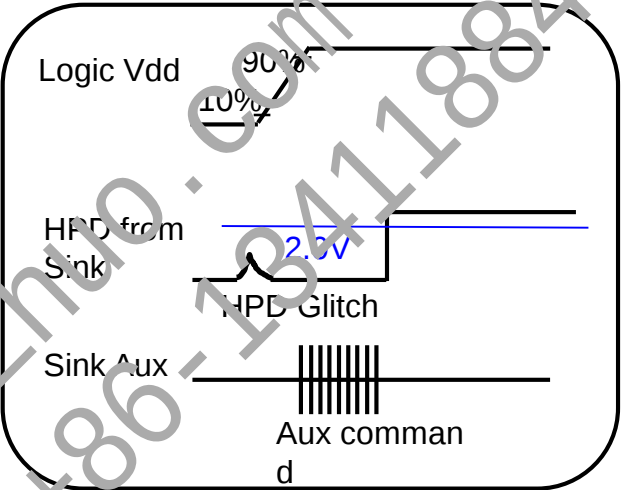
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Appendix C

HPD Signal recognition



Normal Signal (Ignore HPD Glitch)

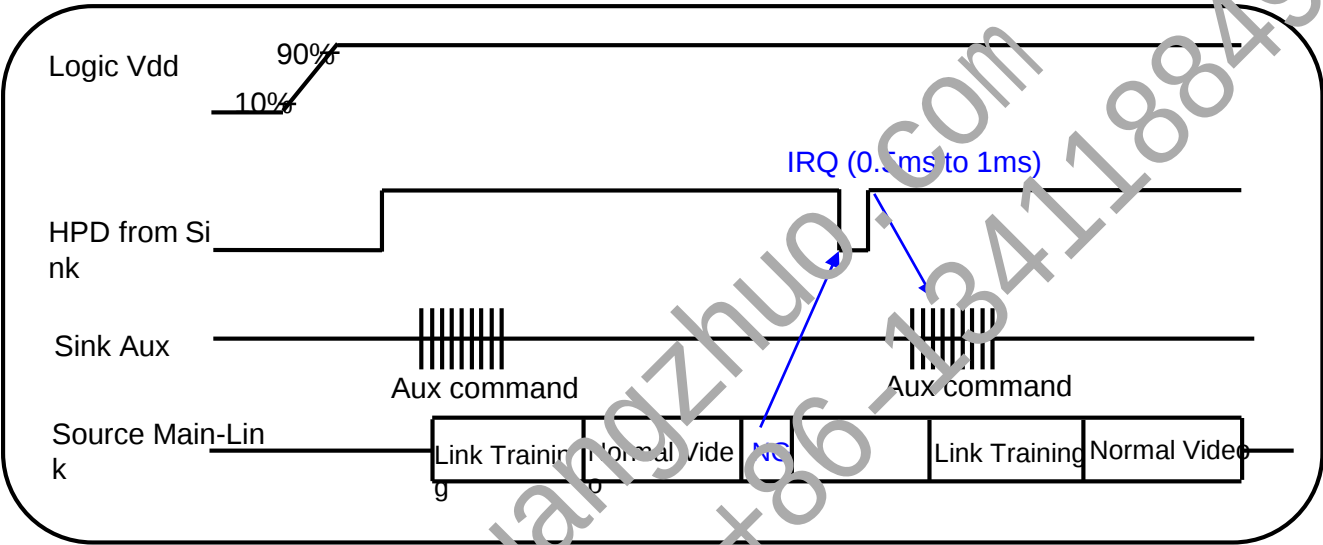


Abnormal Signal

Purpose	When HPD glitch voltage less than 2.0(V), system signal can't output AUX command data.
---------	--

Appendix C

HPD Signal Definition IRQ (Interrupt Request)



Purpose

When HPD signal low than 0.5ms to 1ms, the source device should check sink status field from the DPCD and take link training again.

Appendix C

Main link eye diagram of TP3

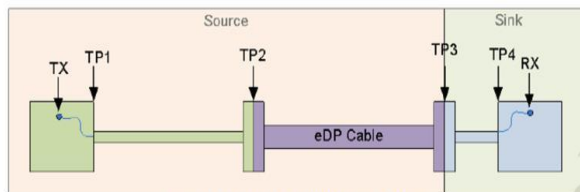
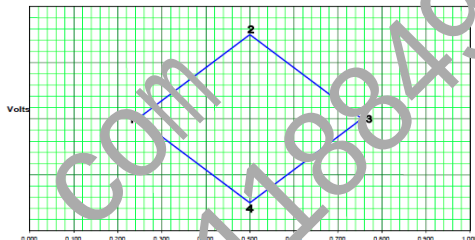


Figure 4-1: Embedded Link Reference Points



Measured TP3 on LCM connector.

Downstream Device Mask at TP3

	UI	Voltage
1	0.246	0
2	0.5	0.075
3	0.755	0
4	0.5	-0.075

Eye for TP3 at HBR

	UI	Voltage
1	0.375	0
2	0.5	0.023
3	0.625	0
4	0.5	-0.023

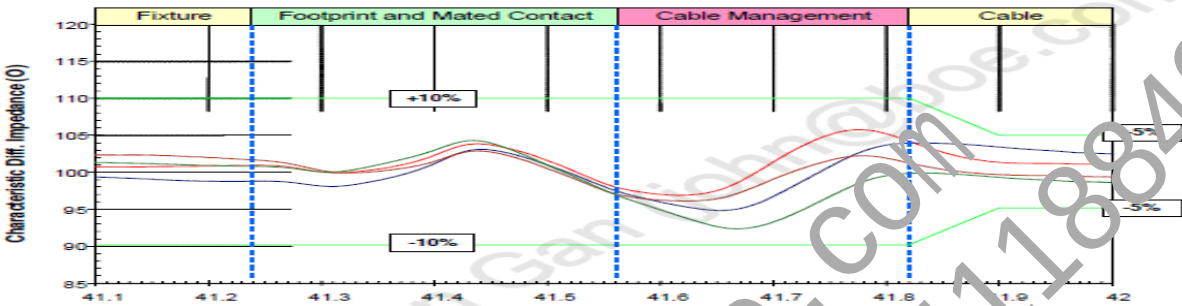
Eye for TP3 at RBR

Purpose

1. Main Link EYE Diagram should meet TP3 point of VESA.
2. The measure method is through access fixture.

Appendix C

Impedance Profile through a DP Connector



Differential Impedance Profile Measurement Data Example

Segment	Differential Impedance Value	Maximum Tolerance
Fixture	100Ω/VESA	±10%
Connector	100Ω/VESA	±10%
Wire management	100Ω/VESA	±10%
Cable	100Ω/VESA	±5%

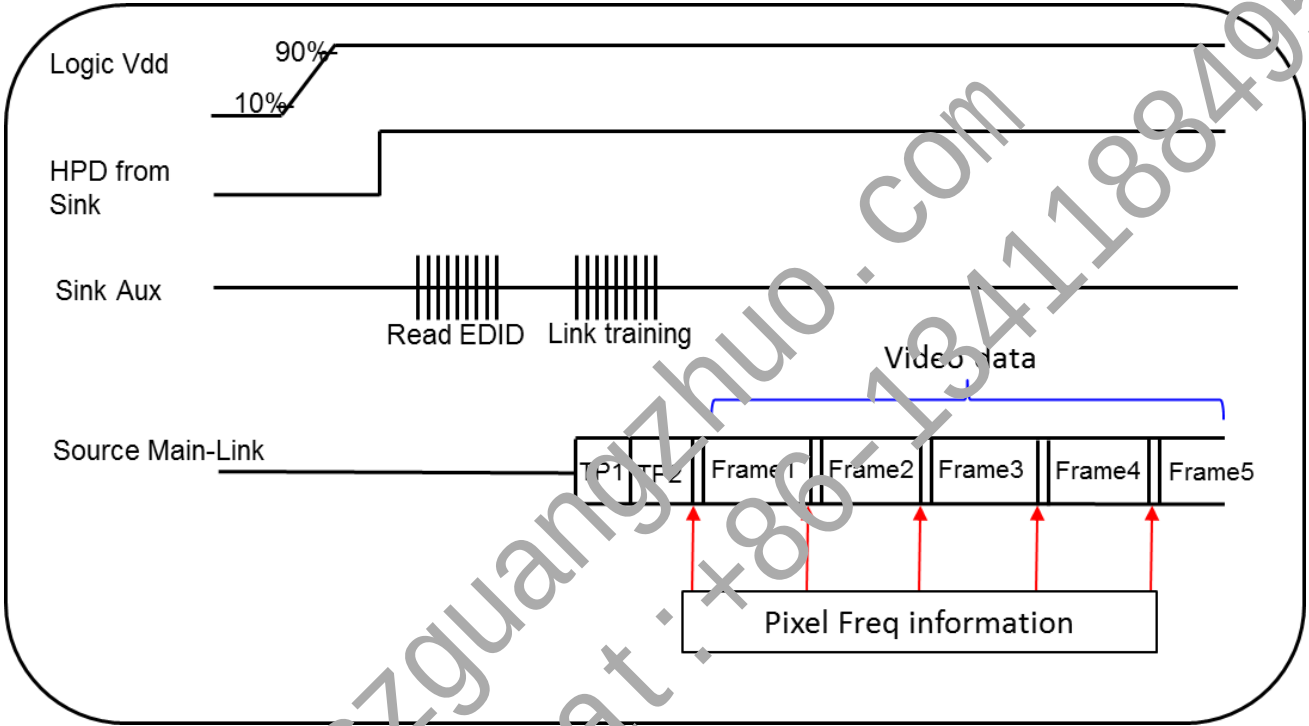
Impedance Profile Values for Cable Assembly

Purpose

Cable Impedance Profile 100ohm for Cable Assembly

Appendix C

Main Link Pixel Freq information value of MSA data

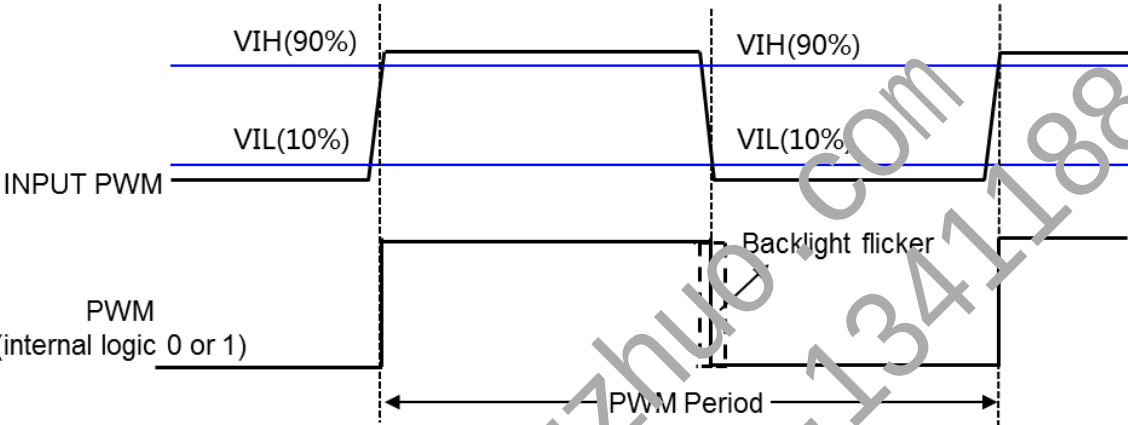


Purpose

1. It need to fix pixel freq information value of MSA data output to prevent the initial abnormal pixel freq information value from incoming after power on.
2. BOE can read DPCD to check this value. Ex: BIOS is 1.62G , but into windows is 2.7G.

Appendix C

System Input PWM Rising/Faling time



Example:

Freq	Cycle Time	PWM Rising Time	PWM Falling Time
200Hz	5ms	≤1us	≤1us
1KHz	1ms	≤200ns	≤200ns

Purpose

1. LED driver need to calculate the duty cycle of input PWM signal.
2. To avoid backlight flicker visible on LCD, system input PWM suggest : PWM rising ≤ 200ppm*cycle time ; PWM falling ≤ 200ppm*cycle time.