TITLE ：NE140QDM-K61

Customer: DELL

Product Specification

Rev. 0

(DELL DPN : 1DDTM)

Nanjing BOE Display Technology Co., Ltd

REVISION HISTORY

( )Preliminary Specification

(√)Final Specification

Revision No.	Page	Description of Changes	Date	Prepared
0	67	Final specification	2025.05.15	Ruan Jun

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Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

NE140QDM-K61 is a color active matrix TFT LCD module using Oxide TFT's (Thin Film Transistors) as an active switching devices. This module has a 14 inch diagonally measured active area with QHD resolutions (2560 horizontal by 1600 vertical pixel array).. Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can 16777216 (8bit) colors and color gamut sRGB 100%. The TFT-LCD panel In Cell Touch Structure and used for this module is a low reflection and higher color type. Therefore, this module is suitable for Notebook PC. The LED driver for back-light driving is built in this model.

All input signals are eDP1.4b interface compatible.

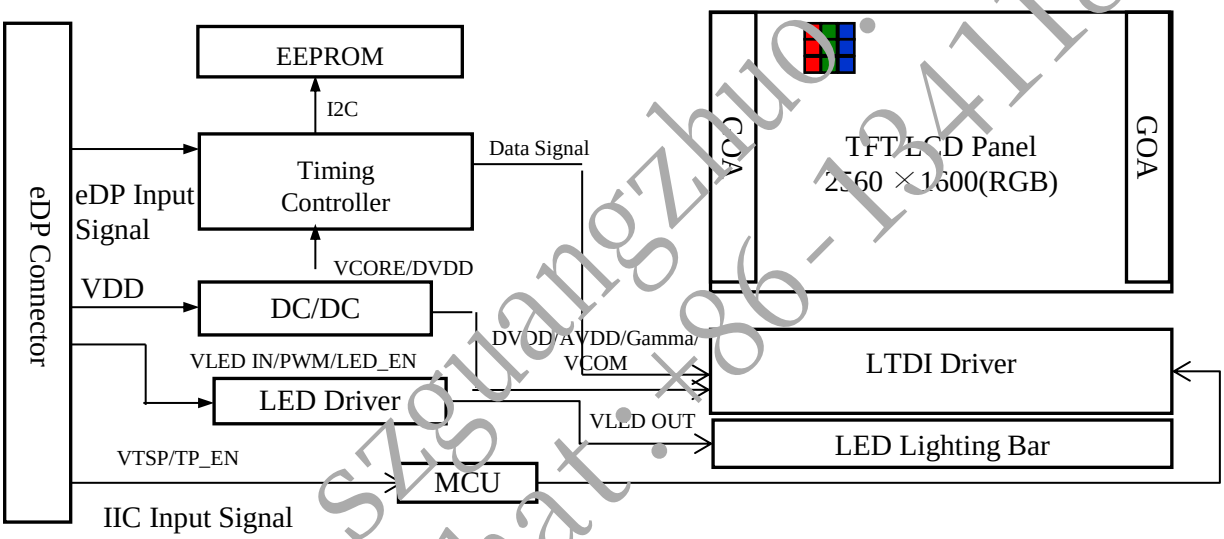


Figure 1. Drive Architecture

1.2 Features

- 2 lane eDP interface with 5.4Gbps link rates
- Thin and light weight, Low Blue Light
- 16777216 (8bit) color depth, gamut sRGB 100%
- Single LED lighting bar (Bottom side/Horizontal Direction)
- Data enable signal mode
- Green product (RoHS & Halogen free product)
- On board LED driving circuit
- Low driving voltage and low power consumption
- On board EDID chip
- DPCD Version 1.4
- Function： BIST/SDRRS/PSR2/SSC
- Adjust backlight brightness with DC mode

1.3 Application

- Notebook PC (Wide type)

1.4 General Specification

The followings are general specifications at the model NE140QDM-K61. (listed in Table 1-1)

<Table 1-1. General Specifications>

Parameter	Specification	Unit	Remarks
Active area	301.5936 (H) ×188.496 (V)	mm	
Number of pixels	2560 (H) ×1600 (V)	pixels	
Pixel pitch	117.81(H) ×117.81(V)	um	
Pixel arrangement	RGB Vertical stripe		
Display colors	16777216 (8bit)		
Color gamut	sRGB 100% typ., 95% min		
Display mode	Normally Black		
Dimensional outline	306.594±0.3(H)×198.396±0.5(V)×2.0(Max.)(W/O PCB) 306.594±0.3(H)×198.396±0.5(V)×4.0(Max.)(W/I PCB)	mm	
Weight	192.18 (Typ.) 210 (Max.)	g	
Surface treatment	Fine AG		
Surface hardness	3H		
Back-light	Bottom edge side, 1-LED lighting bar type		Note 1
Power consumption	P_D : 1.1W(Max.)	W	@Mosaic
	P_{BL} : 2.65(Max.)	W	@VLED=12V
	P_{Total} : 3.75(Max.)	W	@Mosaic

Notes : 1. LED Lighting Bar (60*LED Array)

1.5 Touch General Specification

The followings are touch general specifications at the model NT140WHM-T01. (listed in Table 1-2)

<Table 1-2. General Specifications>

Parameter	Specification	Unit	Remarks
Type of Touch Sensor	Self Capacitance		
Touch Structure	In Cell		
Panel Size	14.0”		
TP Active Area	301.5936 (H) ×188.496 (V)	mm	
Surface treatment	Anti-Glare		
Surface Hardness	3H	H	
Interface	IIC		
Report Rate	120	Hz	
Multi-Touch Point	10 points		
Input method	Finger		
Touch panel sensor IC	SW92513B		LX Semicon Touch
Channel	3840		48*80
Support OS	Win11 compliant		
VID	29BD		
PID	9081		

2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Absolute Maximum Ratings>

Ta=25+/-2°C

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-0.3	4.0	V	Note 1
eDP input Voltage	V_{eDP}	0	1.98	V	
Logic Supply Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V	
Operating Temperature	T_{OP}	0	+50	°C	Note 2
Storage Temperature	T_{ST}	-20	+60	°C	

Notes :
1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.
2. Temperature and relative humidity range are shown in the figure below.
95 % RH Max. (40 °C ≥ Ta) Maximum wet-bulb temperature at 39°C or less.(Ta >40°C)No condensation.

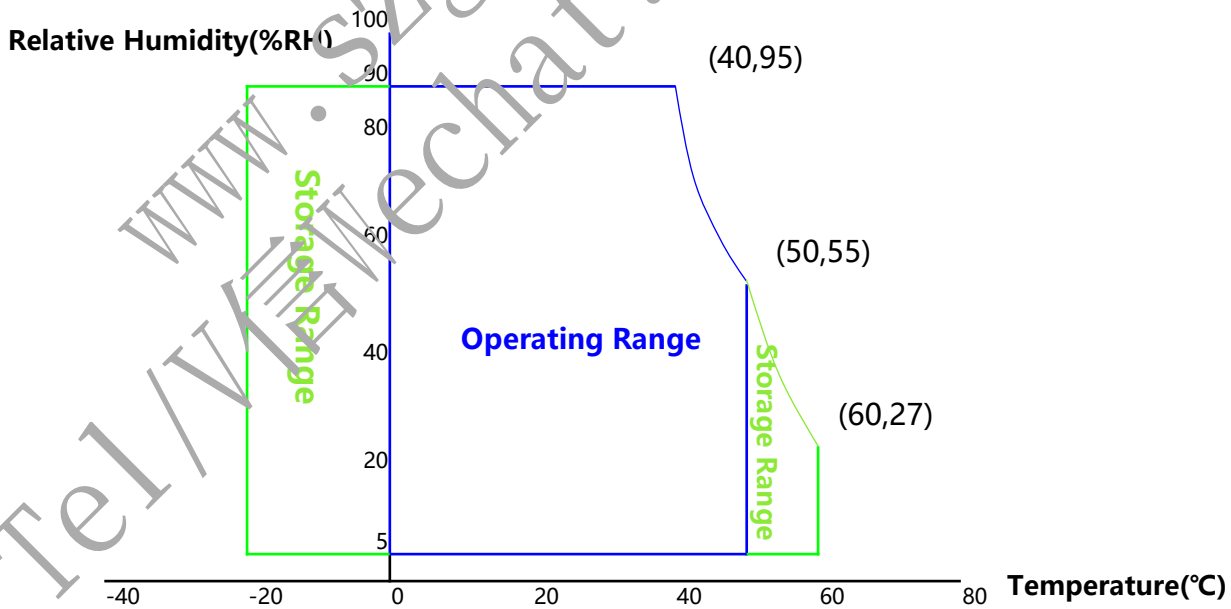


Figure 2. Temperature and Relative Humidity Range

3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

< Table 3-1. Electrical Specifications > Ta=25+/-2°C

Parameter			Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage		V_{DD}	3.0	3.3	3.6	V	Note 1
Permissible Input Ripple Voltage		V_{RF}	-10% VDD	-	+10% VDD	V	@V_{DD} = 3.3V, note4
BIST Control Level		High Level	2.0	-	3.465	V	@V_{IO}=3.3V Note 5
		Low Level	-0.3	-	0.8	V	
Power Supply Inrush Current		I_{nrush}	-	-	2	A	Note3
Power Supply Current	Mosaic	I_{DD}	-	-	334	mA	
	Red		-	-	334	mA	
	Green		-	-	334	mA	
	Blue		-	-	334	mA	
Power Consumption	Mosaic	P_M	-	-	1.1	W	
	Red	P_R	-	-	1.1	W	
	Green	P_G	-	-	1.1	W	
	Blue	P_B	-	-	1.1	W	
	BLU	P_{BL}	-	2.55	2.65	W	Note 2
	Total	P_{Total}	-	-	3.75	W	Note 1

3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

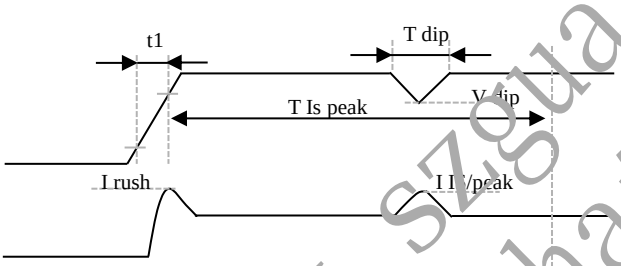
Notes :

1. The supply voltage is measured and specified at the interface connector of LCM.
   The current draw and power consumption specified is for 3.3V at 25 ˚C.(Typ. value for reference)
   a) Mosaic pattern 8*8
   b) R/G/B patterns

(a) (b)

Figure 3. Power Measure Patterns

2. Calculated value for reference ($V_{LED} \times I_{LED}$) , The power consumption with LED Driver are under the VLED = 12.0V , 25℃, PWM Duty 100% .
3. Measure condition (Figure 4)



Item	spec	Remark
V dip	> 2.7V	At LCD Connector
T IS/peak	< 80ms	Follow T3 specification
I IS/peak	≤2A	
T dip	≤10ms	
I rush	≤2A	

Figure 4. Inrush Measure Condition

4. Input voltage range:3.0~3.6V Test condition: Oscilloscope bandwidth 20MHz, AC coupling
5. BIST setting

Pin No	Define	Enable	Disable
14	BIST	Pull High	Pull Low/Floating

3.1 Electrical Specifications

< Table 3-2 Touch specifications >

Parameter			Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage		V_{DD}	3.0	3.3	3.6	V	Note 1
Permissible Input Ripple Voltage		V_{RF}	-	-	100	mV	At V_{DD} = 3.3V
TP_EN	High Level		2.0	-	-	V	@VDDIO
	Low Level		-	-	0.8	V	

Notes : 1. The supply voltage is measured and specified at the interface connector of TLCM
The current draw and power consumption specified is for 3.3V at 25℃ when touch function is active;

3.2 Backlight Unit

< Table 4. LED Driving Guideline Specifications > Ta=25+/-2˚C

Parameter			Min.	Typ.	Max.	Unit	Remarks
LED Forward Voltage		V_F	-	-	2.85	V	
LED Forward Current		I_F	-	13.5	-	mA	
LED Power Input Voltage		V_{LED}	5	12	21	V	
LED Power Input Current		I_{LED}	-	-	220.8	mA	Note 1
LED Power Consumption		P_{LED}	-	2.55	2.65	W	
Power Supply Voltage for LED Driver Inrush		Iled inrush	-	-	1.5	A	
LED Life-Time		N/A	15,000	-		Hour	I_F = 13.5mA Note 2
EN Control Level	Backlight On	V_{BL_ON}	1.2	-	5.0	V	Note 4
	Backlight Off		0	-	0.6	V	
PWM Control Level	High Level	V_{BL_PWM}	2.0	-	3.465	V	
	Low Level		0	-	0.8	V	
PWM Control Frequency		F_{PWM}	200	-	2,000	Hz	
Duty Ratio			5	-	100	%	Note 3

Notes :
1. The current and power consumption with LED Driver are under the VLED = 12.0V , 25℃, PWM Duty 100% .
2. The LED life-time define as the estimated time to 50% degradation of initial luminous.
3. Measure condition (Figure 5).
4.LED_EN&PWM setting

Pin No	Define	Enable	Disable
22	LED_EN	Pull High	Pull Low/Floating
23	PWM	Pull High	Pull Low/Floating

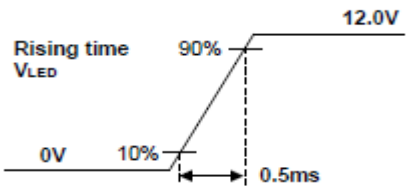


Figure 5. Inrush Measure Condition

3.3 LED Structure

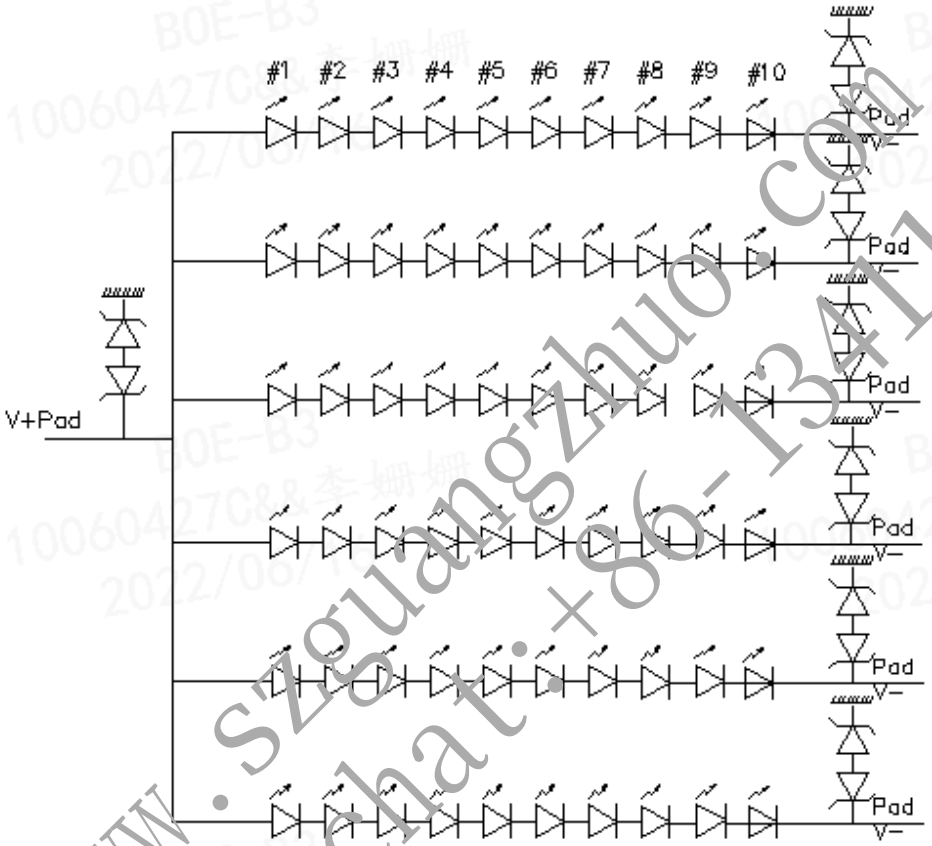


Figure 6. LED Structure

4.0 OPTICAL SPECIFICATION

4.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2℃) with the equipment of luminance meter system (SR-3AR) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to θØ=0 (=θ3) as the 3 o'clock direction (the "right"), θØ=90 (= θ12) as the 12 o'clock direction ("upward"), θØ=180 (= θ9) as the 9 o'clock direction ("left") and θØ=270(= θ6) as the 6 o'clock direction ("bottom"). While scanning θand/or Ø, the center of the measuring spot on the display surface shall stay fixed. The backlight should be operating for 30 minutes prior to measurement. VDD shall be 3.3+/- 0.3V at 25°C.

4.2 Optical Specifications

<Table 5. Optical Specifications>

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ_3	CR > 10	80	85	-	Deg.	Note 1
		Θ_9		80	85	-	Deg.	
	Vertical	Θ_{12}		80	85	-	Deg.	
		Θ_6		80	85	-	Deg.	
Luminance Contrast Ratio		CR	Θ = 0°	1000	1200	-		Note 2
Luminance of White	5 Points	Y_w	Θ = 0° I_{LED} = 13.5mA	340	400	-	cd/m²	Note 3
White Luminance Uniformity	5 Points	ΔY5		80	-	-		Note 4
	13 Points	ΔY13		65	-	-		
White Chromaticity		W_x	Θ = 0°	0.283	0.313	0.343		Note 5
		W_y		0.299	0.329	0.359		
Reproduction of Color	Red	R_x	Θ = 0°	Typ.-0.03	0.655	Typ.+0.03		
		R_y			0.327			
	Green	G_x			0.300			
		G_y			0.606			
	Blue	B_x			0.146			
		B_y			0.059			
Color Gamut				95	100	-	%	sRGB
Response Time (Rising + Falling)		T_{RT}	Ta= 25℃ Θ = 0°	-	30	35	ms	Note 6
Color Temperature				5500	-	7000		
Cross Talk		CT	Θ = 0°	-	-	2.0	%	Note 7
Gamma		-	-	2.0	2.2	2.4		

Notes :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 7).

2. Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see Figure 7) Luminance Contrast Ratio (CR) is defined mathematically:

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Center Luminance of white is defined as luminance values of 5 point average across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 8 for a total of the measurements per display.

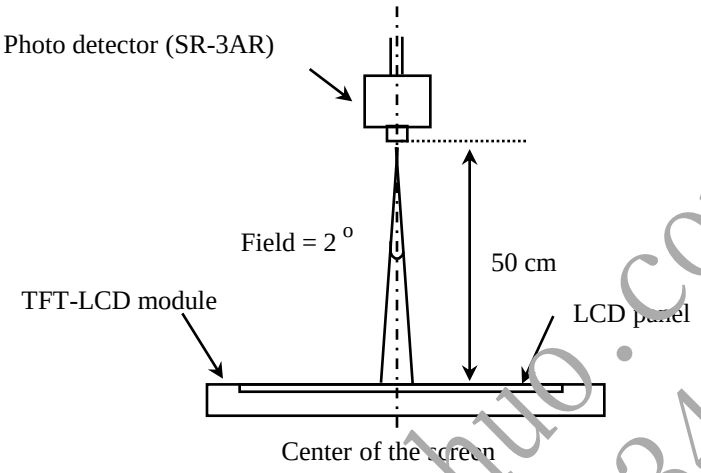
4. The White luminance uniformity on LCD surface is then expressed as : ΔY =Minimum Luminance of 5(or 13) points / Maximum Luminance of 5(or 13) points.(see Figure 8 and Figure 9).

5. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

6. The electro-optical response time measurements shall be made as Figure 10 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_r, and 90% to 10% is T_f.

7. Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (Y_A) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (Y_B) of that same area when any adjacent area is driven dark. (See Figure 11).

4.3 Optical Measurements



Optical characteristics measurement setup

Figure 7. Measurement Set Up

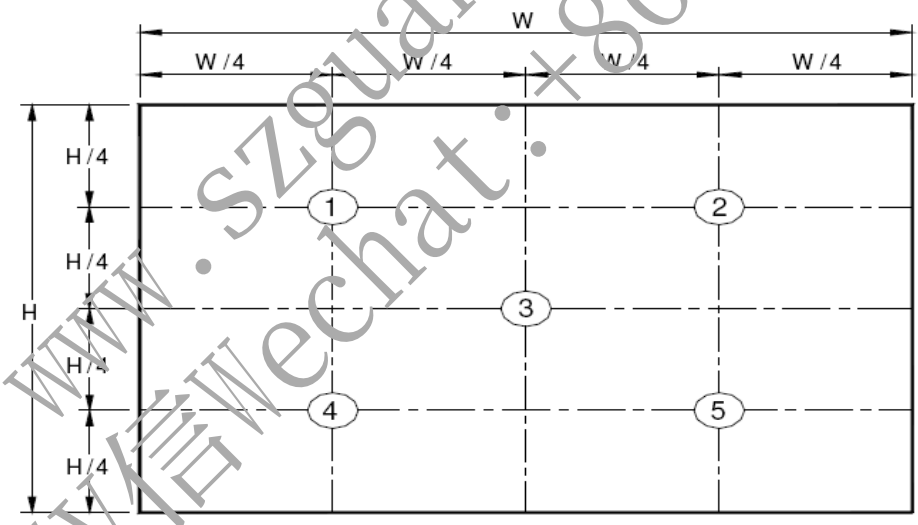


Figure 8. White Luminance and Uniformity Measurement Locations (5 points)

Center Luminance of white is defined as luminance values of center 5 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 7 for a total of the measurements per display.

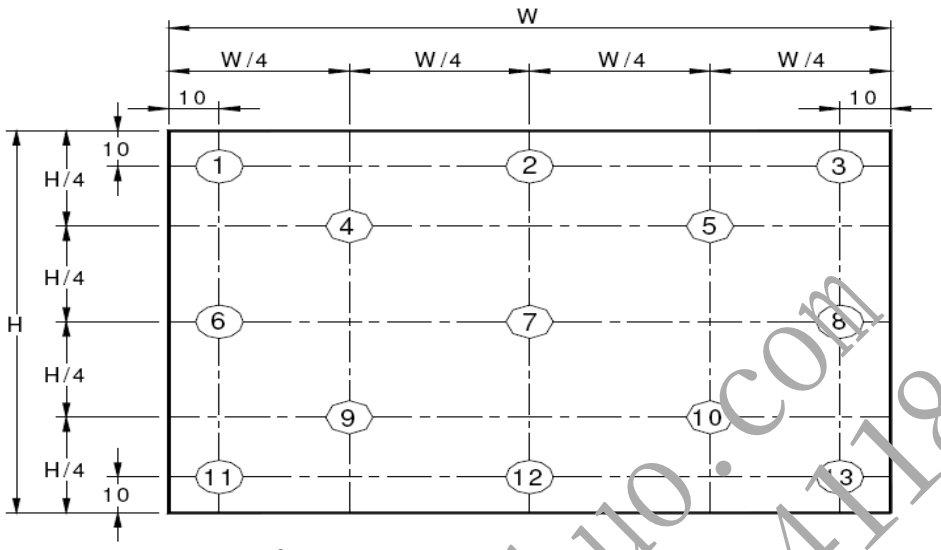


Figure 9. Uniformity Measurement Locations (13 points)

The White luminance uniformity on LCD surface is then expressed as : ΔY5 = Minimum Luminance of five points / Maximum Luminance of five points (see Figure 8) , ΔY13 = Minimum Luminance of 13 points /Maximum Luminance of 13 points (see Figure 9)

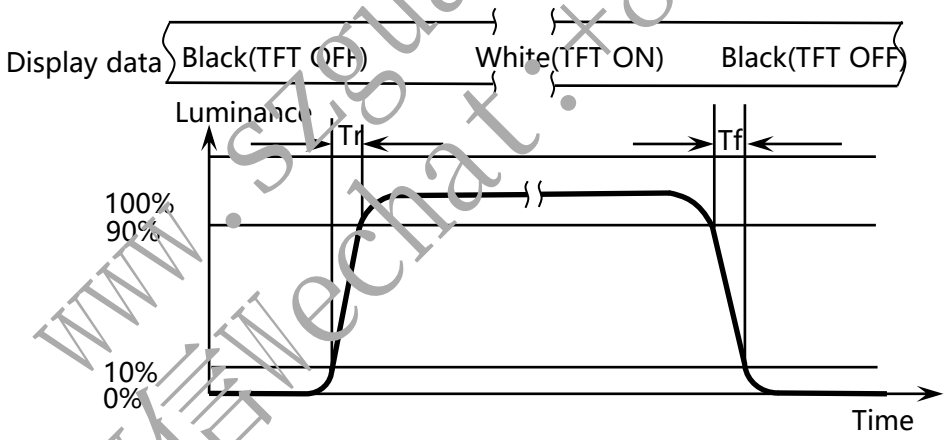
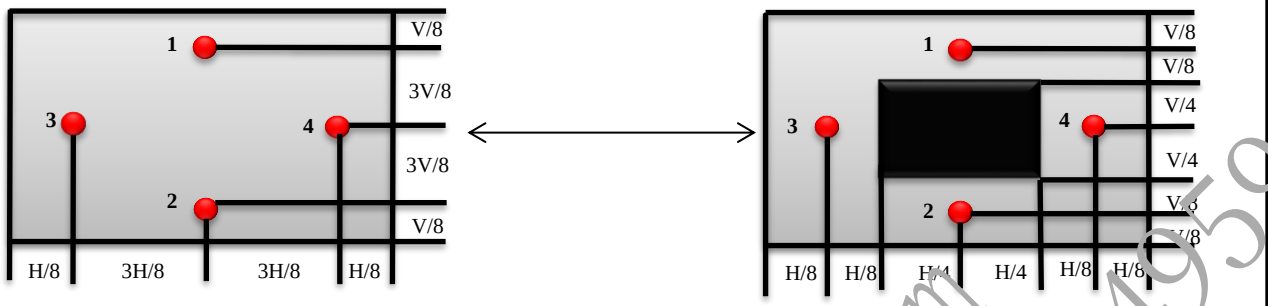


Figure 10. Response Time Testing

The electro-optical response time measurements shall be made as shown in Figure 10 by switching the "data" input signal ON and OFF. Tr: The luminance to change from 10% to 90% ,Tf: The luminance to change from 90% to 10% .

The test system : GRT



$$\text{Cross Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_A} \right| \times 100$$

Figure 11. Cross Talk Modulation Test Description

Where:

Y_A = Initial luminance of measured area (cd/m^2)

Y_B = Subsequent luminance of measured area (cd/m^2)

The location 1/2/3/4 measured will be exactly the same in both patterns. The test background gray is from L64 to L192.Take the largest data as the result.

Cross Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark.(Refer to Figure 11)

The test system: PR730

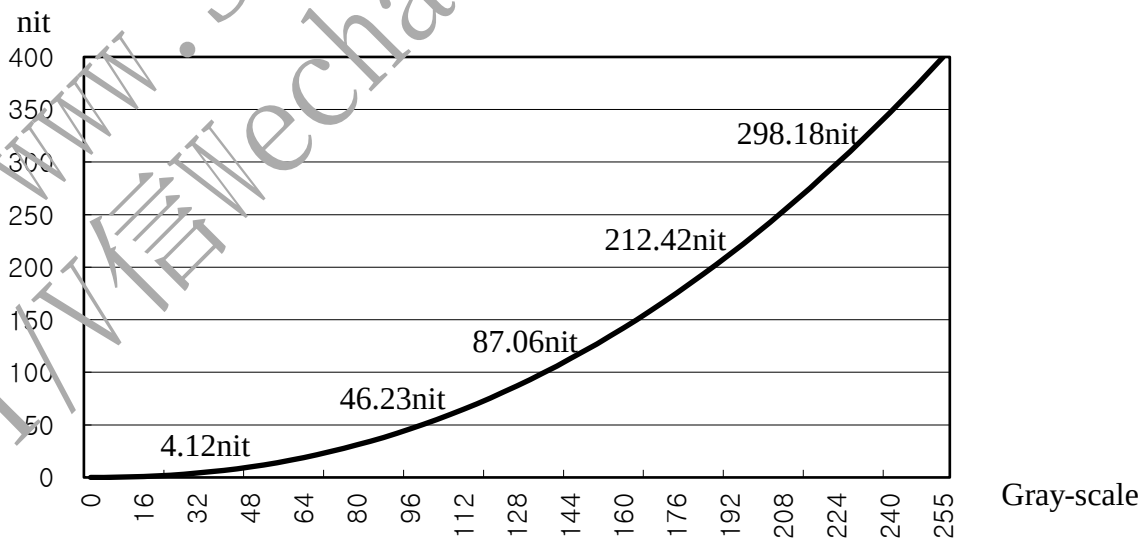


Figure 12. Brightness and Gray-scale Contrast

5.0 INTERFACE CONNECTION

5.1 Electrical Interface Connection

The electronics interface connector is IPEX 20682-040E.

The connector interface pin assignments are listed in Table 6.

<Table 6. Pin Assignments for the Interface Connector>

PIN NO	Symbol Function	Description	PIN NO	Symbol Function	Description
1	DBC_EN	DBC enable from +2.5V to +3.3V; DBC disable on Grounding	21	BL_GND	Backlight ground
2	H_GND	High Speed Ground	22	BL_Enable	Backlight On / Off
3	Lane1_N	Comp Signal Link Lane 1	23	BL_PWM_DIM	System PWM signal Input
4	Lane1_P	True Signal Link Lane 1	24	NC	No connect (Reverse for TEST only)
5	H_GND	High Speed Ground	25	NC	No connect (Reverse for TEST only)
6	Lane0_N	Comp Signal Link Lane 0	26	BL_PWR	Backlight power (5V~21V)
7	Lane0_P	True Signal Link Lane 0	27	BL_PWR	Backlight power (5V~21V)
8	H_GND	High Speed Ground	28	BL_PWR	Backlight power (5V~21V)
9	AUX_CH_P	True Signal Auxiliary Ch.	29	BL_PWR	Backlight power (5V~21V)
10	AUX_CH_N	Comp Signal Auxiliary Ch.	30	NC	No Connect (Reserved for CM)
11	H_GND	High Speed Ground	31	TP_D-	USB Data- for Touch
12	LCD_VCC	LCD logic and driver power	32	TP_D+	USB Data+ for Touch
13	LCD_VCC	LCD logic and driver power	33	GND	Ground–Shield
14	LCD_Self_Test	LCD Panel Self Test Enable	34	VTSP	Touch panel power supply (3.3V)
15	LCD_GND	LCD logic and driver ground	35	VTSP	Touch panel power supply (3.3V)
16	LCD_GND	LCD logic and driver ground	36	TP_EN	Enable/Disable of Touch function
17	HPD	HPD signal pin	37	TP_CLK	I2C Clock for Touch (for IIC interface)
18	BL_GND	Backlight ground	38	TP_Data	I2C Data for Touch (for IIC interface)
19	BL_GND	Backlight ground	39	INT	Interrupt for Touch (for IIC interface)
20	BL_GND	Backlight ground	40	RST	Reset for Touch (for IIC interface)

5.2 eDP Interface

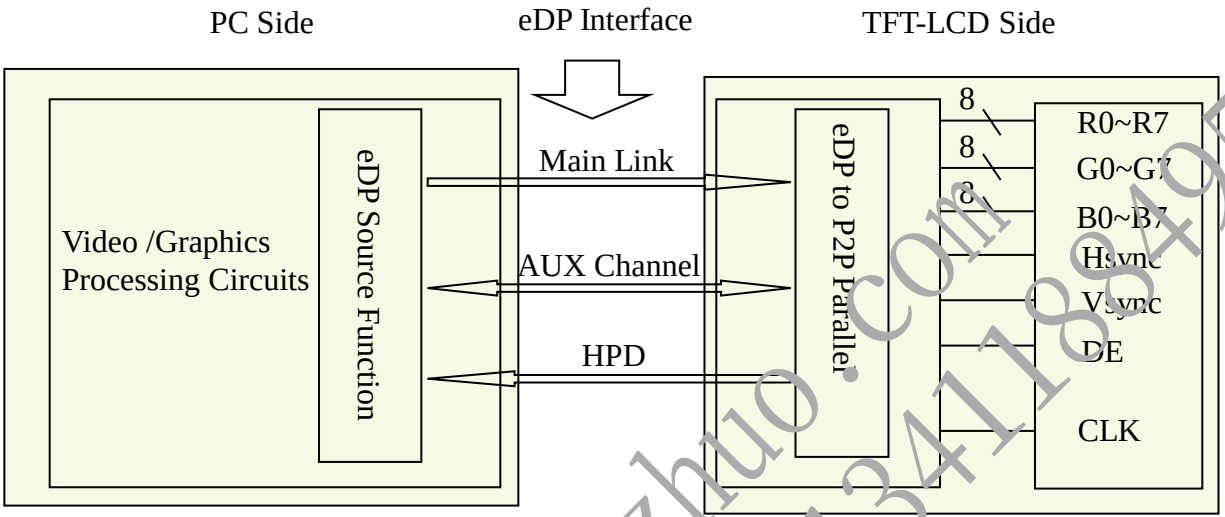


Figure 13. eDP Interface Architecture

Note:
Transmitter : Analogix ANX2167BN.
Transmitter is not contained in module.

5.3 Data Input Format

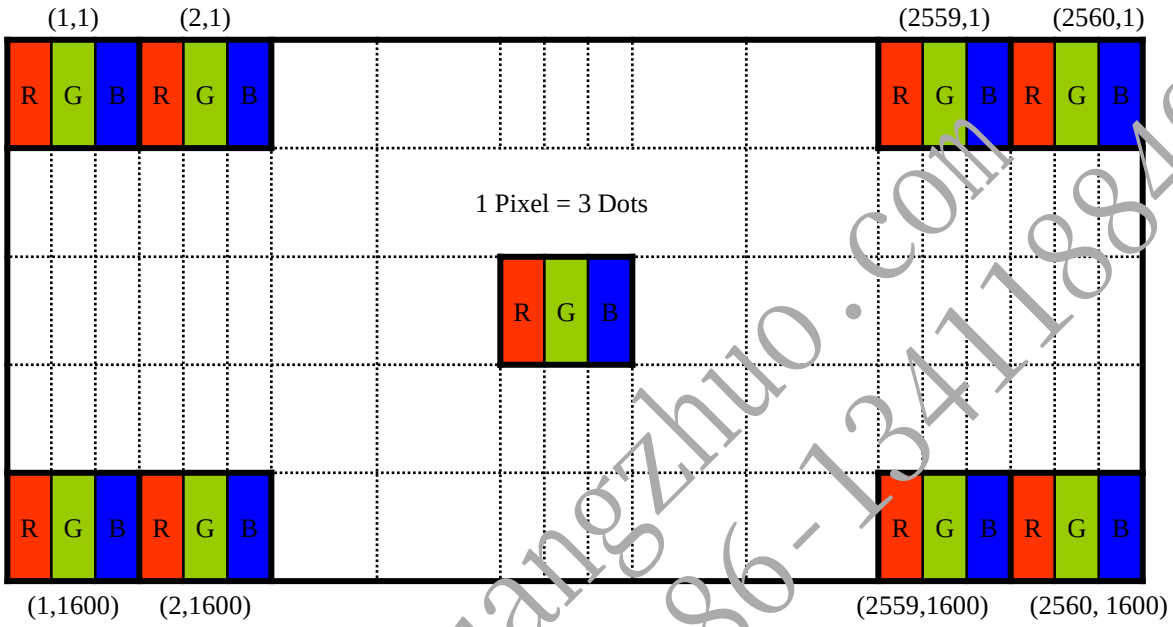


Figure 14. Display Position of Input Data (V-H)

5.4 Back-light & LCM Interface Connection

BLU Interface Connector: EIVW FC0510-L0822W560H100-N0

<Table 7. Pin Assignments for the BLU Connector>

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	LED	LED cathode connection	6	LED	LED cathode connection
2	LED	LED cathode connection	7	GND	Ground Shielding
3	LED	LED cathode connection	8	NC	No Connection
4	LED	LED cathode connection	9	Vout	LED anode connection
5	LED	LED cathode connection	10	Vout	LED anode connection

6.0 SIGNAL TIMING SPECIFICATION

6.1 The NE140QDM-K61 Is Operated By The DE Only

< Table 8. Signal Timing Specification >

Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	-	280.7	-	MHz
Frame Period		Tv	-	1720	-	lines
			-	60	-	Hz
			-	16.67	-	ms
Vertical Display Period		Tvd	-	1600	-	lines
One line Scanning Period		Th	-	2720	-	clocks
Horizontal Display Period		Thd	-	2560	-	clocks

Note :
1.The above timing specification based on refresh rate of 60_typ Hz
2.The above is as optimized setting

6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 9.

<Table 9. eDP Main-Link RX TP4 Package Pin Parameters>

Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock (Link clock down-spreading)	SSC	-	-	0.5	%	
Differential peak-to-peak input voltage at package pins	$V_{RX-DIFFp-p}$	120	-	1200	mV	
Rx input DC common mode voltage	$V_{RX\_DC\_CM}$	0	-	2	V	
Differential termination resistance	$R_{RX-DIFF}$	80	-	100	Ω	
Single-ended termination resistance	R_{RX-SE}	40	-	60	Ω	
Rx short circuit current limit	I_{RX_SHORT}	-	-	20	mA	
Intra-pair skew at Rx package pins (HBR) RX intra-pair skew tolerance at HBR	$L_{RX\_SKEW\_INTRA\_PAIR}$	-	-	60	ps	
AC Coupling Capacitor	C_{SOURCE_ML}	75		200	nF	Source side

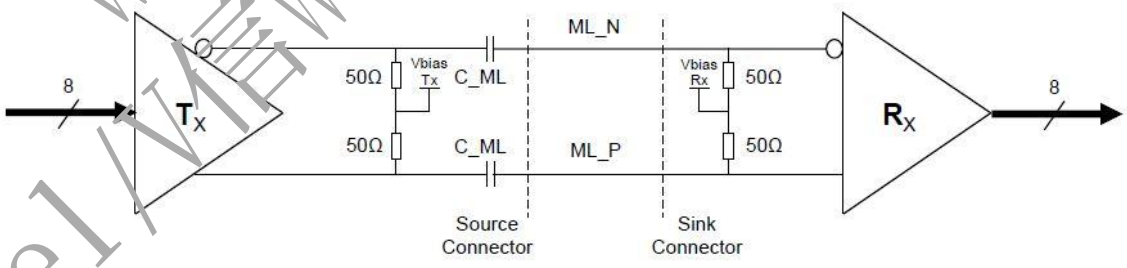


Figure 15. Main link differential pair

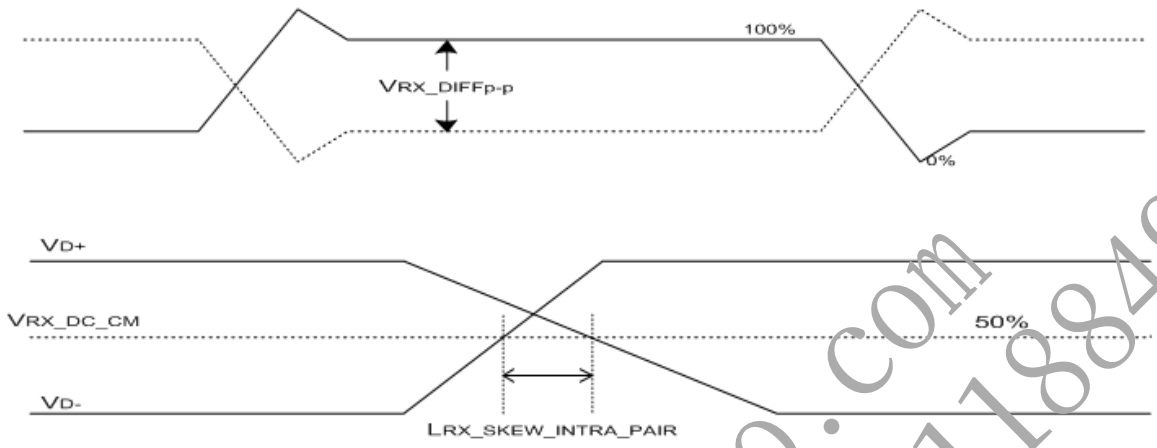


Figure 16. VRX-DIFFp-p & LRX_SKEW_INTRA_PAIR

<Table 10. HPD Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
HPD voltage	V_{HPD}	2.25	-	3.6	V	Sink side
Hot Plug Detection Threshold	-	2.0	-	-	V	Source side
Hot Unplug Detection Threshold	-	-	-	0.8V	V	
HPD_IRQ Pulse Width	HPD_IRQ	0.5	-	1	ms	
HPD_TimeOut	-	2.0	-	-	ms	

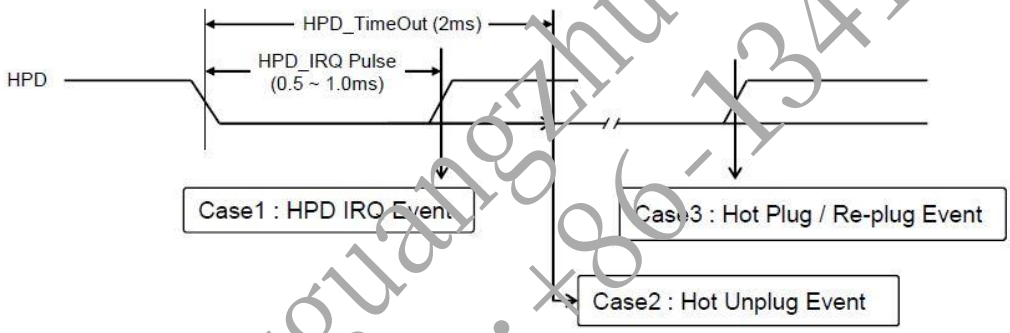


Figure 17. HPD Events

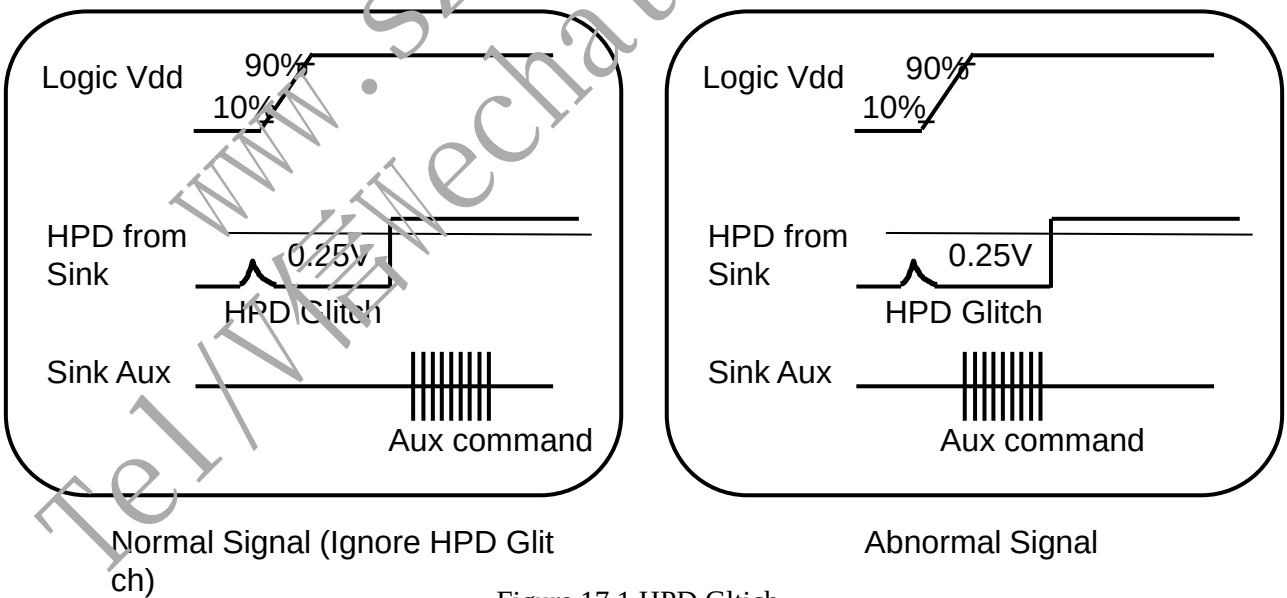


Figure 17.1 HPD Gltich

<Table 11. AUX Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
AUX unit interval	U_{IAUX}	0.4	0.5	0.6	Us	
AUX peak-to-peak input differential voltage	$V_{AUX-RX-DIFFp-p}$	0.29	-	1.38	V	Sink Side Connector Pin
AUX CH termination DC resistance	$R_{AUX-TERM}$	80	100	120	Ohm	
AUX DC common mode voltage	$V_{AUX-DC-CM}$	0	-	2	V	
AUX turn around common mode voltage	$V_{AUX-TURN-CM}$			0.3	V	
AUX short circuit current limit	$I_{AUX-SHORT}$	-	-	90	mA	
AUX AC Coupling Capacitor	$C_{SOURCE-AUX}$	75		200	nF	Source side

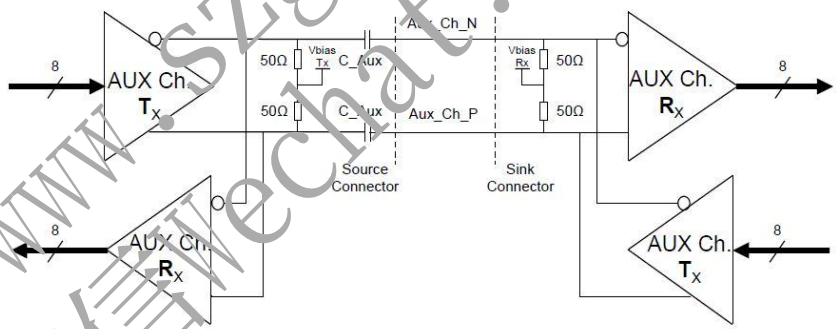


Figure 18. AUX differential pair

7.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

<Table 12. Input Signal & Basic Display Colors & Gray Scale of Colors >

	Colors & Gray scale	Data signal		
		R0 R1 R2 R3 R4 R5 R6 R7	G0 G1 G2 G3 G4 G5 G6 G7	B0 B1 B2 B3 B4 B5 B6 B7
Basic colors	Black	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	Blue	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1
	Green	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0
	Light Blue	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
	Red	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	Purple	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1
	Yellow	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0
	White	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
Gray scale of Red	Black	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	△	1 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	Darker	0 1 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	△	↑	↑	↑
	▽	↓	↓	↓
	Brighter	1 0 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	▽	0 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	Red	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Gray scale of Green	Black	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	△	0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	Darker	0 0 0 0 0 0 0 0	0 1 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	△	↑	↑	↑
	▽	↓	↓	↓
	Brighter	0 0 0 0 0 0 0 0	1 0 1 1 1 1 1 1	0 0 0 0 0 0 0 0
	▽	0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0
	Green	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0
Gray scale of Blue	Black	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	△	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0
	Darker	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 1 0 0 0 0 0 0
	△	↑	↑	↑
	▽	↓	↓	↓
	Brighter	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 0 1 1 1 1 1 1
	▽	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1
	Blue	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1
Gray scale of White& Black	Black	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	△	1 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0
	Darker	0 1 0 0 0 0 0 0	0 1 0 0 0 0 0 0	0 1 0 0 0 0 0 0
	△	↑	↑	↑
	▽	↓	↓	↓
	Brighter	1 0 1 1 1 1 1 1	1 0 1 1 1 1 1 1	1 0 1 1 1 1 1 1
	▽	0 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1
	White	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1

8.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below.

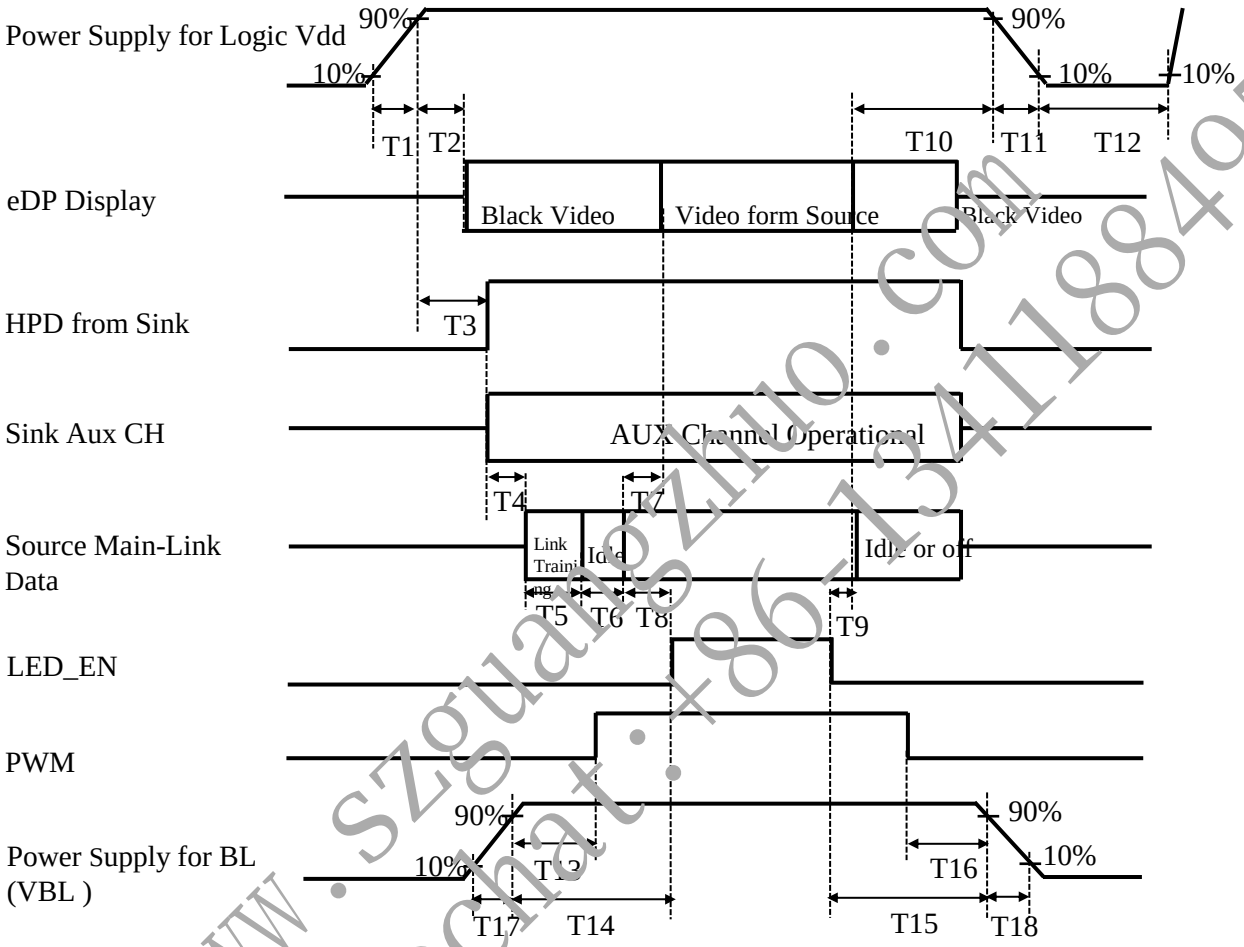


Figure 19-1. Power Sequence

- 0.5ms ≤ T1 ≤ 10 ms
- 0ms < T2 ≤ 80 ms
- 0ms < T3 ≤ 80 ms
- T4+T5+T6+T8>80ms
- 0ms < T7 ≤ 50ms
- 50ms < T8
- 0ms < T9
- 40ms < T10 < 500 ms
- 0.5ms ≤ T11 ≤ 10 ms
- 500ms ≤ T12
- 0ms < T13
- 0ms < T14
- 0ms < T15
- 0ms < T16
- 0.5ms ≤ T17
- 0.5ms ≤ T18

Notes:

1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal are valid.

To prevent a latch-up or DC operation of the TLCM module, the power on/off sequence of Touch shall be as shown in below

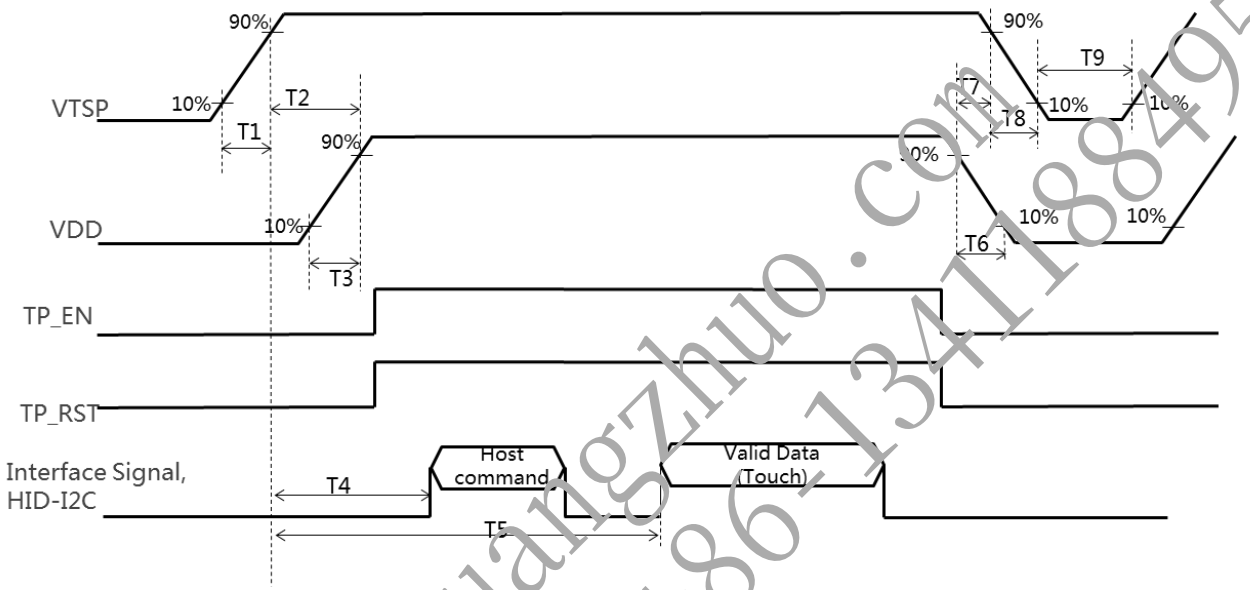


Figure 9-2 .Touch Power Sequence

- 0.5ms ≤ T1 ≤ 10 ms
- 0ms ≤ T2
- 0.5ms ≤ T3 ≤ 10 ms
- T4 > Max(52,T2+23)ms
- 600ms < T5
- 0.5ms ≤ T6 ≤ 10 ms
- 0ms ≤ T7
- 0.5ms ≤ T8 ≤ 10 ms
- 500ms < T9

Notes:

1. If TP_RST signal is Low, it is just touch sensing not work,
2. If TP_EN signal is Low, it does not report the coordinates

9.0 Connector Description

Physical interface is described as for the connector on LCM.
These connectors are capable of accommodating the following signals and will be following components.

9.1 TFT LCD Module

< Table 13. Signal Connector >

Connector Name /Description	For Signal Connector
Manufacturer	I-PEX
Type/ Part Number	I-PEX 20682-040E
Mating Housing/ Part Number	I-PEX 20679-040T

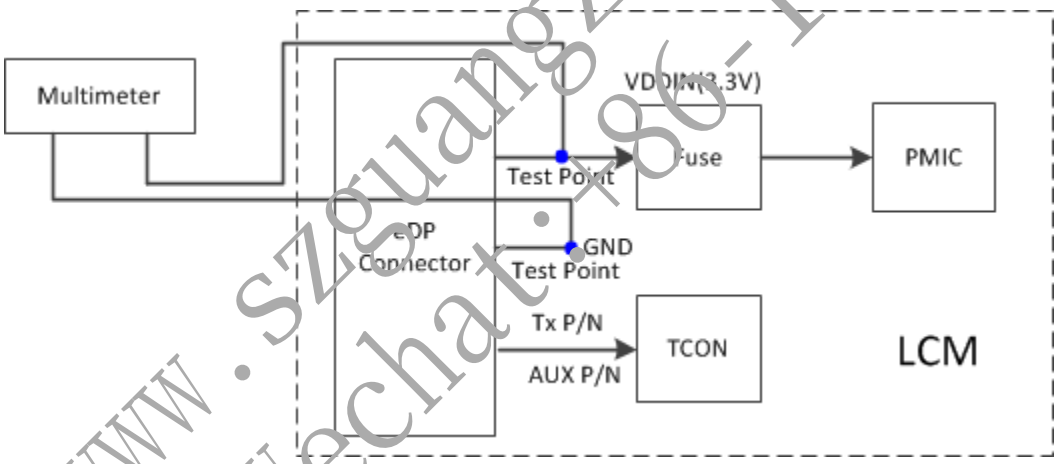
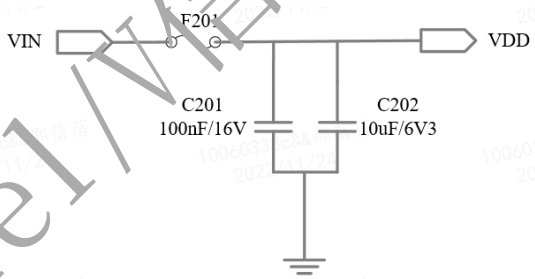


Figure 20. RC Loading Test Schematic Diagram



Item	RC Loading	
0RGNR	R	C
	13.71KΩ	14.3uF

Figure 21. VCC Loop R/C Loading Parameter

10.0 MECHANICAL CHARACTERISTICS

10.1 Dimensional Requirements

Figure 26 shows mechanical outlines for the model NE140QDM-K61.
Other parameters are shown in Table 14.

<Table 14. Dimensional Parameters>

Parameter	Specification	Unit
Active Area	301.5936 (H) ×188.496 (V)	mm
Number of pixels	2560 (H) X 1600(V) (1 pixel = R + G + B dots)	pixels
Pixel pitch	117.81(H) X 117.81(V)	um
Pixel arrangement	RGB Vertical stripe	
Display colors	16777216 (8bit)	
Display mode	Normally Black	
Dimensional outline	306.594±0.3(H)×198.396±0.5(V)×2.0(Max.)(W/O PCB) 306.594±0.3(H)×198.396±0.5(V)×4.0(Max.)(W/I PCB)	mm
Weight	192.18 (Typ.) 210 (Max.)	g

10.2 Mounting

See Figure 25.

10.3 Anti-Glare and Polarizer Hardness.

The surface of the LCD has an Glare coating to minimize reflection and a coating(3H) to reduce scratching.

10.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 350lux.

11.0 RELIABILITY TEST

The reliability test items and its conditions are shown in below.

<Table 15. Reliability Test>

No	Test Items	Conditions	Remark
1	High temperature storage test	Ta = 60˚C , 240 hrs	
2	Low temperature storage test	Ta = -20˚C , 240 hrs	
3	High temperature & high humidity operation test	Ta = 50˚C , 80%RH, 240 hrs	
4	High temperature operation test	Ta = 50˚C , 240 hrs	
5	Low temperature operation test	Ta = 0˚C , 240 hrs	
6	Thermal shock	Ta = -20 °C ↔ 60 °C (0.5 hr), 100 cycle	
7	Vibration test (non-operating)	Ta = 25˚C , 1.5G, 10~500Hz, Sine X,Y,Z / Sweep rate : 1 hour	Note 1
8	Shock test (non-operating)	Ta = 25˚C 220G, Half Sine Wave 2msec ±X, ±Y, ±Z Once for each direction	Note 1
9	Electro-static discharge test (operating)	Air : 150 pF, 330Ω, ±15 KV Contact : 150 pF, 330Ω, ±8 KV Ta = 25˚C ,	Note 2

Notes :

1. The fixture must be hard enough , so that the module would not be twisted or bent.
2. Self- recovery and restart recovery is allowed. No hardware failures.

12.0 HANDLING & CAUTIONS

(1) Cautions when taking out the module
- Pick the pouch only, when taking out module from a shipping package.

(2) Cautions for handling the module
- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation
- When the module is operating, do not lose CLK, ELIAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

(4) Cautions for the atmosphere
- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics
- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions
- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc. Please pack the module not to be broken. We recommend to use the original shipping packages.

13.0 LABEL

(1) Product Label

Figure 22.Product Label

Module ID Naming Rule:

<Table 16. Module ID Naming Rule>

Code \ Digit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Code	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Description	Product Name		Product Grade	Facility Code	Year		Month	Model Extension Code (Last 4 Digits FG Code)				Serial NO.					

Serial number marked part needs to print, show as follows:

1. Dell PPID NO.（2D barcode） 2. FG-CODE
3. DELL DP/N NO 4. Dell PPID NO.
5. Module ID
6. Module ID barcode

Total Size:43×12mm

14.0 PACKING INFORMATION

14.1 Packing Order

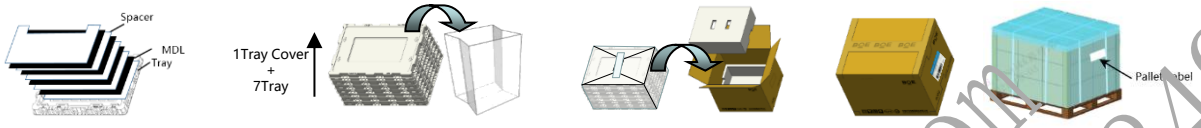


Figure 23. Packing Order

- Put 1pcs EPE Spacer in Tray and 1pcs MDL on Spacer.
  Capacity:4pcs MDL/Tray , 5pcs Spacer/Tray
- Put 7pcs tray and 1pcs tray cover in PE bag.
- Put PE bag with 2pcs EPE cover in the inner box.
  Capacity:28pcs MDL/Box,
- Use Packing Tape to Seal inner box,Stick the box label onto inner box and align it to the label mark.
- Put 18pcs Box on the Pallet , Secure with strapping tape, wrap around film, paper protection Angle.
  Capacity:6pcs Box/Layer, 3Layer, 504pcs MDL/Pallet

14.2 Note

- Box dimension:478mm*358mm*309mm
- Package quantity in one box: 28pcs
- Total weight: （9.06±10%） kg

14.3 Handing SOP



- Personnel shall cut the middle seam from left to right with bamboo sticks for sealing;
- Take out the upper part of the foam through the central opening of the foam with one hand and put it aside;
- Open the packing bag with both hands, take the product out of the carton and place it in the operation area;
- Take the tray cover + the two short sides of the uppermost tray with both hands, pay attention to holding the tray cover with both thumbs, and do not press it vigorously, and then buckle it on the work table;
- Take the product with both hands at the same time and take the 4 / 6 area of the lower gasket to the front of the body, then hold your right hand and move your left hand to area 8. Pay attention to placing your four fingers on the panel side and your thumbs on the back plate surface;
- Take the head of the lighting wire terminal with your right hand, and after checking that the wire has no abnormal appearance, insert the lighting wire terminal straight into the PCB connector;



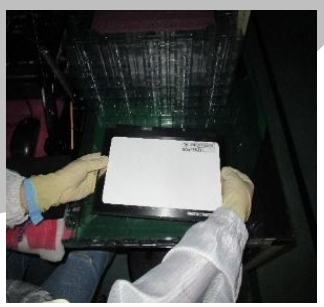



Figure 24. Handing SOP

15.0 MECHANICAL OUTLINE DIMENSION

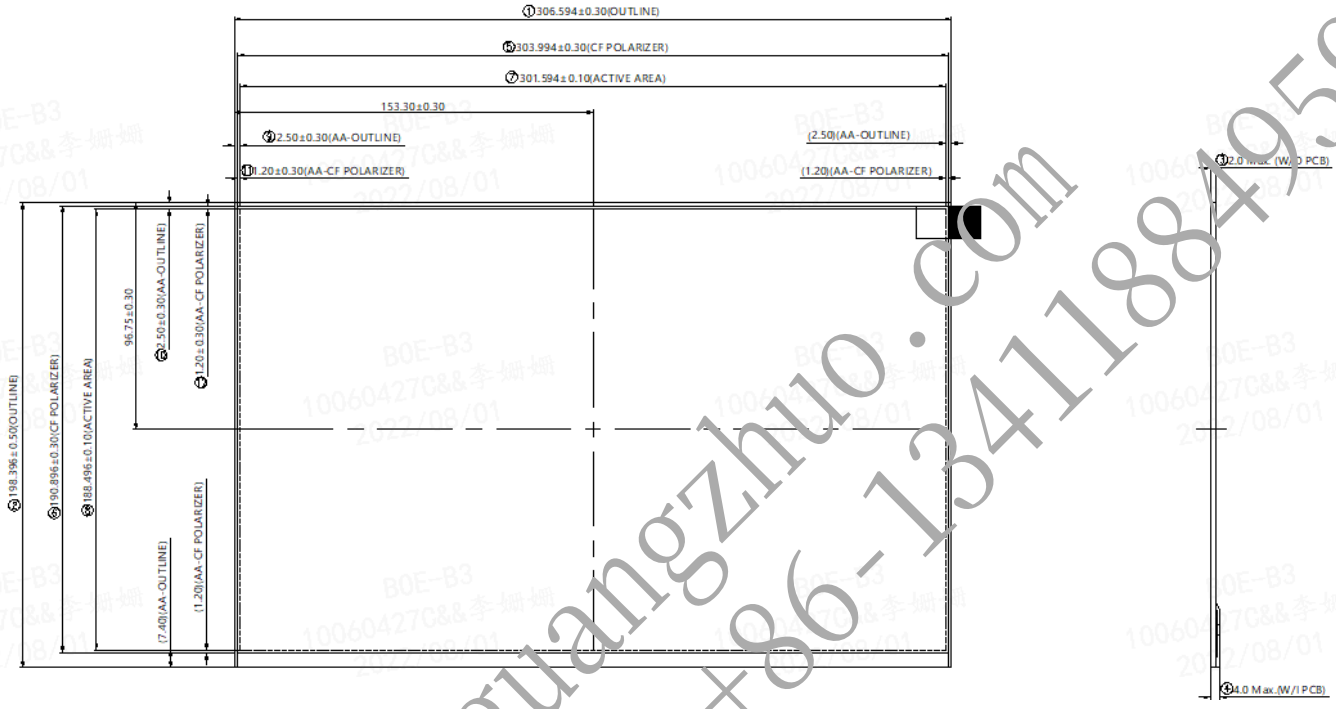


Figure 25. TFT-LCD Module Outline Dimension (Front View)

NOTES:
1.WARPAGE AND DEFORMATION SPEC.: 0.8mm MAX.
2.EDP CONNECTOR IS MEASURED AT PIN 1 AND MATING LINE
3.UNSPECIFIED TOLERANCE REFER TO +/- 0.3mm
4.TOP POLARIZER IS THE HIGHEST PORTION.
5.THE MEASUREMENT METHOD FOR THE DIMENSION OF MODULE, PLEASE REFER TO APPENDIX A.
6.CRITICAL DIMENSION: ①~⑭
CPK: ①~②
7. "()" REFER TO REFERENCE.

Top POL is the highest part.

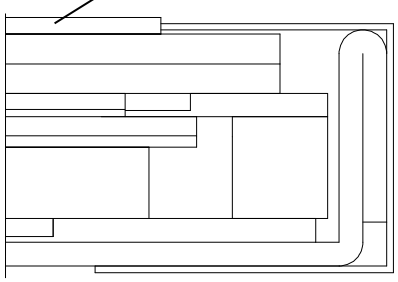


Figure 26. Highest Point Position

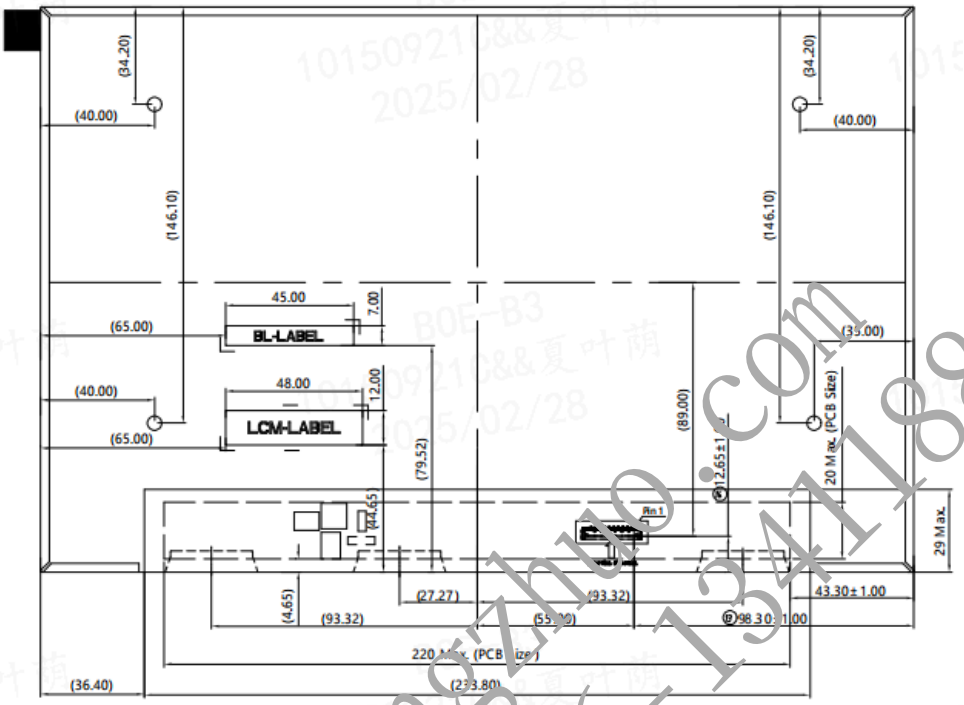
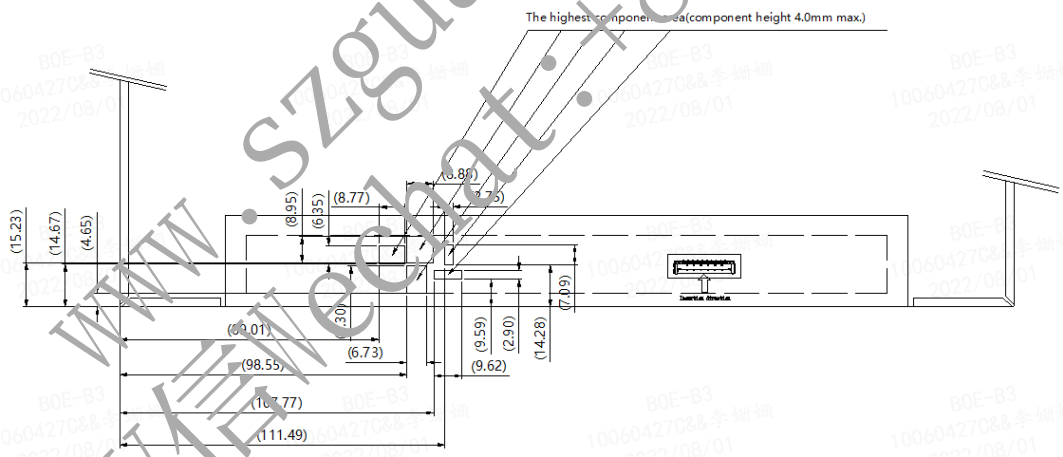


Figure 27. TFT-LCD Module Outline Dimensions (Rear view)



NOTES:
1.WARPAGE AND DEFORMATION SPEC.: 0.8mm MAX.
2.EDP CONNECTOR IS MEASURED AT PIN 1 AND MATING LINE
3.UNSPECIFIED TOLERANCE REFER TO +/- 0.3mm
4.TOP POLARIZER IS THE HIGHEST PORTION.
5.THE MEASUREMENT METHOD FOR THE DIMENSION OF MODULE, PLEASE REFER TO APPENDIX A.
6.CRITICAL DIMENSION:①~⑭
CPK:①~②
7. "()" REFER TO REFERENCE.

16.0 EDID Table

Address (HEX)	Function	Hex	Dec	crc	Input values.	Notes
00	Header	00	0		0	EDID Header
01		FF	255		255	
02		FF	255		255	
03		FF	255		255	
04		FF	255		255	
05		FF	255		255	
06		FF	255		255	
07		00	0		0	
08	ID Manufacturer Name	09	9		BOE	ID = BOE
09		E5	229			
0A	ID Product Code	1E	30		2846	ID = 2846
0B		0B	11			
0C	32-bit serial No.	00	0		0	
0D		00	0		0	
0E		00	0		0	
0F		00	0		0	
10	Week of manufacture	10	16		16	
11	Year of Manufacture	20	32		2022	Manufactured in 2022
12	EDID Structure Ver.	01	1		1	EDID Ver 1.0
13	EDID revision #	04	4		4	EDID Rev. 0.4
14	Video input definition	A5	165		-	Refer to right table
15	Max H image size	1E	30		30	30 cm (Approx)
16	Max V image size	13	19		19	19 cm (Approx)
17	Display Gamma	78	120		2.2	Gamma curve = 2.2
18	Feature support	07	7		-	Refer to right table
19	Red/Green low bits	FD	253		-	Red / Green Low Bits
1A	Blue/White low bits	85	133		-	Blue / White Low Bits
1B	Red x high bits	A7	167	671	0.655	Red (x) = 10100111 (0.655)
1C	Red y high bits	53	83	335	0.327	Red (y) = 01010011 (0.327)
1D	Green x high bits	4C	76	307	0.300	Green (x) = 01001100 (0.3)
1E	Green y high bits	9B	155	621	0.606	Green (y) = 10011011 (0.606)
1F	Blue x high bits	25	37	150	0.146	Blue (x) = 00100101 (0.146)
20	BLue y high bits	0F	15	60	0.059	Blue (y) = 00001111 (0.059)
21	White x high bits	50	80	321	0.313	White (x) = 01010000 (0.313)
22	White y high bits	54	84	337	0.329	White (y) = 01010100 (0.329)
23	Established timing 1	00	0		-	Refer to right table
24	Established timing 2	00	0		-	
25	Established timing 3	00	0		-	

26	Standard timing #1	01	1			Not Used
27		01	1			
28	Standard timing #2	01	1			Not Used
29		01	1			
2A	Standard timing #3	01	1			Not Used
2B		01	1			
2C	Standard timing #4	01	1			Not Used
2D		01	1			
2E	Standard timing #5	01	1			Not Used
2F		01	1			
30	Standard timing #6	01	1			Not Used
31		01	1			
32	Standard timing #7	01	1			Not Used
33		01	1			
34	Standard timing #8	01	1			Not Used
35		01	1			
36	Detailed timing/monitor descriptor #1	A7	167		280.70	280.704MHz Main clock
37		6D	109			
38		00	0		2560	Hor Active = 2560
39		A0	160		160	Hor Blanking = 160
3A		A0	160		-	4 bits of Hor. Active + 4 bits of Hor. Blanking
3B		40	64		1600	Ver Active = 1600
3C		78	120		120	Ver Blanking = 120
3D		60	96		-	4 bits of Ver. Active + 4 bits of Ver. Blanking
3E		30	48		48	Hor Sync Offset = 48
3F		20	32		32	H Sync Pulse Width = 32
40		36	54		3	V sync Offset = 3 line
41		00	0		6	V Sync Pulse width : 6 line
42		2E	46		302	Horizontal Image Size = 301.594 mm (Low 8 bits)
43		BC	188		188	Vertical Image Size = 188.496 mm (Low 8 bits)
44		10	16		-	4 bits of Hor Image Size + 4 bits of Ver Image Size
45		00	0		0	Hor Border (pixels)
46		00	0		0	Vertical Border (Lines)
47		1A	26		-	Refer to right table

48	Detailed timing/monitor descriptor #2	B9	185		224.6	224.5632MHz Main clock
49		57	87			
4A		00	0		2560	Hor Active = 2560
4B		A0	160		160	Hor Blanking = 160
4C		A0	160			4 bits of Hor. Active + 4 bits of Hor. Blanking
4D		40	64		1600	Ver Active = 1600
4E		78	120		120	Ver Blanking = 120
4F		60	96			4 bits of Ver. Active + 4 bits of Ver. Blanking
50		30	48		48	Hor Sync Offset = 48
51		20	32		32	H Sync Pulse Width = 32
52		36	54		3	V sync Offset = 3 line
53		00	0		6	V Sync Pulse width : 6 line
54		2E	46		302	Horizontal Image Size = 301.594 mm (Low 8 bits)
55		BC	188		188	Vertical Image Size = 188.496 mm (Low 8 bits)
56		10	16			4 bits of Hor Image Size + 4 bits of Ver Image Size
57		00	0		0	Hor Border (pixels)
58		00	0		0	Vertical Border (Lines)
59		1A	26			Refer to right above table
5A	Detailed timing/monitor descriptor #3	00	0			ASCII Data Sting Tag
5B		00	0			
5C		00	0			
5D		FE	254			
5E		00	0			
5F		31	49		1	Dell P/N:1DDTM
60		44	68		D	
61		44	68		D	
62		54	84		T	
63		4D	77		M	
64		80	128		10000000	EDID Revison:A00
65		4E	78		N	BOE PN
66		45	69		E	
67		31	49		1	
68		34	52		4	
69		51	81		Q	
6A		44	68		D	
6B		4D	77		M	

6C	Detailed timing/monitor descriptor #4	00	0			Flag
6D		00	0			
6E		00	0			
6F		00	0			Data Type Tag: Manufacturer Specified Data 00
70		00	0			Flag
71		02	2		-	6-bit Color Depth With 2FRC
72		41	65		-	WLED & singal light bar & one light bar
73		31	49		-	Frame rate 40Hz~65Hz
74		A8	168		-	Light Controller:PWM & Max. Luminance300
75		00	0		-	Front Surface:Anti-Glare & RGB v-stripe
76		01	1		-	with DBC
77		00	0		-	no Motion Blur & no Active Gamma
78		00	0		-	no Wireless Enhancement & no In-Cell Scanner
79		1A	26		-	2 Lane edp
7A		41	65		-	Built-In Self Test
7B		0A	10			Format： terminate with ASCII code 0Ah and pad field with ASCII code 20h
7C		20	32			
7D		20	32			
7E	Extension flag	00	0		1	0 ：1個EDID；N-1：N个EDID
7F	Checksum	9E	158	158	-	

17.0 GENERAL PRECAUTIONS

17.1 HANDLING

(1) When the module is assembled, It should be attached to the system firmly using every mounting holes. Be careful not to twist or bend the modules.

(2) Refrain from strong mechanical shock or any force to the module. Otherwise, it may cause improper operation or damage to the module.

(3) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than 1 HB pencil lead.

(4) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use Ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth .In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static , it may cause damage to the module.

(9) Use fingerstalls with soft gloves to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Do not pull or fold the LED FPC.

(l2) Do not touch any component which is located on the back side.

(13) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(14) Pins of connector shall not be touched directly with bare hands.

17.2 STORAGE

(1) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃ and relative humidity of less than 70%.

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.

17.3 OPERATION

(1) Do not connect, disconnect the module in the " Power On" condition.

(2) Power supply should always be turned on/off by following item 8.0 " Power on/off sequence ".

(3) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

(4) The standard limited warranty is only applicable when the module is used for general notebook applications. If used for purposes other than as specified, BOE is not to be held reliable for the defective operations. It is strongly recommended to contact BOE to find out fitness for a particular purpose.

17.4 OTHERS

(1) Avoid condensation of water. It may result in improper operation or disconnection of electrode.

(2) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation, Variation in part contents and environmental temperature, so on) Otherwise the module may be damaged.

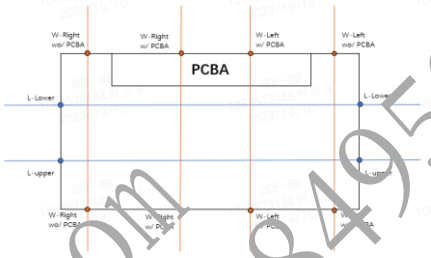
(3) If the module displays the same pattern continuously for a long period of time, it can be the situation when The " image sticks" to the screen.

(4) This module has its circuitry PCB's on the rear or bottom side and should be handled carefully to avoid being stressed.

Appendix A

The Measurement Methods for the Dimensions of Module

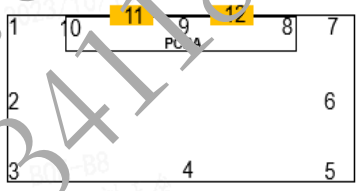
Caliper:
Length of Outline (Without Tape Wrinkle or Bulged)
Width of Outline (Without PCB) (Without Tape Wrinkle or Bulge
Width of Outline (With PCB)



Length & Width test point

Micrometer:
Thickness of Outline (Body)(Point 1~7)

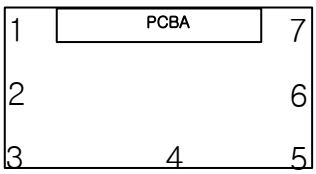
Height Gauge with Pressure Gauge(100g)
Thickness with Soft Area (FPC / COF /Cell Tape) (Point 8~12)



Thickness test point

Coordinate Measuring Machine:
CF Polarizer Size
Active Area (Or AA_BM) Size
Active Area to Outline (Without Tape Wrinkle or Bulged)
Active Area to CF Polarizer
The Distance of Bracket Holes
P-Cover to Outline (Without Tape Wrinkle or Bulged)
Length of P-Cover
Connector Pin 1 to Outline (Without Tape Wrinkle or Bulged)

Feeler Gauge: The Warpage Spec. of Module

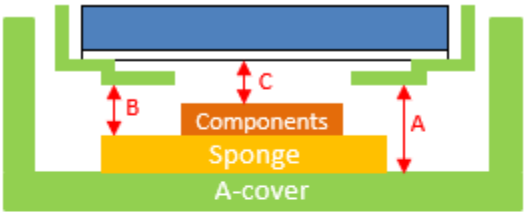


Warpage test point

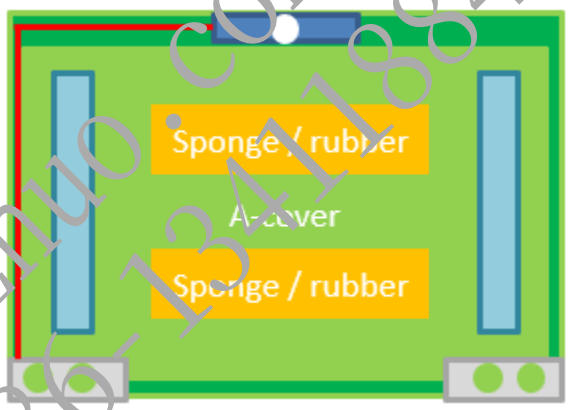
Notes:
Except the Critical Dimensions as Above, Other Dimensions are Measured by Coordinate Meas uring Machine If Necessary.

Appendix B

LCM to A-Cover / sponges Z-gap



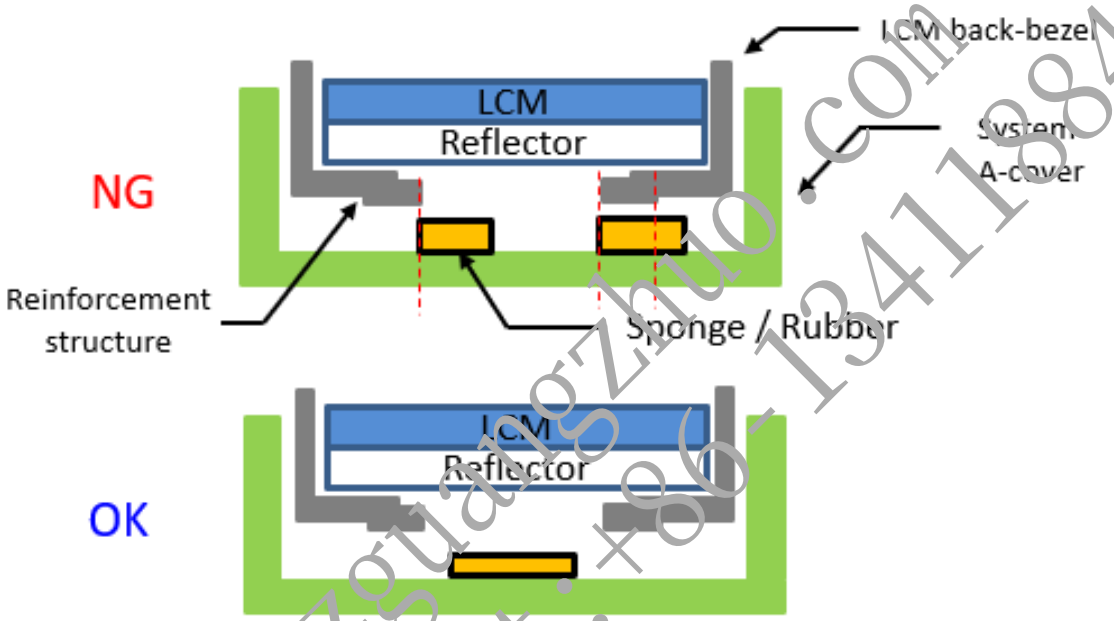
	Plastic Cover	Metal Cover
A	≥ 1.0mm	≥ 0.8mm
B	≥ 0mm	
C	> 0.5mm	



Purpose	The reflector area is very sensitive, BOE would suggest that design enough z-gap to decrease the risk of water ripple, white spots and other abnormal display

Appendix B

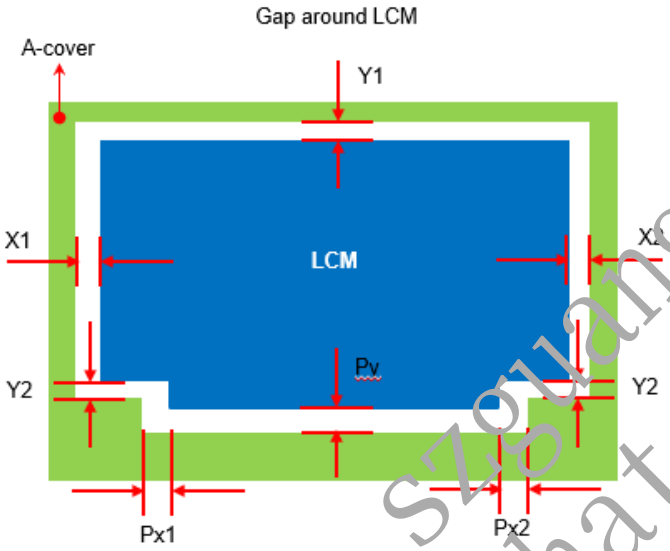
LCM to A-Cover / sponges z-gap



Purpose	If attach sponges or rubbers which correspond to white reflector area, it may cause white spot, pooling or other relative issues. BOE would suggest that attach wide range sponges / rubbers which can cover the LCM back-bezel opening

Appendix B

LCM to side wall / protrusions

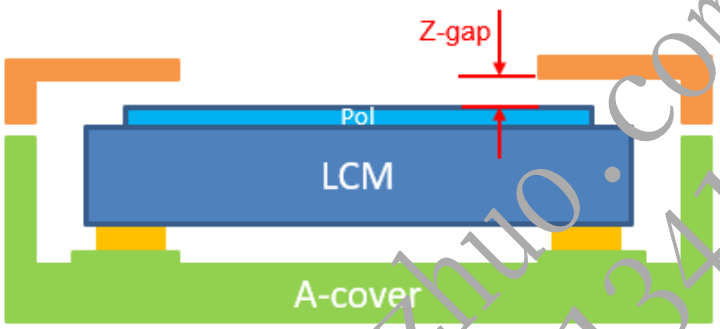


	Normal border (screws)	Narrow border (fix by tapes)
X1 / X2	Min: 0.45mm	Min: 0.35mm
Y1 / Y2	Min: 0.45mm	Min: 0.35mm
Px1 / Px2	Min: 0.55mm	
Pv		

Purpose	BOE would suggest that design enough gap around LCM to prevent shock test failure, or interference, cell crack, abnormal display…etc. in the reliability test

Appendix B

LCM to B-cover z-gap

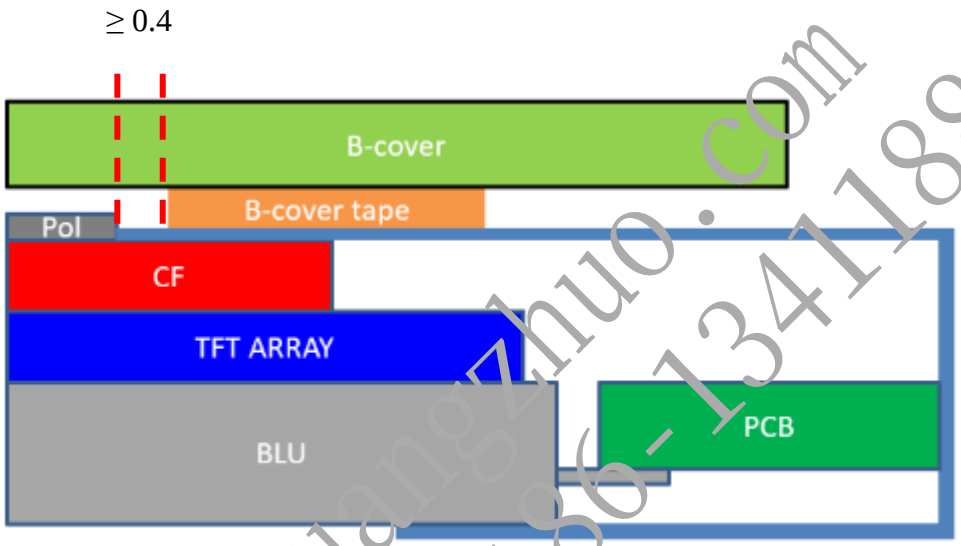


Bezel Tape	Z-Gap
Without	0.15 ~ 0.25mm
With	0.15 ~ 0.20mm

Purpose	Too less z-gap between system B-cover and LCM top pol has high risk that may cause cell crack, pooling, light leakage and other issues

Appendix B

B-cover tape to top pol edge

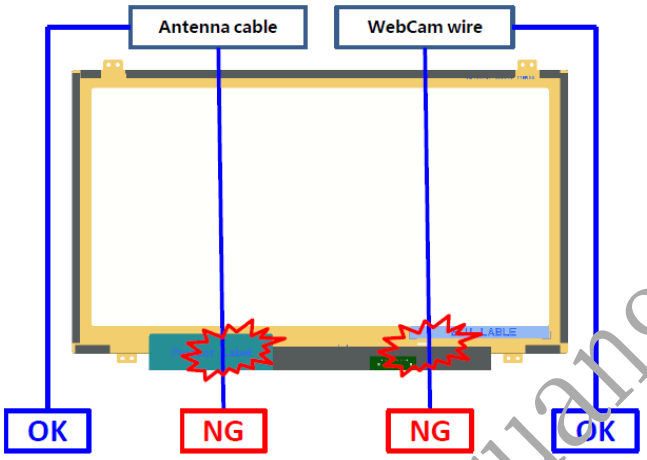


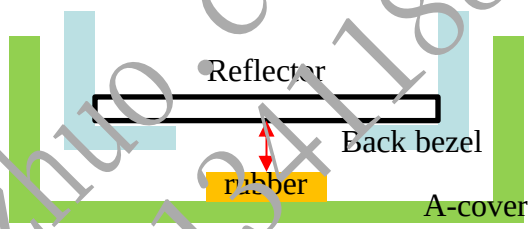
If attach b-cover and LCM with tapes,
Please let tapes to be located out of top pol edges 0.4mm away on 4 sides

Purpose	To avoid the B-cover tape override top pol then cause pooling or light leakage issue

Appendix B

Antenna Cable & Webcam wire



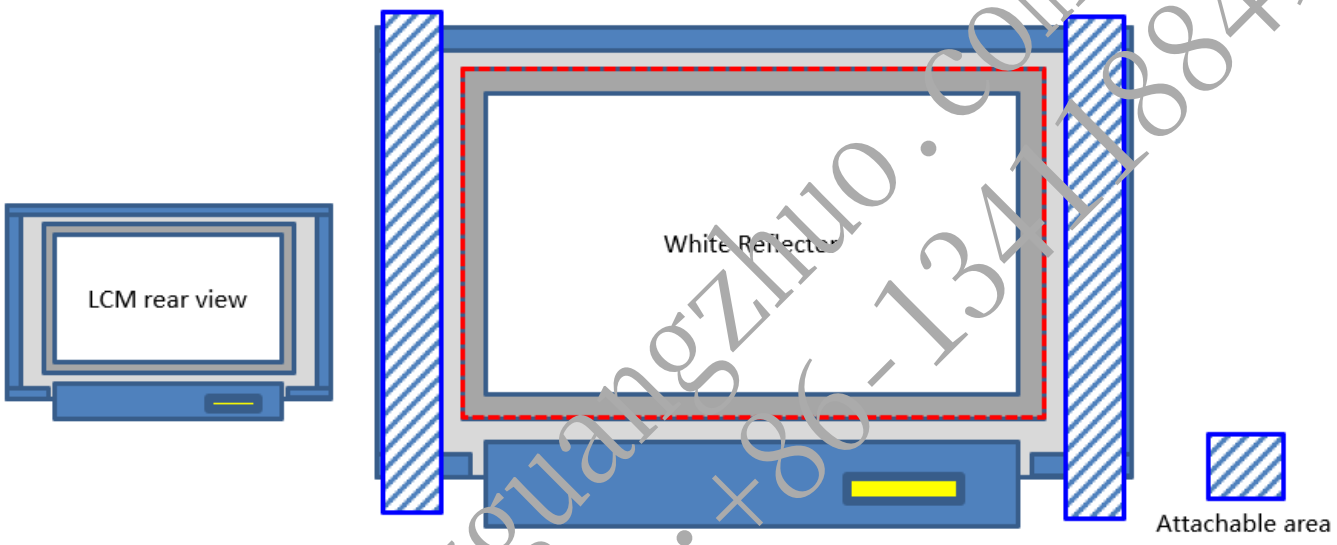


If sponge within the reflector area is necessary, we suggest that the gap between reflector and sponge is more than 0.5mm

Purpose	1. BOE would suggest that do not set Antenna or WebCam cable / wire go behind LCM to avoid backpack test, hinge test ,twist test or pogo test with abnormal display 2. If the cable / wire is necessary to go behind LCM, please make a groove with rounds or chamfers to protect the cable / wire, or attach with higher sponges / rubbers adjacent to the cable / wire route 3. Suggest that attach the cable / wire with tapes to A-cover 4. Do not attach anything with LCM reflector area. If attach cable / wire with LCM reflector area, it may cause pooling, white spot, light leakage and other related issues

Appendix B

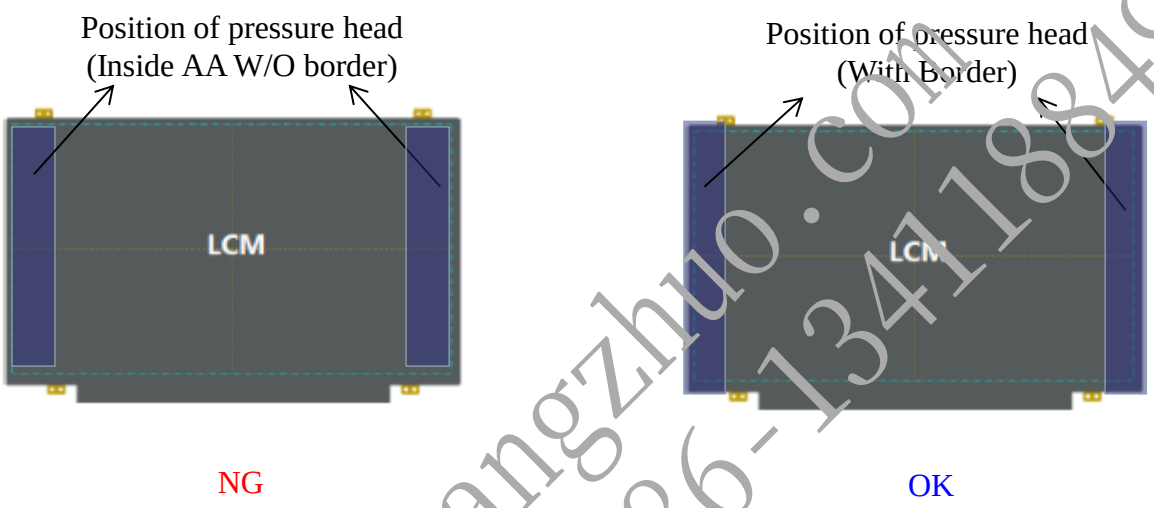
LCM paste area



Purpose	If use the stretch remove tapes to fix LCM with A-cover, please set the stretch remove tapes correspond to the LCM back-bezel and do not let the tapes override the back-bezel's level step of opening

Appendix B

LCM pressable area



Purpose	1. If LCM is fixed on A-cover by using the press jig during assembling. 2. To avoid panel broken the design of pressure head of press jig can not only pin on cell panel. The pressure head needs to pin on the LCM frame, which the LCM frame can share the pressure of the pressing head.

Appendix B

Wire setting	
	
Purpose	Wires should be placed between protrusions/side wall and A-cover. If place the wires between LCM and Protrusions/side wall, it may interfere with LCM when assembling, or even cause LCM broken in reliability test.

Appendix B

A-cover strength

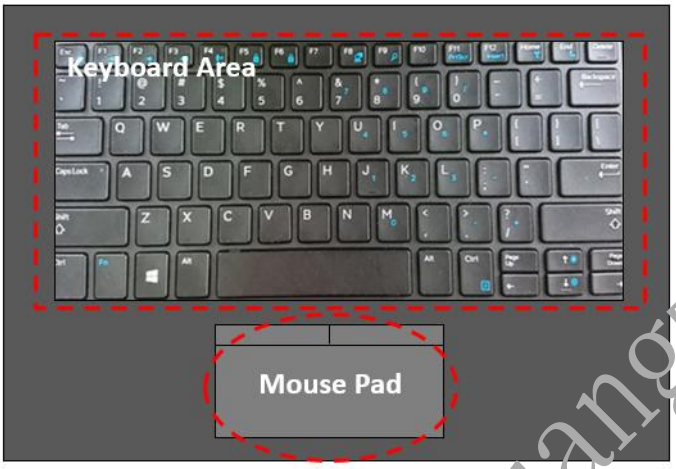
Purpose	1. BOE would recommend that structural Rib/Bracket height is higher than LCM, in order to avoiding pressures to LCM. 2. The L-shape Bracket is recommended.

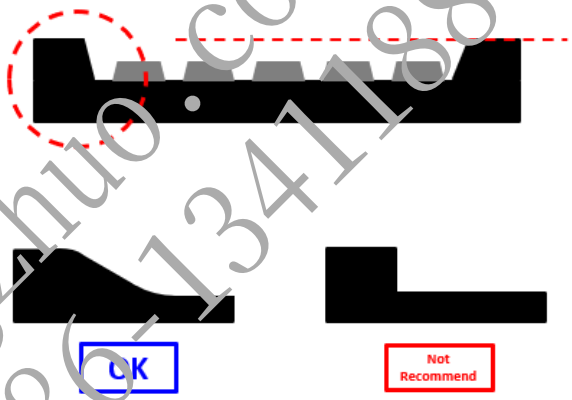
Appendix B

System A-cover Inner Surface	
	
Purpose	There should not exist any burr, segment gap or protrusions beside Logo, which may cause White Spot or Glass Broken by stress concentration.

Appendix B

Keyboard area & Mouse pad

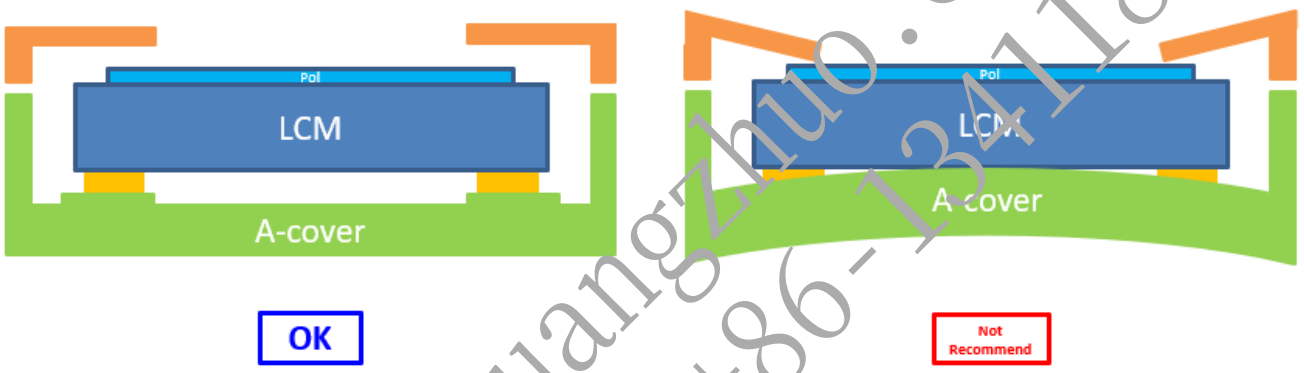




Purpose	The transition surface between keyboard and mouse pad should be smooth and without vertical steps\ too large level steps

Appendix B

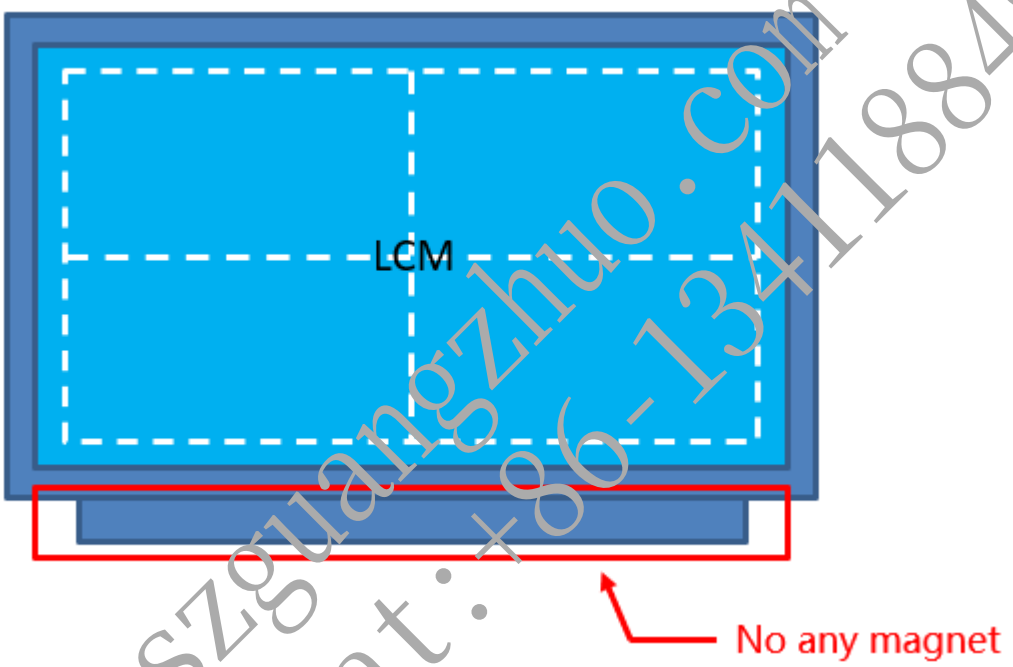
System cover reliability



Purpose	1. No interference between system and LCM in assembly process except compressible grounding gaskets 2. The permanent deformation which caused by Reliability test is not allowed to contact LCM

Appendix B

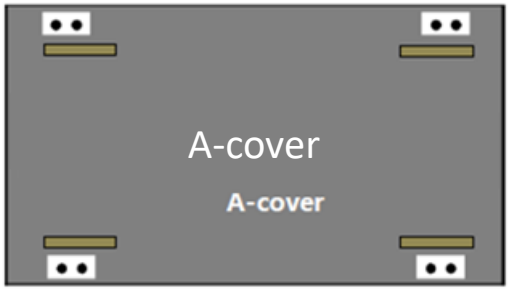
A/B-cover near LCD PCBA



Purpose	There should not been any magnet object close to LCM PCBA, it may cause physical or electricity noise issue

Appendix B

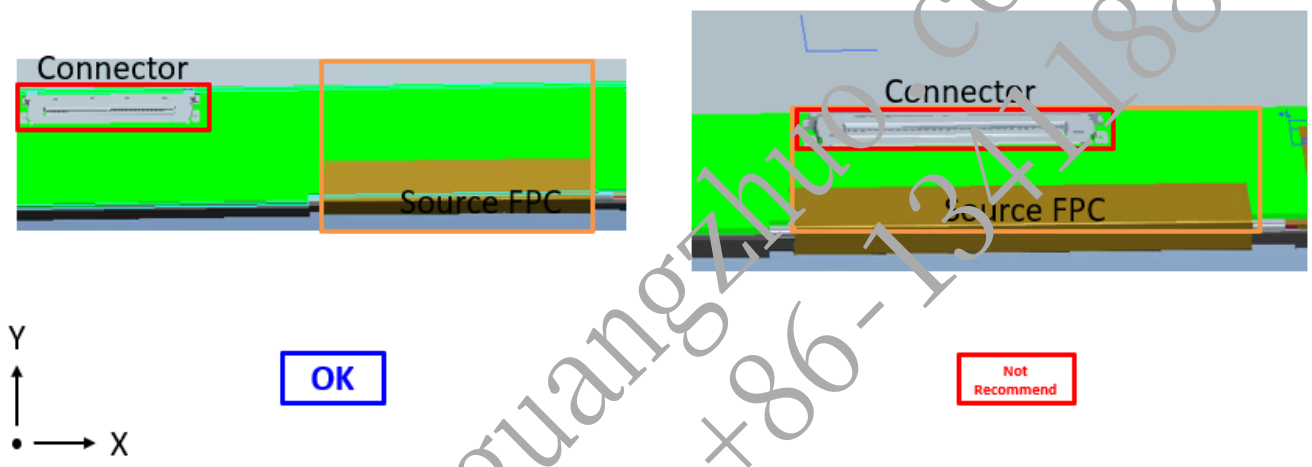
A-cover add sponges on Boss side wall



Purpose	BOE would suggest to attach Sponges to the side-wall of the Boss column of A-cover to reduce the risk of panel broken in assembling process.

Appendix B

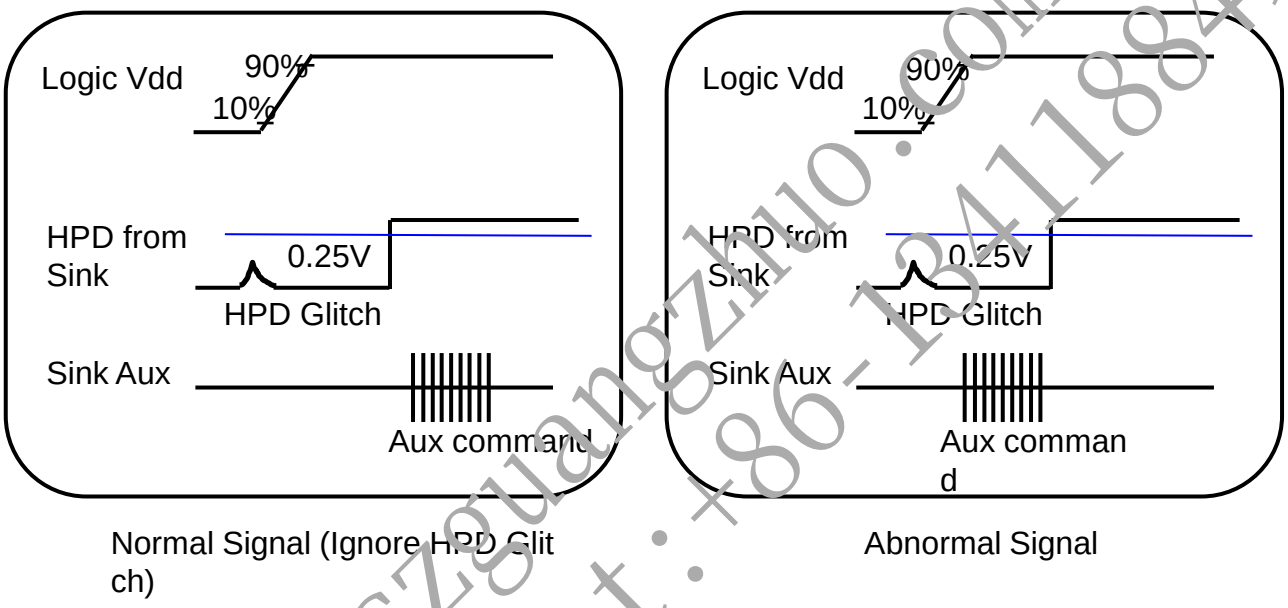
LCM to A-Cover / sponges z-gap



Purpose	Bent type product: The System Connector should not overlap with LCM FPC in X-direction, it may cause FPC lead broken during system connector plug and un-plug process (Panel FPC Bonding location is related to Mask and can not be changed easily)

Appendix C

HPD Signal recognition



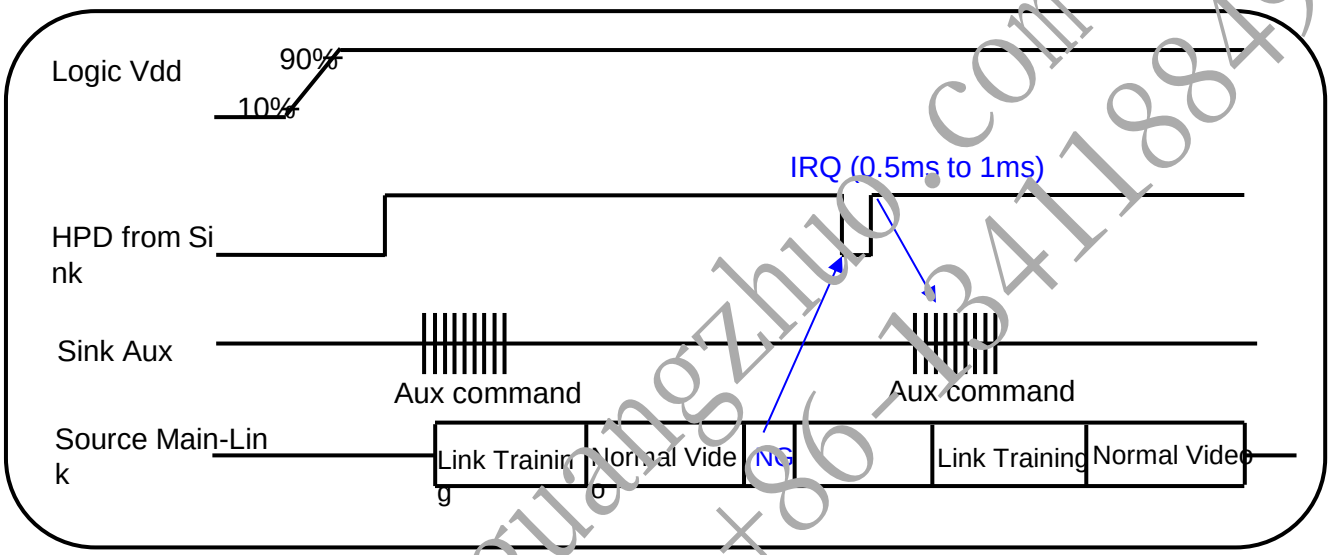
Normal Signal (Ignore HPD Glitch)

Abnormal Signal

Purpose	When HPD glitch voltage less than 2.0(V), system signal can't output AUX command data.

Appendix C

HPD Signal Definition IRQ (Interrupt Request)



Purpose	When HPD signal low than 0.5ms to 1ms, the source device should check sink status field from the DPCD and take link training again.

Appendix C

Main link eye diagram of TP3

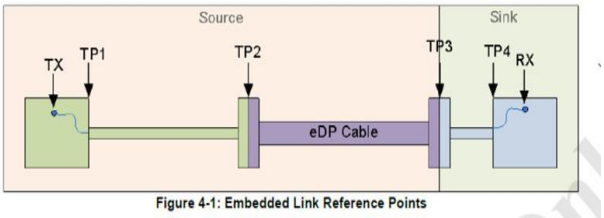
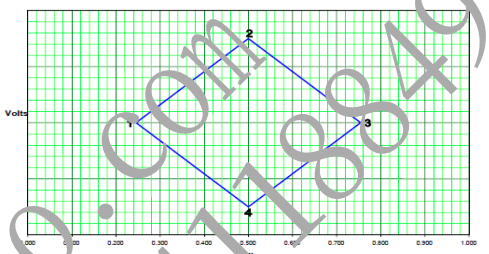


Figure 4-1: Embedded Link Reference Points

Measured TP3 on LCM connector.



Downstream Device Mask at TP3

	UI	Voltage
1	0.246	0
2	0.5	0.075
3	0.755	0
4	0.5	-0.075

Eye for TP3 at HBR

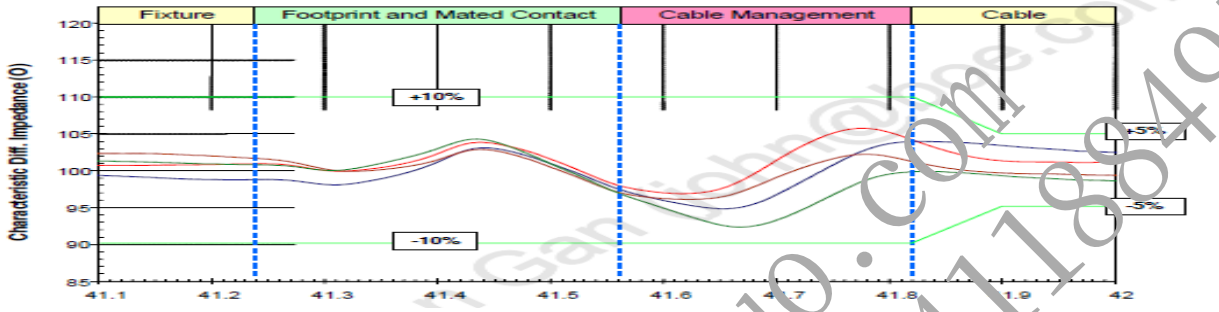
	UI	Voltage
1	0.375	0
2	0.5	0.023
3	0.625	0
4	0.5	-0.023

Eye for TP3 at RBR

Purpose	1. Main Link EYE Diagram should meet TP3 point of VESA. 2. The measure method is through access fixture.

Appendix C

Impedance Profile through a DP Connector



Differential Impedance Profile Measurement Data Example

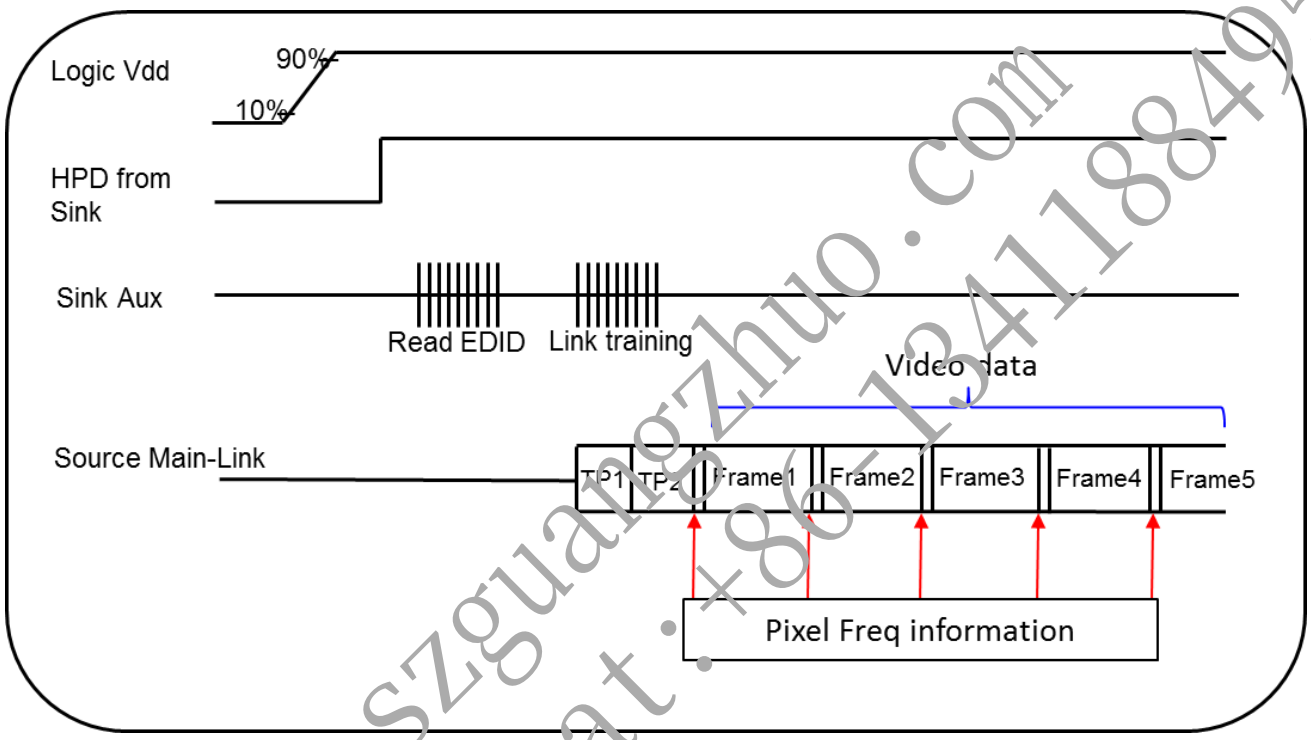
Segment	Differential Impedance Value	Maximum Tolerance
Fixture	100Ω/VESA	±10%
Connector	100Ω/VESA	±10%
Wire management	100Ω/VESA	±10%
Cable	100Ω/VESA	±5%

Impedance Profile Values for Cable Assembly

Purpose	Cable Impedance Profile 100ohm for Cable Assembly

Appendix C

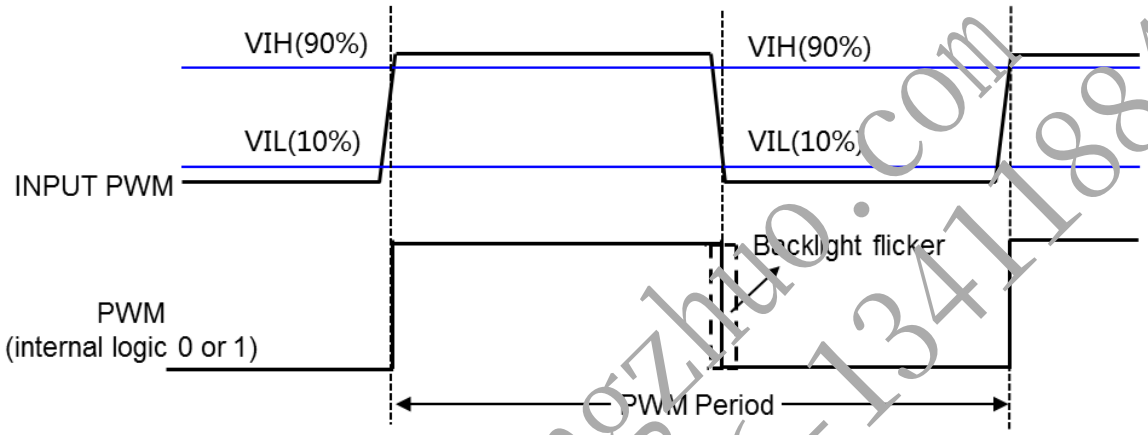
Main Link Pixel Freq information value of MSA data



Purpose	1. It need to fix pixel freq information value of MSA data output to prevent the initial abnormal pixel freq information value from incoming after power on. 2. BOE can read DPCD to check this value. Ex: BIOS is 1.62G , but into windows is 2.7G.

Appendix C

System Input PWM Rising/Faling time



Example:

Freq	Cycle Time	PWM Rising Time	PWM Falling Time
200Hz	5ms	≤1us	≤1us
1KHz	1ms	≤200ns	≤200ns

Purpose	1. LED driver need to calculate the duty cycle of input PWM signal. 2. To avoid backlight flicker visible on LCD, system input PWM suggest : PWM rising≤ 200ppm*cycle time ; PWM falling ≤ 200ppm*cycle time.