Doc. Number:

☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

MODEL NO.: N160JME
SUFFIX: GL2 Rev.C1

Customer: Asus

APPROVED BY **SIGNATURE**

Name / Title
Note：

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
許君逑	許君逑	林宛蒨

CONTENTS

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REVISION HISTORY

Version	Date	Page	Description
3.0	Mar. 16, 2023	All	Arrpoval spec. Ver.3.0 was first issued.
3.1	Jun. 15, 2023	4	Blacklight Unit Special Function: Static DRRS (Not Support) Special Function: PSR Version(PSR2)(support)
3.1	Jun. 15, 2023	17	DISPLAY TIMING SPECIFICATIONS
3.1	Jun. 15, 2023	27	CARTON
3.1	Jun. 15, 2023	39~46	Appendix. SYSTEM COVER DESIGN GUIDANCE

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N160JME-GL2 is a 16.0” (16.0” diagonal) TFT Liquid Crystal Display module with LED Backlight unit and 40 pins eDP interface. This module supports 1920 x 1200 WUXGA mode and can display 16,777,216 colors.

1.2 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Screen Size	16.0” diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1200	pixel	-
Pixel Pitch	0.17952 (H) x 0.17952 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7 M	color	-
Color depth	6bit +2 Hi-FRC		
Interface	eDP 1.4		(2)
eDP Main link rate	HBR(2.7G)		
Transmissive Mode	Normally Black	-	-
Surface Treatment	Hard coating (3H), Anti-Glare	-	-
Color Gamut	100%	sRGB	typ
Luminance, White	300	Cd/m2	
Response Time	Typ:T_R 1 / T_F 9	ms	
Contrast Ratio	Typ:1000/Min:800		
Border size(L/R/U)	2.5/2.5/2.5	mm	
View Angle(U/D/R/L)	89/89/89/89	Deg	
Blacklight Unit	LEDs 12 strings x 3 parallel		
RoHs Compliance	Yes		
Power Consumption	Total 5.97 W (Max.)@cell 1.64 W (Max.), BL 4.33 W (Max.)		(1)
Special Function	G-sync DD (Not support) G-sync nVSR (Not support) Free-sync (support) Static DRRS (Not Support) Seamless DRRS(sDRRS)(Not Support) PSR Version(PSR2)(support) PSR 1+ sDRRS(Not support) PSR 2+ LRR(support) CABC(Not support) FreeSync PSR-SU RC(Support)		

Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, fv = 60 Hz, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 ºC, whereas mosaic pattern is displayed.

Note (2) Display port interface signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.4 (eDP1.4). There are many optional items described in eDP1.4. If some optional item is requested, please contact us.

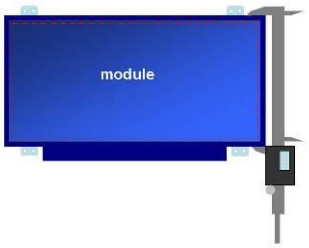
2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	349.38	349.68	349.98	mm	(1)(2)(3)
	Vertical (V) (w/o PCB)	224.12	224.42	224.72	mm	
	Vertical (V) (with PCB)	231.92	232.42	232.92	mm	
	Thickness (T)	2.70	2.85	3.00	mm	
	Thickness (T) with PCB	-	-	3.00	mm	
Active Area	Horizontal	344.58	344.68	344.78	mm	
	Vertical	215.32	215.42	215.52	mm	
Weight		-	-	400	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Dimensions are measured by caliper.

Note (3) Panel thickness is measured with calipers clamping mylar or tape tightly.



2.1 CONNECTOR TYPE

Please refer Appendix Outline Drawing for detail design.

Connector Part No.: 1st STM MSAK24025P40MB

or follow customer approval connector vender list

User's connector Part No: 20453-040T-03

Customer approval connector vender list

Item	Discription				
	Item	Pin 數	Pitch	廠商	廠商料號
LCD Panel Connector Pool	1	40	0.5	I-PEX	**20455-040E-02/12**
					20455-040E-76/66
					20765-040E-11
				Starconn	111A40-0000RA-G3
				STM	**MSAK24025P40**
				Tyco	5-2069716-3
				LSMtrom	GT05Q-40S-10H
				Foxconn	GS13401-1S10S-7H
				JAE	HD1S040HA1
					HD1S040HA2
					HD1S040HA3
				UJU	ISC60-L40B-C10
				MOLEX	MOLEX-104062-4011
	2	30	0.5	I-PEX	**20455-030E-02/12**
					20455-030E-76/66
					20765-030E-11
				Starconn	300E30-0010RA-G3
				JAE	HD2S030HA1
					HD2S030HA2
					HD2S030HA3
				LSMtrom	GT05Q-30S-[illegible]
				STM	**MSAK24025P3[illegible]**
				UJU	ISC60-L30B-C10
	3	40	0.4	I-PEX	20682-040[illegible]-02

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3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

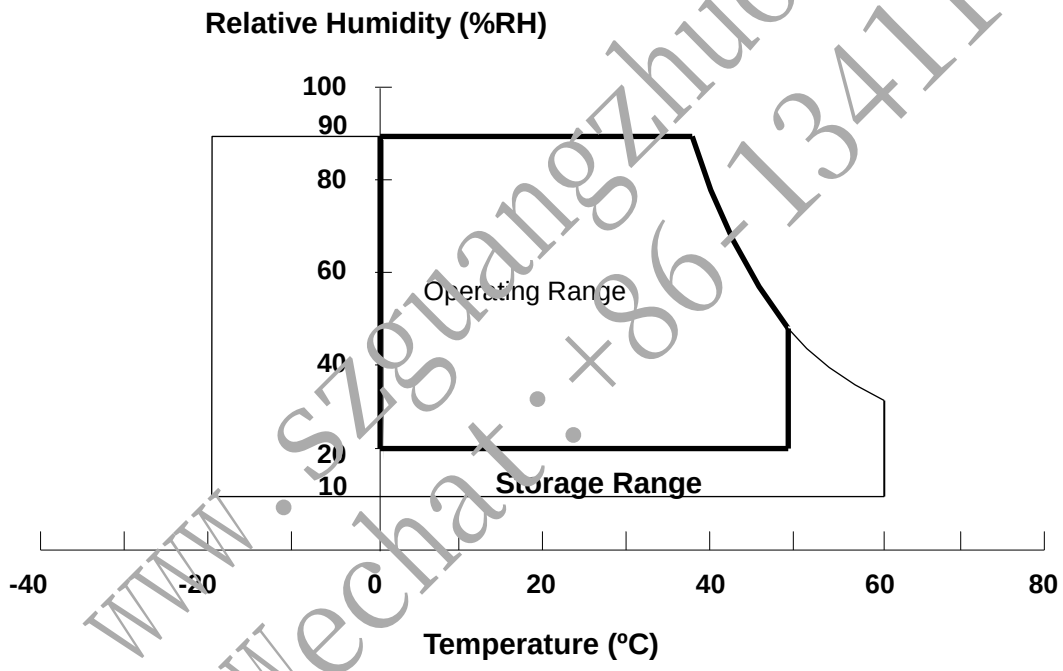
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	--	220/2	G/ms	(3),(4),(5)
Vibration (Non-Operating)	V_{NOP}	--	1.5	G	(3),(4),(6)

Note (1) (a) 90 %RH Max. (Ta < 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max.

(c) No condensation.

Note (2) The temperature of panel surface should be 0 ºC min. and 60 ºC max.



Note (3) criteria: Normal display image with no obvious non-uniformity and no line defect.

Note (4) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

Note (5) half sine wave,1 time for each direction of ±X,±Y,±Z

Note (6) 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z

3.2 ELECTRICAL ABSOLUTE RATINGS

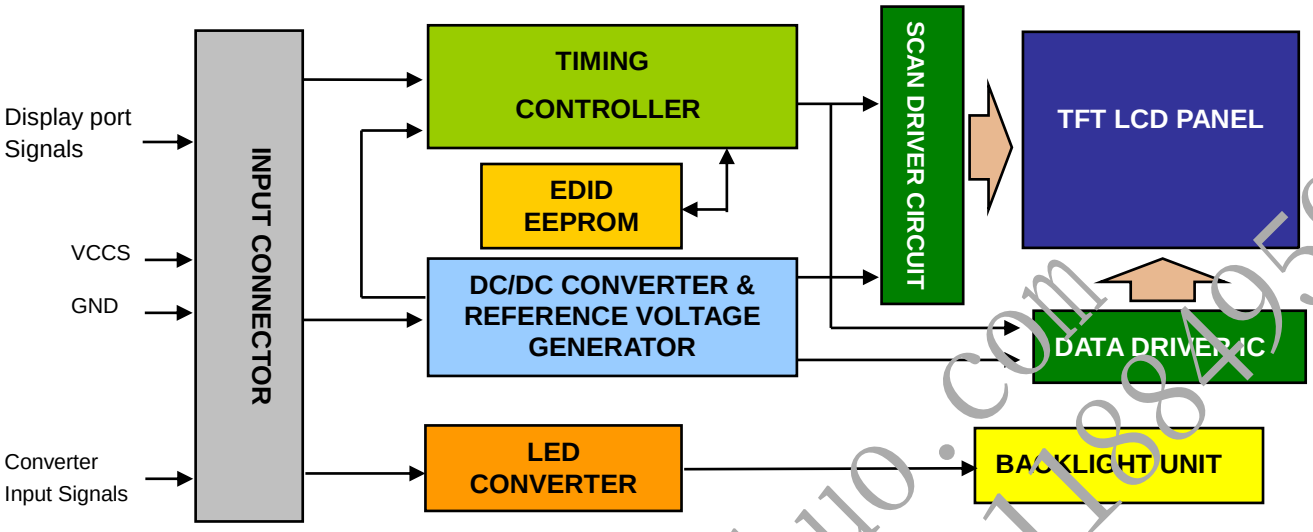
3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	+4.0	V	
Converter Input Voltage	LED_VCCS	-0.3	26	V	(1)
Converter Control Signal Voltage	LED_PWM,	-0.3	3.6	V	1)
Converter Control Signal Voltage	LED_EN	-0.3	3.6	V	(1)

Note (1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “ELECTRICAL CHARACTERISTICS”.

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



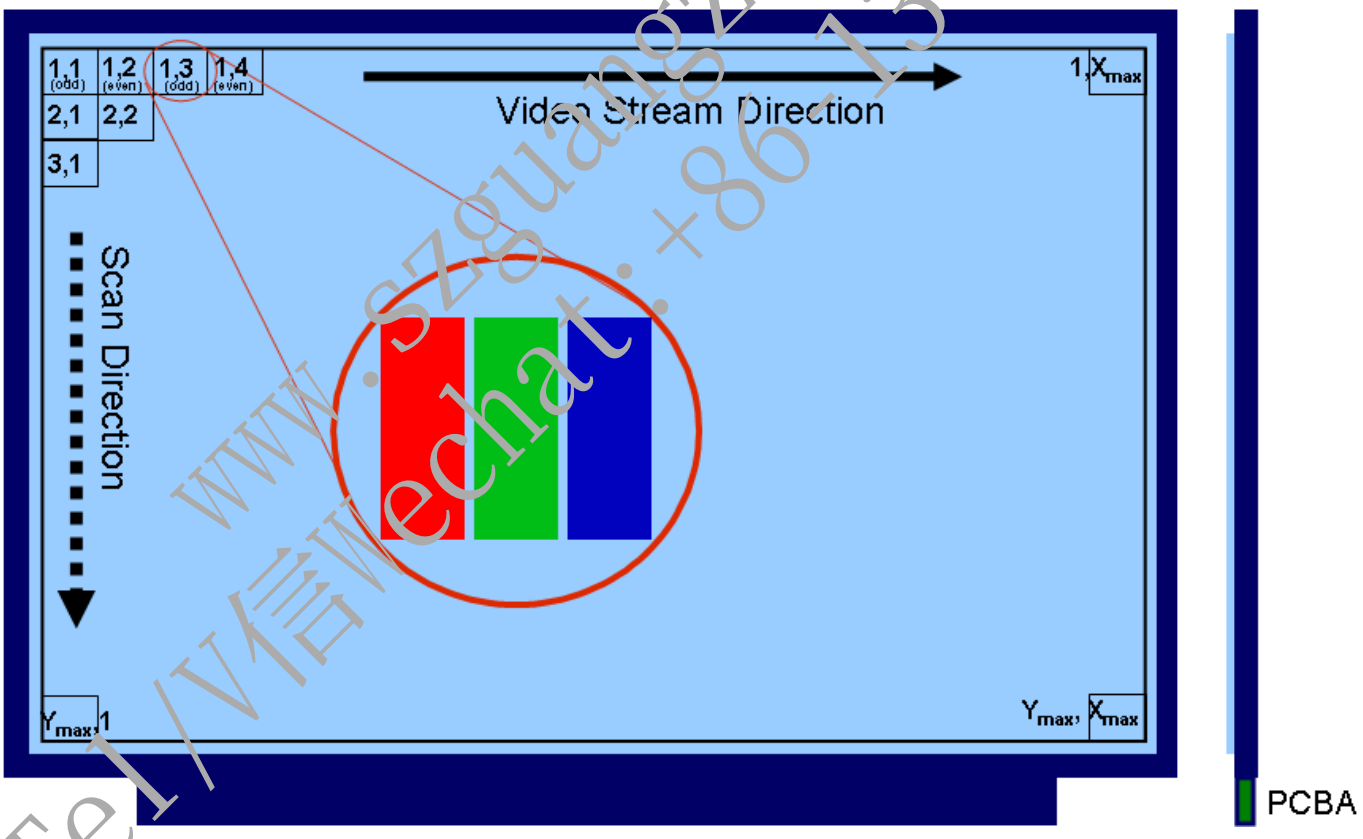
4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserved for LCD test)	
2	H_GND	High Speed Ground	
3	Lane3_N	Complement Signal Link Lane 3	
4	Lane3_P	True Signal Link Lane 3	
5	H_GND	High Speed Ground	
6	Lane2_N	Complement Signal Link Lane 2	
7	Lane2_P	True Signal Link Lane 2	
8	H_GND	High Speed Ground	
9	Lane1_N	Complement Signal Link Lane 1	
10	Lane1_P	True Signal Link Lane 1	
11	H_GND	High Speed Ground	
12	Lane0_N	Complement Signal Link Lane 0	
13	Lane0_P	True Signal Link Lane 0	
14	H_GND	High Speed Ground	
15	AUX_CH_P	True Signal Auxiliary Channel	
16	AUX_CH_N	Complement Signal Auxiliary Channel	
17	H_GND	High Speed Ground	
18	VCCS	LCD logic and driver power	
19	VCCS	LCD logic and driver power	
20	VCCS	LCD logic and driver power	
21	VCCS	LCD logic and driver power	
22	NC	No Connection (Reserved for LCD test)	
23	GND	Ground	
24	GND	Ground	
25	GND	Ground	
26	GND	Ground	

27	HPD	Hot Plug Detect	
28	BL_GND	Backlight ground	
29	BL_GND	Backlight ground	
30	BL_GND	Backlight ground	
31	BL_GND	Backlight ground	
32	LED_EN	BL_Enable Signal of LED Converter	
33	LED_PWM	PWM Dimming Control Signal of LED Converter	
34	NC	No Connection (Reserved for LCD test)	
35	NC	No Connection (Reserved for LCD test)	
36	LED_VCCS	Backlight power	
37	LED_VCCS	Backlight power	
38	LED_VCCS	Backlight power	
39	LED_VCCS	Backlight power	
40	NC	No Connection (Reserved for LCD test)	

Note (1) The first pixel is odd as shown in the following figure.



4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)
Ripple Voltage		V_{RP}	-	-	100	mV	(1),(6)
Inrush Current		I_{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Black	Icc		430	470	mA	(3)
	Mosaic			450	495	mA	(3)
	Solid Pattern			770	850	mA	(3)
	Mosaic @PSR			450	495	mA	(3)a
	Solid Pattern @ PSR			770	850	mA	(3)a
HPD Impedance		R_{HPD}	30K			ohm	(4)
HPD	High Level		2.3	2.7	3.6	V	(5)
	Low Level		0		0.6	V	(5)

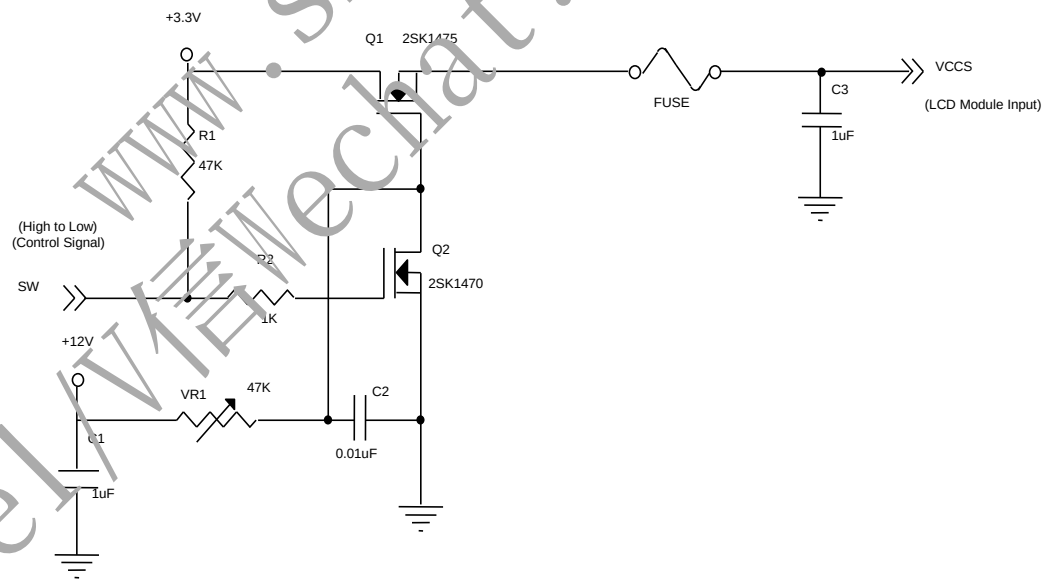
Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

Note (2) I_{RUSH}: the maximum current when VCCS is rising

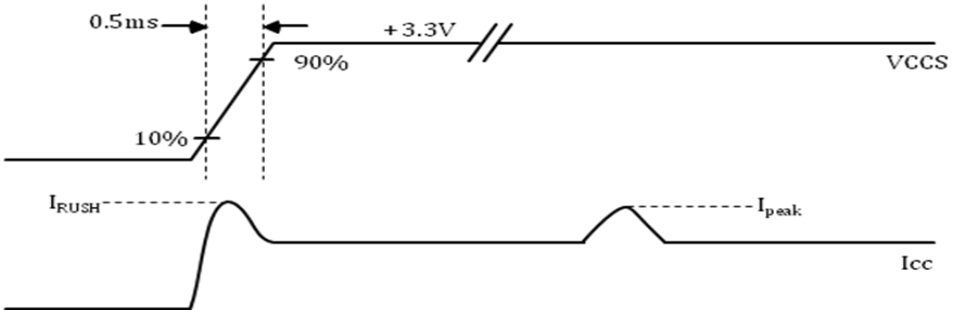
Measurement Conditions: Shown as the following figure. VCCS=Min, Test pattern: black.

I_{pek}: the maximum current after power-on

Measurement Conditions: Shown as the following figure. VCCS=Min, Test pattern: H-strip one line.

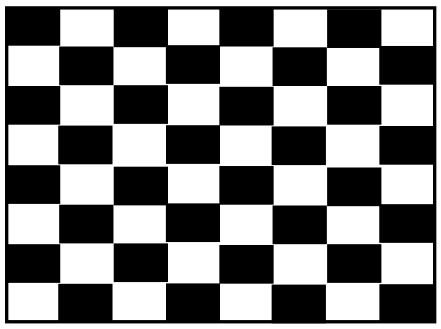


VCCS rising time is 0.5ms



Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ºC, DC Current and f_v = 60 Hz, whereas a specified power dissipation check pattern is displayed.

1. Mosaic Pattern



Active Area

2. The solid pattern is the largest one of R/G/B pattern.

Note(3) a. The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ºC, DC Current and PSR mode enable, whereas a power dissipation check pattern is displayed.

Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. Please refer to Note (4) of 4.3.2 LED CONVERTER SPECIFICATION to obtain more information.

Note (5) When a source detects a low-going HPD pulse, it must be regarded as a HPD event. Thus, the source must read the link / sink status field or receiver capability field of the DPCD and take corrective action.

Note (6) The VCCS voltage drop will occur at the frame start. We only consider the ripple voltage during active area instead of the blanking area. Meanwhile,the min VCCS need to meet “Power Supply Voltage” criteria.

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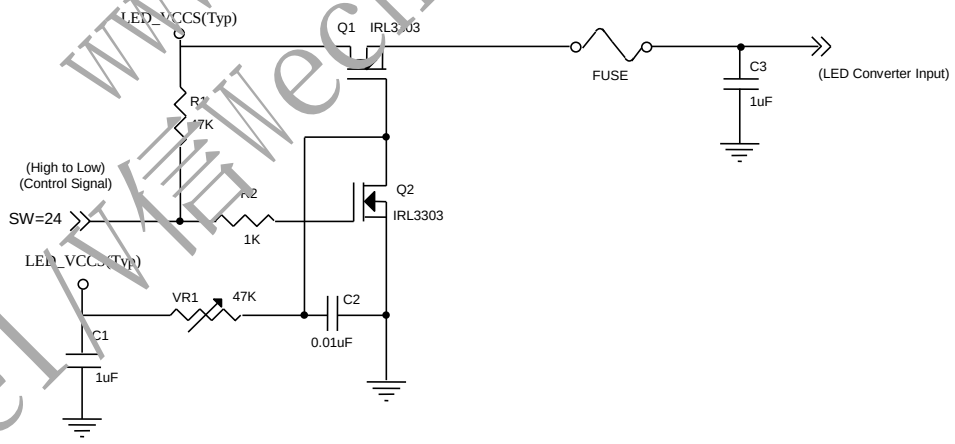
4.3.2 LED CONVERTER SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input power supply voltage		LED_Vccs	8.0	12.0	21.0	V	
Converter Inrush Current		$ILED_{RUSH}$	-	1.28	1.54	A	(1)
LED_EN Control Level	Backlight On		2.2	-	5.0	V	(4)
	Backlight Off		0	-	0.6	V	(4)
LED_EN Impedance		R_{LED_EN}	30K			ohm	(4)
PWM Control Level	PWM High Level		2.2	-	5.0	V	(4)
	PWM Low Level		0	-	0.6	V	(4)
PWM Impedance		R_{PWM}	30K			ohm	(4)
PWM Control Duty Ratio			5	-	100	%	(5)
PWM Control Permissive Ripple Voltage		V_{PWM_pp}		-	100	mV	
PWM Control Frequency		f_{PWM}	190	-	10K	Hz	(2)
LED Power Current	LED_VCCS =Typ.	ILED		341	361	mA	(3)

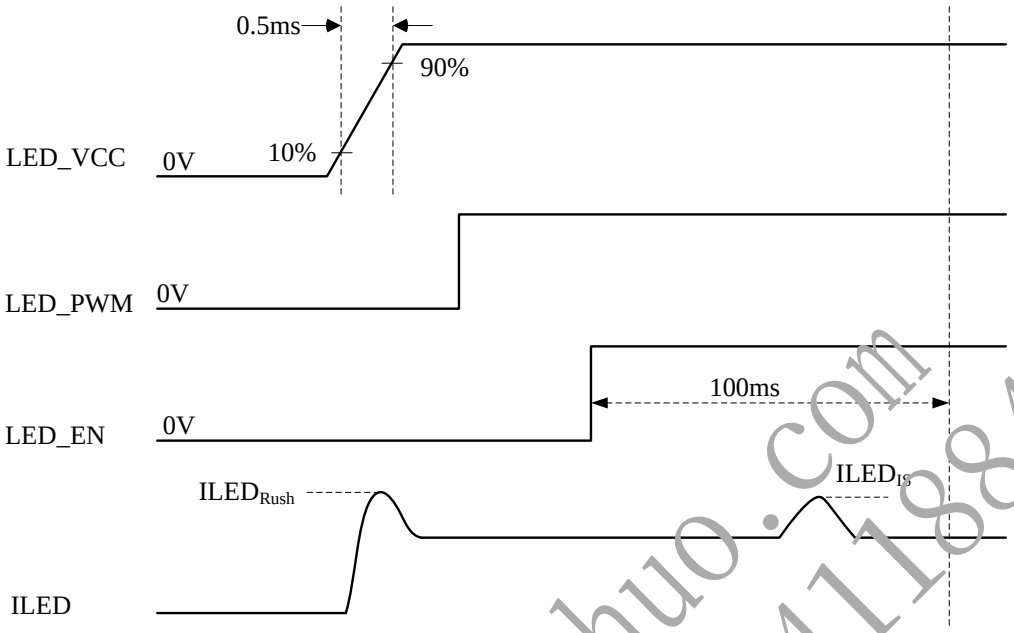
Note (1) $ILED_{RUSH}$: the maximum current when LED_VCCS is rising,

$ILED_{IS}$: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Min, Ta = 25 ± 2 ºC, Duty=100%,White pattern.



VLED rising time is 0.5ms



Note (2) If PWM control frequency is applied in the range less than 1KHz, the "waterfall" phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

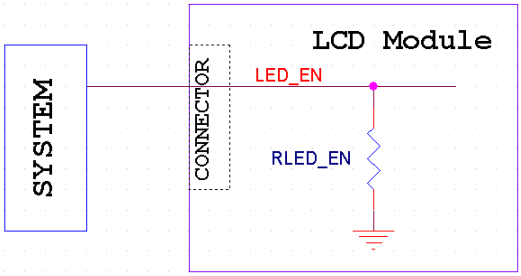
$$(N + 0.33) * f \leq f_{PWM} \leq (N + 0.66) * f$$

N : Integer $(N \geq 3)$

f : Frame rate

Note (3) The specified LED power supply current is under the conditions at "LED_VCCS = Typ.", Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.

Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. For example, the figure below describes the equivalent pull down impedance of LED_EN (if it exists). The rest pull down impedances of other signals (eg. HPD, PWM …) are in the same concept.



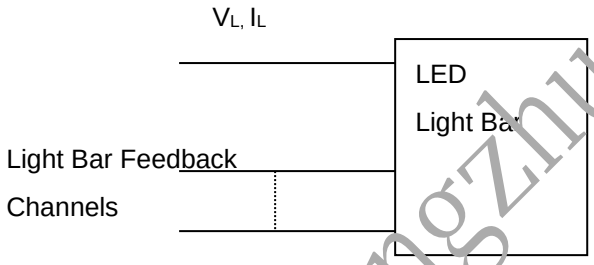
Note (5) If the cycle-to-cycle difference of PWM duty exceeds 0.1%, especially when the PWM duty is low, slight brightness change might be observed.

4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	32.4	34.2	36	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L		105		mA	
Power Consumption	P_L		3.591	3.78	W	(3)
LED Life Time	L_{BL}	15000			Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) PL = IL ×VL (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 oC and IL = 17.5mA (Per EA) until the brightness becomes ≦ 50% of its original value.

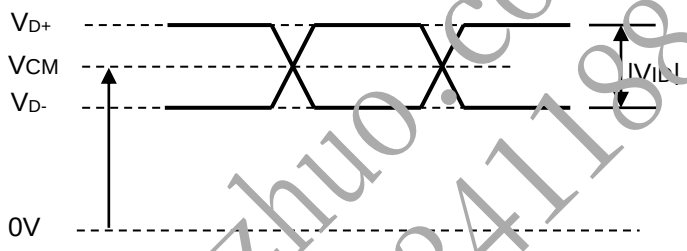
4.4 DISPLAY PORT INPUT SIGNAL TIMING SPECIFICATIONS

4.4.1 DISPLAY PORT INTERFACE

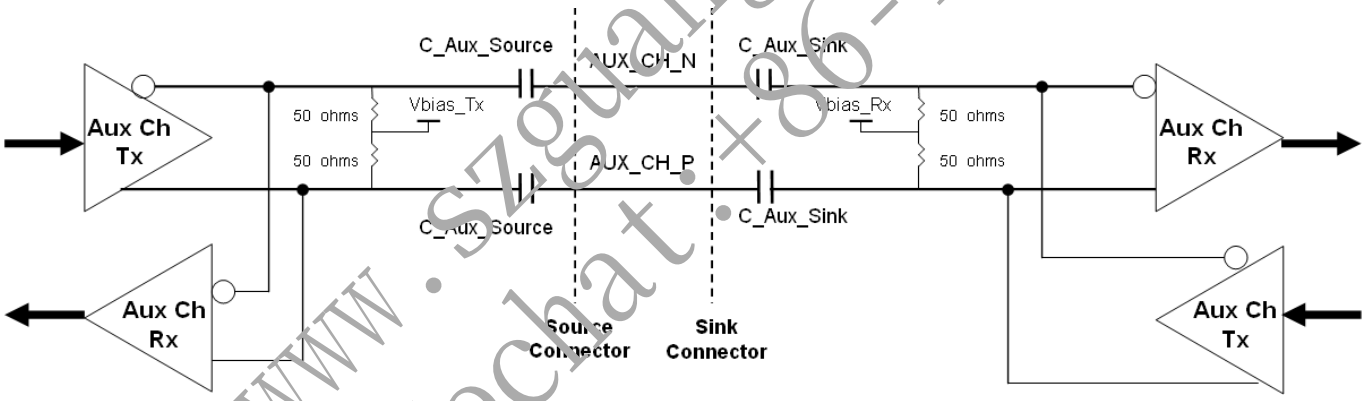
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Signal Common Mode Voltage(MainLink and AUX)	VCM	0		2	V	(1) (4)
AUX AC Coupling Capacitor	C_Aux_Source	75		200	nF	(2)
Main Link AC Coupling Capacitor	C_ML_Source	75		200	nF	(3)

Note (1)Display port interface related AC coupled signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2. There are many optional items described in eDP1.2. If some optional item is requested, please contact us.

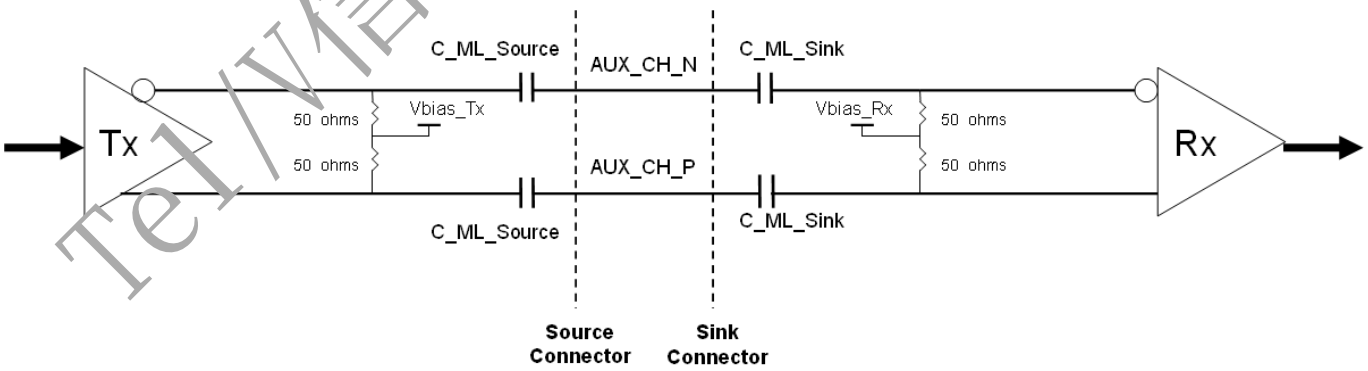
Single Ended



(2) Recommended eDP AUX Channel topology is as below and the AUX AC Coupling Capacitor (C_Aux_Source) should be placed on the source device.



(3) Recommended Main Link Channel topology is as below and the Main Link AC Coupling Capacitor (C_ML_Source) should be placed on the source device.



(4) The source device should pass the test criteria described in DisplayPortCompliance Test Specification (CTS) 1.1

4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

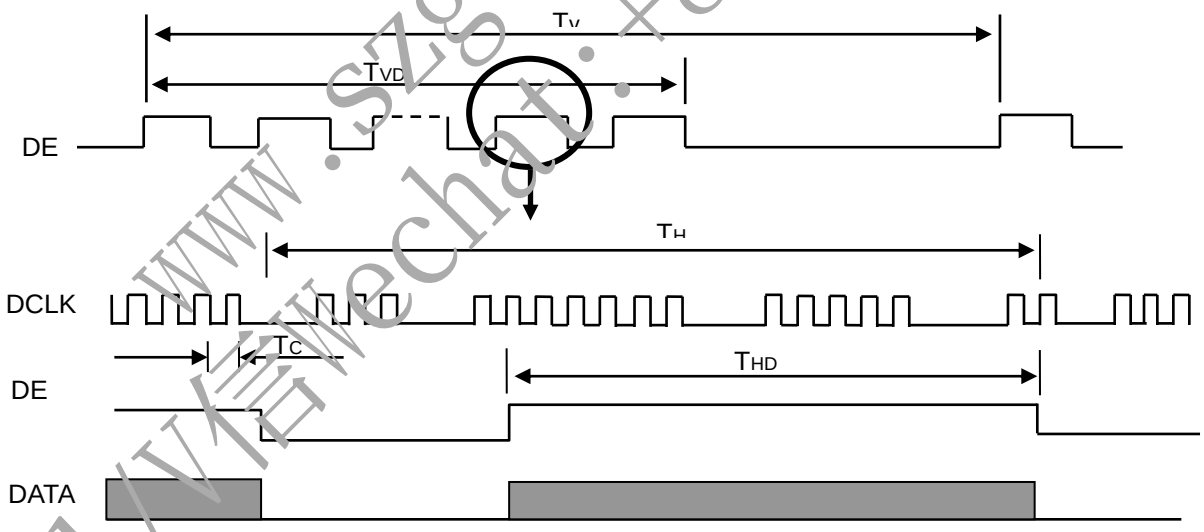
Refresh rate 120Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	313.94	318.00	322.05	MHz	-
DE	Vertical Total Time	TV	1270	1274	1278	TH	-
	Vertical Active Display Period	TVD	1200	1200	1200	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	74	TV-TVD	TH	-
	Horizontal Total Time	TH	2060	2080	2100	Tc	-
	Horizontal Active Display Period	THD	1920	1920	1920	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	160	TH-THD	Tc	-

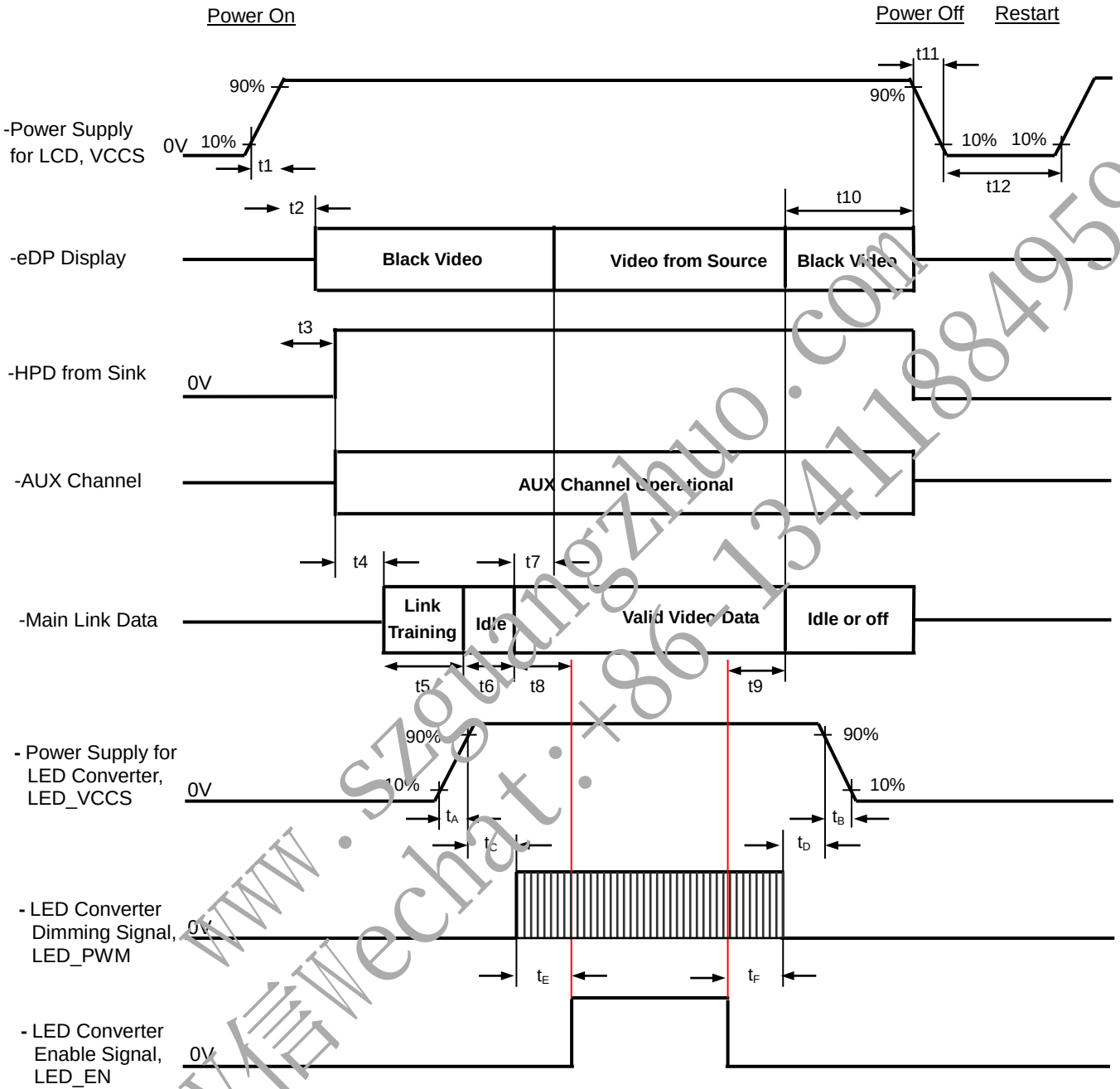
Refresh rate 60Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	314.44	318.00	321.55	MHz	-
DE	Vertical Total Time	TV	2544	2548	2552	TH	-
	Vertical Active Display Period	TVD	1200	1200	1200	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	1348	TV-TVD	TH	-
	Horizontal Total Time	TH	2060	2080	2100	Tc	-
	Horizontal Active Display Period	THD	1920	1920	1920	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	160	TH-THD	Tc	-

INPUT SIGNAL TIMING DIAGRAM



4.6 POWER ON/OFF SEQUENCE



Timing Specifications:

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	Power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t2	Delay from LCD,VCCS to black video generation	Sink	0	80	ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source (see Notes:2 and 3 below)
t3	Delay from LCD,VCCS to HPD high	Sink	0	80	ms	Sink AUX Channel must be operational upon HPD high (see Note:4 below)
t4	Delay from HPD high to link training initialization	Source	0	-	ms	Allows for Source to read Link capability and initialize
t5	Link training duration	Source	0	-	ms	Dependant on Source link training protocol
t6	Link idle	Source	0	-	ms	Min Accounts for required BS Idle pattern. Max allows for Source frame synchronization
t7	Delay from valid video data from Source to video on display	Sink	0	50	ms	Max value allows for Sink to validate video data and timing. At the end of T7, Sink will indicate that it detected valid video data by setting the RECEIVE_PORT_0_STATUS bit in the SINK_STATUS register (DPCD Address 00205h and 0200Fh, bit 0; see DP v1.3) to logic 1, and Sink will no longer generate automatic Black Video
t8	Delay from valid video data from Source to backlight on	Source	80	-	ms	Source must assure display video is stable*: Recommended by INX. To avoid garbage image.
t9	Delay from backlight off to end of valid video data	Source	0	-	ms	Source must assure backlight is no longer illuminated. At the end of T9, Sink will indicate that it did not detect valid video data by setting the RECEIVE_PORT_0_STATUS bit in the SINK_STATUS register (DPCD Address 00205h and 0200Fh, bit 0; see DP v1.3) to logic 0, and Sink will automatic display Black Video (See Notes: 2&3)
t10	Delay from end of valid video data from Source to power off	Source	0	500	ms	Black video will be displayed after receiving idle or off signals from Source
t11	VCCS power rail fall time, 90% to 10%	Source	0.5	10	ms	-
t12	VCCS Power off time	Source	500	-	ms	-
t_A	LED power rail rise time, 10% to 90%	Source	0.5	10	ms	-

tB	LED power rail fall time, 90% to 10%	Source	0	10	ms	-
tC	Delay from LED power rising to LED dimming signal	Source	1	-	ms	-
tD	Delay from LED dimming signal to LED power falling	Source	1	-	ms	-
tE	Delay from LED dimming signal to LED enable signal	Source	0	-	ms	-
tF	Delay from LED enable signal to LED dimming signal	Source	0	-	ms	-

Note (1) Please don't plug or unplug the interface cable when system is turned on.

Note (2) The Sink must include the ability to automatically generate Black Video autonomously. The Sink must automatically enable Black Video under the following conditions:

- Upon LCDVCC power-on (within T2 max)
- When the "NoVideoStream_Flag" (VB-ID Bit 3) is received from the Source (at the end of T9)

Note (3) The Sink may implement the ability to disable the automatic Black Video function, as described in Note (2), above, for system development and debugging purposes.

Note (4) The Sink must support AUX Channel polling by the Source immediately following LCDVCC power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to response to an AUX Channel transaction with the time specified within T3 max.

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	105	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	800	1000	-	-	(2), (5),(7)
Response Time		T_R		-	11	14	ms	(3),(7)
		T_F		-	9	11	ms	
Average Luminance of White		L_{AVE}		255	300	-	cd/m²	(4), (6),(7)
Color Chromaticity	Red	Rx		Typ – 0.03	0.640	Typ + 0.03	-	(1),(7)
		Ry			0.330		-	
	Green	Gx			0.300		-	
		Gy			0.600		-	
	Blue	Bx			0.150		-	
		By			0.060		-	
	White	Wx			0.313		-	
		Wy			0.329		-	
sRGB		CG	θ_x=0°, θ_Y =0° Viewing Normal Angle	96	100	-	%	(5),(7),(8)
Cross talk		CT		-	-	2	%	(5),(7),(9)
Viewing Angle	Horizontal	θ_x+	CR≥10	80	89	-	Deg.	(1),(5), (7)
		θ_x-		80	89	-		
	Vertical	θ_Y+		80	89	-		
		θ_Y-		80	89	-		
White Variation of 5 Points		δW_{5p}	θ_x=0°, θ_Y =0°	-	-	1.25	-	(5),(6), (7)
White Variation of 13 Points		δW_{13p}	θ_x=0°, θ_Y =0°	-	-	1.5		(5),(6), (7)

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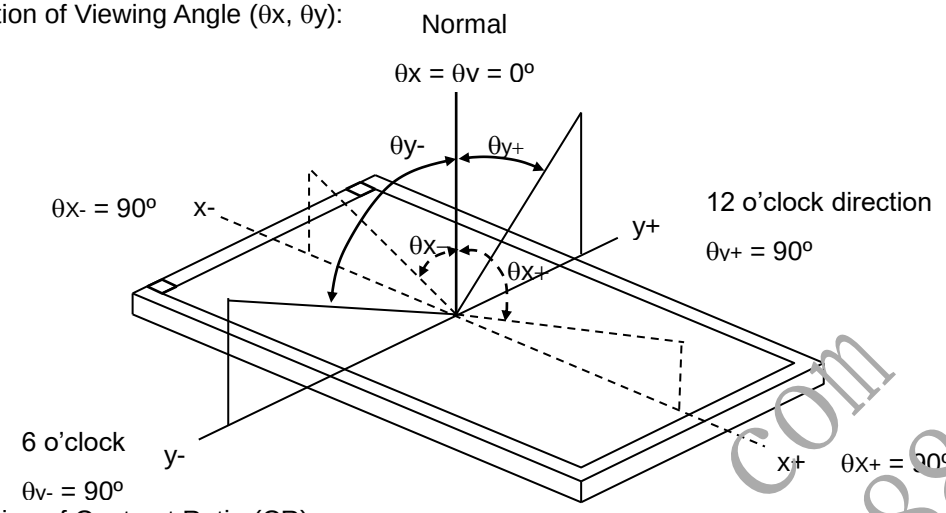
Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

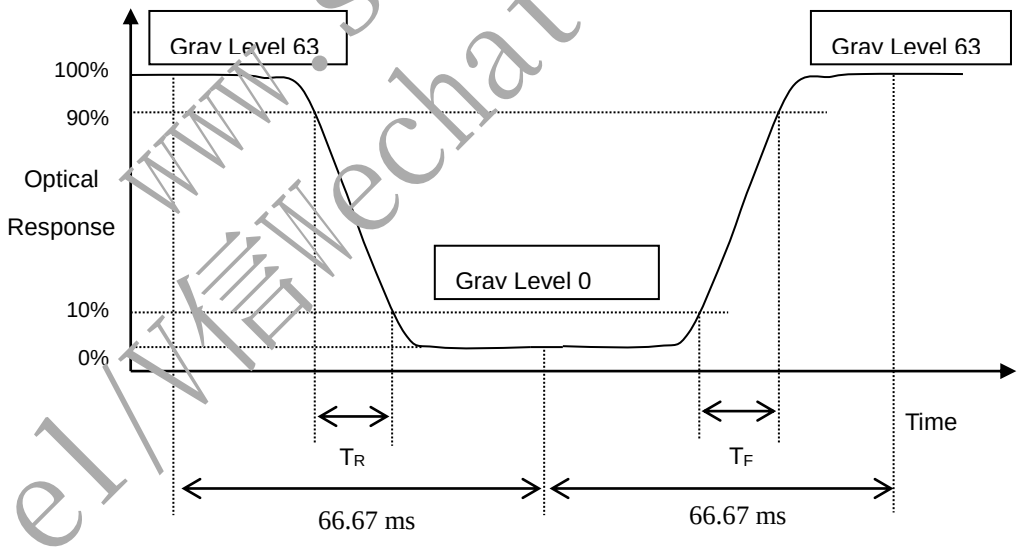
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

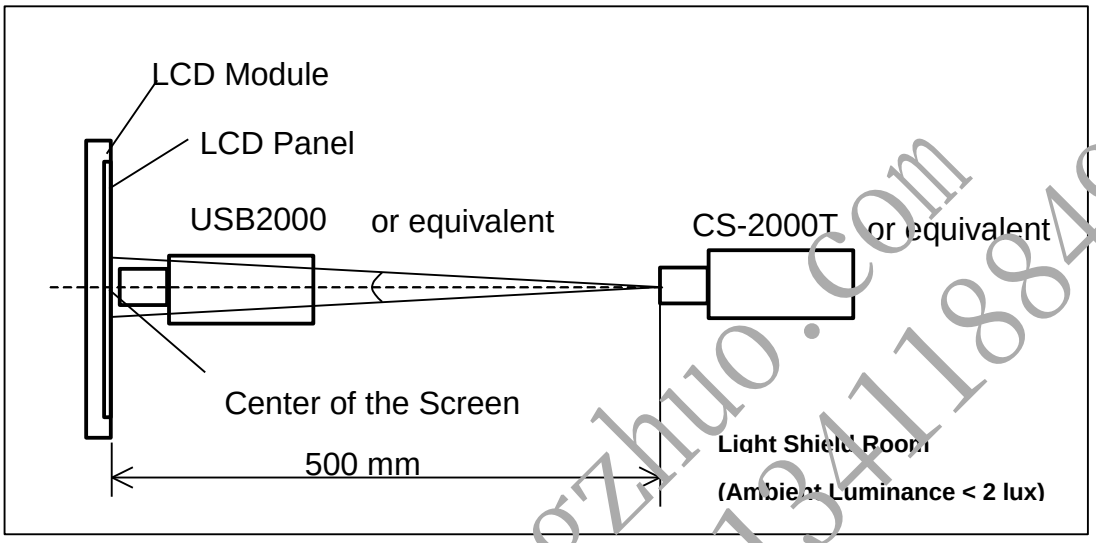
Measure the luminance of White at 5 points

L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

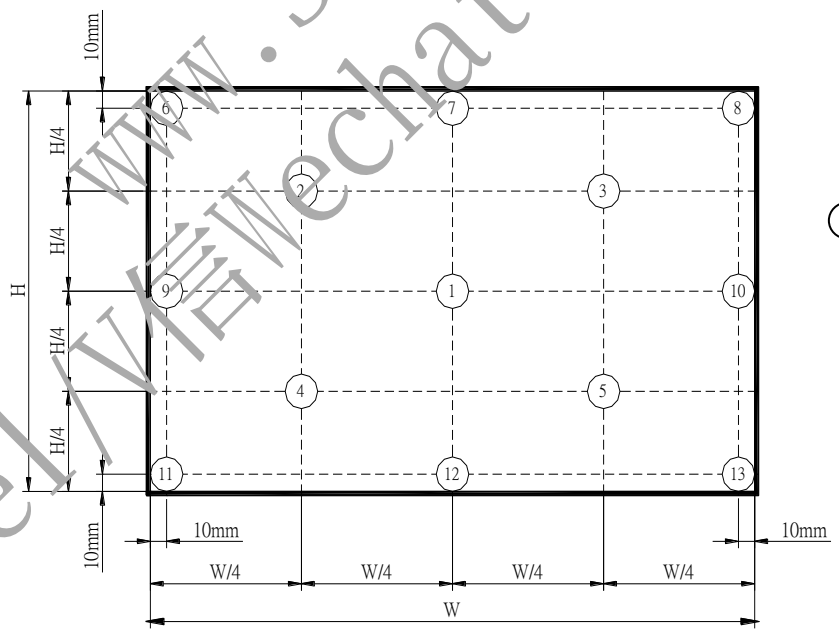


Note (6) Definition of White Variation (δW):

Measure the luminance of White at 5 points

δW_{5p} = {Maximum [L (1)~L (5)] / Minimum [L (1)~ L (5)]}*100%

δW_{13p} = {Maximum [L (1)~L (13)] / Minimum [L (1)~ L (13)]}*100%



Ⓧ : Test Point

X=1 to 13

Active area

Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

Note (8) Definition of color gamut (C.G%):

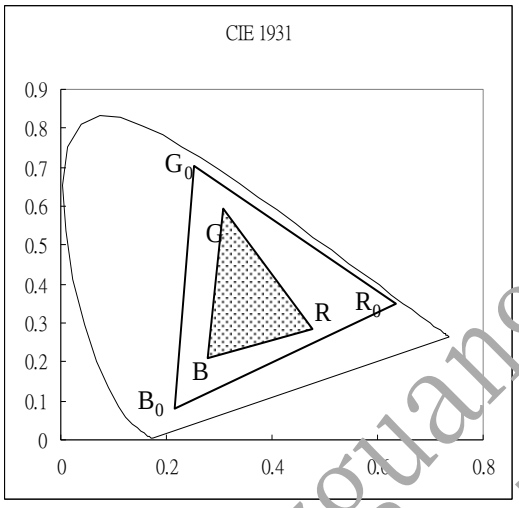
C.G%= Area (R, G, B) / Area (R_0, G_0, B_0,)* 100%

R_0, G_0, B_0: CIE1931 coordinates of red, green, and blue defined by sRGB.

R, G, B: CIE1931 coordinates of red, green, and blue in module at 63 gray level.

Area (R_0, G_0, B_0): Area of the triangle defined by coordinate R_0, G_0, B_0.

Area(R, G, B): Area of the triangle defined by coordinate R, G, B And just take the part that inside the Area(R_0, G_0, B_0), ignoring extension area.



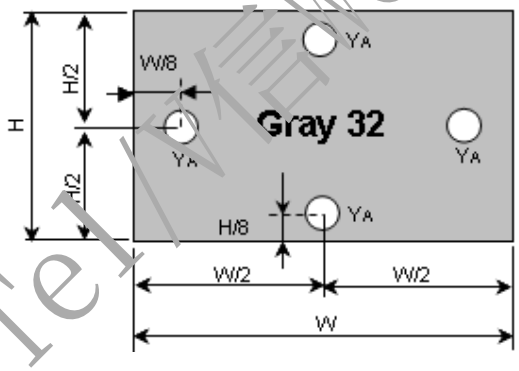
Note (9) Cross Talk (CT):

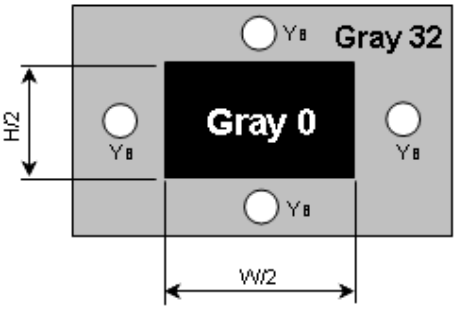
CT= | Y_B − Y_A | / Y_A ×100%

Where

Y_A=Luminance of measured location in left figure

Y_B=Luminance of measured location in right figure





6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60ºC, 240 hours	(1) (2)
Low Temperature Storage Test	-20ºC, 240 hours	
Thermal Shock Storage Test	-20ºC, 0.5hour←→60℃, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	50ºC, 240 hours	
Low Temperature Operation Test	0ºC, 240 hours	
High Temperature & High Humidity Operation Test	50°C, 80% RH, 240 hours	
High Temperature & High Humidity Storage Test	40°C, 90% RH, 240 hours	
ESD Test (Operation)	150pF, 330Ω, 1sec/cycle Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±15KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave,1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

7. PACKING

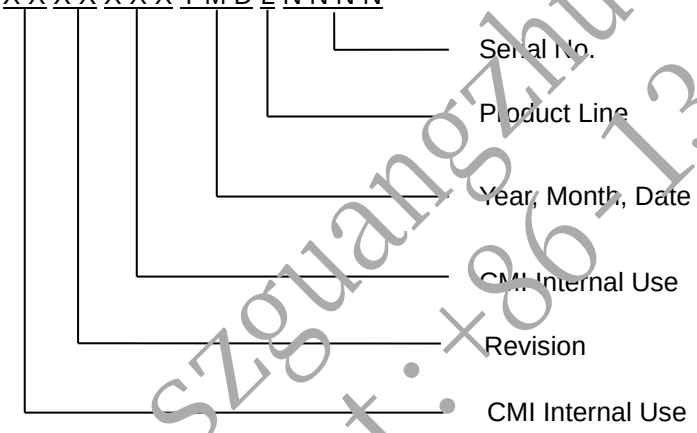
7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.
(The model name and revision shown at right side on the label is for customer recognition,
and the left side is for INX internal use.).

(a) Model Name: N160JME –GL2

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X X X X X X X Y M D L N N N N



(d) Production Location: MADE IN XXXX.

(e) UL/CB logo: XXXX is UL factory ID.

Serial ID includes the information as below:

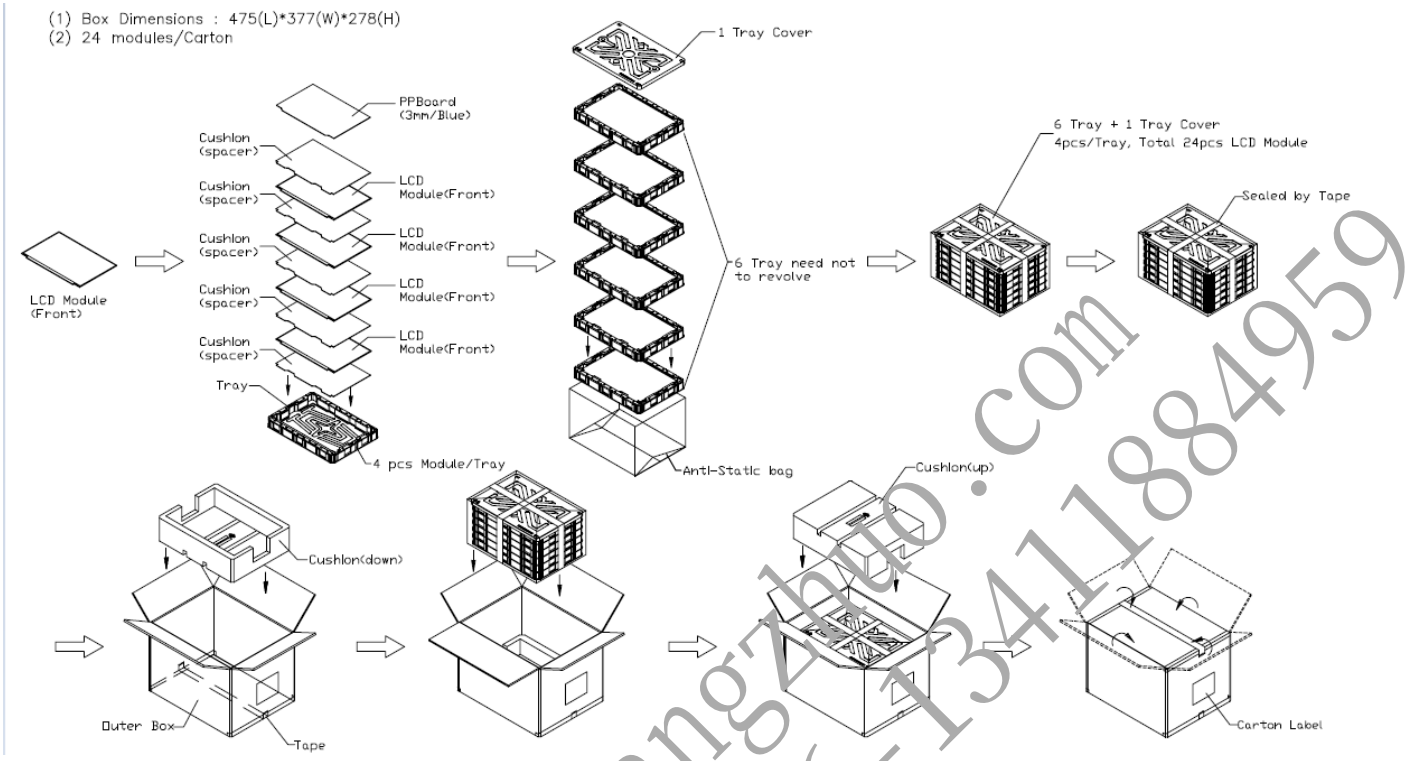
(a) Manufactured Date: Year: 0~9, for 2010~2019
Month: 1~9, A~C, for Jan. ~ Dec.
Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

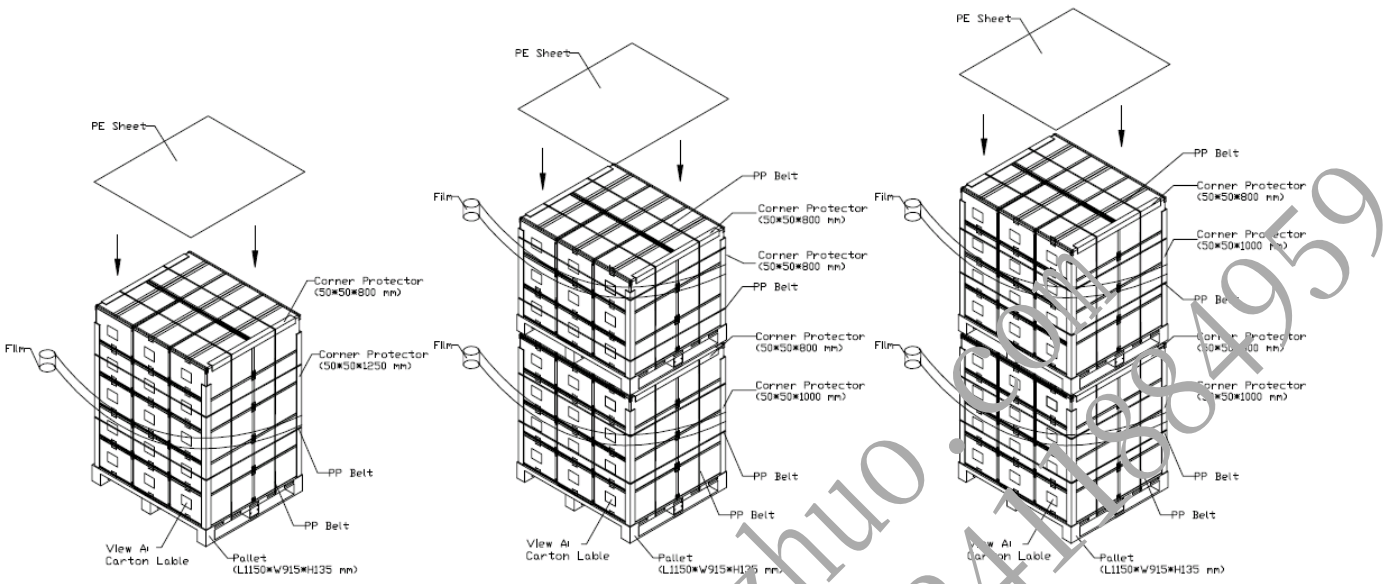
(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

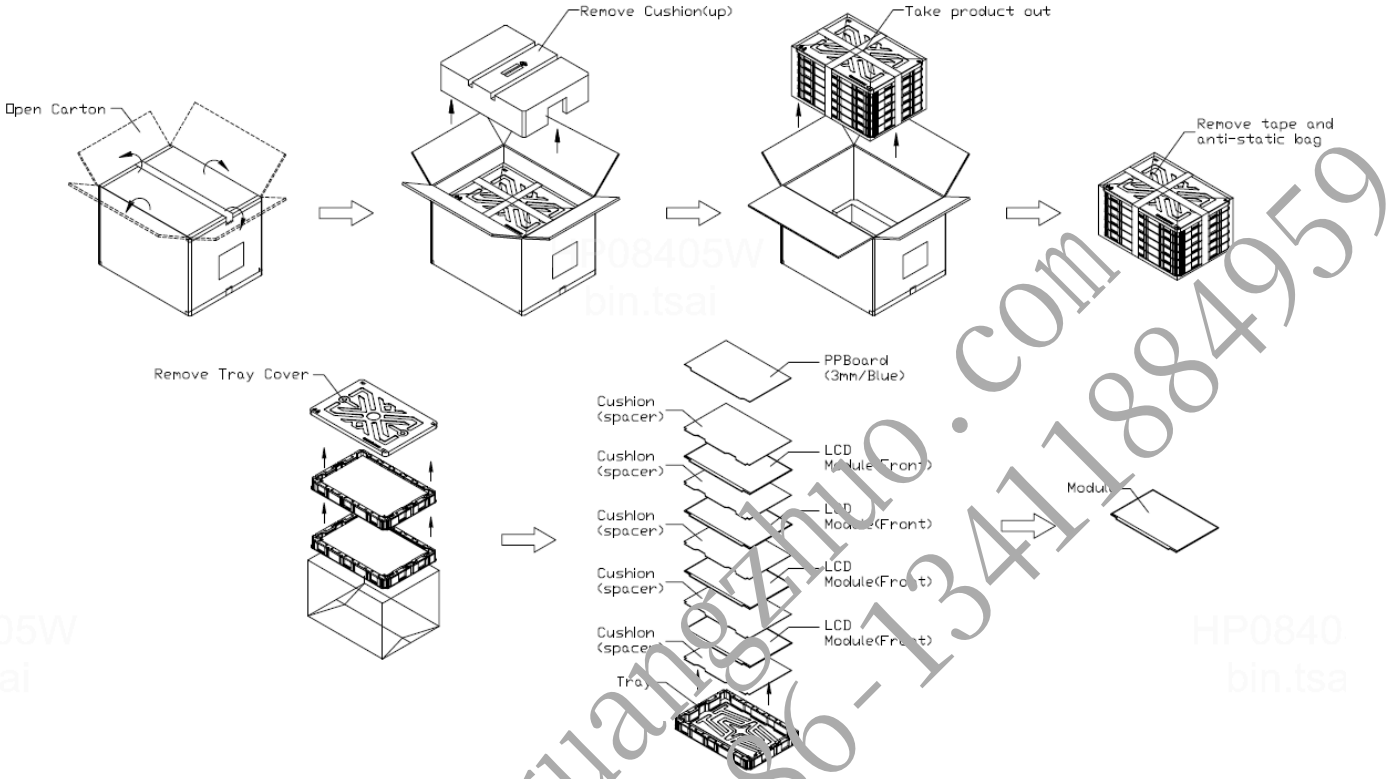
7.2 CARTON



7.3 PALLET



7.4 UN-PACKAGING METHOD



8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMIS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

Appendix. EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
1	00	Header	00	00000000
2	01	Header	FF	11111111
3	02	Header	FF	11111111
4	03	Header	FF	11111111
5	04	Header	FF	11111111
6	05	Header	FF	11111111
7	06	Header	FF	11111111
8	07	Header	00	00000000
9	08	EISA ID manufacturer name ("CMN")	0D	00001101
10	09	EISA ID manufacturer name	AE	10101110
11	0A	ID product code (LSB)	27	00100111
12	0B	ID product code (MSB)	16	00010110
13	0C	ID S/N (fixed "0")	00	00000000
14	0D	ID S/N (fixed "0")	00	00000000
15	0E	ID S/N (fixed "0")	00	00000000
16	0F	ID S/N (fixed "0")	00	00000000
17	10	Week of manufacture (fixed week code)	1B	00011011
18	11	Year of manufacture (fixed year code)	20	00100000
19	12	EDID structure version ("1")	01	00000001
20	13	EDID revision ("4")	04	00000100
21	14	Video I/P definition ("Digital")	A5	10100101
22	15	Active area horizontal (“34.468cm“)	22	00100010
23	16	Active area vertical (“21.542cm“)	16	00010110
24	17	Display Gamma (Gamma = "2.2")	78	01111000
25	18	Feature support ("RGB, continous")	03	00000011
26	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	EE	11101110
27	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	95	10010101
28	1B	Rx=0.64	A3	10100011
29	1C	Ry=0.33	54	01010100
30	1D	Gx=0.3	4C	01001100
31	1E	Gy=0.6	99	10011001
32	1F	Bx=0.15	26	00100110
33	20	By=0.06	0F	00001111
34	21	Wx=0.313	50	01010000
35	22	Wy=0.329	54	01010100
36	23	Established timings 1	00	00000000
37	24	Established timings 2	00	00000000
38	25	No manufacturer's specific timing	00	00000000
39	26	Standard timing ID # 1	01	00000001
40	27	Standard timing ID # 1	01	00000001
41	28	Standard timing ID # 2	01	00000001
42	29	Standard timing ID # 2	01	00000001

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43	2A	Standard timing ID # 3	01	00000001
44	2B	Standard timing ID # 3	01	00000001
45	2C	Standard timing ID # 4	01	00000001
46	2D	Standard timing ID # 4	01	00000001
47	2E	Standard timing ID # 5	01	00000001
48	2F	Standard timing ID # 5	01	00000001
49	30	Standard timing ID # 6	01	00000001
50	31	Standard timing ID # 6	01	00000001
51	32	Standard timing ID # 7	01	00000001
52	33	Standard timing ID # 7	01	00000001
53	34	Standard timing ID # 8	01	00000001
54	35	Standard timing ID # 8	01	00000001
55	36	Detailed timing description # 1 Pixel clock ("318.00MHz")	38	00111000
56	37	# 1 Pixel clock (hex LSB first)	7C	01111100
57	38	# 1 H active ("1920")	80	10000000
58	39	# 1 H blank ("160")	A0	10100000
59	3A	# 1 H active : H blank	70	01110000
60	3B	# 1 V active ("1200")	B0	10110000
61	3C	# 1 V blank ("74")	4A	01001010
62	3D	# 1 V active : V blank	40	01000000
63	3E	# 1 H sync offset ("48")	30	00110000
64	3F	# 1 H sync pulse width ("32")	20	00100000
65	40	# 1 V sync offset : V sync pulse width ("10 : 6")	A6	10100110
66	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width	00	00000000
67	42	# 1 H image size (“344 mm“)	58	01011000
68	43	# 1 V image size (“215 mm“)	D7	11010111
69	44	# 1 H image size : V image size	10	00010000
70	45	# 1 H boarder ("0")	00	00000000
71	46	# 1 V boarder ("0")	00	00000000
72	47	# 1 Non-interlaced, Normal, No stereo, Separate sync, H/V pol Negatives	18	00011000
73	48	Detailed timing description # 2 Pixel clock ("318.00MHz")	38	00111000
74	49	# 2 Pixel clock (hex LSB first)	7C	01111100
75	4A	# 2 H active ("1920")	80	10000000
76	4B	# 2 H blank ("160")	A0	10100000
77	4C	# 2 H active : H blank	70	01110000
78	4D	# 2 V active ("1200")	B0	10110000
79	4E	# 2 V blank ("1348")	44	01000100
80	4F	# 2 V active : V blank	45	01000101
81	50	# 2 H sync offset ("48")	30	00110000
82	51	# 2 H sync pulse width ("32")	20	00100000
83	52	# 2 V sync offset : V sync pulse width ("10 : 6")	A6	10100110
84	53	# 2 H sync offset : H sync pulse width : V sync offset : V sync width	00	00000000
85	54	# 2 H image size (“344 mm“)	58	01011000
86	55	# 2 V image size (“215 mm“)	D7	11010111
87	56	# 2 H image size : V image size	10	00010000
88	57	# 2 H boarder ("0")	00	00000000
89	58	# 2 V boarder ("0")	00	00000000

90	59	# 2 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
91	5A	Detailed timing description # 3	00	00000000
92	5B	# 3 Flag	00	00000000
93	5C	# 3 Reserved	00	00000000
94	5D	# 3 Data Type Tag	FD	11111101
95	5E	# 3 FreeSync Setting - Display Range Limits Offset V : H ("0 : 0")	00	00000000
96	5F	# 3 FreeSync Setting - Minimum Vertical Rate ("48Hz")	30	00110000
97	60	# 3 FreeSync Setting - Maximum Vertical Rate ("120Hz")	78	01111000
98	61	# 3 FreeSync Setting - Minimum Horizontal Rate ("153kHz")	99	10011001
99	62	# 3 FreeSync Setting - Maximum Horizontal Rate ("153kHz")	99	10011001
100	63	# 3 FreeSync Setting - Maximum Pixel Clocks ("320MHz")	20	00100000
101	64	# 3 FreeSync Setting - Video Timing Support Flag ("Range Limit Only")	01	00000001
102	65	# 3 FreeSync Setting ("Line Feed")	0A	00001010
103	66	# 3 Padding with "Blank" character	20	00100000
104	67	# 3 Padding with "Blank" character	20	00100000
105	68	# 3 Padding with "Blank" character	20	00100000
106	69	# 3 Padding with "Blank" character	20	00100000
107	6A	# 3 Padding with "Blank" character	20	00100000
108	6B	# 3 Padding with "Blank" character	20	00100000
109	6C	Detailed timing description # 4	00	00000000
110	6D	# 4 Flag	00	00000000
111	6E	# 4 Reserved	00	00000000
112	6F	# 4 ASCII string Model Name	FC	11111100
113	70	# 4 Flag	00	00000000
114	71	# 4 Character of Model name ("N")	4E	01001110
115	72	# 4 Character of Model name ("1")	31	00110001
116	73	# 4 Character of Model name ("6")	36	00110110
117	74	# 4 Character of Model name ("0")	30	00110000
118	75	# 4 Character of Model name ("J")	4A	01001010
119	76	# 4 Character of Model name ("M")	4D	01001101
120	77	# 4 Character of Model name ("E")	45	01000101
121	78	# 4 Character of Model name ("-")	2D	00101101
122	79	# 4 Character of Model name ("G")	47	01000111
123	7A	# 4 Character of Model name ("L")	4C	01001100
124	7B	# 4 Character of Model name ("2")	32	00110010
125	7C	# 4 New line character indicates end of ASCII string	0A	00001010
126	7D	# 4 Padding with "Blank" character	20	00100000
127	7E	Extension flag	01	00000001
128	7F	Checksum for 00h~7Eh	FD	11111101
129	80	EDID Extension Tags	02	00000010
130	81	Revision Number	03	00000011
131	82	Start of Timing Data (00:No detailed timing descriptors are provided and no data is provided in the reserved data block)	22	00100010
132	83	Total number of Detailed Timing formats in entire E-EDID structure.	00	00000000
133	84	Tag Code [7:5], Length of data [4:0]	E3	11100011
134	85	Extended Tag Code	05	00000101
135	86	Colorimetry Support Flags	80	10000000
136	87	Colorimetry Metadata Support Flags	00	00000000

137	88	Tag Code [7:5], Length of data [4:0]	E6	11100110
138	89	Extended Tag Code	06	00000110
139	8A	Supported Electro-Optical Transfer Function	05	00000101
140	8B	SM_0 =1: Static Metadata Type 1	01	00000001
141	8C	Desired Content Max Luminance data	53	01010011
142	8D	Desired Content Max Frame-average Luminance data	53	01010011
143	8E	Desired Content Min Luminance data	2F	00101111
144	8F	Datablock 1: AMD Vendor specific Data Block(Total :18 byte)(3 Bytes for IEEE OUI + 15 Bytes)	72	01110010
145	90	AMD IEEE OUI Value(0x00001A)	1A	00011010
146	91	AMD IEEE OUI Value(0x00001A)	00	00000000
147	92	AMD IEEE OUI Value(0x00001A)	00	00000000
148	93	AMD VSDB Version	03	00000011
149	94	Freesync Capability(01:Freesync support,00:Freesync no support)	01	00000001
150	95	Min refresh Rate [Hz]	30	00110000
151	96	Max refresh Rate [Hz]	78	01111000
152	97	FreeSync MCCS VCP Code; required if EDID update not possible to indicate current state of FreeSync support.	00	00000000
153	98	Supported WCG and HDR feature	00	00000000
154	99	Max Luminance 1	00	00000000
155	9A	Min Luminance 1	00	00000000
156	9B	Max Luminance 2	00	00000000
157	9C	Min Luminance 2	00	00000000
158	9D	Max refresh Rate [Hz]:Bits 7:0	78	01111000
159	9E	Max refresh Rate [Hz]:Bits 15:8	00	00000000
160	9F	Maximum Fast Transport Input Pixel Rate [kHz] - bits 7:0	00	00000000
161	A0	Maximum Fast Transport Input Pixel Rate [kHz] - bits 15:8	00	00000000
162	A1	Maximum Fast Transport Input Pixel Rate [kHz] - bits 23:16	00	00000000
163	A2	Reserved	00	00000000
164	A3	Reserved	00	00000000
165	A4	Reserved	00	00000000
166	A5	Reserved	00	00000000
167	A6	Reserved	00	00000000
168	A7	Reserved	00	00000000
169	A8	Reserved	00	00000000
170	A9	Reserved	00	00000000
171	AA	Reserved	00	00000000
172	AB	Reserved	00	00000000
173	AC	Reserved	00	00000000
174	AD	Reserved	00	00000000
175	AE	Reserved	00	00000000
176	AF	Reserved	00	00000000
177	B0	Reserved	00	00000000
178	B1	Reserved	00	00000000
179	B2	Reserved	00	00000000
180	B3	Reserved	00	00000000
181	B4	Reserved	00	00000000
182	B5	Reserved	00	00000000

183	B6	Reserved	00	00000000
184	B7	Reserved	00	00000000
185	B8	Reserved	00	00000000
186	B9	Reserved	00	00000000
187	BA	Reserved	00	00000000
188	BB	Reserved	00	00000000
189	BC	Reserved	00	00000000
190	BD	Reserved	00	00000000
191	BE	Reserved	00	00000000
192	BF	Reserved	00	00000000
193	C0	Reserved	00	00000000
194	C1	Reserved	00	00000000
195	C2	Reserved	00	00000000
196	C3	Reserved	00	00000000
197	C4	Reserved	00	00000000
198	C5	Reserved	00	00000000
199	C6	Reserved	00	00000000
200	C7	Reserved	00	00000000
201	C8	Reserved	00	00000000
202	C9	Reserved	00	00000000
203	CA	Reserved	00	00000000
204	CB	Reserved	00	00000000
205	CC	Reserved	00	00000000
206	CD	Reserved	00	00000000
207	CE	Reserved	00	00000000
208	CF	Reserved	00	00000000
209	D0	Reserved	00	00000000
210	D1	Reserved	00	00000000
211	D2	Reserved	00	00000000
212	D3	Reserved	00	00000000
213	D4	Reserved	00	00000000
214	D5	Reserved	00	00000000
215	D6	Reserved	00	00000000
216	D7	Reserved	00	00000000
217	D8	Reserved	00	00000000
218	D9	Reserved	00	00000000
219	DA	Reserved	00	00000000
220	DB	Reserved	00	00000000
221	DC	Reserved	00	00000000
222	DD	Reserved	00	00000000
223	DE	Reserved	00	00000000
224	DF	Reserved	00	00000000
225	E0	Reserved	00	00000000
226	E1	Reserved	00	00000000
227	E2	Reserved	00	00000000
228	E3	Reserved	00	00000000
229	E4	Reserved	00	00000000

230	E5	Reserved	00	00000000
231	E6	Reserved	00	00000000
232	E7	Reserved	00	00000000
233	E8	Reserved	00	00000000
234	E9	Reserved	00	00000000
235	EA	Reserved	00	00000000
236	EB	Reserved	00	00000000
237	EC	Reserved	00	00000000
238	ED	Reserved	00	00000000
239	EE	Reserved	00	00000000
240	EF	Reserved	00	00000000
241	F0	Reserved	00	00000000
242	F1	Reserved	00	00000000
243	F2	Reserved	00	00000000
244	F3	Reserved	00	00000000
245	F4	Reserved	00	00000000
246	F5	Reserved	00	00000000
247	F6	Reserved	00	00000000
248	F7	Reserved	00	00000000
249	F8	Reserved	00	00000000
250	F9	Reserved	00	00000000
251	FA	Reserved	00	00000000
252	FB	Reserved	00	00000000
253	FC	Reserved	00	00000000
254	FD	Reserved	00	00000000
255	FE	Reserved	00	00000000
256	FF	EDID Extension Block Checksum	FA	11111010

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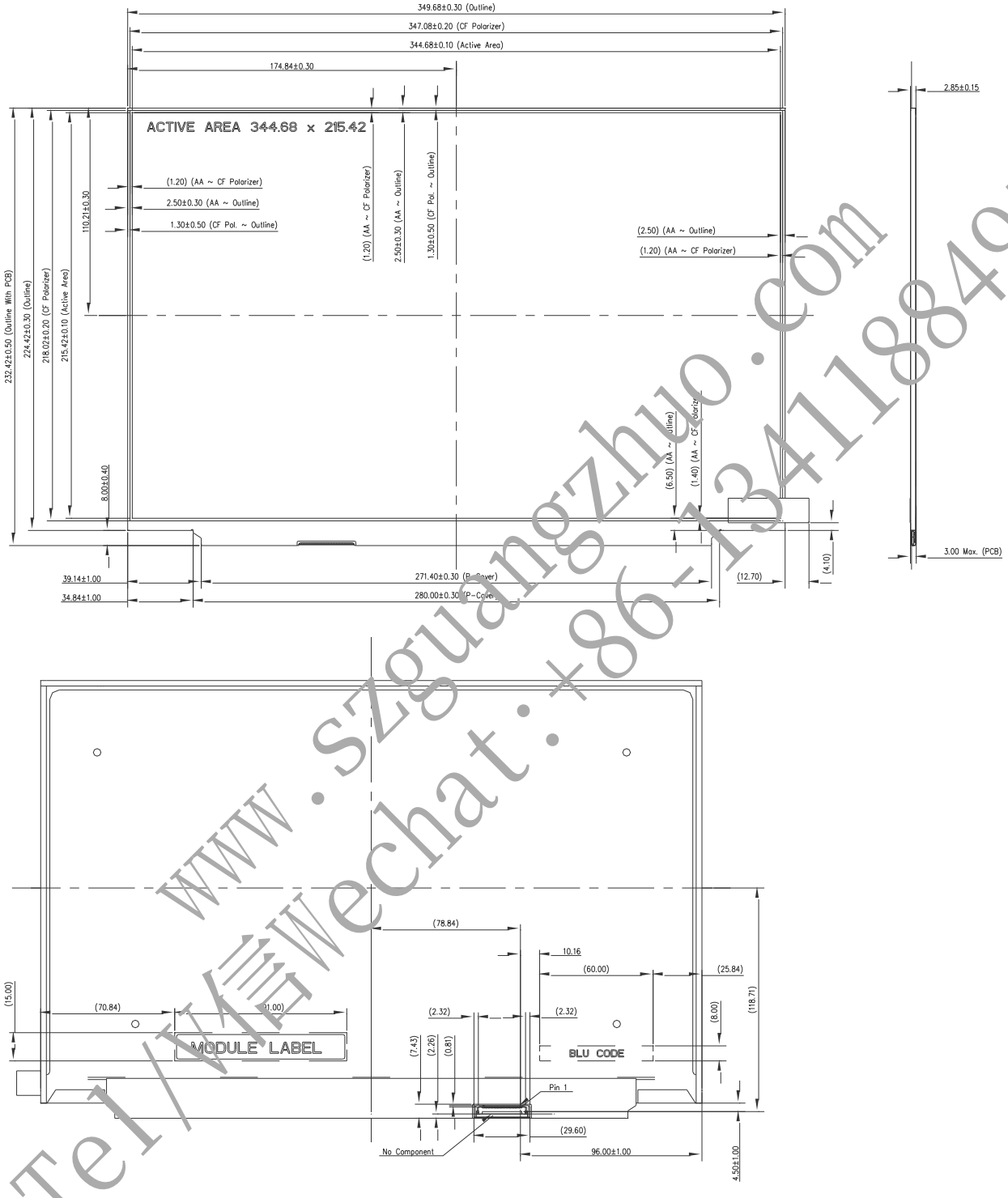
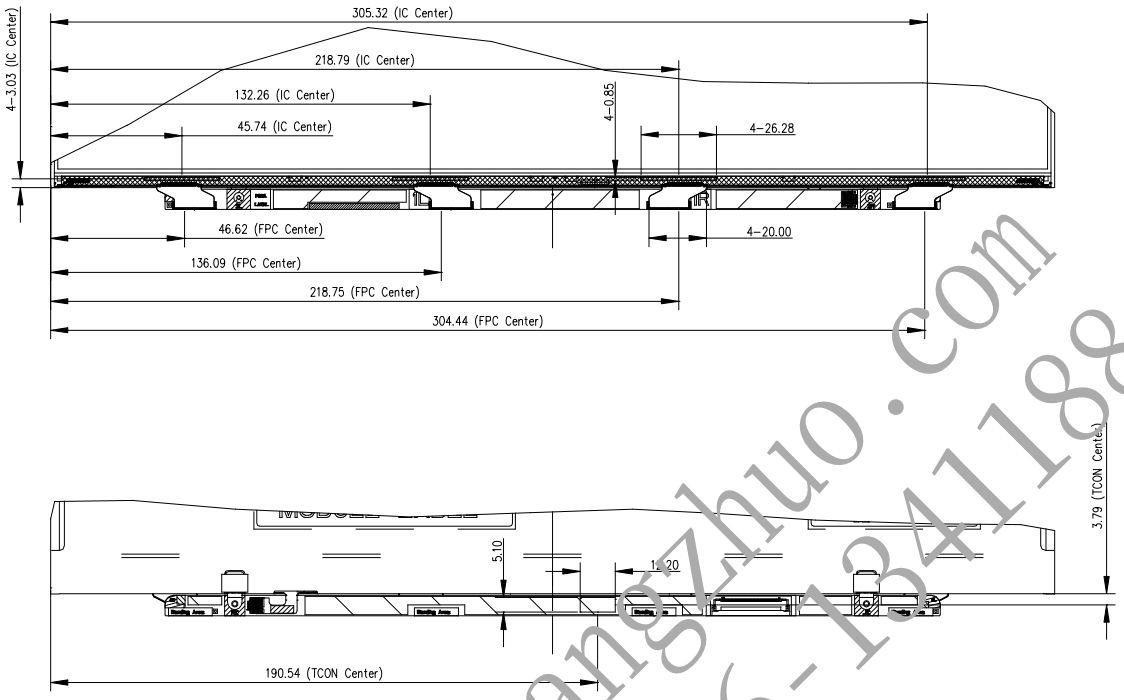
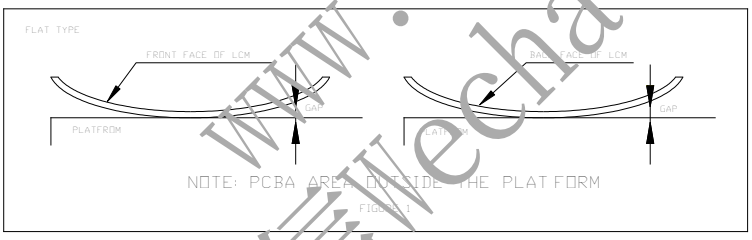
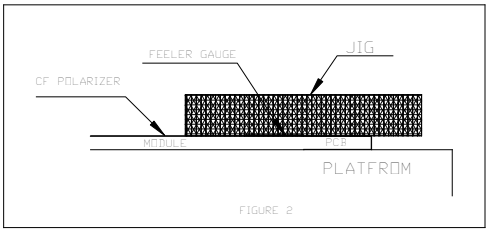
Appendix. OUTLINE DRAWING

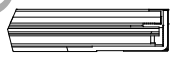








NOTES :
1. IN ORDER TO AVOID ABNORMAL DISPLAY, POOLING AND WHITE SPOT, NO OVERLAPPING IS SUGGESTED AT CABLES, ANTENNAS, CAMERA, WLAN, WAN OR FOREIGN OBJECTS OVER FPC/COF, T-CON AND VR LOCATIONS.
2. LVDS/EDP CONNECTOR IS MEASURED AT PIN1 AND ITS MATING LINE.
3. MODULE FLATNESS SPEC (0.5 mm) MAX. (SEE FIGURE 1) (SPEC. WILL BE MODIFIED AFTER DVT CHECK).
4. "( )" MARKS THE REFERENCE DIMENSION.
5. LCD HIGHEST PORTION MUST BE TOP POLARIZER AND OTHER LCM MATERIALS MUST BE LOWER THAN TOP POLARIZER. [MEASURED BY JIG(WEIGHT 100g)&FEELER GUAGE(0.1mm)] (SEE FIGURE 2) THE SOP SHOULD REFER TO "LN0566762" IN INX
6. MEASUREMENT OF THICKNESS MUST BE MEASURED BY CALIPER OR MICROMETER.
7. MODULE TYPE SECTION X-X.



SECTION X-X

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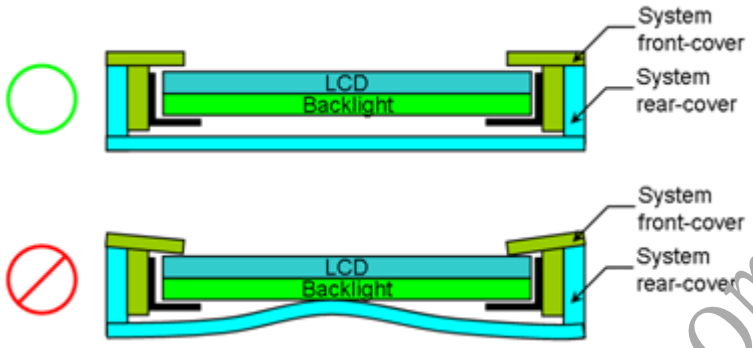
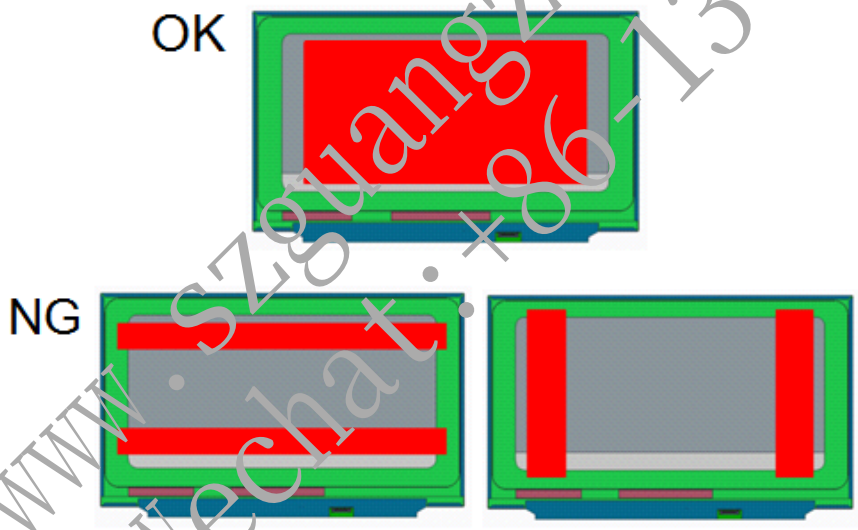
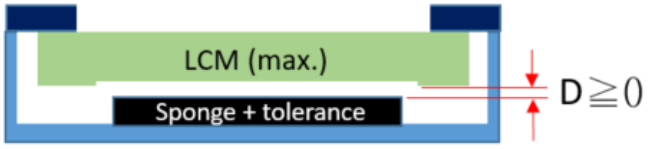
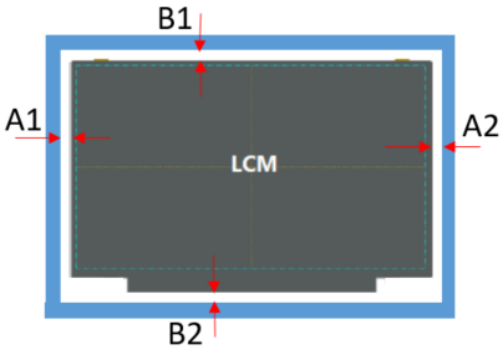
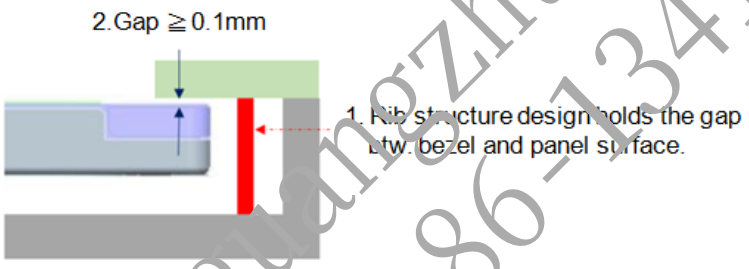
Appendix. SYSTEM COVER DESIGN GUIDANCE

0.	**Permanent deformation of system cover after reliability test**
	
Definition	System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack. Note: If the interference can't be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
1.	**Sponge area design behind panel**
	
Definition	Sponge area design behind panel can't be across the panel metal rear and the reflector at the same time. It can be on the reflector area only.
2.	**Gap between system rear-cover & panel**
	
Definition	The maximum thickness of sponge on the system rear-cover can't interfere to the maximum thickness of panel. Because the interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur. Note: If the interference can't be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
3.	**Gap Design between panel & around structure**

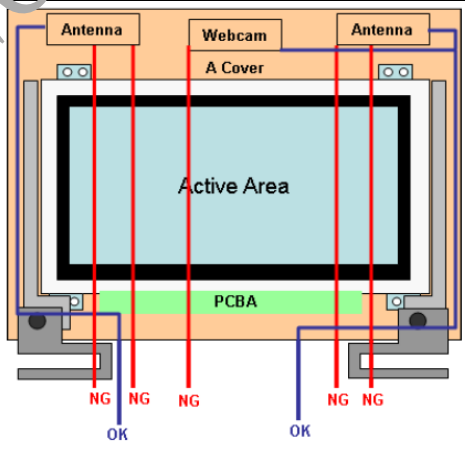


Item	Suggestion	Remark
A1	A1≧0.5	Gap≧ Panel outline max. tolerance + Assembly max. tolerance
A2	A2≧0.5	
B1	B1≧0.5	
B2	B2≧0.8	

Definition	Gap Design between panel & around structure needs to consider the maximum tolerances of panel outline and assembly at the same time. Gap Design suggestion is shown as A1/A2/B1/B2 on the chart.
4.	**Gap between panel & bezel**

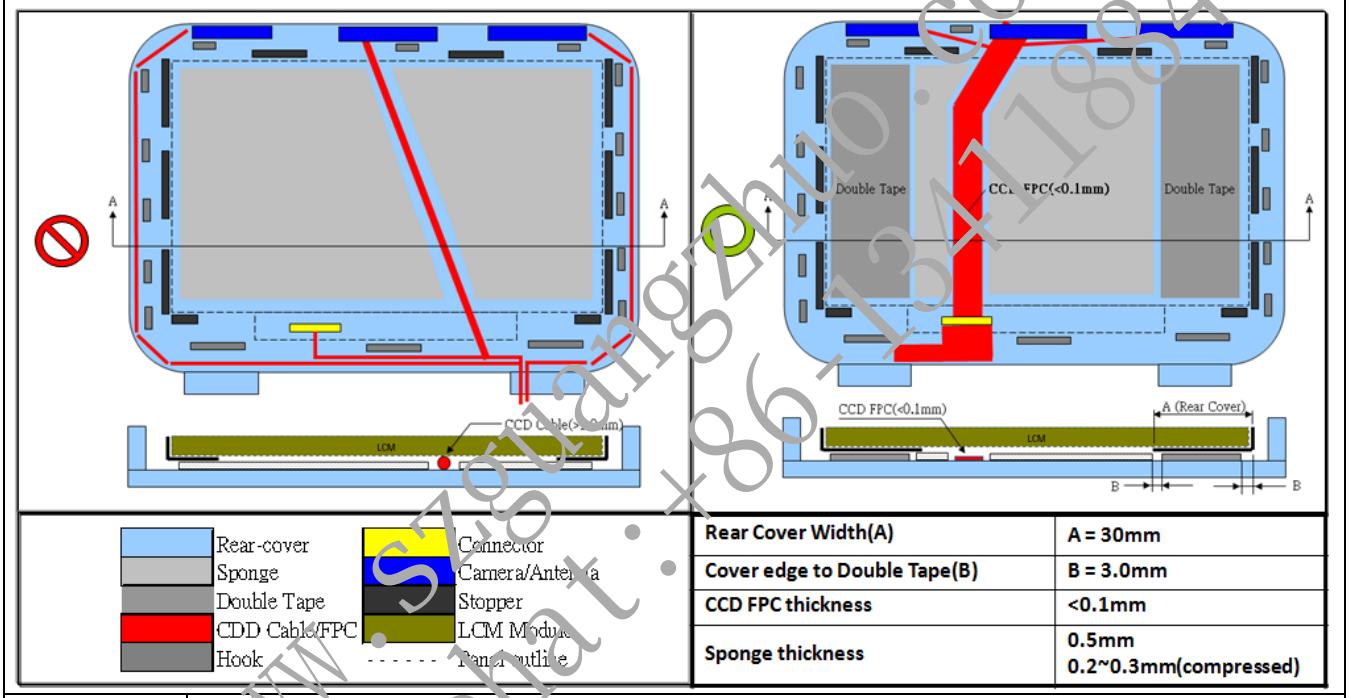


Definition	The gap between system bezel & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system font-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test, or during pooling inspection procedure. To remain the sufficient gap, design with system rib higher than maximum panel thickness is recommended. The sufficient gap design is greater or equal to 0.1mm.
5.	**Cable routing behind panel**



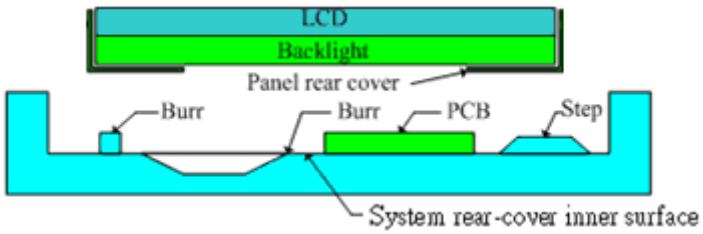
Definition	It is strongly recommended that cables route around the panel outline, not overlap with the panel outline (including PCB). Because issue such as abnormal display & white spot after backpack test, hinge test, twist test or pogo test may occur. If any routings across panel outline are needed, we suggest design as below: -Using FFC/FPC to replace cables. -Routing at the right or left area of panel metal rear. -Avoid any routings at the step of panel or A cover. -No interference to panel. -It should not overlap TCON, COF/FPC, Driver IC
6.	**Interference examination of antenna cable and Web Cam wire**

- To prevent panel damage, we suggest using CCD FPC to replace CCD cable
- Using double tape to fix LCM module for no bracket design.

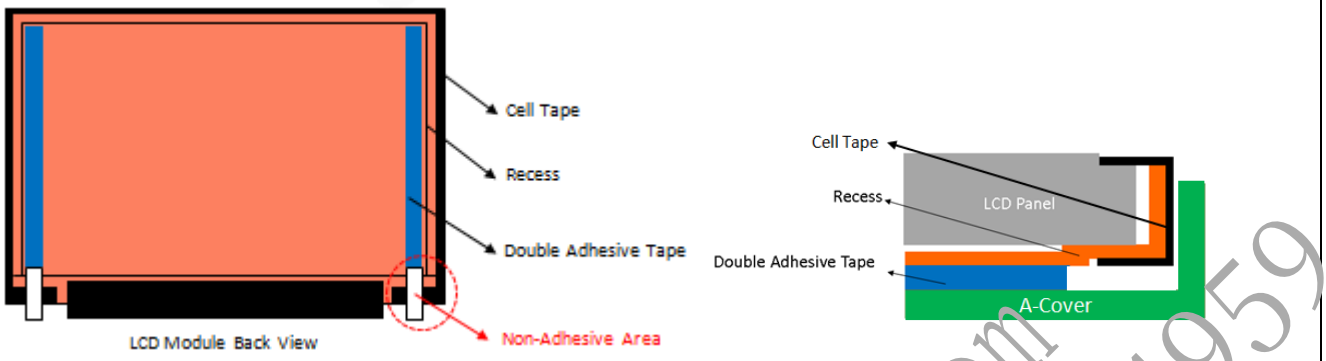
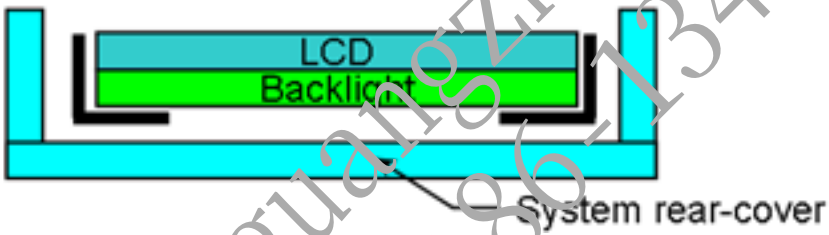
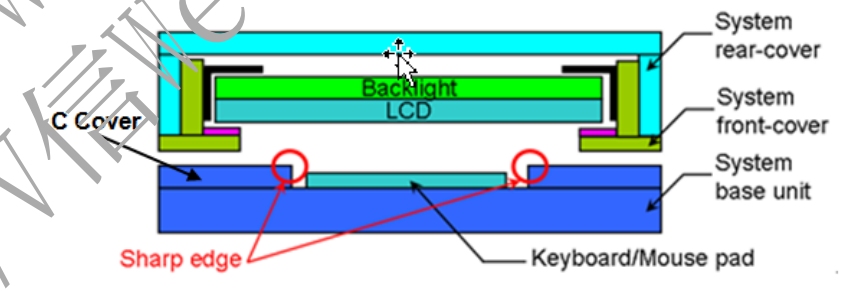
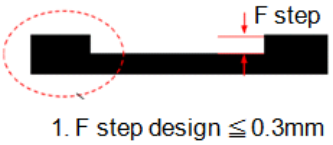


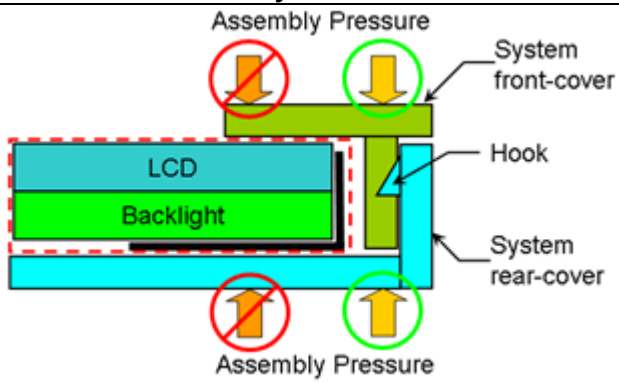
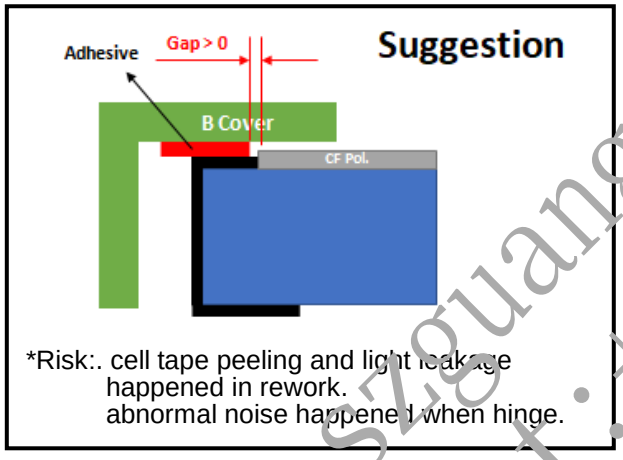
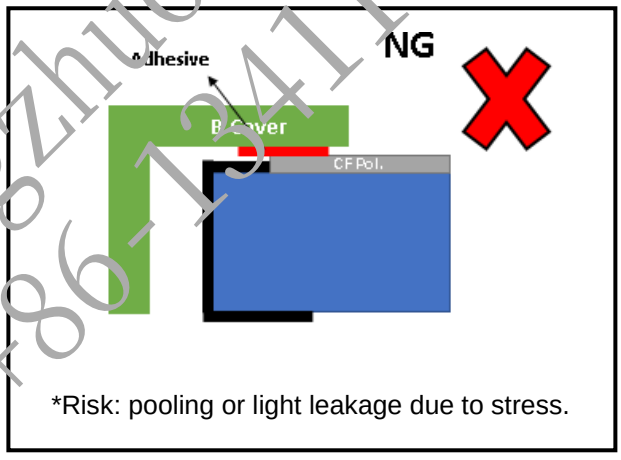
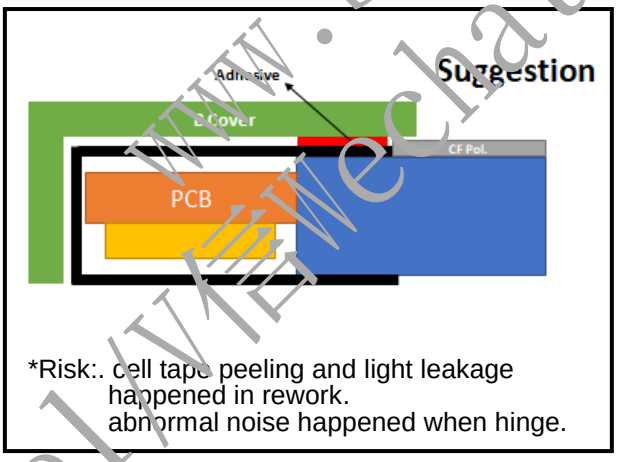
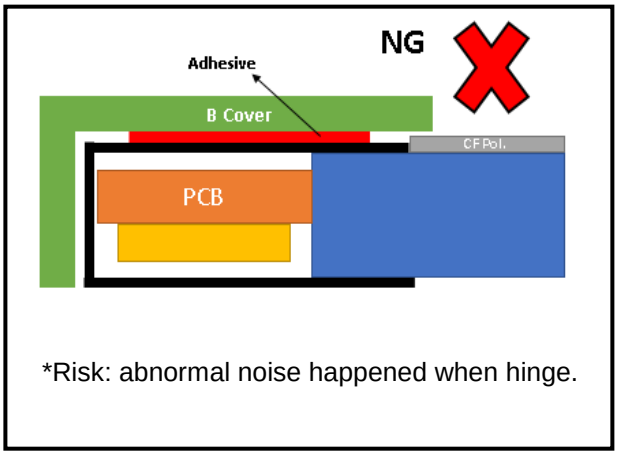
Rear Cover Width(A)	**A = 30mm**
Cover edge to Double Tape(B)	**B = 3.0mm**
CCD FPC thickness	**<0.1mm**
Sponge thickness	**0.5mm** **0.2~0.3mm(compressed)**

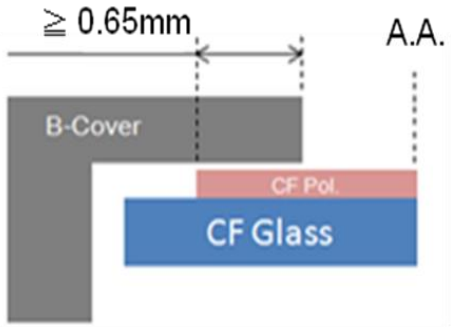
Definition	If the antenna cable or Web Cam wire must overlap with the panel outline, both sides of the antenna cable or Web Cam wire must have a sponge (Sponge material can not contain NH3) and sponge require higher antenna cable or Web Cam wire. (Antenna cable or Web Cam wire should not overlap with TCON, COF/FPC, Driver IC) Note: If the interference can't be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
7.	**System rear-cover inner surface examination**



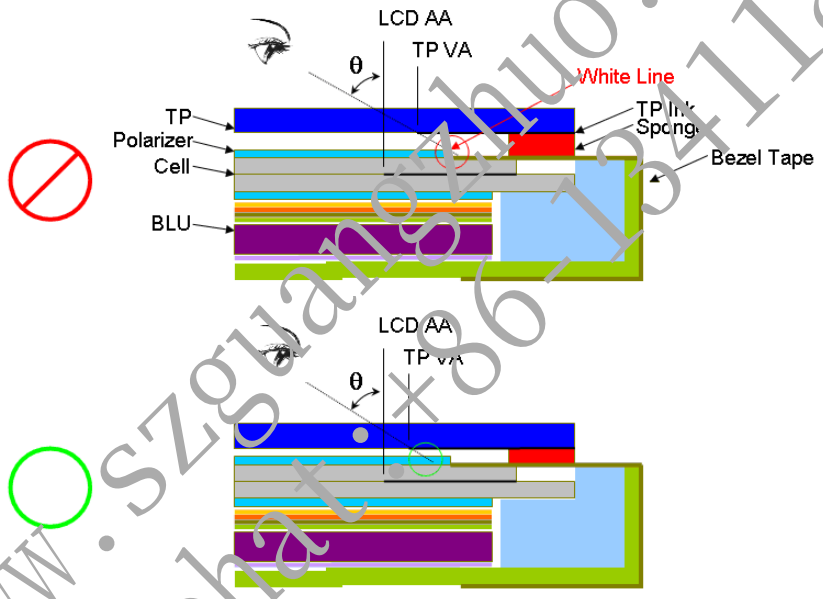
Definition	Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.

8.	**Tape/sponge design on system inner surface**
	
Definition	To prevent noise cause by system opening and closing. To prevent peeling the cell tape in rework process. The double adhesive tape need to avoid overlap LCD rear recess and the cell tapes of module. There are recess on the lower left and lower right of the module, and double adhesive tape should avoided.
9.	**Material used for system rear-cover**
 System rear-cover material: Al-Mg alloy	
Definition	System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.
10.	**C cover shape design**
  1. F step design ≦0.3mm  2. If F step > 0.3mm, slop edge design is needed to prevent panel crack.	
Definition	The F step design on C Cover less than or equal to 0.3mm is recommended. If F step exceeds 0.3mm, the slop edge design is necessary to prevent panel crack.

11.	**Assembly SOP examination for system front-cover with Hook design**
	
Definition	To prevent panel crack during system front-cover assembly process with hook design, it is not recommended to press panel or any location that related directly to the panel.
12.	**Adhesive design between panel & B-cover**
	 *Risk:. cell tape peeling and light leakage happened in rework. abnormal noise happened when hinge.
	 *Risk: pooling or light leakage due to stress.
	 *Risk:. cell tape peeling and light leakage happened in rework. abnormal noise happened when hinge.
	 *Risk: abnormal noise happened when hinge.
Definition	To prevent panel crack during system front-cover assembly process with double tape design, When system applied adhesive between B-Cover and LCD module, please design a distance >0mm between B-Cover's adhesive and CF pol. Do **NOT** put adhesive on CF pol.and Do **NOT** put adhesive on PCB area. Adhesive material need be qualified to prevent from doing damage to cell tape after rework. Adhesive material need be qualified to prevent abnormal noise when hinge swinging test.

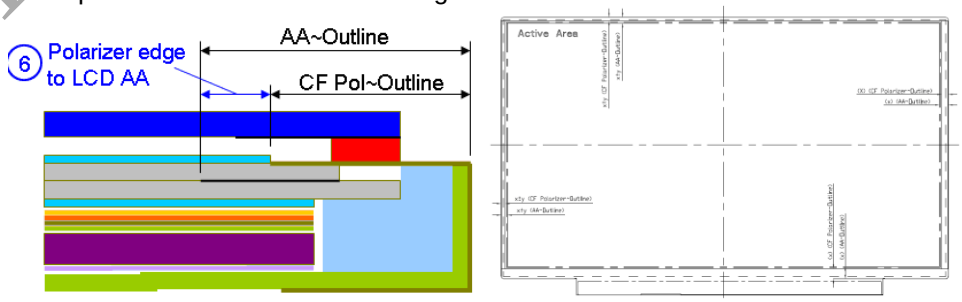
13.	System front-cover opening area reference with TFT-LCD module
	
Definition	To prevent panel the noise of B-cover & CF Pol. Distance from CF Pol. edge to front-cover edge more than 0.65mm.

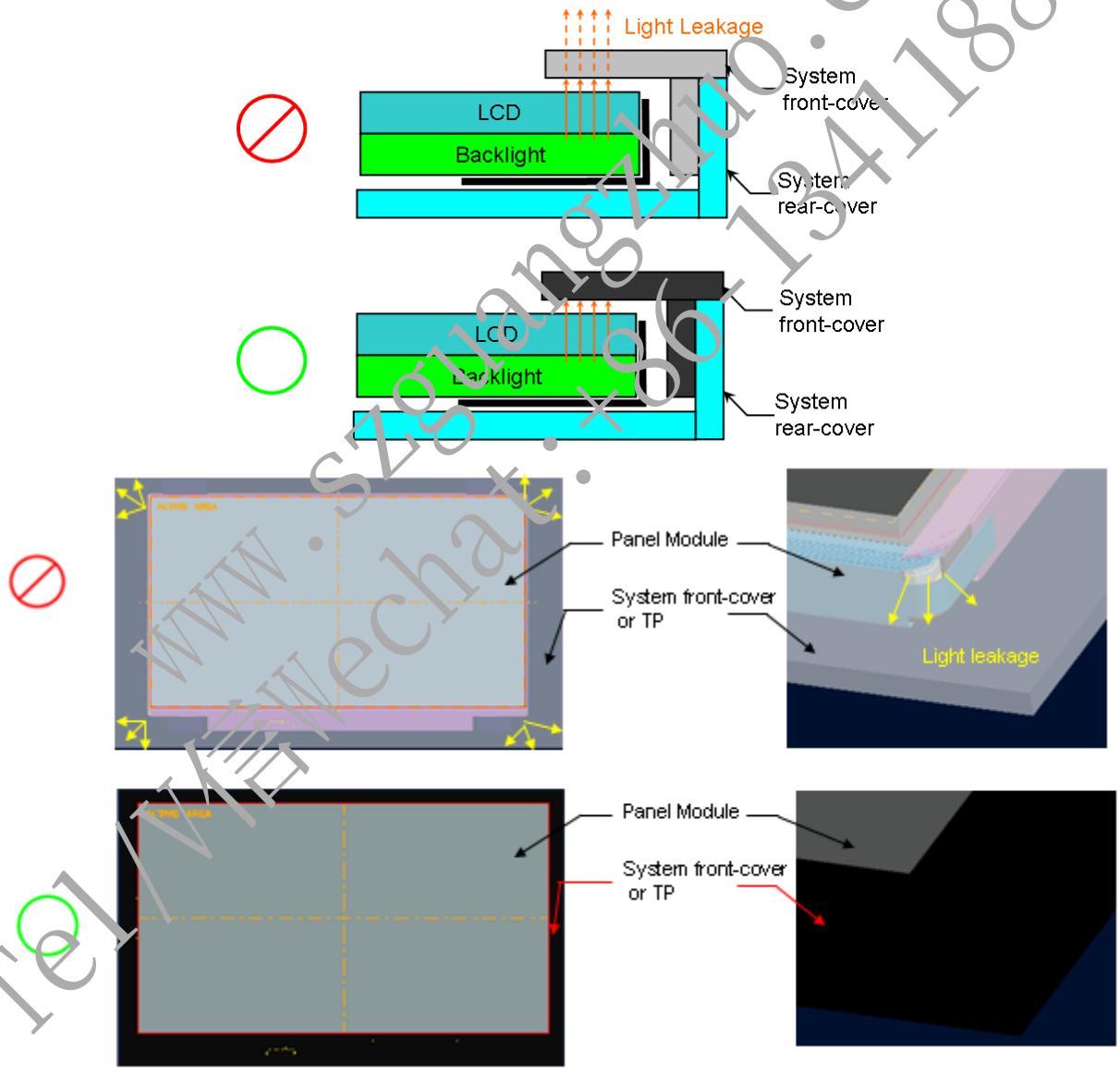
14.	Touch Application : TP and LCD Module Combination for White Line Prevention

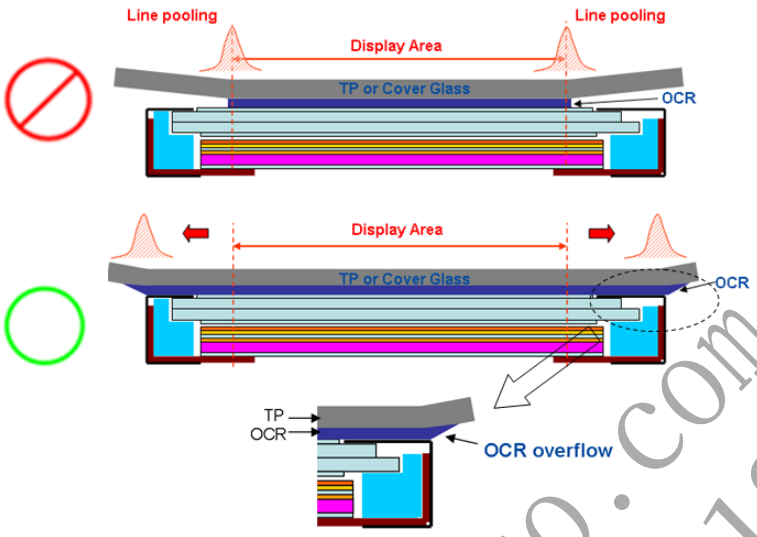
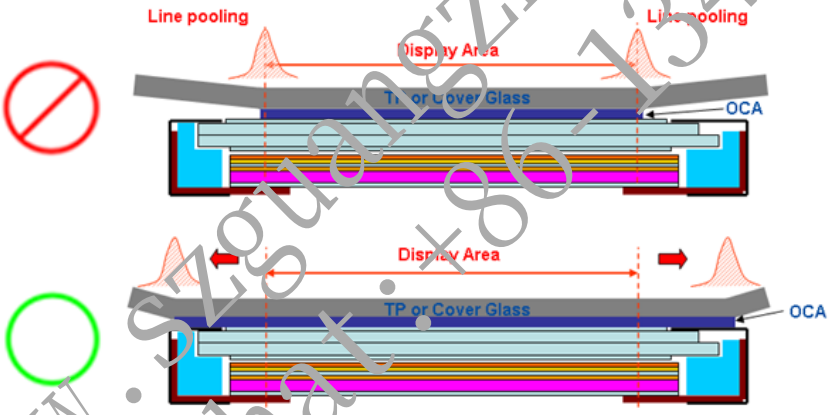


Parameter consideration for White Line Issue :	
1	TP VA to LCD AA distance
2	TP Assembly tolerance
3	TP Ink Printing tolerance
4	Sponge thickness and tolerance
5	Inspection/Viewing Angle specification
6	Polarizer edge to LCD AA distance and tolerance

Polarizer edge to LCD AA distance can be derived by “AA to Outline” – “CF Pol to Outline” with respect to INX 2D Outline Drawing on each side.



Definition	For using in Touch Application: to prevent White Line appears between TP and LCD module combination, the maximum inspection angle location must not fall onto LCD polarizer edge, otherwise light line near edge of polarizer will be appear. Parameters such as TP VA to LCD AA distance, TP assembly tolerance, TP Ink printing tolerance, Sponge thickness and tolerance, and Maximum Inspection/Viewing Angle, must be considered with respect to LCD module's Polarizer edge location and tolerance. This consideration must be taken at all four edges separately. The goal is to find parameters combination that allow maximum inspection angle falls inside polarizer black margin area. Note: Information for Polarizer edge location and its tolerance can be derived from INX 2D Outline Drawing ("AA to Outline" – "CF Pol to Outline"). Note: Please feel free to contact INX FAE Engineer. By providing value of parameters above on each side, we can help to verify and pass the white line risk assessment for customer reference.
15.	**Color of system front-cover material**
	
Definition	To prevent light leakage is seen at system front-cover due to material transparency, we suggest using dark color material (black) for system front-cover design.

16.	Use OCR Lamination
	
Definition	OCR glue as possible beyond module, in order to avoid Line Pooling
17.	**Use OCA Lamination**
	
Definition	OCA glue as possible plastered throughout the module, in order to avoid Line Pooling.

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Appendix. LCD MODULE HANDLING MANUAL

Purpose	• **This SOP is prepared to prevent panel dysfunction possibility through incorrect handling procedure.** • **This manual provides guide in unpacking and handling steps.** • **Any person which may contact / related with panel, should follow guide stated in this manual to prevent panel loss.**
1.	**Unpacking**

2.	**Panel Lifting**

3.	Do and Don't

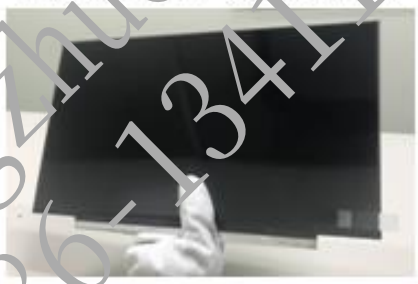
Do :

- Handle with both hands.
- Handle panel at left and right edge.

Don't :

- Lifting with one hand.

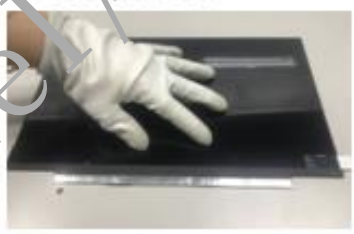
- Handle at PCBA side.



Don't :

- Stack panels.

- Press panel.

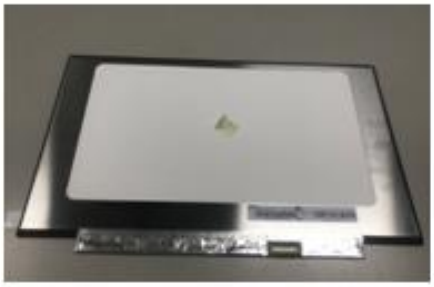


Don't :

- Put foreign stuff onto panel

- Put foreign stuff under panel

Don't :
- Paste any material unto white reflector sheet



Don't :
- Pull / Push white reflector sheet

Don't :
- Hold at panel corner.

Don't :
- Twist panel.

Connectors must be inserted in parallel to avoid :
1. PCB hitting the panel and causing the panel to break.
2. PCB deformation and warping causes PCB/P-Cover higher than CF pol side, so that PCB components are higher than the back of module, which leads to component cracking.
3. Connector deformation or connector pins skewed resulting in abnormal display.
4. Panel link peeling or lead broken causes abnormal display.

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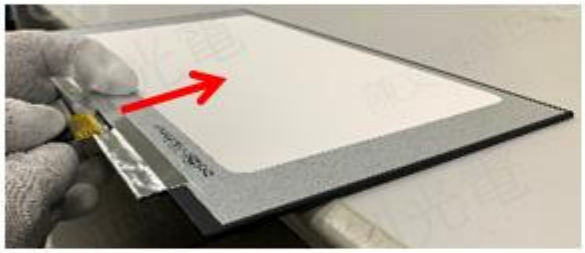
Do:

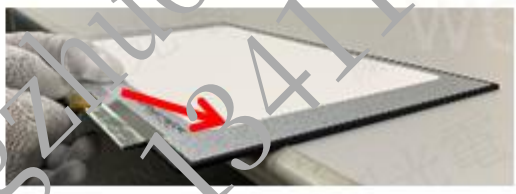
- Hold panel at bottom edge on a plate or Jig Parallel while inserting connector.



Don't:

- Hold panel at bottom edge up while inserting connector.

- Hold panel at bottom edge down while inserting connector.



Do:

- Hold panel at bottom edge on a plate or Jig Parallel while inserting connector.

Don't:

- Hold panel at bottom edge up while inserting connector.

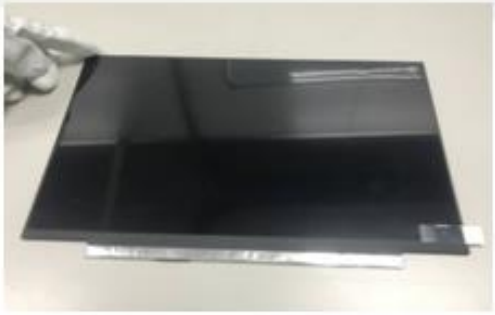
- Hold panel at bottom edge down while inserting connector.

Do:
- Remove panel protector film starts from Lower-right corner to Top-left

Don't:
- Remove panel protector Film parallel X-direction

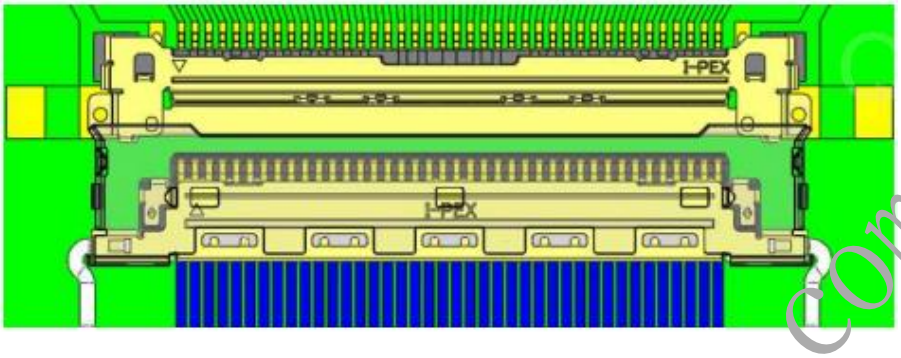
Do :
- Remove panel protector film starts from pull tape

Don't :
- Remove panel protector film From film another side.

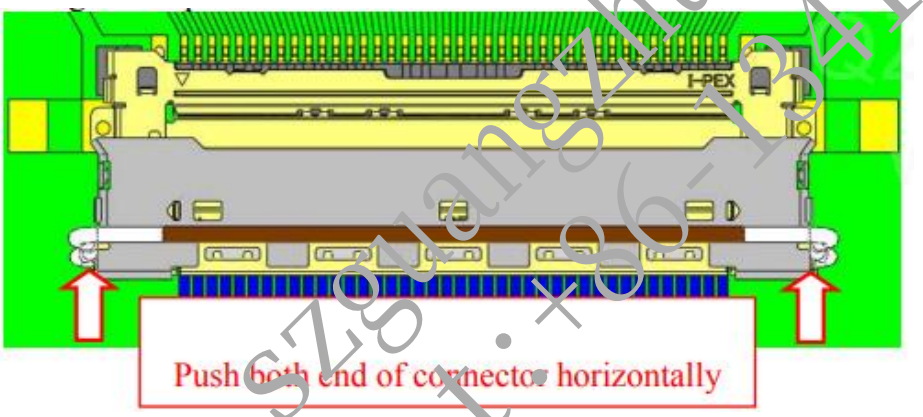


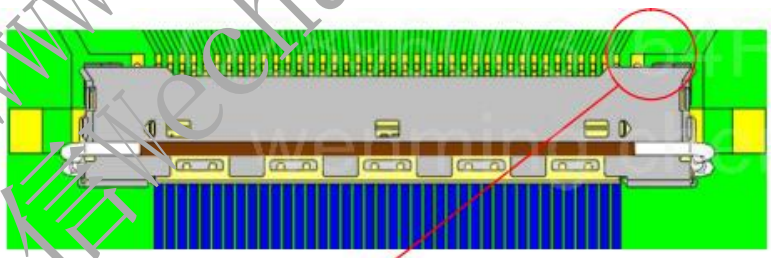
4.	Connector Insertion Method And Caution

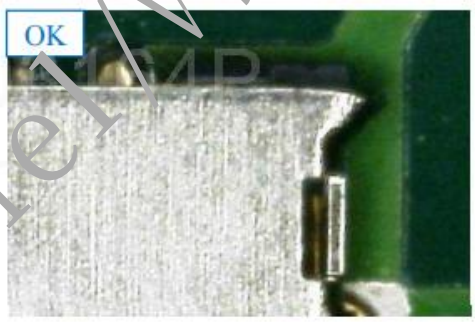
① Please set the tip of Plug connector's Alignment Cover on Receptacle connector.



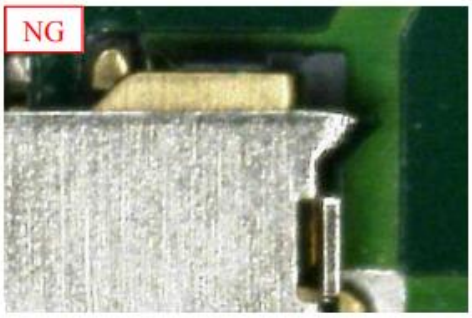
② Push both ends of Plug connector horizontally. When position relations of the tip of Plug connector's Alignment Cover and Receptacle's shell, mating is completion





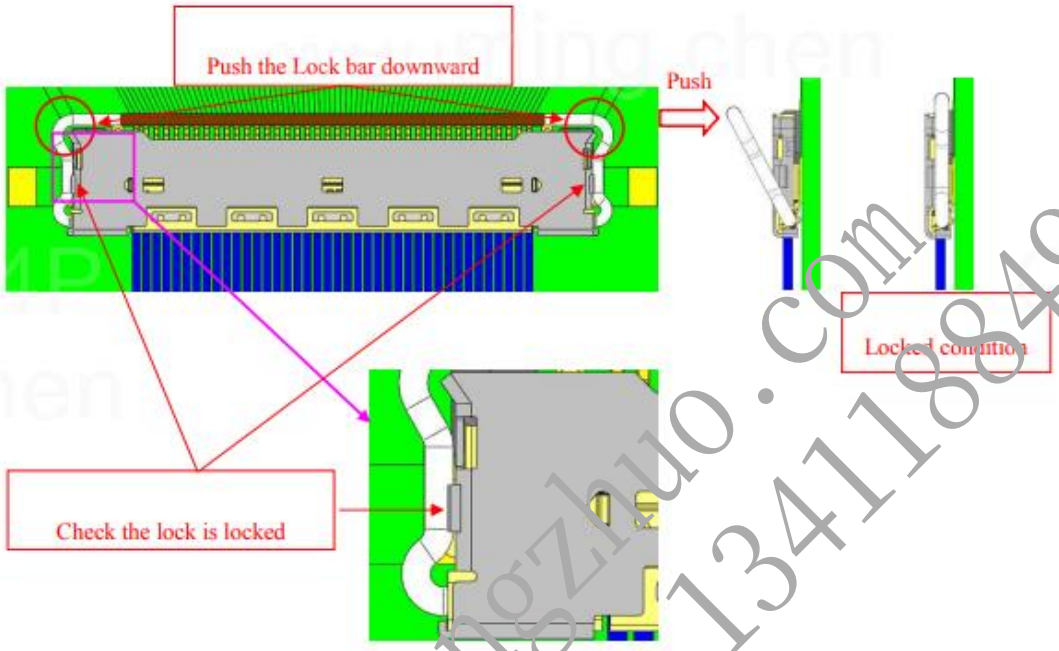


(a) 嵌合完了／State of complete mating



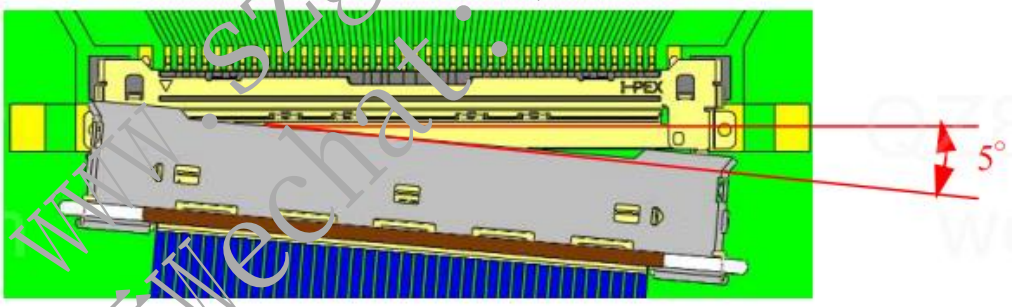
(b) 嵌合不完全／State of incomplete mating

③ Push the circled positions of the Lock bar to the PCB side and lock it with Plug connector's Alignment Cover.



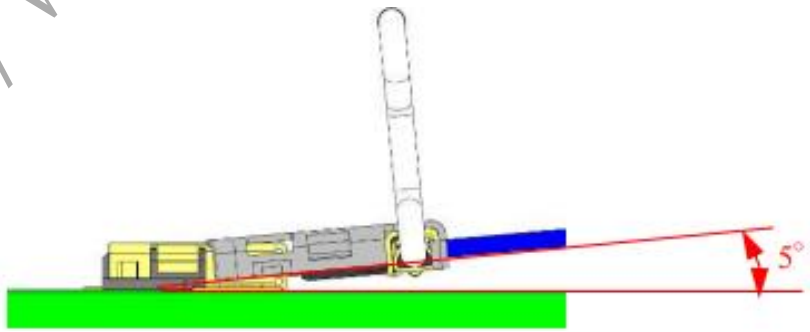
Caution 1：

Please keep insert slant 5 ° or less in horizontal direction. By inserting with the slant more than 5°, deformation of the connector will occur.



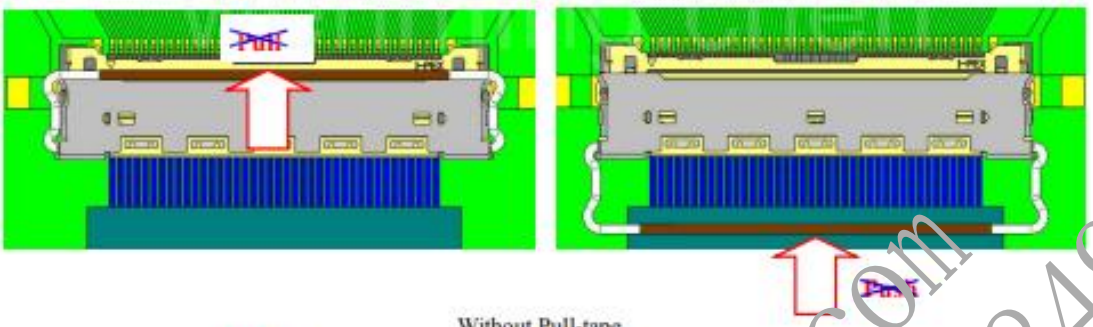
Caution 2：

At starting the insertion, please keep the slant 5 ° or less in vertical direction. By inserting with the slant more than 5°, deformation of the connector will occur.

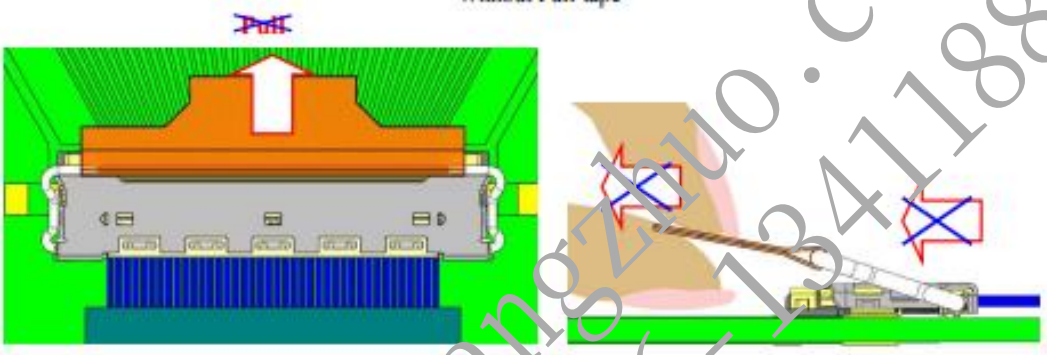


Caution 3：

Please do not insert a Plug connector using Lock bar and Pull-tape. There are possibilities to cause the Lock bar and connector deformation.



Without Pull-tape



With Pull-tape

Caution 4：

Please do not apply force toward the PCB side to the Plug connector in insertion. PCB will be damaged like below and it may cause the disconnection of the pattern or the short.