

Product Specification Sheet

Customer: _____

Model Name: MNG007DA5-3

HW: V0A

Date: 2025/2/13

Version: V07

Customer's Approval		CSOT	
Signature	Date	Approved By	Date
		Reviewed By	Date
		Prepared By:	Date

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Record of Revision

Version	Revise Date	Page	Content
V01	2024/04/11	All	Preliminary Specification
	2024/08/08	P29	Label drawing
V02	2024/08/30	P11; P15; P16; P21	Function pin feature ; LED Power consumption; Backlight unit; APOL version
V03	2024/09/05	P31	EDID information
V04	2024/09/12	P49	OUTLINE DRAWING
V05	2024/09/27	P20; P29; P32	DISPLAY TIMING SPECIFICATIONS, EDID DATA STRUCTURE; Label drawing
V06	2025/1/17	P23; P49	T19 SEQUENCE Appendix. Checksum of DDS, EDID and FPC
V07	2025/2/13	P8 P13 P34	Pin assignment note LCD electronics Appendix. EDID DATA STRUCTURE

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1. GENERAL DESCRIPTION

1.1 OVERVIEW

MNG007DA5-3 is a 16.0 WQ 165Hz TFT Liquid Crystal Display Low blue light module with LED Backlight unit and 40 pins eDP 1.4 interface. This module supports 2560 x 1600 mode and can display 16.7M colors.

1.2 SPECIFICATION SUMMARY

No.	Item	Specification	Unit	Note
1	LCD size	16.0	inch	
2	Resolution	2560 x RGB x 1600		WQ
3	Pixel Arrangement	RGB		
4	Model Type	LCM		
5	TFT Technology	LTPS		
6	Display mode	FFS, Normally Black		
7	Active Area	344.6784*215.424	mm	
8	pixel pitch	44.88(H)×134.54(V)	um	
9	Display Colors	16.7M		@ true 8bit
10	Contrast Ratio	1200:1(Typ)		1200:1(Typ) 960:1(Min)
11	sRGB Coverage	sRGB 100% (Typ) 95% (min)		sRGB 100% (Typ) 95% min
12	LCM Outline Dimension	349.63×224.42×3.05	mm	Bent without PCBA,TYP
13	Luminance	400 (Typ)	nits	
14	Low blue light ratio	Y	%	Max
15	Surface treatment(TYP)	Fine AG(Haze 25%)	--	Pol.
16	Interface	eDP 1.4b		4 lane@5.4G
17	HDR function	NA		
18	Method of Inversion	Column Inversion		
19	Power consumption of Panel	1.8 (Max)	W	3.3V@Mosaic 165Hz
	Power consumption of Backlight	4.24 (Max)	W	
20	Weight	400 (Max)	g	

Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS =3.3 V, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 °C, whereas mosaic pattern is displayed.

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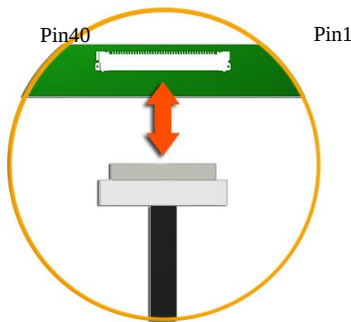
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2. MECHANICAL SPECIFICATIONS

Parameter		Min.	Typ.	Max.	Unit	Note
Unit outline dimensions	Width	349.38	349.68	349.98	mm	
	Height	224.12	224.42	224.72	mm	Without PCB
	Depth	2.90	3.05	3.20	mm	
Weight		-	-	400	g	

2.1 INTERFACE CONNECTION



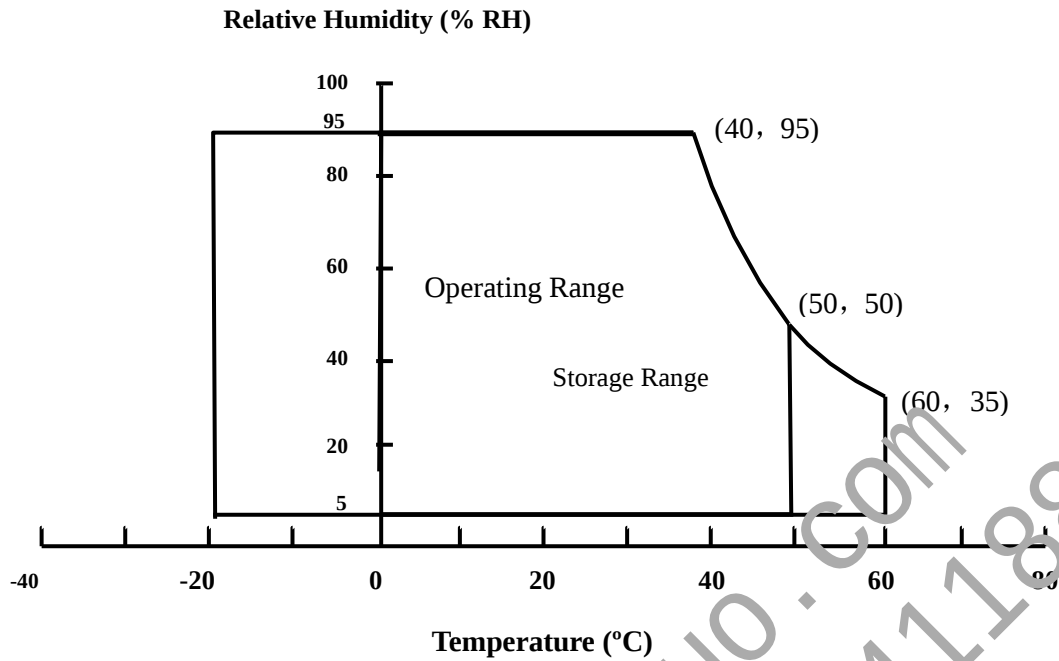
Please refer Appendix Outline Drawing for detail design.

Connector Part No.: **STM-MSAK24025P40M**

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (2)



Note (1)

- (a) 95% RH Max. ($T_a \leq 40^\circ\text{C}$).
- (b) Wet-bulb temperature should be 39°C Max. ($T_a \leq 40^\circ\text{C}$).
- (c) No condensation.

Note (2) The temperature of panel surface should be 0°C min. and 60°C max.

3.2 ELECTRICAL ABSOLUTE RATINGS

3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4	V	(1)
Logic Input Voltage	V _{IN}	-0.3	+3.6	V	(1)
Converter Input Voltage	LED_VCCS	-0.3	26	V	(1)
Converter Control Signal Voltage	LED_PWM,	-0.3	+3.6	V	(1)
Converter Control Signal Voltage	LED_EN	-0.3	+3.6	V	(1)

Note (1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “ELECTRICAL CHARACTERISTICS”.

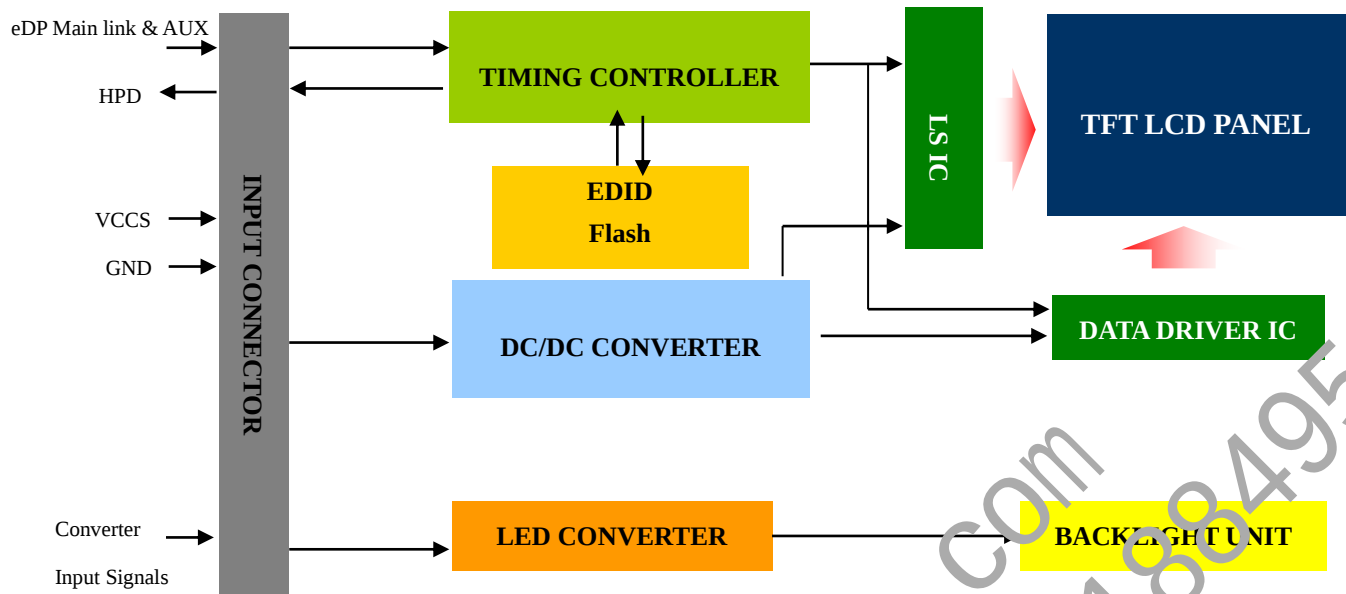
4. ELECTRICAL SPECIFICATIONS

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4.1 FUNCTION BLOCK DIAGRAM



4.2 INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Note
1	I2C_SCL	I2C Serial Clock Signal	I2C SCL for APOL VIH 1.08V VIL 0.54V
2	H_GND	High Speed Ground	
3	ML3-	Complement Signal-Lane 3	
4	ML3+	True Signal-Main Lane 3	
5	H_GND	High Speed Ground	
6	ML2-	Complement Signal-Lane 2	
7	ML2+	True Signal-Main Lane 2	
8	H_GND	High Speed Ground	
9	ML1-	Complement Signal-Lane 1	
10	ML1+	True Signal-Main Lane 1	
11	H_GND	High Speed Ground	
12	ML0-	Complement Signal-Lane 0	
13	ML0+	True Signal-Main Lane 0	
14	H_GND	High Speed Ground	
15	AUX+	True Signal-Auxiliary Channel	

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16	AUX-	Complement Signal-Auxiliary Channel	
17	H_GND	High Speed Ground	
18	VCCS	Power Supply +3.3V (typical)	
19	VCCS	Power Supply +3.3V (typical)	
20	VCCS	Power Supply +3.3V (typical)	
21	VCCS	Power Supply +3.3V (typical)	
22	BIST	Built-In Self Test (active high)	Default low VIH 0.81 V VIL 0.72V
23	ABOT	ABOT enable (Disable@high(default),enable@low)	(Disable@high(default),enable@low) VIH 0.81 V VIL 0.72V
24	GND	Ground	
25	GND	Ground	
26	GND	Ground	
27	HPD	Hot Plug Detect	Output pin, >2.5V
28	BL_GND	BL Ground	
29	BL_GND	BL Ground	
30	BL_GND	BL Ground	
31	APOLC	APOL control signal	Output pin, $\geq 1.8V$
32	LED_EN	BL Enable Signal of LED Converter	VIH 1.2V VIL 0.7V
33	LED_PWM	PWM Dimming Control Signal of LED Converter	VIH 1.35V VIL 0.72V
34	I2C_SDA	I2C Serial Data Signal	I2C SDA for APOL VIH 1.08V VIL 0.54V
35	HW	MOS preventing I2C overwrite*	For CSOT Use (customer must NC)
36	LED_VCCS	LED Power Supply	
37	LED_VCCS	LED Power Supply	
38	LED_VCCS	LED Power Supply	
39	LED_VCCS	LED Power Supply	

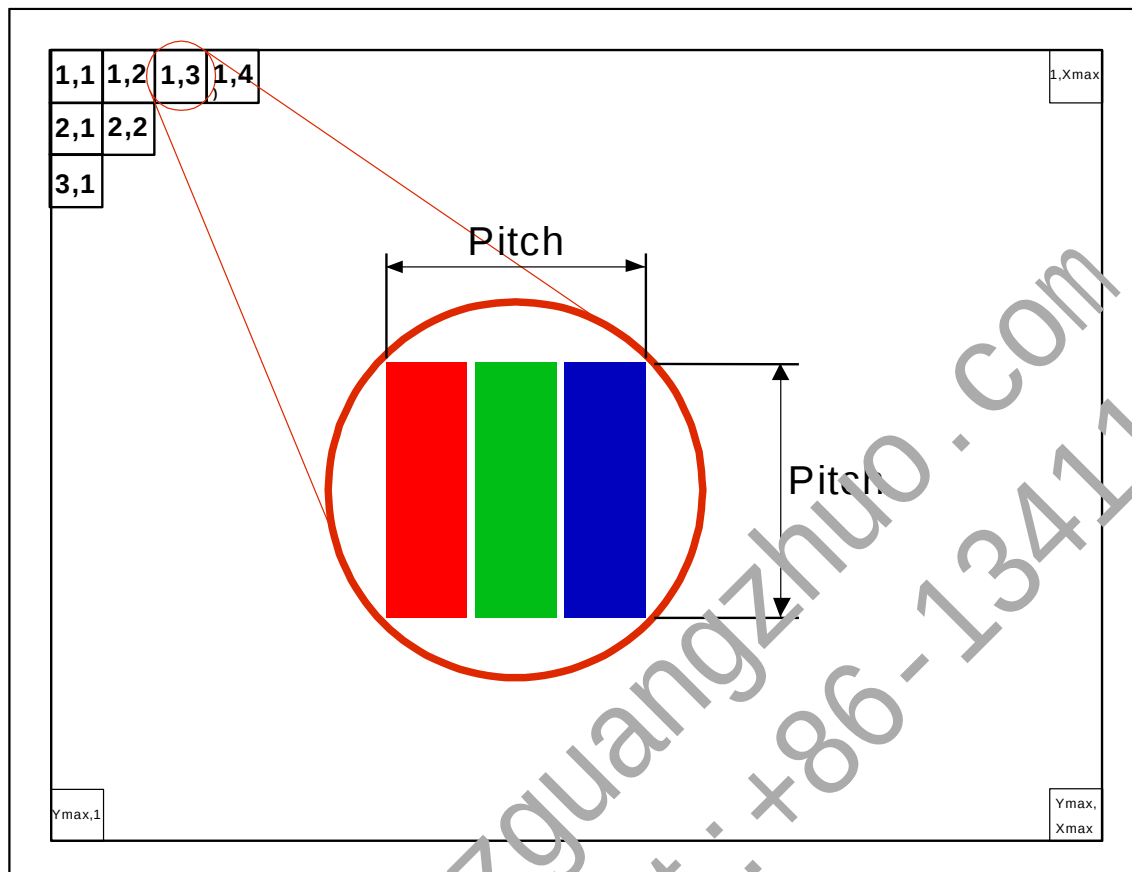
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40	OD_EN	Over Drive enable Pull high(1): OD off; Pull low(0): OD on	(Disable@high(default) VIH 0.81 V VIL 0.72V
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Note (1) The pixel is shown in the following figure.

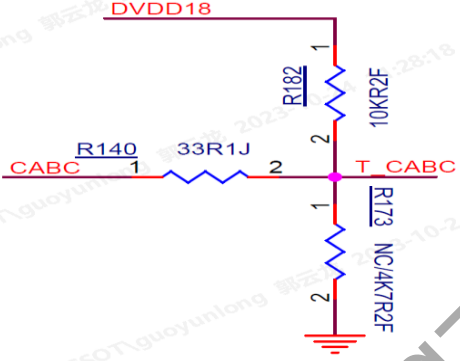
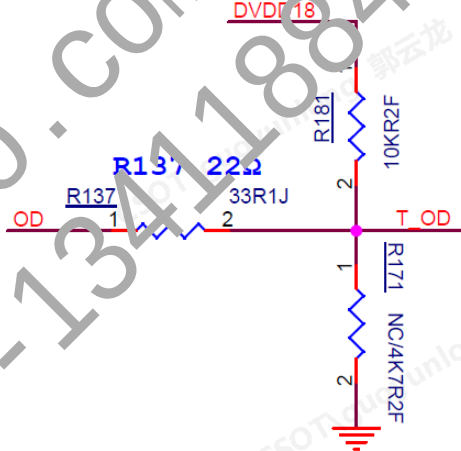
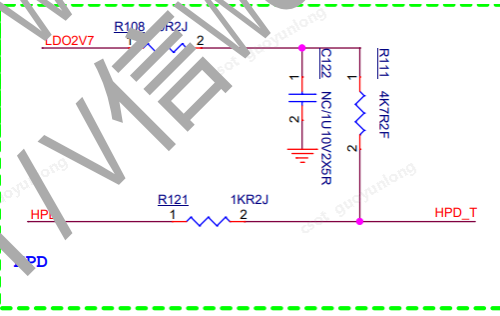
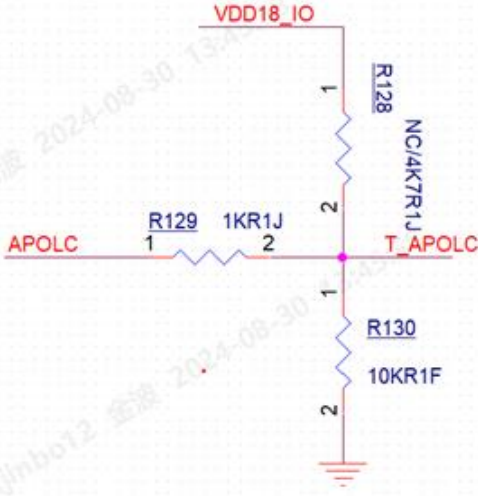


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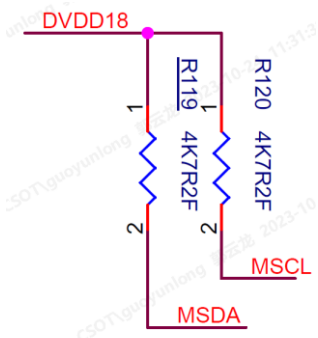
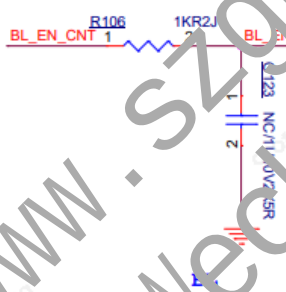
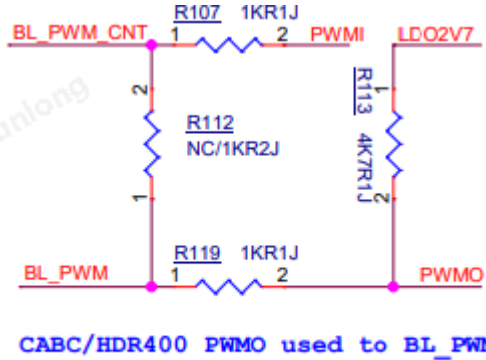
Note2 : function pin feature

CSOT/MNG007DA5-3		
Pin No.	23	40
Symbol	ABOT	OD_EN
I/O	Input	Input
Input status	High	Disable
	Floating	Disable
	Low	Enable
Circuit		
Pin No.	27	31
Symbol	HPD	APOLC
I/O	Output	Output
Circuit		

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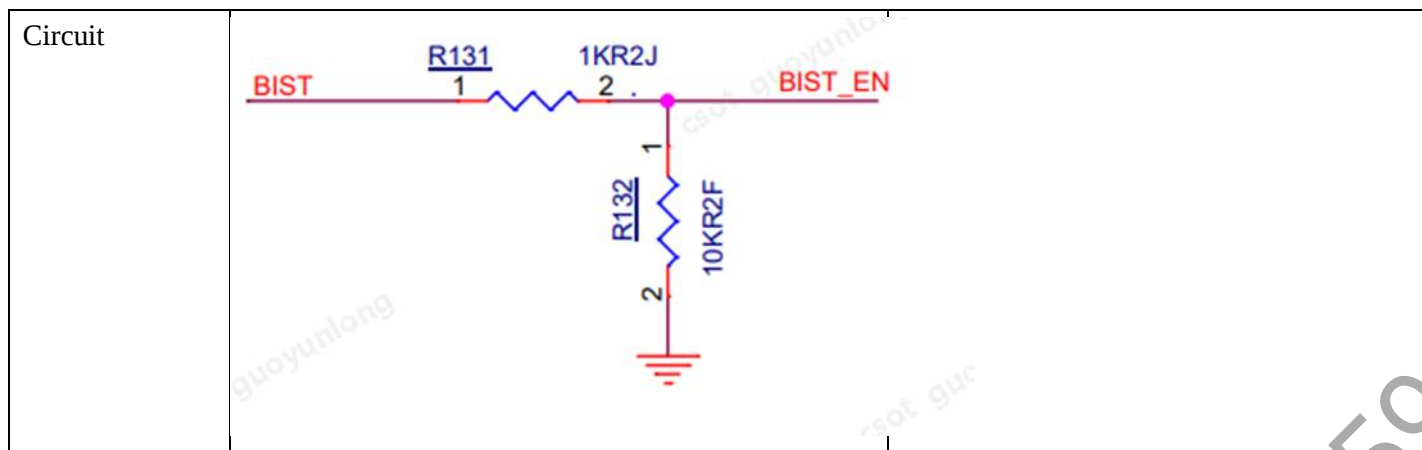
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Pin No.	1/34	
Symbol	I2C	
I/O	Input/Output	
Circuit		
Pin No.	32	33
Symbol	LED_EN	LED_PWM
I/O	Input	Input
Input status	High	Enable
	Floating	Disable
	Low	Disable
Circuit		 CABC/HDR400 PWM0 used to BL_PWM
Pin No.	22	
Symbol	BIS1	
I/O	Input	
Input status	High	Enable
	Floating	Disable
	Low	Disable

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4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.5	V	(1)
BIST Control Level		BIST on	0.81	0.5	3.6	V	(1)
		BIST off	0	-	0.5	V	(1)
I2C(SDA/SCL)		on	1.65	1.8	2.2	V	(1)
		off	0	-	0.5	V	(1)
OD(Over Driver)		on	1.65	1.8	2.2	V	(1)
		off	0	-	0.5	V	(1)
Ripple Voltage		V _{RP}	-	-	100	mV	(1)
Inrush Current		I _{RUSH}	-	-	1.5	A	(1)(2)
Power Supply Current	Mosaic	I _{LCD}	-	515	545	mA	(3)
Power consumption	Mosaic	P _{LCD}	-	1.7	1.8	W	(3)
Power Supply Current	Heavy loading	I _{LCD}	-	1.1	1300	mA	(4)
Power consumption	Heavy loading	P _{LCD}	-	3.63	4.29	W	(4)

Note (1) The ambient temperature is $T_a = 25 \pm 2^\circ\text{C}$.

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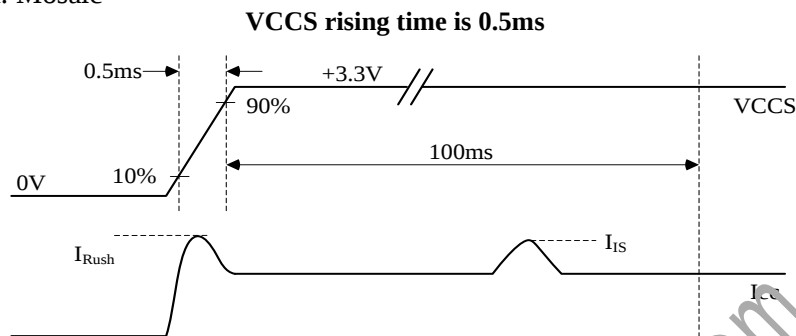
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Note (2) I_{RUSH} : the maximum current when VCCS is rising

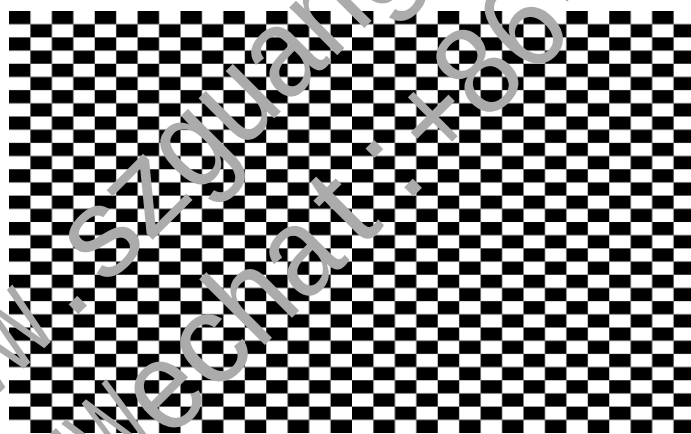
I_{IS} : the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure.

Test pattern: Mosaic



Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, $T_a = 25 \pm 2^\circ\text{C}$, DC Current and $f_v = 240\text{ Hz}$, whereas a power dissipation check pattern below is displayed.



Note (4) The specified power supply current is under the conditions at VCCS = 3.3 V, $T_a = 25 \pm 2^\circ\text{C}$, DC Current and $f_v = 240\text{ Hz}$, whereas a power dissipation Heavy loading pattern below is displayed.



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LED CONVERTER SPECIFICATION

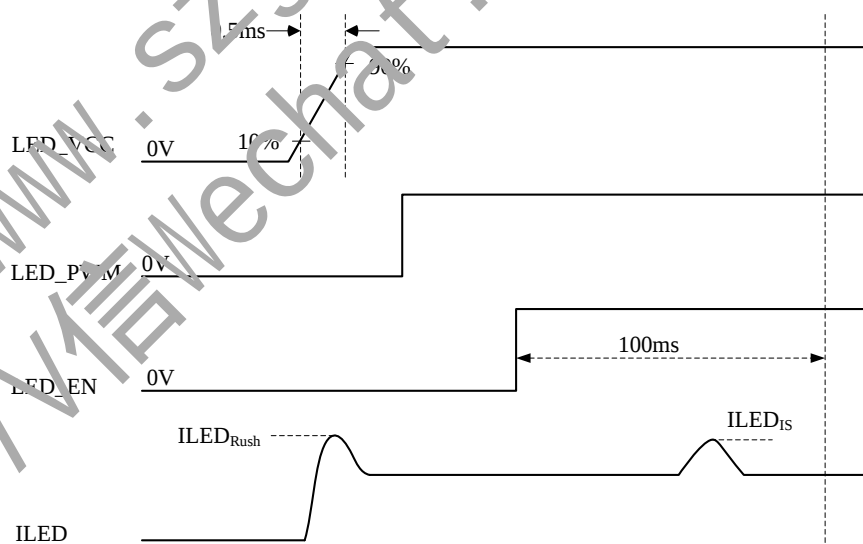
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input power supply voltage		LED_Vccs	5.0	12.0	21.0	V	
Converter Inrush Current		I _{LED_RUSH}	-	-	1.5	A	(1)
EN Control Level	Backlight On		1.5	-	3.6	V	
	Backlight Off		0	-	0.5	V	
PWM Control Level	PWM High Level		1.5	-	3.6	V	
	PWM Low Level		0	-	0.5	V	
PWM Control Duty Ratio			1	-	100	%	
PWM Control Permissive Ripple Voltage		V _{PWM_pp}	-	-	100	mV	
PWM Control Frequency		f _{PWM}	200		2000	Hz	
LED Power consumption		P _L	-	-	4.10	W	(2)
LED Power Current	LED_VCCS =Typ.	I _L -	-		354	mA	(3)

Note (1) I_{LED_RUSH}: the maximum current when LED_VCCS is rising,

I_{LED_IS}: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 °C, f_{PWM} = 200 Hz, Duty=100%.

LED rising time is 0.5ms



Note(2) $P_L = I_L \times V_L$ (With LED converter transfer efficiency);

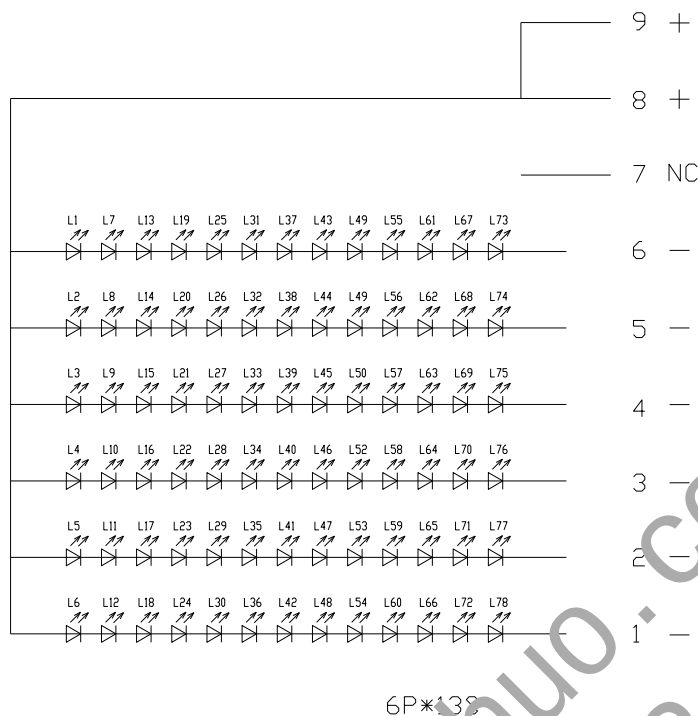
Note (3) The specified LED power supply current is under the conditions at “LED_VCCS = Typ.”, Ta = 25 ± 2 °C, f_{PWM} = 200 Hz, Duty=100%.

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4.4.1 BACKLIGHT UNIT



Ta = 25 ± 2 °C

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage (whole backlight)	VL	-	-	36.79	V	(1)(2)
LED Light Bar Power Supply Current (whole backlight)	IL	-	99	-	mA	(Duty100%)
LED Light Bar Power Supply Voltage (per LED string)	VL	-	-	2.83	V	(3)
LED Light Bar Power Supply Current (per LED string)	IL	-	16.5	-	mA	(4)
Power Consumption (whole backlight)	PL	-	-	3.65	W	(5)
LED Life Time	L _{BL}	15000	-	-	Hrs	(6)

Note (1) LED current is measured by utilizing a high frequency current meter :

Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light bar.

Note (3) VL(per LED string) = VL(whole backlight) / Series quantity

Note (4) IL(per LED string) = IL(whole backlight) / Parallel quantity

Note (5) PL = IL(whole backlight) × VL(whole backlight) (Without LED converter transfer efficiency)

Note (6) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ± 2 °C and IL = 20 mA(Per EA) until the brightness becomes ≦ 50% of its original value.

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4.4 INPUT SIGNAL TIMING SPECIFICATIONS

4.5.1 eDP AUX Channel Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Unit Interval for AUX channel	UI _{AUX}	0.4	-	0.6	μS	
Peak-to-peak voltage at TP1	V _{AUX-DIFF-pp}	0.18	0.2	1.38	V	
AUX DC Common mode Voltage	V _{AUX-DC-CM}	0	-	1.2	V	
AUX Short current limit	I _{AUX_SHORT}	-	-	90	mA	
AUX CH termination DC resistor	R _{AUX_TERM}	80	90	100	Ω	Differential input
AUX AC coupling capacitor	C _{AUX}	75	-	200	nF	
Number of pre-charge pulses	Pre-charge pulses	10	-	16		

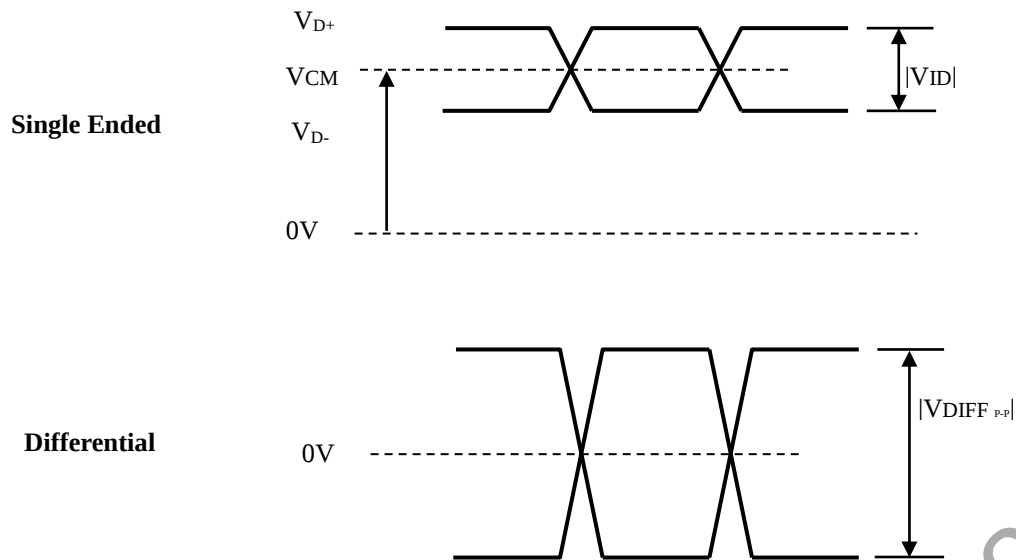
4.5.2 eDP Main Link Receiver Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Link clock down spreading	Down_Spread_Amplitude	0	-	0.5	%	
Differential Peak-to-peak Input Voltage at Rx package pins	V _{RX-DIFFp-p}	100	-	1320	mV	
Differential termination resistance	R _{RX-TERM}	80	90	100	Ω	
RX short circuit Current Limit	I _{RX-SHORT}	-	-	50	mA	
Lane Intra-pair Skew at RX package pins	T _{RX-SKEW-INTRA-PAIR} (High-Bit-Rate)	-	-	50	ps	

4.5.3 eDP AUX Channel Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Hot plug Detect	V _{HPD}	2.5	-	2.8	V	

Note (1) Display port interface related AC coupled signals are following VESA Display Port Standard V1.4b.



4.5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

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Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0

Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specification is showed as the following table and timing diagram.

Signal	Item	Symbol	Min.		Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	-		777.322	-	MHz	-

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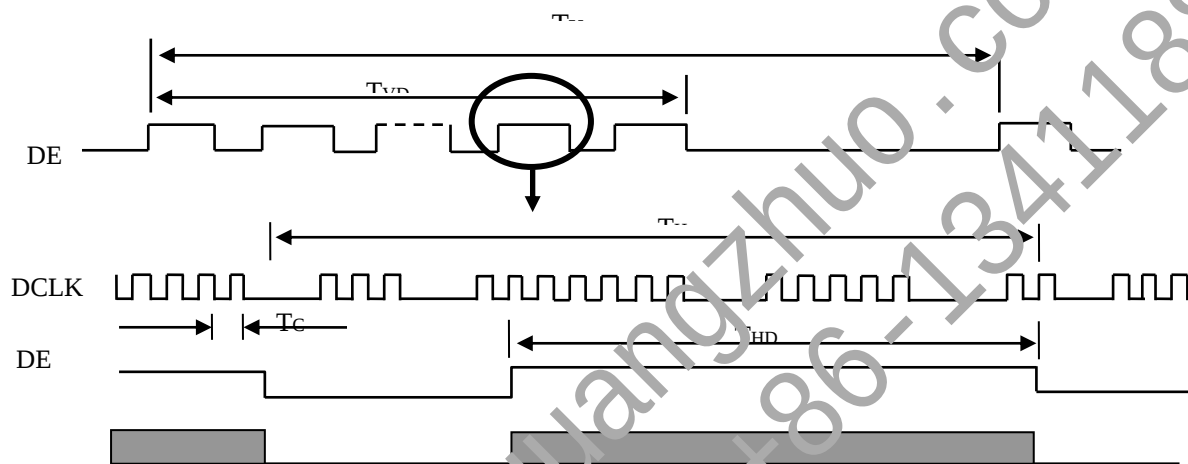
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DE	Vertical Total Time	TV	-		1732	-	TH	-
	Vertical Active Display Period	TVD	1600		1600	1600	TH	-
	Vertical Active Blanking Period	TVB	-		132	-	TH	-
	Horizontal Total Time	TH	-		2720	-	Tc	-
	Horizontal Active Display Period	THD	2560		2560	2560	Tc	-
	Horizontal Active Blanking Period	THB	-		160	-	Tc	-

Note (1) Display timing signal should be contained and transferred by Display Port Main Link stream data packing described in VESA Display Port Standard V1.4b.

INPUT SIGNAL TIMING DIAGRAM

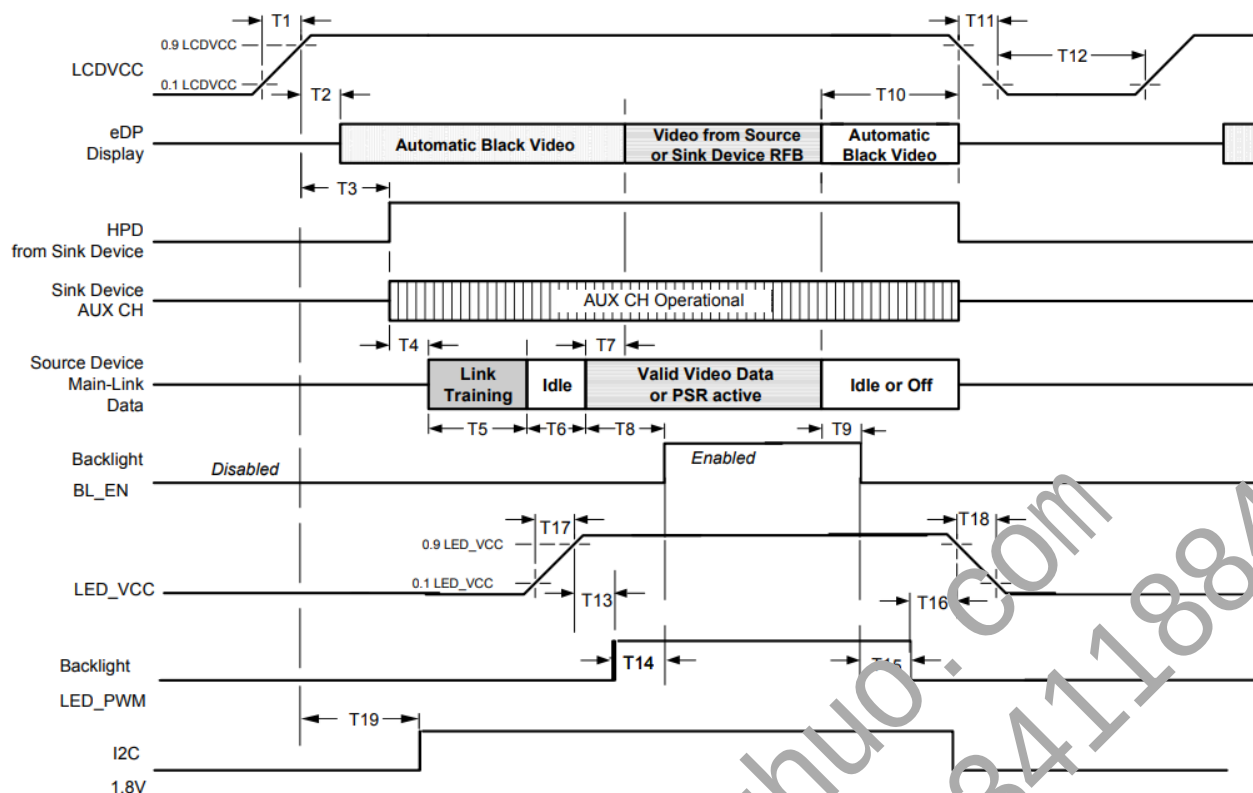


4.6 POWER ON/OFF SEQUENCE

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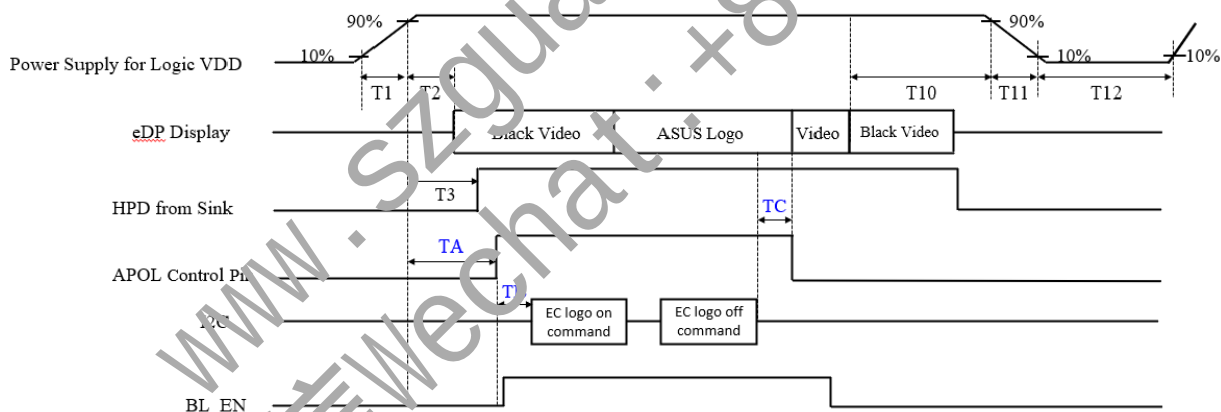
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APOL version: V3.0

(1) Power on



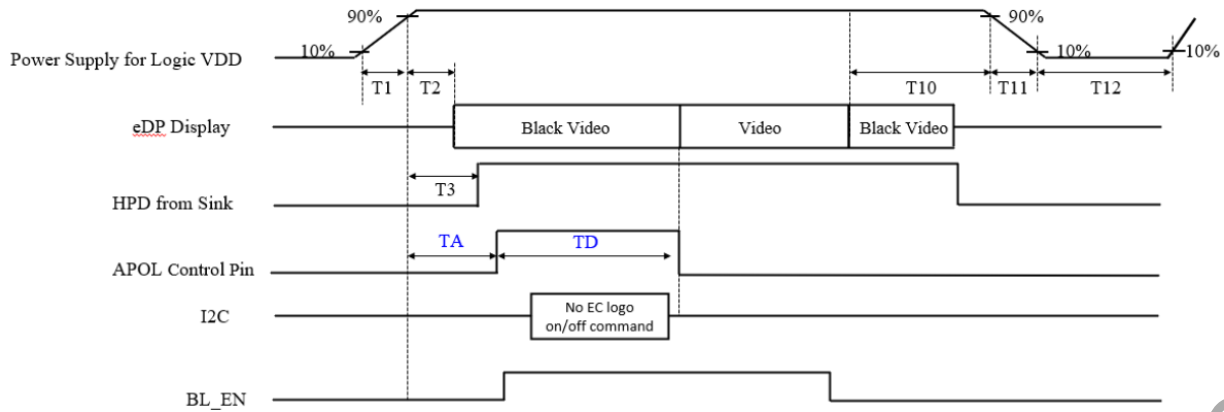
Other mode:

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(2) Others mode



Symbol	Description	Min	Typ.	Max	Unit	Note
T1	Power rail rise time, 10% to 90%	0.5		10	ms	
T2	Delay from LCD,VCCS to eDP Display	0		80	ms	
T3	Delay from LCD,VCCS to HPD high	0		80	ms	
T4	Delay from Sink AUX to link training initialization	-		-	ms	
T5	Link training duration	-		-	ms	
T6	Link idle	-		-	ms	
T7	Delay from valid video data from Source to video on display	0		50	ms	
T8	Delay from valid video data from Source to backlight on	-		-	ms	
T9	Delay from backlight off to end of valid video data	0		T10-50	ms	
T10	Delay from end of valid video data from Source to power off	50		500	ms	
T11	VCCS power rail fall time, 90% to 10%	-		10	ms	(1)
T12	VCCS Power off time	500		-	ms	
T13	Delay from VCC to PWM	0		-	ms	
T14	Delay from PWM to LED ENABLE	0		-	ms	
T15	Delay from LED ENABLE to PWM Disable	0		-	ms	
T16	Delay from PWM Disable to VBL 90%	0		-	ms	
T17	Delay from VBL 10% to VBL 90%	0		-	ms	
T18	VBL power rail fall time, 90% to 10%	0		-	ms	

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TA	Delay from LCD,VCCS to APOL on	0	-	100	ms	
TB	Delay from APOL on to EC logo on command	0	-	25	ms	
TC	Delay from EC logo off command to APOL off	0	-	1	frame	
TD	APOL keep on timing	0	-	50	ms	
T19	VDD 3.3 to I2C 1.8V	-	-	20	ms	

Note (1) Please follow the power on/off sequence described above. Otherwise, the LCD module might abnormal display or be damaged.

Note (2) Please avoid floating state of interface signal at invalid period. When the interface signal is invalid, be sure to pull down the power supply of LCD VCCS to 0 V.

Note (3) The backlight must be turned on after the power supply for the logic and the interface signal is valid. The backlight must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Please follow the LED backlight power sequence as above. If the customer could not follow, it might cause backlight flash issue during display ON/OFF or damage the LED backlight controller

5. Optical characteristics

Ta=25°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing angle range	Left/Right	CR>10	80	-	89	Deg.	(1), (3), (4), (6)
	Upper/Lower		80	-	89		
Contrast ratio	CR		960	1200	-	-	(2), (4), (6)
Response time	tr+td	$\theta=0 \text{ deg.}$	-	9	10	ms	(5)
	GTG AVE.(w/o O.D.)		-	7	-	ms	
	GTG AVE.(w/ O.D.)		-	-	3.8	ms	
Chromaticity of white	x	$\theta=0 \text{ deg.}$	Typ. -0.030	0.313	Typ. +0.030	-	(2), (6) Normal operation
	y			0.329		-	
Chromaticity of red	x			0.640		-	
	y			0.330		-	
Chromaticity of green	x			0.300		-	
	y			0.600		-	
Chromaticity of blue	x			0.150		-	
	y			0.060		-	
sRGB Coverage	%		95%	100%	-	sRGB	
Luminance of	Y _{LI}	@5 point	340	400	-	cd/m ²	(7)

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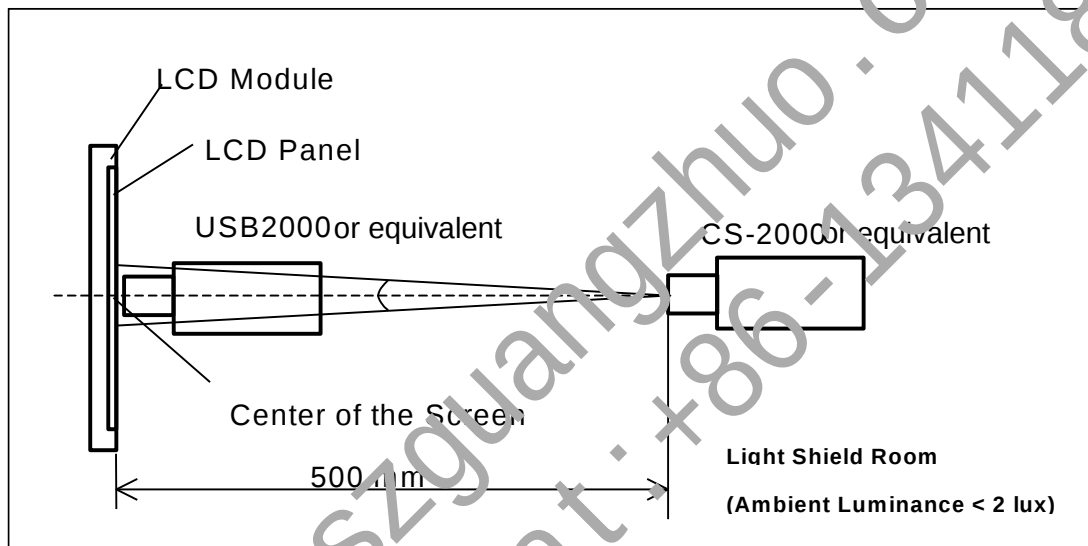
gamma	--	--	2.0	2.2	2.4	--	--
White uniformity	δ_w	$\theta=0$ deg.	-	-	1.5	--	(8)
Eye safe	--	--	-				
CCT	--	--	-	-	-	K	(2), (8)

※The measurement shall be taken 5 minutes after lighting the LCM at the following rating.

※The optical characteristics shall be measured in a dark room or equivalent.

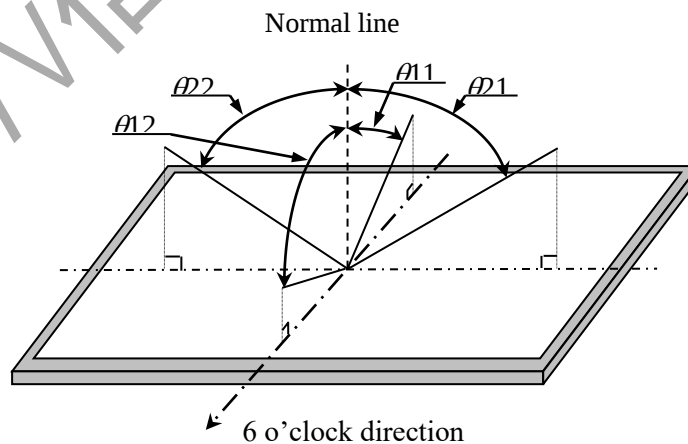
Note (1) Measurement of viewing angle range

Note (2) Measurement of luminance and Chromaticity and Contrast.



Measurement of Contrast, Luminance, Chromaticity, White variation, Crosstalk and Color temperature variation

Note (3) Definitions of viewing angle range:



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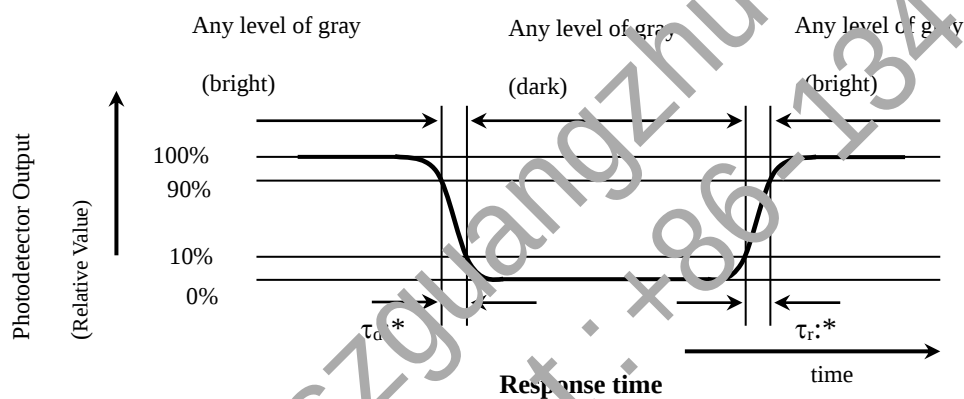
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Viewing angle

Note (4) Definition of contrast ratio:

The contrast ratio is defined as the following.

$$\text{Contrast Ratio} = \frac{\text{Luminance(Brightness) with all pixels white}}{\text{Luminance(Brightness) with all pixels Black}}$$



		Start Gray								
		0	31	63	95	127	159	191	223	255
End Gray	0									
	31									
	63									
	95									
	127									
	159									
	191									
	223									
	255									

Response time

Note (5) Definition of response time:

The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white" .

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$$GTG_{ave} = \frac{t_{0-31} + t_{31-0} + t_{0-63} + t_{63-0} + \dots + t_{223-255} + t_{255-223}}{8 * 9}$$

Note (6) This shall be measured at center of the screen.

Note (7) The Luminance of White is the average of 5 points measurements (4,5,7,9,10) showing in the Fig.9-5.

Note (8) Definition of white uniformity: White uniformity of 13 points is defined as the following with 13 measurements(1~13).

$$\delta_{W2} = \frac{\text{Maximum Luminance of 13 Points(Brightness)}}{\text{Minimum Luminance of 13 Points(Brightness)}}$$

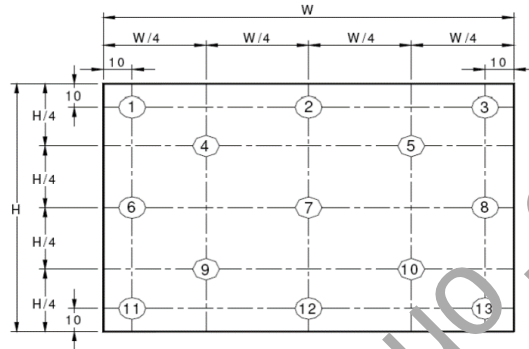


Fig 9-5

6. Reliability Test Items

No	Test Item	Conditions
1	ESD	Non OP ESD a. Surface discharge Air discharged +/- 15kV Criteria C Contact discharged +/-8kV Criteria C b. Golden Finger/ Connector pin Contact discharged +/- 2kV Criteria OP ESD Air discharged +/- 15kV Criteria B Contact discharged +/-8kV Criteria B
2	LS	a. pattern: 8*4 chess board temperature: 25° 10s/5mins/10mins/20mins/30mins/1hr @ 5s recovery with nude eye 6hrs @ 10mins recovery with nude eye -->recovery by G127, and checked by G127 b. pattern:QTR test pattern temperature:40°, humidity: 85% 24hrs @ white(G255) pattern 1hrs recovery(under 25°) with nude eye

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		-->recovery by G255, and checked by G127 and G255
3	High temperature storage test	60°C, 240Hrs
4	Low temperature storage test	-20°C, 240Hrs
5	Low temperature operation test	0°C, 240hrs
6	High temperature operation test	50°C, 240Hrs
7	High temperature & high humidity operation test	40°C, 90% RH, 240Hrs
8	Thermal shock test	-20°C/30min、60°C/30min、100cycles
9	Vibration	1.5G/10-500Hz, Sine wave, 30min/cycle, 1cycle for each X,Y,Z
10	Shock	220G, 2ms, half sine wave, 1 time for each direction of ±X,±Y,±Z

[Result Evaluation Criteria] Under the display quality test condition with normal operation state.

Do not change these condition as such changes may affect practical display function.

[Normal operation state] temperature : + 15°C~ + 35°C · Humidity : 45~75% · Atmospheric pressure : 86~106kPa

7. Display Quality

The display quality of the color TFT-LCD Module shall be in compliance with the Incoming Inspection Standard.

8. Packaging Condition

8.1 Packing Specifications

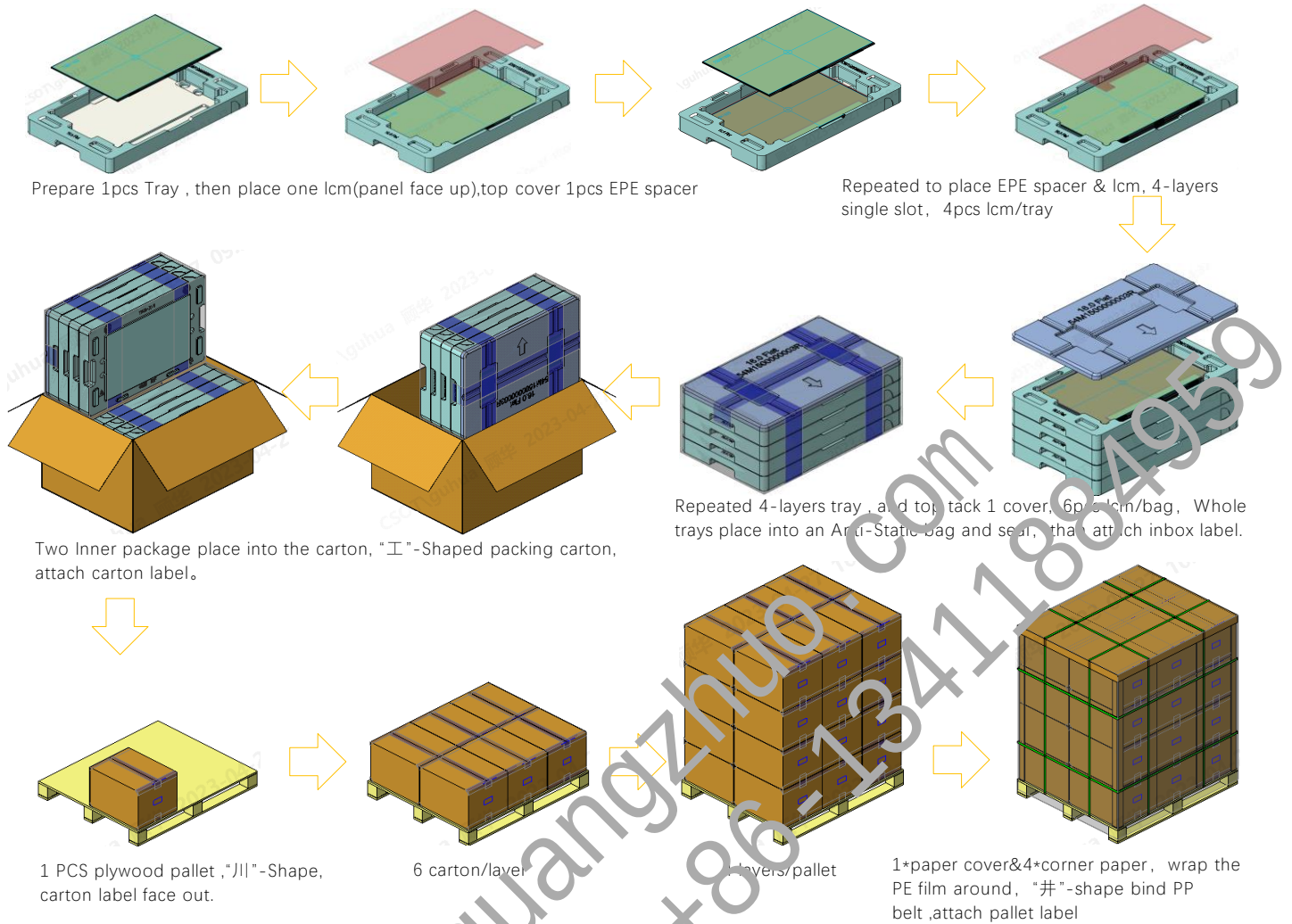
Item	Specification	Remark
Carton(Box) Packing	32 PCS/Carton(Box)	4 PCS/Tray, (4+1) *2
Carton(Box) Packing Size	490mm(L)x392mm(W)x310mm(H)	Length x Width x Height
Pallet Packing	24 Carton(Box)/Pallet	6*4
Pallet Packing Size	1200mm(L)x1000mm(W)x1360mm(H)	Length x Width x Height

8.2 Packing Method

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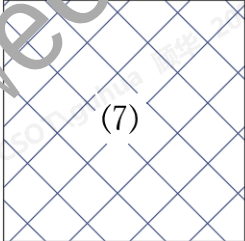
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8.3 Label

Module label

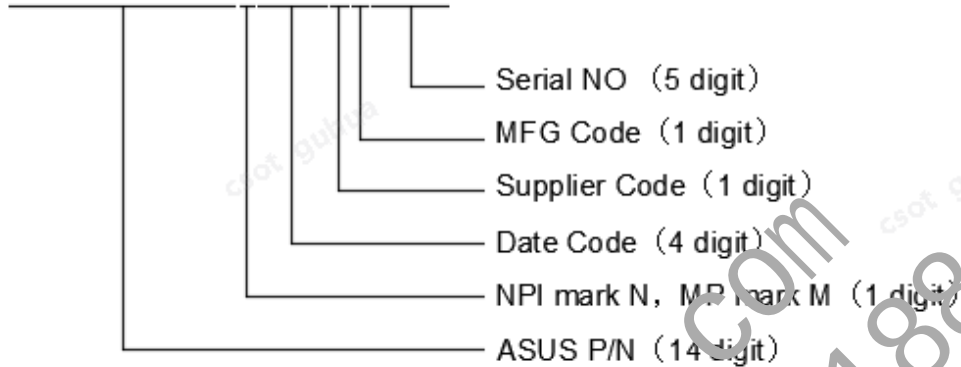
(1)  华星光电 CSOT (2)  US (3) RoHS (4) MADE IN CHINA	(7) 	MNG007DA5-3 (5) 18010-16060700N24 9BCB00001 (6)
---	--	--

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- (1) CSOT logo: Stands for panel manufactured by CSOT
- (2) UL logo
- (3) Green product mark: RoHS, stands for the product accord to RoHS standard
- (4) Production location: MADE IN CHINA, CHINA stands for production location
- (5) CSOT model name: MNG007DA5-3
- (6) Serial ID: 18010-16060700N249BCB00001



- (7) Serial ID DM code: same content as (6)

Serial ID includes the information as below

- a. ASUS P/N: 18010-16060700
- b. Stage Code: N,NPI stage mark N,MP stage mark M
- c. Date Code: 24,Year: last two code of the year,Month: 1~9,A,B,C,B,day: 1~Z,Except I/O/Q/U
- d. Supplier: C,CSOT
- e. MFG Code: B,Wuhan,A/B/C....
- f. Serial NO : 00001, 0~9

Inbox label

RoHS			
Model Name: MNG007DA5-3		Ver.: ##	
Part No.: 11NG007DA53001		Qty.: 16	
Customer No.: 18010-16060700		WT: ##.### KG	
			
Inbox Id: Z ₁ Z ₂ Z ₃ Z ₄ Z ₅ Z ₆ Z ₇ Z ₈ Z ₉ Z ₁₀ Z ₁₁ Z ₁₂ Z ₁₃ Z ₁₄ Z ₁₅ Z ₁₆ Z ₁₇ Z ₁₈ Z ₁₉ Z ₂₀			
Note: NPI		Made In China	

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Pallet label

ASUSTEK	华硕电脑有限公司	Ver.: ##
厂商	华星光电技术有限公司	
厂商料号	 MNG007DA5-3 MNG007DA5-3	
华硕料号	 18010-16060700 18010-16060700	
栈板ID	 ZZ-ZZ-ZZ-ZZ-ZZ-ZZ-ZZ-ZZ-ZZ-ZZ	
栈板总数量	 768 768	 24 24
最旧制造周别 (D/C)	 2404 2404	
原产地	 China China	
交货日期	 240125 240125	

This LCD Module is compliant with RoHS Directive.

- a) Be sure to turn off the power supply when inserting or disconnecting the cable .Please insert for too much stress not to join a connector in the case of insertion of a connector.
- b) Be sure to design the cabinet so that the Module can be installed without any extra stress such as warp or twist.
- c) Since the front polarizer is easily damaged, pay attention not to scratch it.
- d) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- e) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- f) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface. Handle with care.

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- g) Since CMOS LSI is used in this Module, take care of static electricity and injure the human earth when handling. Observe all other precautionary requirements in handling components.
- h) This Open-cell has its circuitry PCBs on the side and should be handled carefully in order not to be stressed.
- i) Laminate film is attached to the Module surface to prevent it from being scratched. Peel the laminate film off slowly just before the use with strict attention to electrostatic charges. Ionized air shall be blown over during the action. Blow off the 'dust' on the polarizer by using an ionized nitrogen gun, etc. Working under the following environments is desirable.
 - All workers wear conductive shoes, conductive clothes, conductive fingerstalls and grounding belts without fail.
 - Use Ionized blower for electrostatic removal, and peel of the laminate film with a constant speed. (Peeling of it at over 2 seconds)
- j) The polarizer surface on the panel is treated with Anti Glare . In case of attaching protective board over the LCD, be careful about the optical interface fringe etc. which degrades display quality.
- k) Do not expose the LCD Module to a direct sunlight, for a long period of time to protect the Module from the ultra violet ray.
- l) When handling LCD Modules and assembling them into cabinets, please be noted that long-term storage in the environment of oxidization or deoxidization gas and the use of such materials as reagent, solvent, adhesive, resin, etc. which generate these gasses, may cause corrosion and discoloration of the Modules.
- m) Liquid crystal contained in the panel may leak if the LCD is broken. Rinse it as soon as possible if it gets inside your eye or mouth by mistake.
- n) Disassembling the Module can cause permanent damage and should be strictly avoided.(Except for protection film of the panel.)
- o) Be careful when using it for long time with fixed pattern display as it may cause afterimage.(Please use a screen saver etc., in order to avoid an afterimage.)
- p) If a minute particle enters in the Module and adheres to an optical material, it may cause display non-uniformity issue, etc. Therefore, fine-pitch filters have to be installed to cooling and inhalation hole if you intend to install a fan.
- q) Epoxy resin (amine series curing agent), silicone adhesive material (dealcoholization series and oxime series), tray forming agent (azl compound) etc, in the cabinet or the packing materials may induce abnormal display with polarizer film deterioration regardless of contact or noncontact to polarizer film.Be sure to confirm the component of them.
- r) Do not use polychloroprene. If you use it, there is some possibility of generating Cl₂ gas that influences the reliability of the connection between LCD panel and driver IC.
- s) Do not put a laminate film on LCD Module, after peeling of the original one. If you put on it, it may cause discoloration or spots because of the occurrence of air gaps between the polarizer and the film.
- t) Ground module bezel to stabilize against EMI and external noise.

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Appendix. EDID DATA STRUCTURE:

00	EDID Header	"00h" fixed	00
01		"FFh" fixed	FF
02		"FFh" fixed	FF
03		"FFh" fixed	FF
04		"FFh" fixed	FF
05		"FFh" fixed	FF
06		"FFh" fixed	FF
07		"00h" fixed	00
08	ID Manufacturer Name	08h -> "30h" fixed	0E
09		09h -> "AEh" fixed (30AEh) LEN	77
0A	ID Product Code	PID	56
0B			16
0C	ID Serial Number (32-bit serial number)	Basically "00h"	00
0D		Basically "00h"	00
0E		Basically "00h"	00
0F		Basically "00h"	00
10	Manufacture week (1-53) & Model year Flag (FFh)	Panel EDID: "00h" or Manufacture week	00
11	Manufacture year (year -1990) or Model year	Manufacture year	22

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12	EDID Structure version		01
13	EDID Revision		04
14	Video Input Definition		A5
15	H screen size (cm) or Aspect Ratio	H screen size (cm)	22
16	V screen size (cm) or Aspect Ratio	V screen size (cm)	16
17	Display gamma (gamma x 100)-100		78
18	Feature support(DPMS)	Bit 0" must be set to "1", to indicate that the display supports continuous frequency	07
19	Red/Green Low Bits	Basically enter the same value as CAS.	EE
1A	Blue/White Low Bits		95
1B	Red x		A3
1C	Red y		54
1D	Green x		4C
1E	Green y		99
1F	Blue x		26
20	Blue y		0F
21	White x		50

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22	White y		54
23	Established Timing 1	"00h" fixed	00
24	Established Timing 2	"00h" fixed	00
25	Manufacturer's Reserved Timings	"00h" fixed	00
26	Standard Timing Identification	"01h" fixed	01
27	#1	"01h" fixed	01
28	Standard Timing Identification	"01h" fixed	01
29	#2	"01h" fixed	01
2A	Standard Timing Identification	"01h" fixed	01
2B	#3	"01h" fixed	01
2C	Standard Timing Identification	"01h" fixed	01
2D	#4	"01h" fixed	01
2E	Standard Timing Identification	"01h" fixed	01
2F	#5	"01h" fixed	01
30	Standard Timing Identification	"01h" fixed	01
31	#6	"01h" fixed	01
32	Standard Timing Identification	"01h" fixed	01
33	#7	"01h" fixed	01
34	Standard Timing Identification	"01h" fixed	01
35	#8	"01h" fixed	01
36	Pixel Clock/10,000 (LSB)	BIOS EDID: Preferred(Typical)	6B

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37	Pixel Clock/10,000 (MSB) /	Timing Mode	6E
38	Horizontal Active		00
39	Horizontal Blanking		A0
3A	Horizontal Active : Horizontal Blanking		A0
3B	Vertical Active		40
3C	Vertical Blanking		24
3D	Vertical Active : Vertical Blanking		60
3E	Horizontal Sync. Offset		30
3F	Horizontal Sync Pulse Width		20
40	Vertical Sync Offset : Sync Width		66
41	Horizontal Vertical Sync Offset/Width		00
42	Horizontal Image Size		58
43	Vertical Image Size		D7
44	Horizontal & Vertical Image Size		10
45	Horizontal Border		00
46	Vertical Border		00
47	Signal Interface Type		18

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48	Reserved for definition	48h -> "00h" fixed	00
49	Reserved for definition	49h -> "00h" fixed	00
4A	Reserved for definition	4Ah -> "00h" fixed	00
4B	ASCII String	4Bh -> "FDh" fixed	FD
4C	Vertical Rate Offsets	4Ch -> "00h" fixed	
		52h -> "01h" fixed	0C
		53h -> "0Ah" fixed	
4D	Minimum Vertical Rate	54h -> "20h" fixed	20
4E	Maximum Vertical Rate:	55h -> "20h" fixed	A5
4F	Minimum Horizontal Rate:	56h -> "20h" fixed	1F
50	Maximum Horizontal Rate	57h -> "20h" fixed	1F
51	Maximum Pixel Clock,Binary coded clock rate in MHz ÷ 10,	58h -> "20h" fixed	
		59h -> "20h" fixed	4E
52	Video Timing Support, vendor Flags.01h,Range Limits Only	4D-51 need confirm with LCD	01
53	Line Feed (if Byte 10 = 00h or 01h)		0A
54	Space (if Byte 10 = 00h or 01h)		20
55	Space (if Byte 10 = 00h or 01h)		20
56	Space (if Byte 10 = 00h or 01h)		20
57	Space (if Byte 10 = 00h or 01h)		20
58	Space (if Byte 10 = 00h or 01h)		20
59	Space (if Byte 10 = 00h or 01h)		20

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5A	ASUS customized data block	5Ah -> "00h" fixed	00
5B		5Bh -> "00h" fixed	00
5C		5Ch -> "00h" fixed	00
5D		5Dh -> "FEh" fixed	FE
5E		5Eh -> "00h" fixed	00
5F		5Fh -> "4Ch" fixed	00
5F	ASUS customized flag	60h -> "45h" fixed	3D
60	data type	61h -> "4Eh" fixed	4C
61	APOL version	62h -> "4Fh" fixed	33
62	APOL sub version	63h -> "56h" fixed	33
63	ABOT version	64h -> "4Fh" fixed	31
64	ABOT sub version	65h -> "0Ah" fixed	31
65	Space	66h -> "20h" fixed	20
66	Space	67h -> "20h" fixed	20
67	Space	68h -> "20h" fixed	20
68	Space	69h -> "20h" fixed	20
69	Space	6Ah -> "20h" fixed	20
6A	Space	6Bh -> "20h" fixed	20
6B	Space		FF
6C	Indicates descriptor #3 is a display Descriptor	6Ch -> "00h" fixed	00
6D		6Dh -> "00h" fixed	00

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6E	Reserved	6Eh -> "00h" fixed	00
6F	Tag: ASCII String	6Fh -> "FEh" fixed	FC
70	Reserved	70h -> "00h" fixed	00
71	Manufacture name	71h -> "4Ch" fixed	4D
72		72h -> "4Fh" fixed	4E
73		73h -> "56h" fixed 71~73:	47
74		LEN	30
75		74h -> "Size	30
76		75h -> "Size	27
77		76h -> "Size	44
78		74~76: Size	41
79		77h -> "Resolution	35
7A		78h -> "Resolution	2D
7B		79h -> "Resolution	33
7C		7Ah -> "Resolution	0A
7D		7Bh -> "Resolution	20
7E		7Ch -> "Resolution	01
7F		7Dh -> "Resolution 77~7D:	06
		Resolution	

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80	EDID Extension Tags		70
81	Display ID version		20
82	section size		79
83	product Type identifier		02
84	extension count		00
85	block tag		21
86	block revision and other data		00
87	payload		1D
88	Horizontal Image Size		77
89			0D
8A	Vertical Image Size		6A
8B			08
8C	Horizontal Pixel Count	2560 horizontal pixels.	00
8D			0A
8E	Vertical Pixel Count	1600 vertical pixels.	40
8F			06
90	Feature Support Flags		80
91	Native Color Chromaticity (Red Chromaticity,	RED x=0.640, y=0.330	3D
92			8A
93			54
94	Native Color Chromaticity	GREEN x=0.300, y=0.600	CD

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	(Green Chromaticity)		
95			A4
96			99
97	Native Color Chromaticity (Blue Chromaticity)	BLUE x=0.150, y=0.060	66
98			62
99			0F
9A	Native Color Chromaticity (White Chromaticity)	WHITE x=0.313, y=0.329	02
9B			45
9C			54
9D	Native Maximum Luminance (Full Coverage)	300 cd/m2	40
9E			5E
9F	Native Maximum Luminance (10% Coverage)	300 cd/m2	40
A0			5E
A1	Native Minimum Luminance	0.25cd/m2	00
A2			44
A3	Native Color Depth and Display Device Technology		12
A4	Native Gamma EOTF	Gamma = 2.2	78
A5	block tag		22

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A6	block rev		00
A7	Payload		14
A8	Pixel Clock	777.3216	69
A9			DC
AA			B
AB	timing options		85
AC	H-Active	2560	FF
AD			09
AE	H-Blanking	160	9F
AF			00
B0	H-offset	48	2F
B1			00
B2	H-sync pulse width	32	1F
B3			00
B4	V-Active	1600	3F
B5			6
B6	V-Blanking	132	83
B7			0
B8	V-offset	3	05
B9			00
BA	V-sync pulse width	6	5
BB			00

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BC	Adaptive-Sync Data Block		2B
BD	Block revision = 0		00
BE	Number of Payload Bytes in block= 6 byte		0C
BF	FAVT and AVT Supported,Native panel range,successive frame duration Decrease met with in RR Range.		27
C0	00h = Flicker performance is met in any duration increase within the refresh rate range without jitter impact.		00
C1	Minimum Refresh Rate(60/1.001)Hz		30
C2	Maximum Refresh Rate(165x1.00035)Hz		A4
C3			00
C4	00h = Flicker performance is met in any duration decrease within the refresh rate range		00
C5	FAVT and AVT Supported,Native panel range,successive frame		27

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	duration Decrease met with in RR Range.		
C6	00h = Flicker performance is met in any duration increase within the refresh rate range without jitter impact.		00
C7	Minimum Refresh Rate(48/1.001)Hz		30
C8	Maximum Refresh Rate(60x1.00035)Hz		3B
C9			00
CA	00h = Flicker performance is met in any duration decrease within the refresh rate range		00
CB			2E
CC			00
CD			06
CE			00
CF			44
D0			40
D1			5E
D2			40
D3			5E

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D4	DID2.0 Data block tag[81h] = CTA DisplayID		81
D5	Block revision		00
D6	Number of Payload Bytes in block=		20
D7	CTA Block1 Tag Code and Block1 Length = Vendor Specific Data Block(03h) +Length of following data block (in bytes)		74
D8	AMD IEEE OUI value (0x00001A)		1A
D9	(Hex. LSB first)		00
DA	(Hex. LSB first)		00
DB	AMD VSDB Version 3		03
DC	Freesync Capability : Seamless Local Dimming Disable Control Not Supported , Seamless Native Color Space & Transfer Switching Curve Not Supported , Seamless Variable Frame Rate Switching Supported		71

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DD	Min Refresh Rate =		30
DE	Max Refresh Rate =		A5
DF	Freesync MCCS VCP Code		0
E0	Support WCG and HDR features : Seamless Gamma 2.2 EOTF Not Supported , Seamless PQ EOTF Not Supported		0
E1	Max Luminance 1 (for HDR) =		60
E2	Min Luminance 1 (for HDR) =		FF
E3	Max Luminance 2 (for HDR) =		60
E4	Min Luminance 2 (for HDR) =		FF
E5	Freesync Maximum Refresh Rate (LSB) : (Range : 0Hz (000h) ~ 1023Hz (3FFh), for VSDB v3)		A5
E6	Freesync Maximum Refresh Rate (MSB)		00
E7	Maximum Fast Transport Input Pixel Rate [kHz] - bits 7:0		B7
E8	Maximum Fast Transport Input Pixel Rate [kHz] - bits 15:8		3A
E9	Maximum Fast Transport Input Pixel Rate [kHz] - bits 23:16		0D

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EA			8D
EB			00
EC			E3
ED			05
EE			04
EF			00
F0			E6
F1			06
F2			01
F3			00
F4			60
F5		"00h" fixed	60
F6		"00h" fixed	FF
F7		"00h" fixed	00
F8		"00h" fixed	00
F9		"00h" fixed	00
FA		"00h" fixed	00
FB		"00h" fixed	00
FC		"00h" fixed	00
FD		"00h" fixed	00
FE		"00h" fixed	78
FF	Checksum		90

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Appendix. eDP link rate config:

Table1 is link rate capability for TCON, Table2 is actual link rate.

Table1

eDP link rate			
NT71877 TCON link rate capability			
	DSC	Without DSC	Unit
10bpc (HDR/SDR)	8.1G	8.1G	Gbps/Lane
8bpc (SDR)	8.1G	8.1G	Gbps/Lane

Table2

eDP link rate			
Actual link rate			
	DSC	Without DSC	Unit
10bpc (HDR/SDR)	N/A	N/A	Gbps/Lane
8bpc (SDR)	5.4G	N/A	Gbps/Lane

Table3

Link training condition		
eDP link training Default link training form	SOP0	Ex: SOP0
TCON → SOURCE SSC percentage	0.5%	Ex: 0.5%

Appendix. Checksum of DDS, EDID and FW:

Item	checksum	remark
DDS	0XAE52	
Total FW	0x03B0	
Main FW	0X133A	
Back up FW	0XE88C	

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