**Doc. Number :**

☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

# MODEL NO.: M238HCA
# SUFFIX: L7Z

**Customer:**

**APPROVED BY** **SIGNATURE**

**Name / Title**

Note
Product Version C1

Please return 1 copy for your confirmation with your signature and comments.

| Approved By | Checked By | Prepared By |
|---|---|---|
| 陳立錚 | 陳彥宇 | 李建霆 |

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# REVISION HISTORY

| Version | Date | Page | Description |
|---|---|---|---|
| 2.0 | 2020/12/16 | All | Appoval Spec Ver. 2.0 was first issued. |
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# 1. GENERAL DESCRIPTION

## 1.1 OVERVIEW

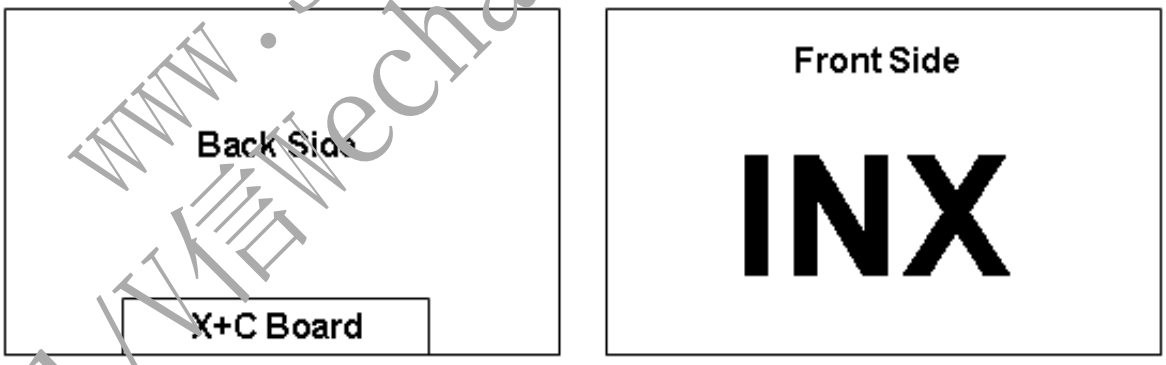
M238HCA-L7Z is a 23.8” TFT Liquid Crystal Display MNT module with WLED Backlight unit and 51 pins and 41 pins 4ch-LVDS interface.. This module supports 1920 x 1080 FHD mode and can display up to 16.7M colors. The converter module for Backlight is not built in.

## 1.2 GENERAL SPECIFICATIONS

| Item | Specification | Unit | Note |
|---|---|---|---|
| Screen Size | 23.8” real diagonal | | |
| Driver Element | a-si TFT active matrix | - | - |
| Outline Dimension | 535(H) x 313(V) x 12.0(T) mm(Typ.) | | |
| Pixel Number | 1920 x R.G.B. x 1080 | pixel | - |
| Pixel Pitch | 0.2745 (H) x 0.2745 (V) | mm | - |
| Pixel Arrangement | RGB vertical stripe | - | - |
| Display Colors | 16.7M | color | - |
| Transmissive Mode | Normally black | - | - |
| Surface Treatment | AG type, 3H hard coating, Haze 25 | - | - |
| Luminance, White | 300 | Cd/m2 | |
| Color Gamut | DCI-P3 90%(min.) | - | (3)(5) |
| Display Orientation | Signal input with “ INX” | | (2) |
| RoHS,Halogen Free | RoHS, Halogen Free | | |
| Low Blue Light | Compliance blue-violet segment of the blue light spectrum ratio 50% (Max) | | (4) |
| Power Consumption | Total 20.08 W (Max.) @ cell 8.28 W (Max.), BL 17.8 W (Max.) | | (1) |

Note (1) The specified power consumption : Total= cell (reference 4.3.1)+BL (reference 4.3.3)

Note (2)




Note (3) Based on Coverage of DCI-P3 color space on CIE -1976 system.

Note (4) The ratio of display emission light in the range from 415-455nm to the display emission of 400-500nm shall be less than 50%

Note (5) Corresponding to sRGB color mode, the coverage ratio meets 95% in CIE 1931.

Maximum ±5% deviation to the specified limit above is allowed for the mass production.

2. MECHANICAL SPECIFICATIONS

| | | |
|---|---|---|
| Module Size | Horizontal (H) | 535 mm(Typ) |
| | Vertical (V) | 313 mm (Typ) |
| | Thickness (T) | 12.0 mm (Typ) |
| Bezel Area | Horizontal | - |
| | Vertical | - |
| Active Area | Horizontal | 527.04 mm |
| | Vertical | 296.46 mm |
| Weight | | Typ: 2230g. Max: 2340g |

Note Please refer to the attached drawings for more information of front and back outline dimensions.

## 3. ABSOLUTE MAXIMUM RATINGS

### 3.1 ABSOLUTE RATINGS OF ENVIRONMENT

| Item | Symbol | Value | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Storage Temperature | TST | -20 | 60 | ºC | (1) |
| Operating Ambient Temperature | TOP | 0 | 50 | ºC | (1), (2) |

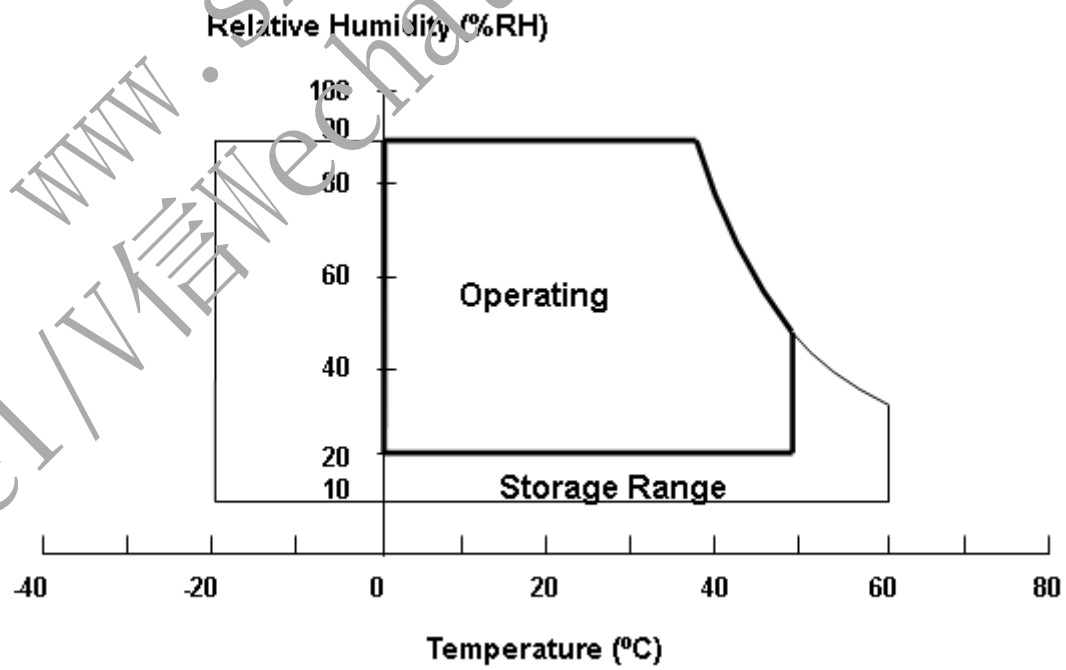
Note (1)

(a) 90 %RH Max.

(b) Wet-bulb temperature should be 39 ºC Max.

(c) No condensation.

Note (2) Panel surface temperature should be 0℃ min. and 65℃ max under Vcc=10.0V, fr =60Hz, typical LED string current, 25℃ ambient temperature, and no humidity control . Any condition of ambient operating temperature ,the surface of active area should be keeping not higher than 65℃.



## 3.2 ELECTRICAL ABSOLUTE RATINGS

### 3.2.1 TFT LCD MODULE

| Item | Symbol | Value | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Power Supply Voltage | VCCS | -0.3 | 13.2 | V | (1) |
| Logic Input Voltage | $V_{IN}$ | -0.3 | 3.6 | V | |

### 3.2.2 BACKLIGHT UNIT

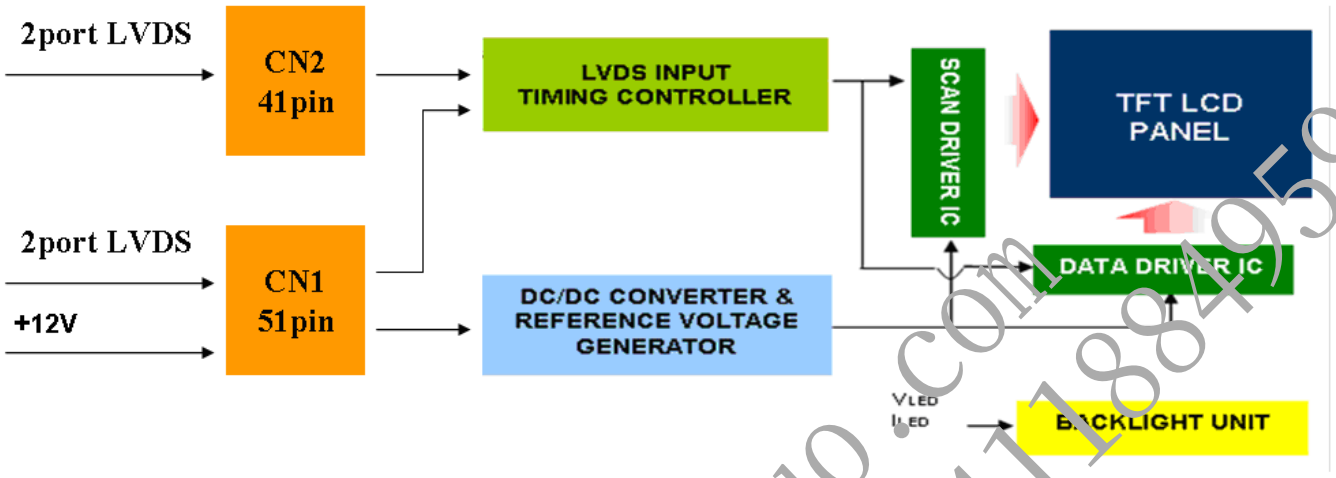
| Item | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|
| | | Min. | Typ | Max. | | |
| LED Forward Current Per Input Pin | $I_F$ | 130 | 135 | 140 | mA | (1), (2) Duty=100% |
| LED Reverse Voltage Per Input Pin | $V_R$ | --- | --- | --- | V | |
| LED Pulse Forward Current Per Input Pin | $I_P$ | --- | --- | 300 | mA | (1), (2) Pulse Width≦10msec. and Duty≦10% |

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for input pin of LED light bar at Ta=25±2 ℃ (Refer to 4.3.3 and 4.3.4 for further information).

4. ELECTRICAL SPECIFICATIONS

## 4.1 FUNCTION BLOCK DIAGRAM



## 4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT (CN1：51pins)

| Pin | Name | Description |
|---|---|---|
| 1 | NC | For LCD internal use only, Do not connect |
| 2 | NC | For LCD internal use only, Do not connect |
| 3 | NC | For LCD internal use only, Do not connect |
| 4 | NC | For LCD internal use only, Do not connect |
| 5 | NC | For LCD internal use only, Do not connect |
| 6 | NC | For LCD internal use only, Do not connect |
| 7 | NC | For LCD internal use only, Do not connect |
| 8 | NC | For LCD internal use only, Do not connect |
| 9 | NC | For LCD internal use only, Do not connect |
| 10 | NC | For LCD internal use only, Do not connect |
| 11 | GND | Ground |
| 12 | ALV0N | 1st LVDS Receiver Signal(0-) |
| 13 | ALV0P | 1st LVDS Receiver Signal(0+) |
| 14 | ALV1N | 1st LVDS Receiver Signal(1-) |
| 15 | ALV1P | 1st LVDS Receiver Signal(1+) |
| 16 | ALV2N | 1st LVDS Receiver Signal(2-) |
| 17 | ALV2P | 1st LVDS Receiver Signal(2+) |
| 18 | GND | Ground |
| 19 | ALVCKN | 1st LVDS Receiver Signal(CLK-) |
| 20 | ALVCKP | 1st LVDS Receiver Signal(CLK+) |
| 21 | GND | Ground |
| 22 | ALV3N | 1st LVDS Receiver Signal(3-) |
| 23 | ALV3P | 1st LVDS Receiver Signal(3+) |
| 24 | NC | For LCD internal use only, Do not connect |
| 25 | NC | For LCD internal use only, Do not connect |
| 26 | NC | For LCD internal use only, Do not connect |
| 27 | NC | For LCD internal use only, Do not connect |
| 28 | BLV0N | 2nd LVDS Receiver Signal(0-) |
| 29 | BLV0P | 2nd LVDS Receiver Signal(0+) |
| 30 | BLV1N | 2nd LVDS Receiver Signal(1-) |
| 31 | BLV1P | 2nd LVDS Receiver Signal(1+) |
| 32 | BLV2N | 2nd LVDS Receiver Signal(2-) |
| 33 | BLV2P | 2nd LVDS Receiver Signal(2+) |
| 34 | GND | Ground |
| 35 | BLVCKN | 2nd LVDS Receiver Signal(CLK-) |
| 36 | BLVCKP | 2nd LVDS Receiver Signal(CLK+) |
| 37 | GND | Ground |
| 38 | BLV3N | 2nd LVDS Receiver Signal(3-) |
| 39 | BLV3P | 2nd LVDS Receiver Signal(3+) |
| 40 | NC | For LCD internal use only, Do not connect |
| 41 | NC | For LCD internal use only, Do not connect |
| 42 | NC | For LCD internal use only, Do not connect |
| 43 | NC | For LCD internal use only, Do not connect |
| 44 | GND | Ground |
| 45 | GND | Ground |
| 46 | GND | Ground |
| 47 | NC | For LCD internal use only, Do not connect |

| | | |
|---|---|---|
| 48 | VIN(12V) | +12.0V power supply |
| 49 | VIN(12V) | +12.0V power supply |
| 50 | VIN(12V) | +12.0V power supply |
| 51 | VIN(12V) | +12.0V power supply |

Connector Information

Note (1) Reserved for internal use. Please leave it open.

Note (2) Connector Part No.:

P-TWO:187059-51221 or

FCN:WF23-402-5133

Note (3) User's connector Part No:

Mating Wire Cable Connector Part No.: FI-RE51HL(JAE) or compatible

PIN ASSIGNMENT (CN2：41pins)

| Pin | Name | Description |
|---|---|---|
| 1 | NC | For LCD internal use only, Do not connect |
| 2 | NC | For LCD internal use only, Do not connect |
| 3 | NC | For LCD internal use only, Do not connect |
| 4 | NC | For LCD internal use only, Do not connect |
| 5 | NC | For LCD internal use only, Do not connect |
| 6 | NC | For LCD internal use only, Do not connect |
| 7 | NC | For LCD internal use only, Do not connect |
| 8 | NC | For LCD internal use only, Do not connect |
| 9 | GND | Ground |
| 10 | CLV0N | 3rd LVDS Receiver Signal(0-) |
| 11 | CLV0P | 3rd LVDS Receiver Signal(0+) |
| 12 | CLV1N | 3rd LVDS Receiver Signal(1-) |
| 13 | CLV1P | 3rd LVDS Receiver Signal(1+) |
| 14 | CLV2N | 3rd LVDS Receiver Signal(2-) |
| 15 | CLV2P | 3rd LVDS Receiver Signal(2+) |
| 16 | GND | Ground |
| 17 | CLVCKN | 3rd LVDS Receiver Signal(CLK-) |
| 18 | CLVCKP | 3rd LVDS Receiver Signal(CLK+) |
| 19 | GND | Ground |
| 20 | CLV3N | 3rd LVDS Receiver Signal(3-) |
| 21 | CLV3P | 3rd LVDS Receiver Signal(3+) |
| 22 | NC | For LCD internal use only, Do not connect |
| 23 | NC | For LCD internal use only, Do not connect |
| 24 | GND | Ground |
| 25 | GND | Ground |
| 26 | DLV0N | 4th LVDS Receiver Signal(0-) |
| 27 | DLV0P | 4th LVDS Receiver Signal(0+) |
| 28 | DLV1N | 4th LVDS Receiver Signal(1-) |
| 29 | DLV1P | 4th LVDS Receiver Signal(1+) |
| 30 | DLV2N | 4th LVDS Receiver Signal(2-) |
| 31 | DLV2P | 4th LVDS Receiver Signal(2+) |
| 32 | GND | Ground |
| 33 | DLVCKN | 4th LVDS Receiver Signal(CLK-) |
| 34 | DLVCKP | 4th LVDS Receiver Signal(CLK+) |
| 35 | GND | Ground |
| 36 | DLV3N | 4th LVDS Receiver Signal(3-) |

| | | |
|---|---|---|
| 37 | DLV3P | 4th LVDS Receiver Signal(3+) |
| 38 | NC | For LCD internal use only, Do not connect |
| 39 | NC | For LCD internal use only, Do not connect |
| 40 | GND | Ground |
| 41 | GND | Ground |

Connector Information

Note (1) Reserved for internal use. Please leave it open.

Note (2) Connector Part No.:

P-TWO: 187060-41221 or

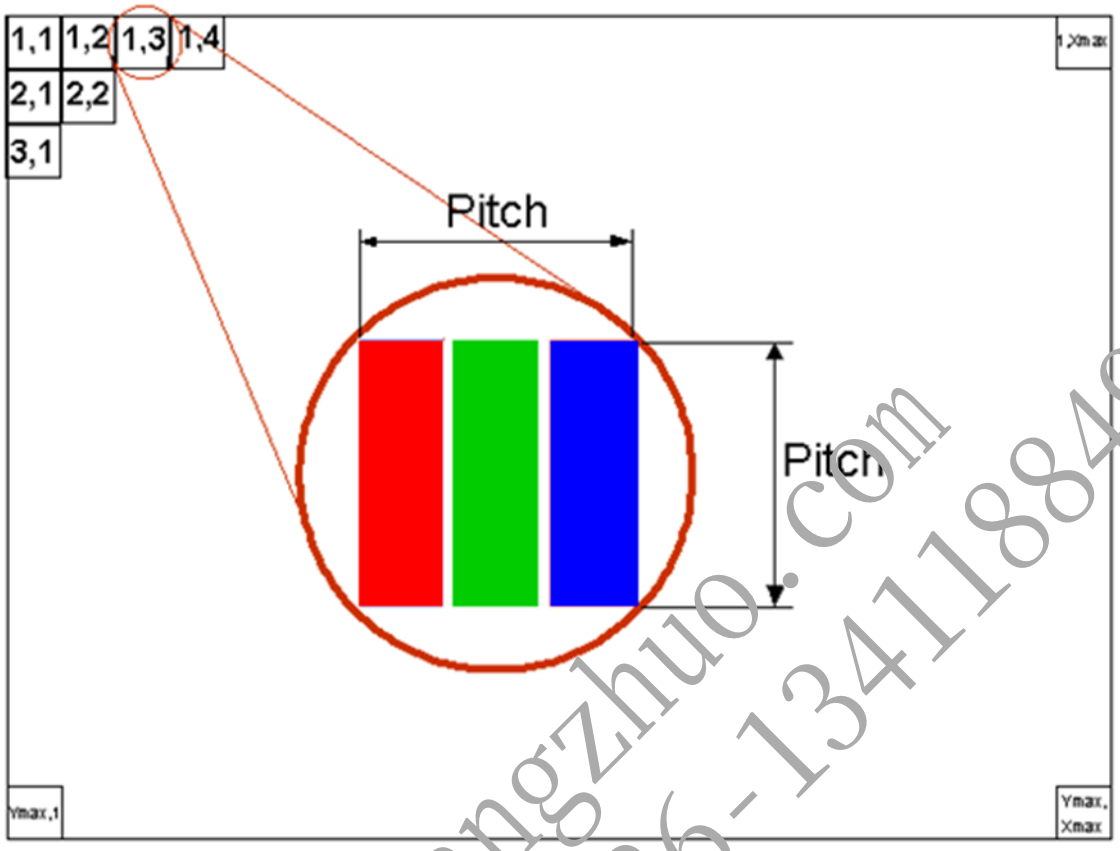
FCN: WF23-400-413C

Note (3) User's connector Part No:

Mating Wire Cable Connector Part No.: FI-RE41HL(JAE) or compatible

Note (4) LVDS 4-port Data Mapping.

| Port | Channel of LVDS | Data Stream |
|---|---|---|
| 1st Port | First Pixel | 1,5,9,..... 1913,1917 |
| 2nd Port | Second Pixel | 2,6,10,..... 1914,1918 |
| 3rd Port | Third Pixel | 3,7,11,..... 1915,1919 |
| 4th Port | Fourth Pixel | 4,8,12,..... 1916,1920 |




Note (2) Input signal of 4 port LVDS clock should be the same timing.

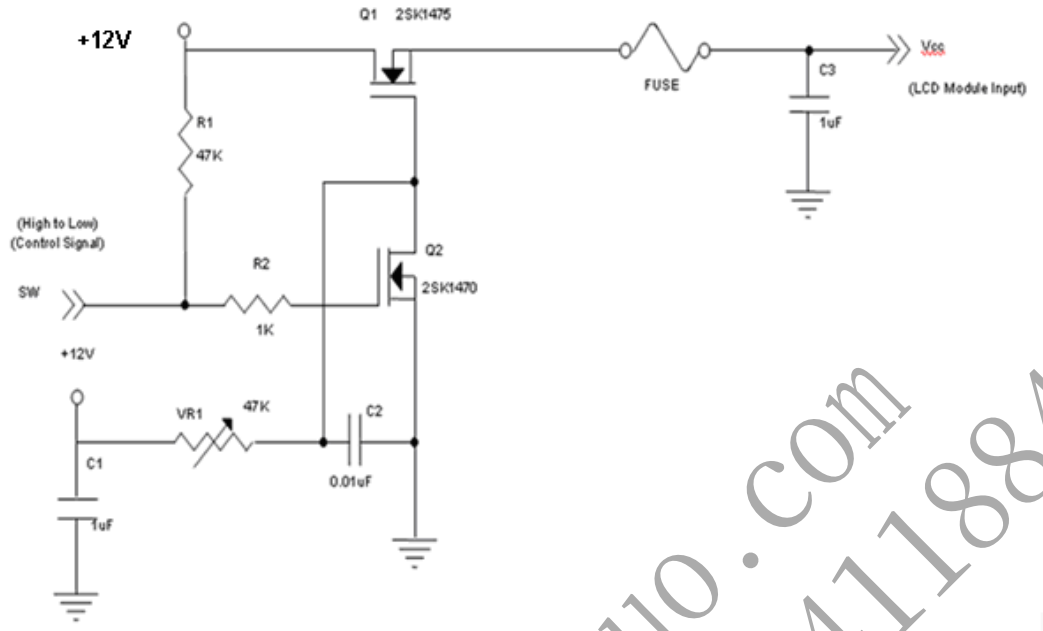
## 4.3 ELECTRICAL CHARACTERISTICS

### 4.3.1 LCD ELETRONICS SPECIFICATION

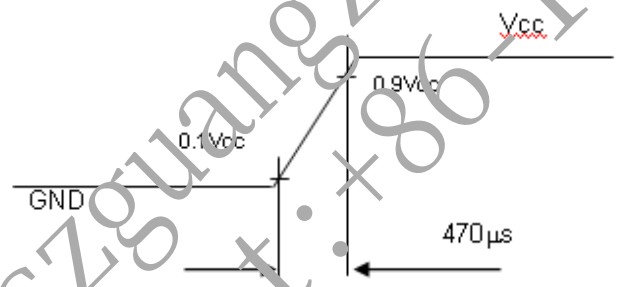
| Parameter | | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Power Supply Voltage | | Vcc | 10.8 | 12 | 13.2 | V | - |
| Ripple Voltage | | $V_{RP}$ | | | 300 | mV | - |
| Rush Current | | $I_{RUSH}$ | | | 3 | A | (2) |
| Power Supply Current | White | | | 0.35 | 0.42 | A | (3)a |
| | Black | | | 0.35 | 0.41 | A | (3)b |
| | Horizontal Stripe | | | 0.58 | 0.69 | A | (3)c |
| Power Consumption | | PLCD | | 6.96 | 8.28 | Watt | (4) |
| LVDS differential input voltage | | Vid | 100 | | 600 | mV | |
| LVDS common input voltage | | Vic | 1.0 | 1.2 | 1.4 | V | |
| Logic High Input Voltage | | VIH | | | +100 | V | |
| Logic Low Input Voltage | | VIL | -100 | | | V | |

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

Note (2) Measurement Conditions:




**Vcc rising time is 470µs**



Note (3) The specified power supply current is under the conditions at Vcc = 12.0V, Ta = 25 ± 2 ºC, Fr = 120Hz, whereas a power dissipation check pattern below is displayed.

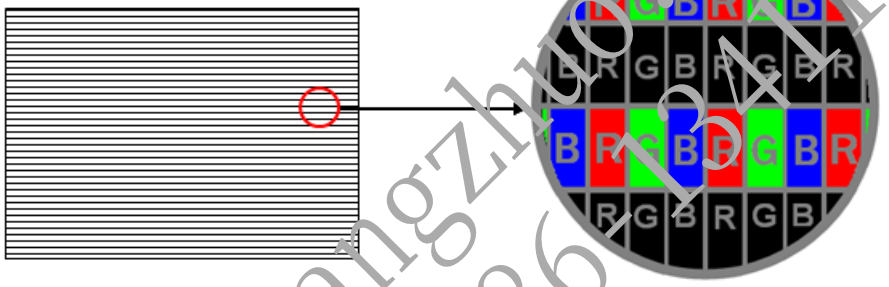
a. White Pattern

Active Area

b. Black Pattern

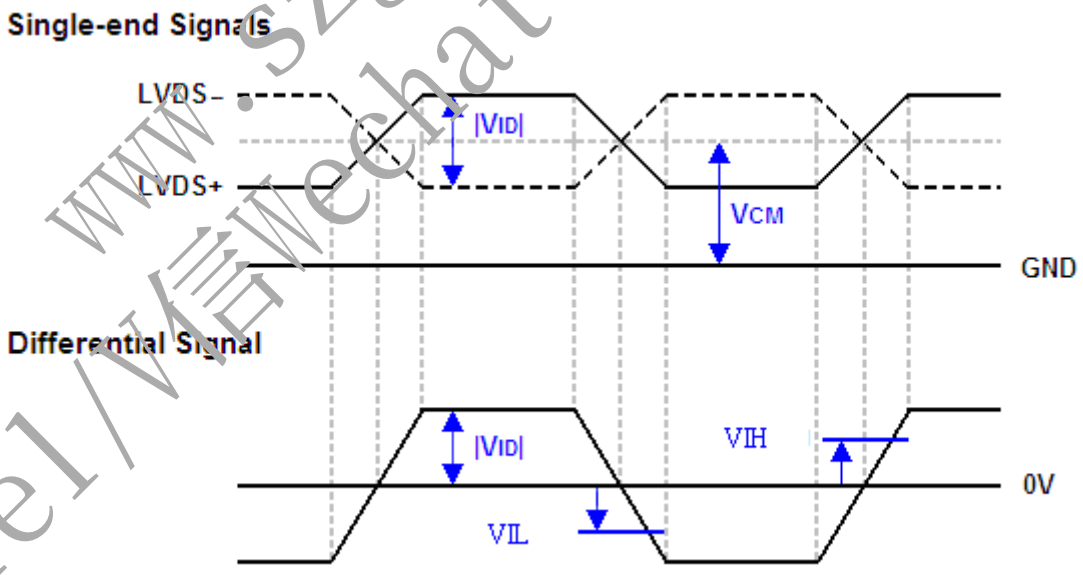
Active Area

c. Horizontal Pattern

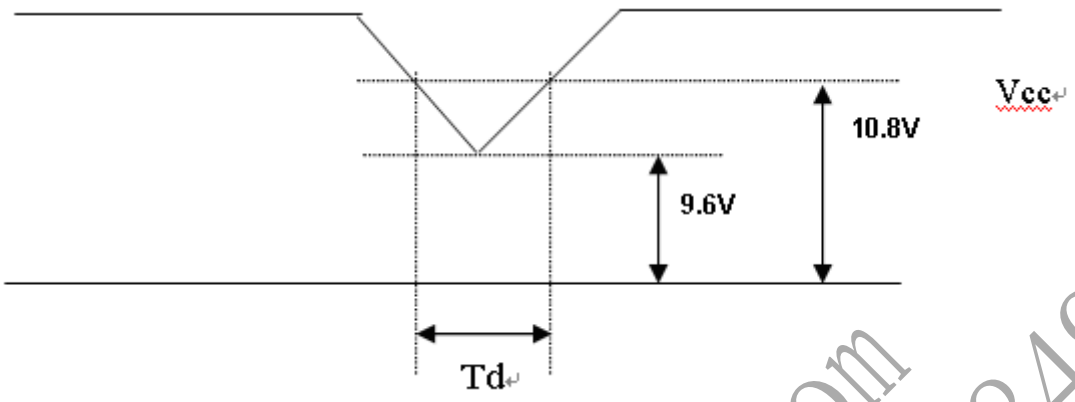



Note (4) The power consumption is specified at the pattern with the maximum current.

Note (5) VID waveform condition



4.3.2 VCC POWER DIP CONDITION




Dip condition : 9.6V≦Vcc≦10.8V, Td≦20ms

### 4.3.3 BACKLIGHT UNIT

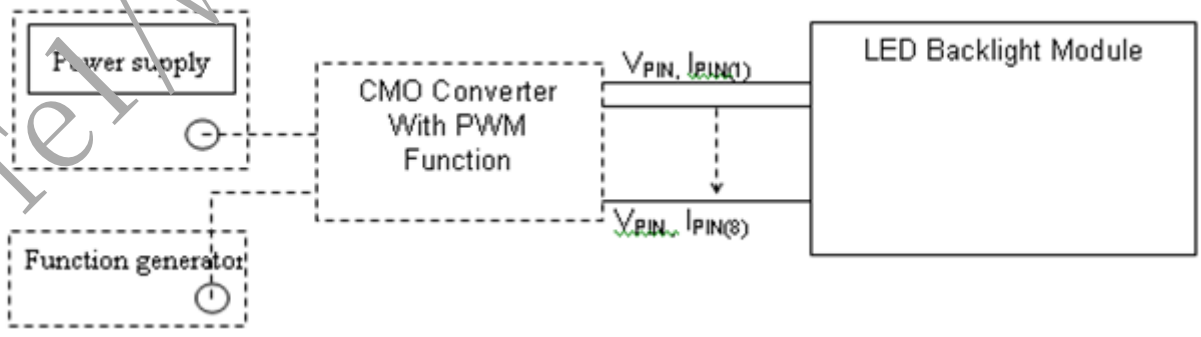
| Parameter | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| LED Light Bar Input Voltage Per Input Pin | VPIN | 27.3 | 28.1 | 33 | V | (1), Duty=100%, IPIN=(135)mA |
| LED Light Bar Current Per Input Pin | IPIN | 130 | 135 | 140 | mA | (1), (2) Duty=100% |
| LED Life Time | LLED | 30000 | | | Hrs | (3) |
| Power Consumption | PBL | --- | 15.2 | 17.8 | W | (1) Duty=100%, IPIN=(135)mA |

Note (1) LED light bar input voltage and current are measured by utilizing a true RMS multimeter as shown below:

Note (2) PBL = IPIN × VPIN × ( 4 ) input pins ,

Note (3) The lifetime of LED is defined as the time when LED packages continue to operate under the conditions at Ta = 25 ±2 ℃ and I= (67.5)mA (per chip) until the brightness becomes ≦ 50% of its iginal value.

Note (4) The module must be operated with constant driving current.

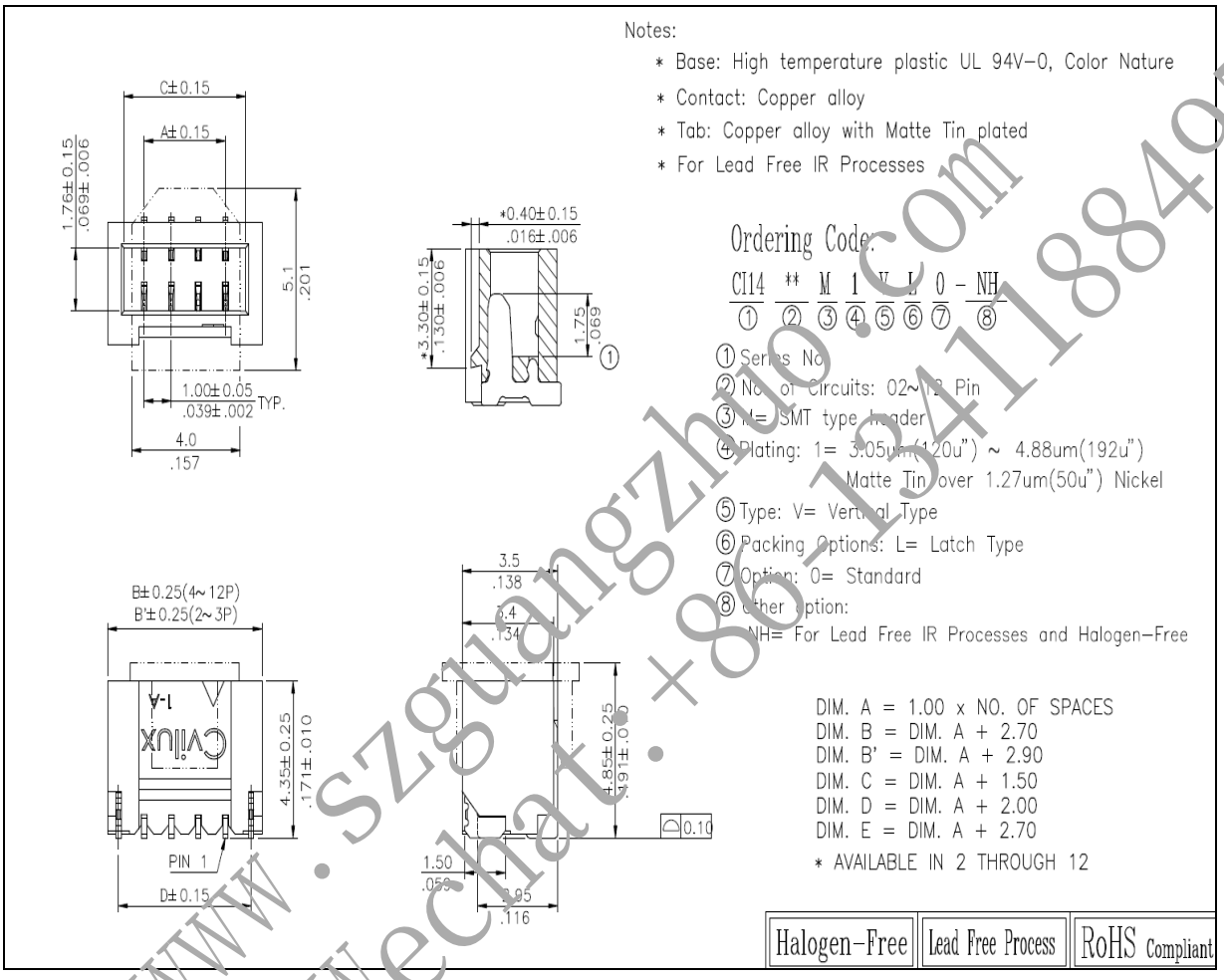


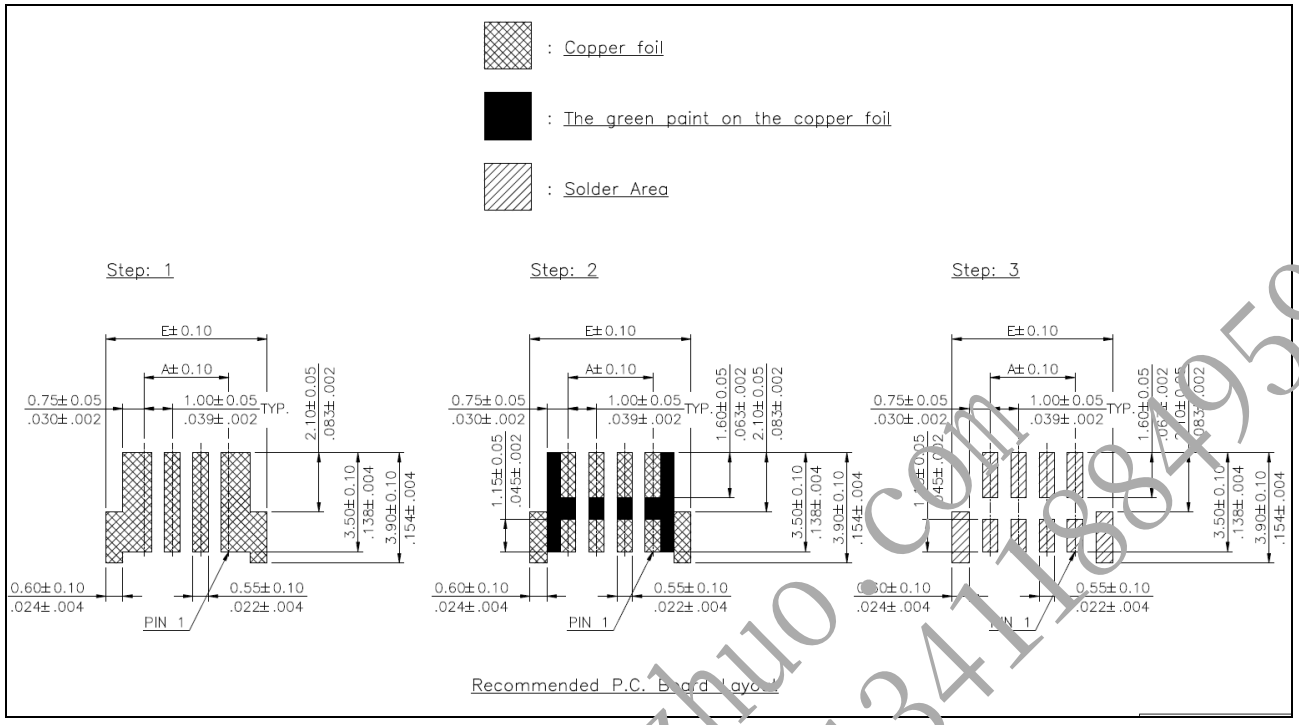
### 4.3.4 LIGHTBAR CONNECTOR PIN ASSIGNMENT

Connector:

Note(1) Connector(wire type): CviLux(CI1406M1VL0-NH)or equivalent.

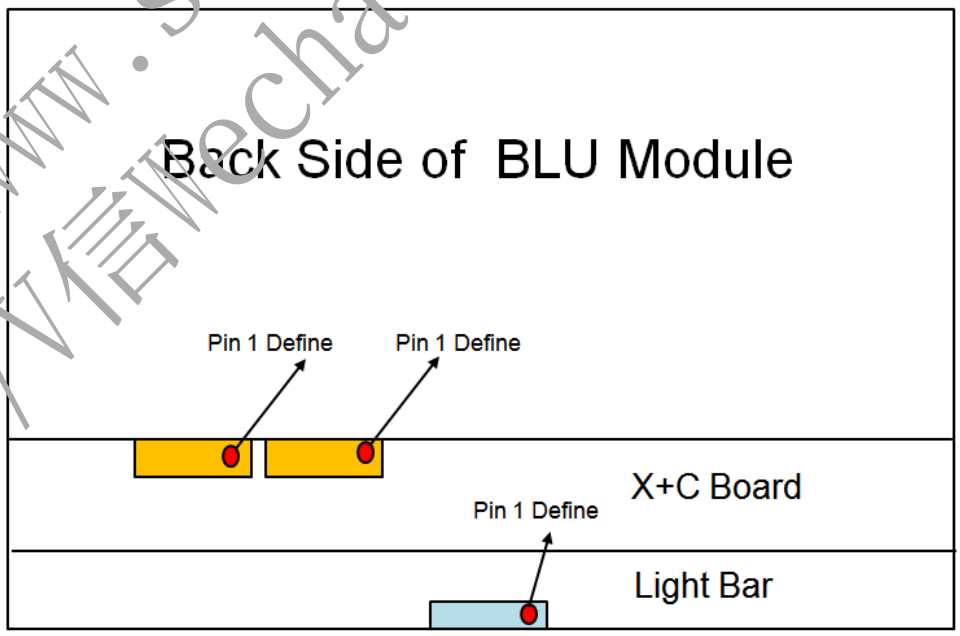
Note(2) User's mating connector part No.: FCN(WF1300106-B) or CviLux(CI1406SL000-NH) and hook width must be less than 4.5mm.






CN1

| Pin number | Description |
|---|---|
| 1 | Cathode of LED string |
| 2 | Cathode of LED string |
| 3 | VLED |
| 4 | VLED |
| 5 | Cathode of LED string |
| 6 | Cathode of LED string |



## 4.4 LVDS INPUT SIGNAL SPECIFICATIONS

### 4.4.1 LVDS DATA MAPPING TABLE

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| LVDS Channel ALV0 | LVDS output | D7 | D6 | D4 | D3 | D2 | D1 | D0 |
| | Data order | 1G0 | 1R5 | 1R4 | 1R3 | 1R2 | 1R1 | 1R0 |
| LVDS Channel ALV1 | LVDS output | D18 | D15 | D14 | D13 | D12 | D9 | D8 |
| | Data order | 1B1 | 1B0 | 1G5 | 1G4 | 1G3 | 1G2 | 1G1 |
| LVDS Channel ALV2 | LVDS output | D26 | D25 | D24 | D22 | D21 | D20 | D19 |
| | Data order | DE | NA | NA | 1B5 | 1B4 | 1B3 | 1B2 |
| LVDS Channel ALV3 | LVDS output | D23 | D17 | D16 | D11 | D10 | D5 | D27 |
| | Data order | NA | 1B7 | 1B6 | 1G7 | 1G6 | 1R7 | 1R6 |
| LVDS Channel BLV0 | LVDS output | D7 | D6 | D4 | D3 | D2 | D1 | D0 |
| | Data order | 2G0 | 2R5 | 2R4 | 2R3 | 2R2 | 2R1 | 2R0 |
| LVDS Channel BLV1 | LVDS output | D18 | D15 | D14 | D13 | D12 | D9 | D8 |
| | Data order | 2B1 | 2B0 | 2G5 | 2G4 | 2G3 | 2G2 | 2G1 |
| LVDS Channel BLV2 | LVDS output | D26 | D25 | D24 | D22 | D21 | D20 | D19 |
| | Data order | DE | NA | NA | 2B5 | 2B4 | 2B3 | 2B2 |
| LVDS Channel BLV3 | LVDS output | D23 | D17 | D16 | D11 | D10 | D5 | D27 |
| | Data order | NA | 2B7 | 2B6 | 2G7 | 2G6 | 2R7 | 2R6 |
| LVDS Channel CLV0 | LVDS output | D7 | D6 | D4 | D3 | D2 | D1 | D0 |
| | Data order | 3G0 | 3R5 | 3R4 | 3R3 | 3R2 | 3R1 | 3R0 |
| LVDS Channel CLV1 | LVDS output | D18 | D15 | D14 | D13 | D12 | D9 | D8 |
| | Data order | 3B1 | 3B0 | 3G5 | 3G4 | 3G3 | 3G2 | 3G1 |
| LVDS Channel CLV2 | LVDS output | D26 | D25 | D24 | D22 | D21 | D20 | D19 |
| | Data order | DE | NA | NA | 3B5 | 3B4 | 3B3 | 3B2 |
| LVDS Channel CLV3 | LVDS output | D23 | D17 | D16 | D11 | D10 | D5 | D27 |
| | Data order | NA | 3B7 | 3B6 | 3G7 | 3G6 | 3R7 | 3R6 |
| LVDS Channel DLV0 | LVDS output | D7 | D6 | D4 | D3 | D2 | D1 | D0 |
| | Data order | 4G0 | 4R5 | 4R4 | 4R3 | 4R2 | 4R1 | 4R0 |
| LVDS Channel DLV1 | LVDS output | D18 | D15 | D14 | D13 | D12 | D9 | D8 |
| | Data order | 4B1 | 4B0 | 4G5 | 4G4 | 4G3 | 4G2 | 4G1 |
| LVDS Channel DLV2 | LVDS output | D26 | D25 | D24 | D22 | D21 | D20 | D19 |
| | Data order | DE | NA | NA | 4B5 | 4B4 | 4B3 | 4B2 |
| LVDS Channel DLV3 | LVDS output | D23 | D17 | D16 | D11 | D10 | D5 | D27 |
| | Data order | NA | 4B7 | 4B6 | 4G7 | 4G6 | 4R7 | 4R6 |

### 4.4.2 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

| Color | | Data Signal | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Red | | | | | | | | Green | | | | | | | | Blue | | | | | | | |
| | | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 | G7 | G6 | G5 | G4 | G3 | G2 | G1 | G0 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Basic Colors | Black | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Cyan | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Magenta | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Yellow | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | White | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Gray Scale Of Red | Red(0) / Dark | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red(1) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red(2) | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | Red(253) | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | :0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | :0 |
| | Red(254) | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red(255) | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Gray Scale Of Green | Green(0) / Dark | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green(1) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green(2) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | Green(253) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green(254) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green(255) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Gray Scale Of Blue | Blue(0) / Dark | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Blue(1) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| | Blue(2) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | Blue(253) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| | Blue(254) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| | Blue(255) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Note (1) 0: Low Level Voltage, 1: High Level Voltage

## 4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

| Signal | Item | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| LVDS Clock | Frequency | Fc | 60 | 74.25 | 96 | MHz | - |
| | Period | Tc | - | 13.468 | - | ns | |
| | Input cycle to cycle jitter | $T_{rcl}$ | -0.02*Tc | - | 0.02*Tc | ns | (1) |
| | Input Clock to data skew | TLVCCS | -0.02*Tc | | 0.02*Tc | | (2) |
| | Spread spectrum modulation range | Fclkin_mod | 0.97*Fc | - | 1.03*Fc | MHz | (3) |
| | Spread spectrum modulation frequency | $F_{SSM}$ | | - | 100 | KHz | |
| Vertical Display Term | Frame Rate | Fr | 47 | 120 | 165 | Hz | Tv=Tvd+Tvb |
| | Total | Tv | 1100 | 1125 | 3500 | Th | - |
| | Active Display | Tvd | 1080 | 1080 | 1080 | Th | - |
| | Blank | Tvb | 20 | 45 | 2420 | Th | - |
| Horizontal Display Term | Frequency | Fh | 54 | 66 | 88 | KHz | |
| | Total | Th | 525 | 550 | 575 | Tc | Th=Thd+Thb |
| | Active Display | Thd | 480 | 480 | 480 | Tc | - |
| | Blank | Thb | 45 | 70 | 95 | Tc | - |

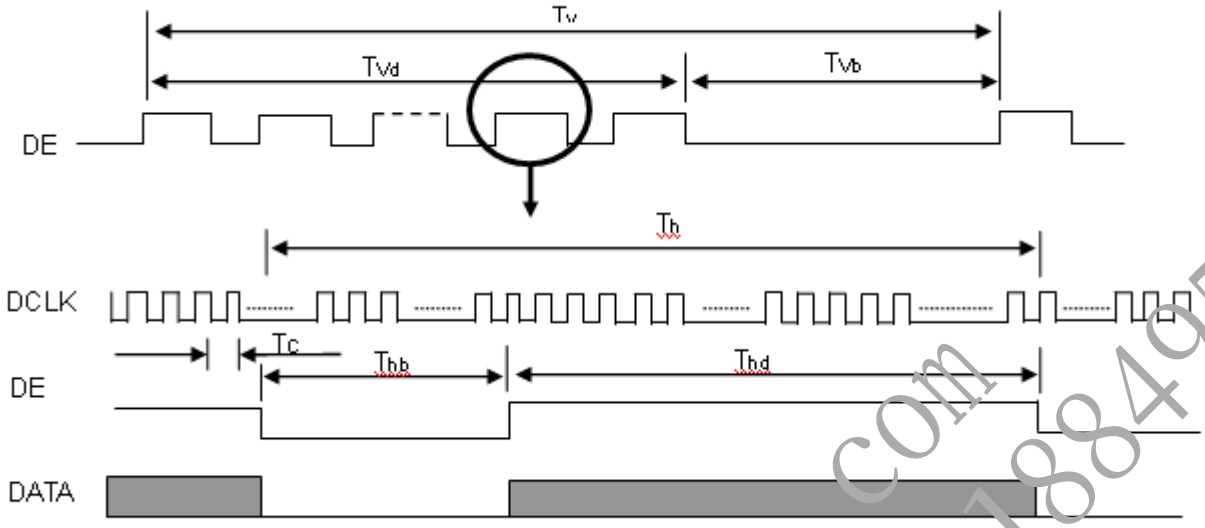
Note: Because this module is operated by DE only mode, Hsync and Vsync input signals are ignored.

Fc = Fr X Tv X Th

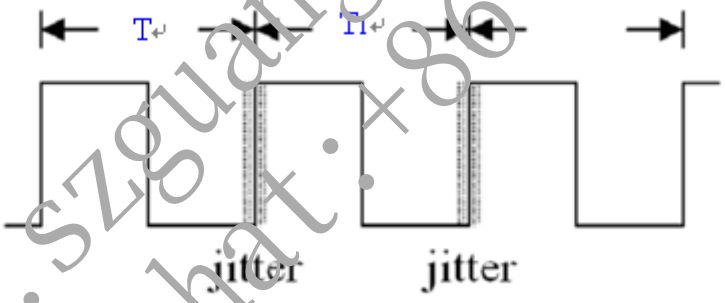
Fh(min.)=Fc(min.)/Tv(min.), Fh(typ.)=Fc(typ.)/Tv(typ.),Fh(max.)=Fc(max.)/Tv(min.)

Please make sure the range of pixel clock has follow the below equation and Fc, Fr, Tv , Th not allowed to get beyond the min or max spec.

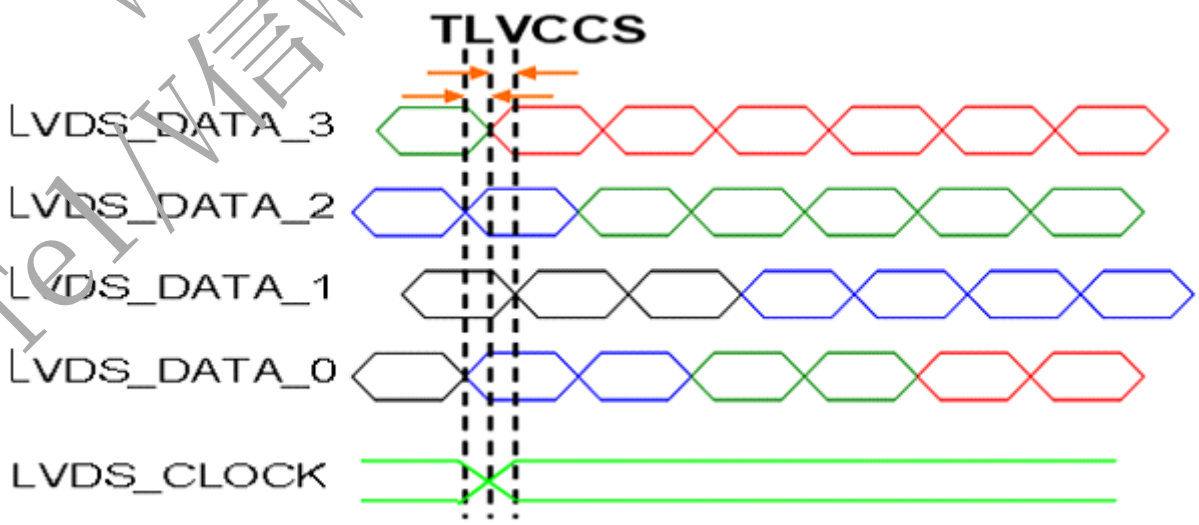
INPUT SIGNAL TIMING DIAGRAM




Note (1) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = $|T_1 - TI$




Note (2) Input Clock to data skew is defined as below figures.









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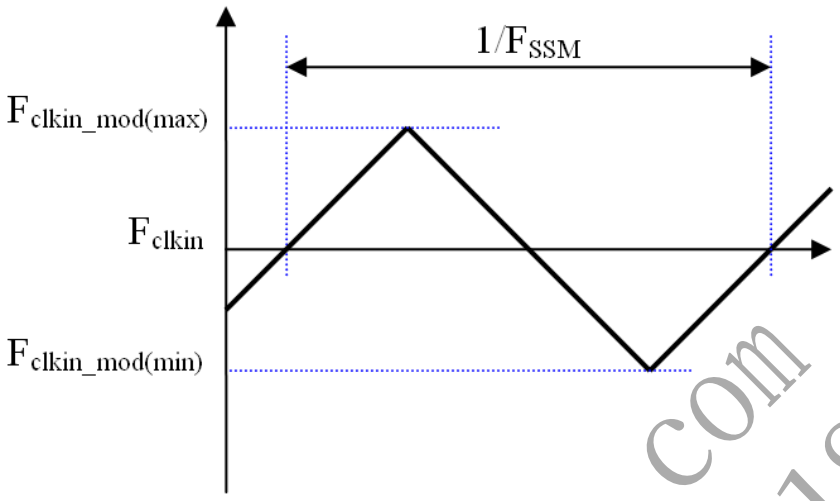
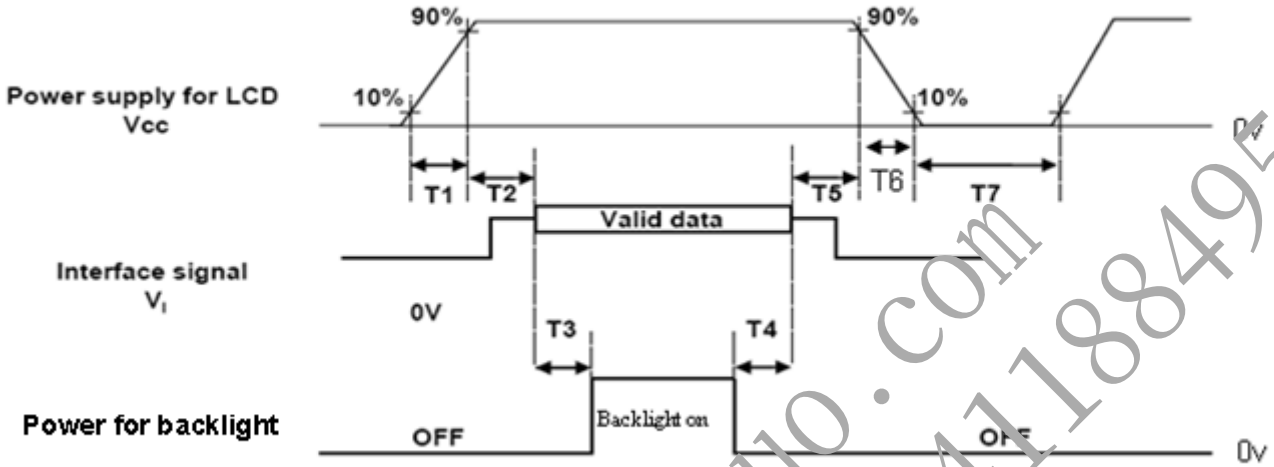
Note (3) The SSCG (Spread spectrum clock generator) is defined as below figures.




**Note (4) The DCLK range at last line of V-blank should be set in 0 to Hdisplay/2**

## 4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.




Timing Specifications:

| Parameters | Values | | | Units |
|---|---|---|---|---|
| | Min | Typ | Max | |
| T1 | 0.5 | - | 10 | ms |
| T2 | 0 | 30 | 50 | ms |
| T3 | 450 | - | - | ms |
| T4 | 100 | 250 | - | ms |
| T5 | 0 | 20 | 50 | ms |
| T6 | 0.1 | - | 100 | ms |
| T7 | 1000 | - | - | ms |

Note (1) The supply voltage of the external system for the module input should be the same as the definition of Vcc.

Note (2) When the backlight turns on before the LCD operation of the LCD turns off, the display may momentarily become abnormal screen.

Note (3) In case of VCC = off level, please keep the level of input signals on the low or keep a high impedance.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

Note (6) INX won't take any responsibility for the products which are damaged by the customers not following the Power Sequence.

Note (7) There might be slight electronic noise when LCD is turned off (even backlight unit is also off). To avoid this symptom, we suggest "Vcc falling timing" to follow "t6 spec".

# 5. OPTICAL CHARACTERISTICS

## 5.1 TEST CONDITIONS

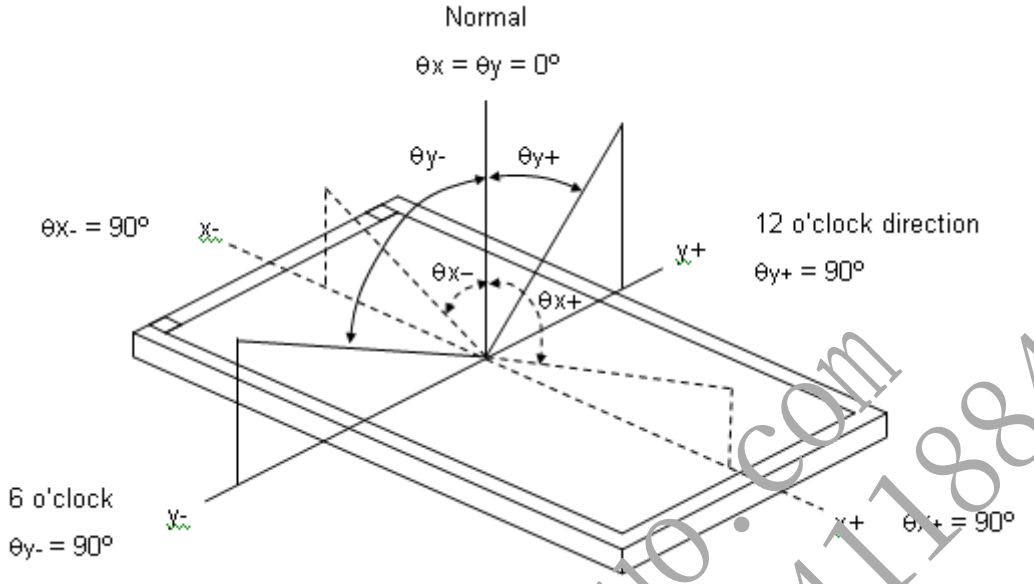
| Item | Symbol | Value | Unit |
|---|---|---|---|
| Ambient Temperature | Ta | 25±2 | °C |
| Ambient Humidity | Ha | 50±10 | %RH |
| Supply Voltage | $V_{CC}$ | 10 | V |
| Input Signal | According to typical value in "3. ELECTRICAL CHARACTERISTICS" | | |
| LED Light Bar Input Current Per Input Pin | $I_{PIN}$ | 135 ±1.5 | $mA_{DC}$ |
| PWM Duty Ratio | D | 100 | % |
| LED Light Bar Test Converter | INX 27-D041745 | | |

## 5.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 5.2. The following items should be measured under the test conditions described in 5.1 and stable environment shown in Note (5).

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| Color Chromaticity (CIE 1931) | Red | Rx | $\theta_x$=0°, $\theta_Y$ =0° CS-2000 R=G=B=255 Gray scale | Typ 0.03 | 0.678 | Typ + 0.03 | - | (1), (5) |
| | | Ry | | | 0.31[illegible] | | | |
| | Green | Gx | | | 0.272 | | | |
| | | Gy | | | 0.622 | | | |
| | Blue | Bx | | | 0.146 | | | |
| | | By | | | 0.054 | | | |
| | White | Wx | | | 0.313 | | | |
| | | Wy | | | 0.329 | | | |
| Center Luminance of White (Center of Screen) | | $L_C$ | | 240 | 300 | - | $cd/m^2$ | (4), (5) |
| Contrast Ratio | | CR | | 700 | 1000 | - | - | (2), (5) |
| Response Time | | $T_{GtG\ AVE}$ | | | 5 | 11 | | (3) |
| White Variation | | W | $\theta_x$=0°, $\theta_Y$ =0° | 75 | - | - | % | (5), (6) |
| Viewing Angle | Horizontal | θx- + θx+ | CR ≧ 10 | 170 | 178 | - | Deg. | (1), (5) |
| | Vertical | θy- + θy+ | | 170 | 178 | - | | |

Note (1) Definition of Viewing Angle (θx, θy):




Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

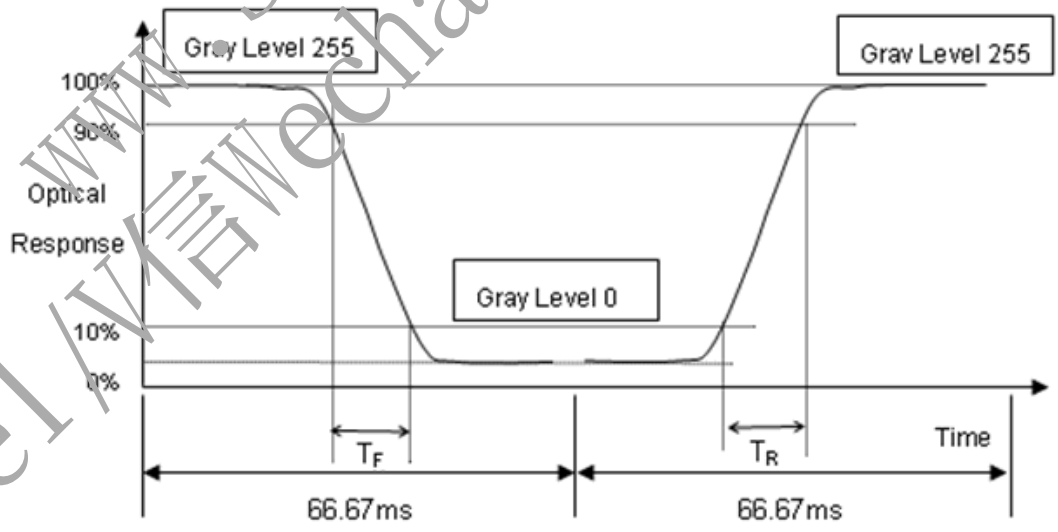
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time ($T_R$, $T_F$):




- $T_{GtG\_AVE}$ is the total average of the $T_{GtG}$ data (Measured by INX GTG instrument)
- The gray (N,M) stands for the (0,63,~255) as the following table.
- If system uses ODC ( Over Driving Circuit) function, $T_{GtG\_AVE}$ may be 5ms~10ms.

* It depends on Overshoot rate.

| Gray to Gray | | Rising time | | | | |
|---|---|---|---|---|---|---|
| | | 0 | 63 | 127 | 191 | 255 |
| Falling time | 0 | | | | | |
| | 63 | | | | | |
| | 127 | | | | | |
| | 191 | | | | | |
| | 255 | | | | | |

Note (4) Definition of Luminance of White ($L_C$):

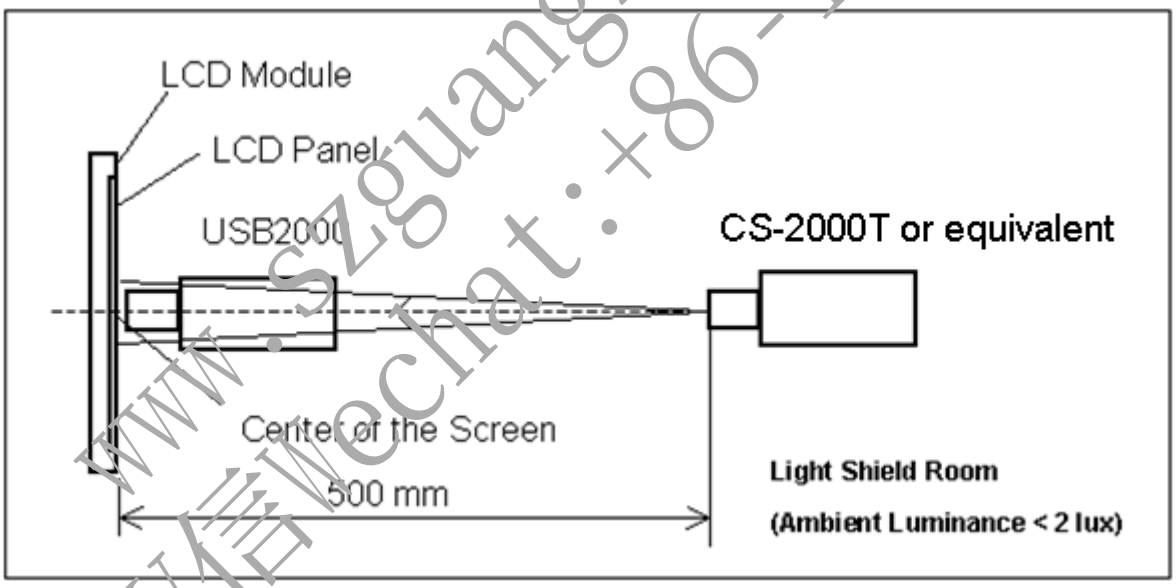
Measure the luminance of gray level 255 at center point

$L_C$ = L (5)

L (x) is corresponding to the luminance of the point X at Figure in Note (6).

Note (5) Measurement Setup:

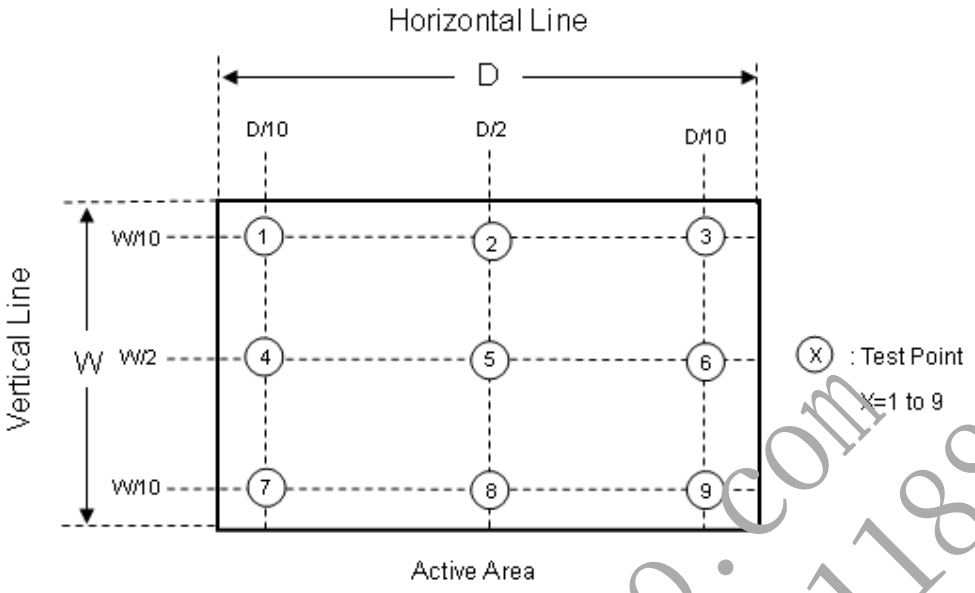
The LCD module should be stabilized at given temperature for 40 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 40 minutes in a windless room.




Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 9 points

δW = ( Minimum [L (1) ~ L (9)] / Maximum [L (1) ~ L (9)] ) *100%



## 6. RELIABILITY TEST ITEM

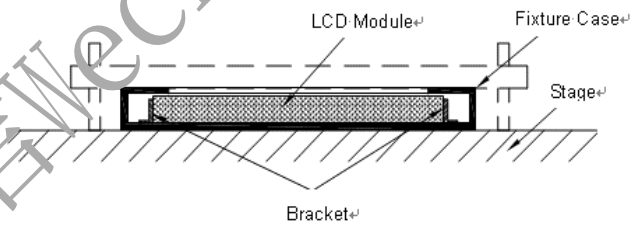
| Items | Required Condition | Note |
|---|---|---|
| Temperature Humidity Bias (THB) | Ta= 50℃ , 80%RH, 240hours | (1)(2) |
| High Temperature Operation (HTO) | Ta= 50℃ , 240hours | |
| Low Temperature Operation (LTO) | Ta= 0℃ , 240hours | |
| High Temperature Storage (HTS) | Ta= 60℃ , 240hours | |
| Low Temperature Storage (LTS) | Ta= -20℃ , 240hours | |
| Vibration Test (Non-operation) | Acceleration: 1.5 G<br>Wave: sine<br>Frequency: 10 - 300 Hz<br>Sweep: 30 Minutes each Axis (X, Y, Z) | (1)(3) |
| Shock Test (Non-operation) | Acceleration: 50 G<br>Wave: Half-sine<br>Active Time: 11 ms<br>Direction : ± X, ± Y, ± Z.(one time for each Axis) | |
| Thermal Shock Test (TST) | -20℃/30min , 60℃ / 30min, 100 cycles | (1)(2) |
| On/Off Test | 25℃ ,On/10sec , Off/10sec , 30,000 cycles | (1)(2) |
| ESD (Electro Static Discharge) | Contact Discharge: ± 8KV, 150pF(330Ω) | (1) |
| | Air Discharge: ± 15KV, 150pF(330Ω) | (1) |
| Altitude Test | Operation:10,000 ft / 24hours<br>Non-Operation:30,000 ft / 24hours | (1)(2) |

Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

The fixing condition is shown as below:



# 7. MECHANICAL STRENGTH CHARACTERISTICS

## 7.1 MECHANICAL STRENGTH SPECIFICATIONS

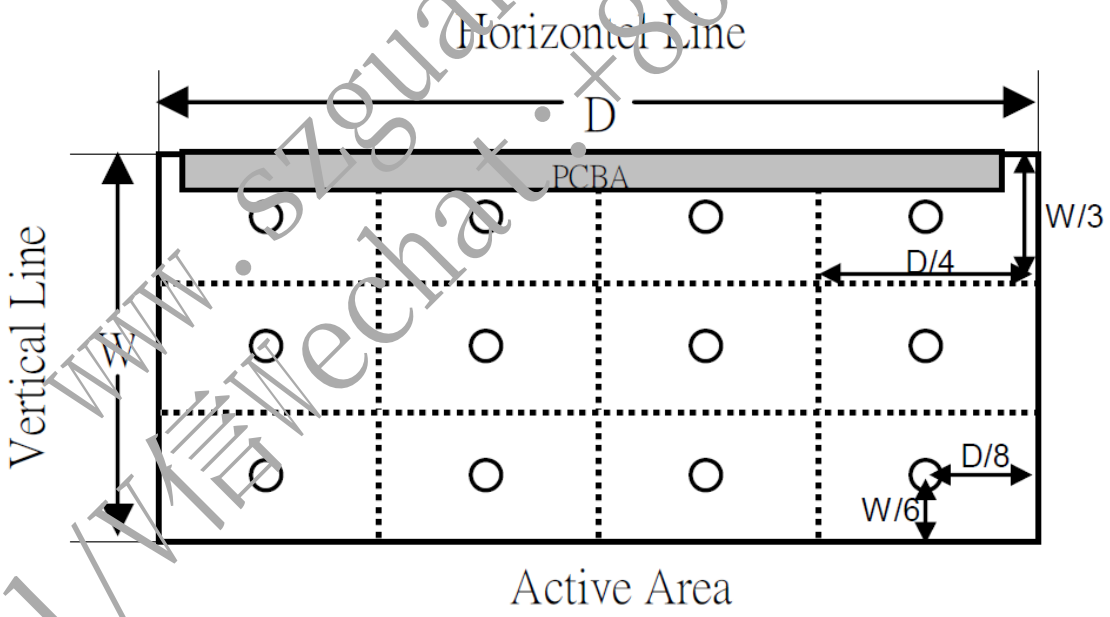
| Item | Condition | Min | Unit | Note |
|---|---|---|---|---|
| Mechanical Strength | 128th Gray Pattern | 0.6 | Kgf | |

## 7.2 TEST CONDITIONS

| Items | Description |
|---|---|
| Test Condition | 1. Ambient Illumination : 10~15 lux<br>2. Test Pattern : 128 Gray<br>3. Distance of the judgment : 30cm from the surface of module<br>4. Viewing angle of the judgment : Front |
| Gage Information | 1. Push pull guage<br>a. Model name : HF-50, maker : ALGOL<br>b. Shape of gage tip<br>- Diameter : 2mm<br>- Thickness : 2mm |
| Definition of Minimum force | To measure minimum force when operator detects any white spot and light leakage that have occurred while operator presses on back side of module with push pull gage. |

## 7.3 DEFINITION OF TEST POINTS

Measure the minimum force of test points at 128th Gray pattern. The test points at back side of module area is showing as below (If the test points on the PCBA or TP board, these points are not included).



# 8. PACKING

## 8.1 PACKING SPECIFICATIONS

(1) 12 LCD modules / 1 Box

(2) Box dimensions: 620(L) X 348(W) X 390(H) mm

(3) Weight: approximately: 30.4kg

## 8.2 PACKING METHOD

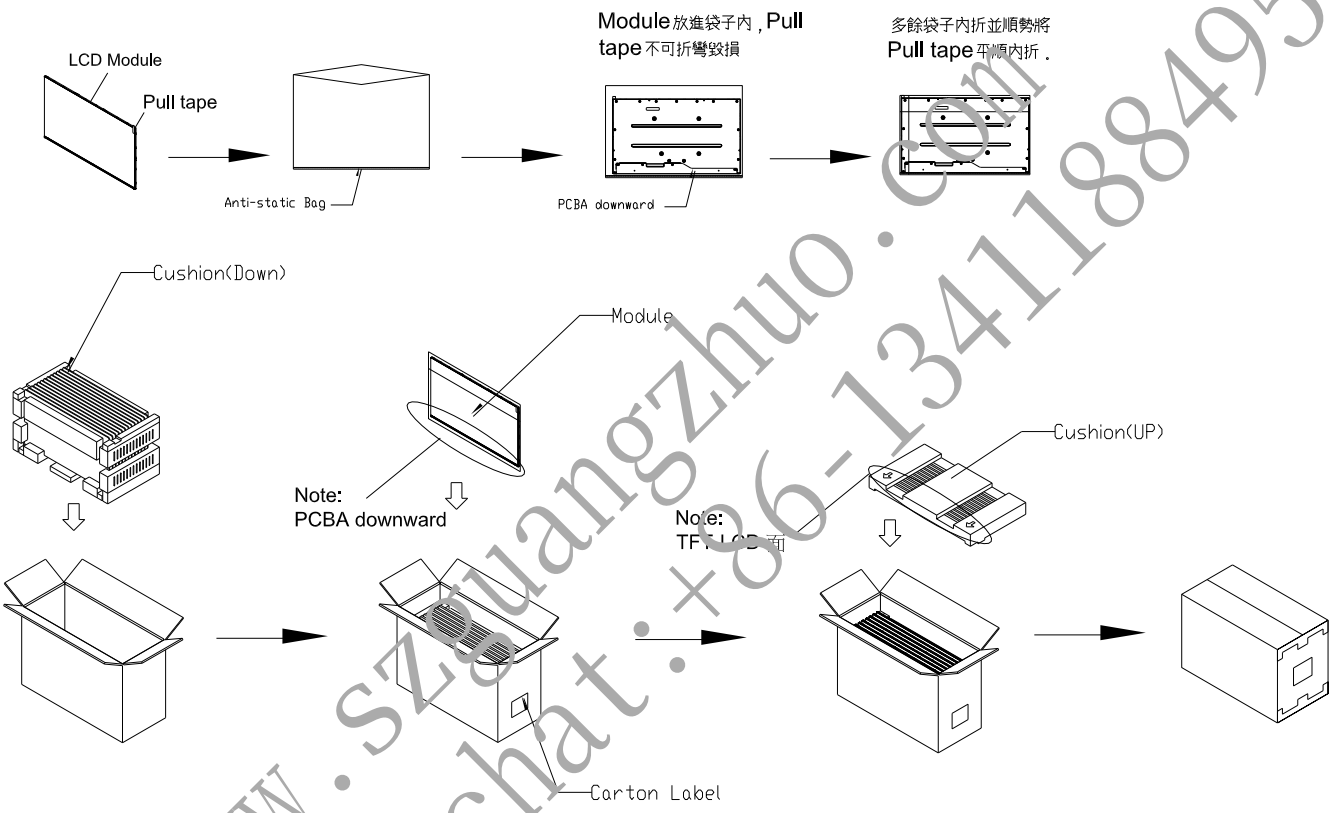
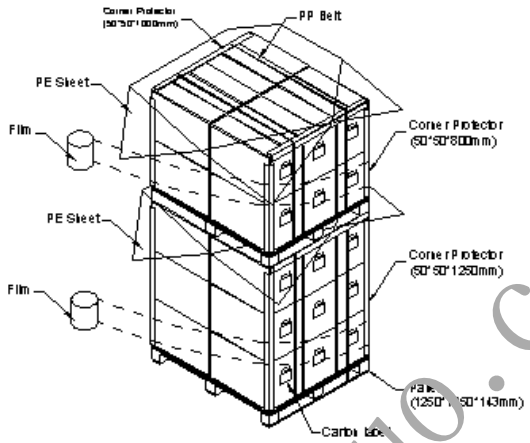



Figure. 8-1 Packing method

## 8.3 PALLET

For ocean shipping

Sea / Land Transportation (40ft HQ/40ft Container)




For air transport

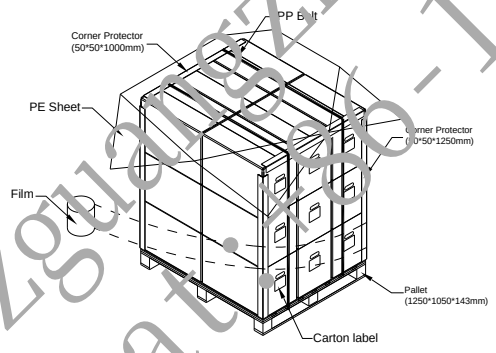



Figure. 8-2 Packing method

## 8.4 UN-PACKAGING METHOD

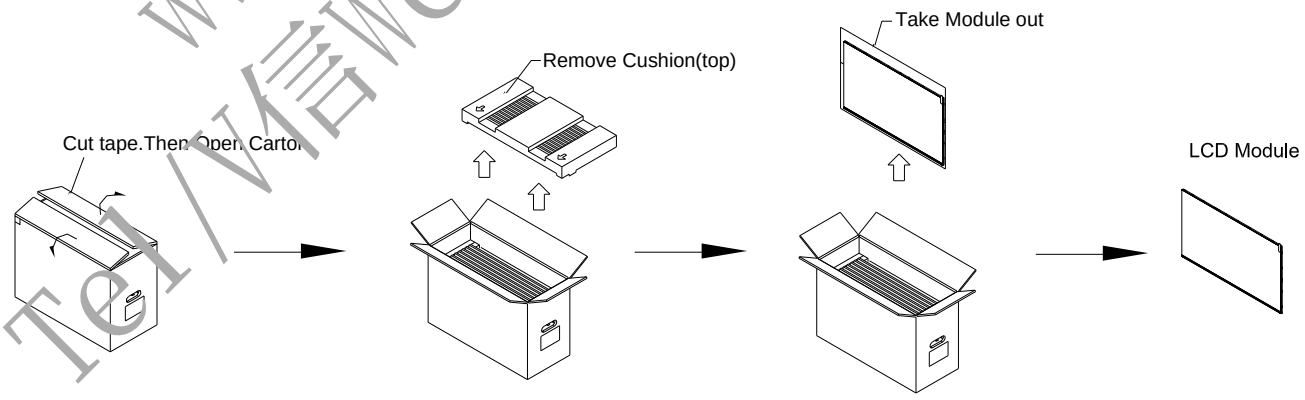



Figure. 8-3 Un-Packing method

## 9. INX MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.


(a) Model Name: M238HCA-L7Z

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) INX barcode definition:

Serial ID: XX-XX-X-XX-YMD-L-NNNN

| Code | Meaning | Description |
|---|---|---|
| XX | INX internal use | - |
| XX | Revision | Cover all the change |
| X | INX internal use | - |
| XX | INX internal use | - |
| YMD | Year, month, day | Year: 0~9, 2001=1, 2002=2, 2003=3…2010=0, 2011=1, 2012=2…<br>Month: 1~12=1, 2, 3, ~, 9, A, B, C<br>Day: 1~31=1, 2, 3, ~, 9, A, B, C, ~, W, X, Y, exclude I, O, and U. |
| L | Product line # | Line 1=1, Line 2=2, Line 3=3, … |
| NNNN | Serial number | Manufacturing sequence of product |

(d) Customer's barcode definition:

Serial ID: CM- XXXXX-X-X-X-XX-L-XX-L-YMD-NNNN

| Code | Meaning | Description |
|---|---|---|
| CM | Supplier code | INX=CM |
| XXXXX | Model number | M238HCA-L7Z= XXXXX |
| X | Revision code | Non ZBD: 1,2,~,8,9 / ZBD: A~Z |
| X | Source driver IC code | Century=1, CLL=2, Demos=3, Epson=4, Fujitsu=5, Himax=6, Hitachi=7, Hynix=8, LDI=9, Matsushita=A, NEC=B, Novatek=C, OKI=D, Philips=E, Renasas=F, Samsung=G, Sanyo=H, Sharp=I, TI=J, Topro=K, Toshiba=L, Windbond=M, ILITEK=Q, Fiti=Y, None IC =Z |
| X | Gate driver IC code | |
| XX | Cell location | Tainan Taiwan=TN, Ningbo China=CN, Hsinchu Taiwan=SC |
| L | Cell line # | 1,2,~,9,A,B,~,Y,Z |
| XX | Module location | Tainan, Taiwan=TN ; Ningbo China=NP ; Shenzhen China=SH ; Nanhai China=NH |
| L | Module line # | 1,2,~,9,A,B,~,Y,Z |
| YMD | Year, month, day | Year: 0~9, 2001=1, 2002=2, 2003=3…2010=0, 2011=1, 2012=2…<br>Month: 1~12=1, 2, 3, ~, 9, A, B, C<br>Day: 1~31=1, 2, 3, ~, 9, A, B, C, ~, T, U, V |
| NNNN | Serial number | By LCD supplier |

(e) FAB ID(UL Factory ID):

| Region | Factory ID |
|---|---|
| TWINX | GEMN |
| NBINX | LEOO |
| NBINX | VIRO |
| NHINX | CAPG |

# 10. PRECAUTIONS

## 10.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) To assemble or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) It's not permitted to have pressure or impulse on the module because the LCD panel and Backlight will be damaged.

(4) Always follow the correct power sequence when LCD module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.

(5) Do not pull the I/F connector in or out while the module is operating.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) It is dangerous that moisture come into or contacted the LCD module, because moisture may damage LCD module when it is operating.

(9) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(10)When ambient temperature is lower than 10ºC may reduce the display quality. For example, the response time will become slowly.

## 10.2 STORAGE PRECAUTIONS

(1) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0℃ to 35℃ and relative humidity of less than 90%

(2) Do not store the TFT – LCD module in direct sunlight

(3) The module should be stored in dark place. It is prohibited to apply sunlight or fluorescent light in storing

## 10.3 OPERATION PRECAUTIONS

(1) The LCD product should be operated under normal condition.

Normal condition is defined as below :

Temperature : 20±15℃

Humidity: 65±20%

Display pattern : continually changing pattern(Not stationary)

(2) If the product will be used in extreme conditions such as high temperature,high humidity,high altitude ,display pattern or operation time etc…It is strongly recommended to contact INX for application engineering advice . Otherwise , Its reliability and function may not be guaranteed.

## 10.4 SAFETY PRECAUTIONS

(1) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(2) After the module's end of life, it is not harmful in case of normal operation and storage.

## 10.5 SAFETY STANDARDS

The LCD module should be certified with safety regulations as follows:

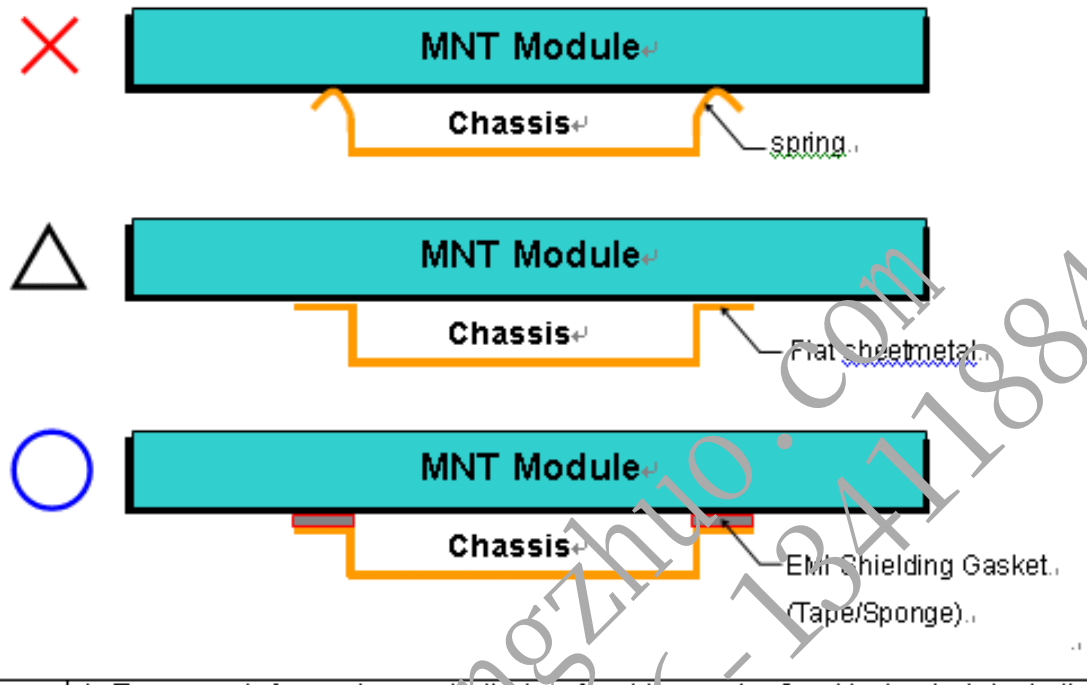
(1) UL60950-1 or updated standard.

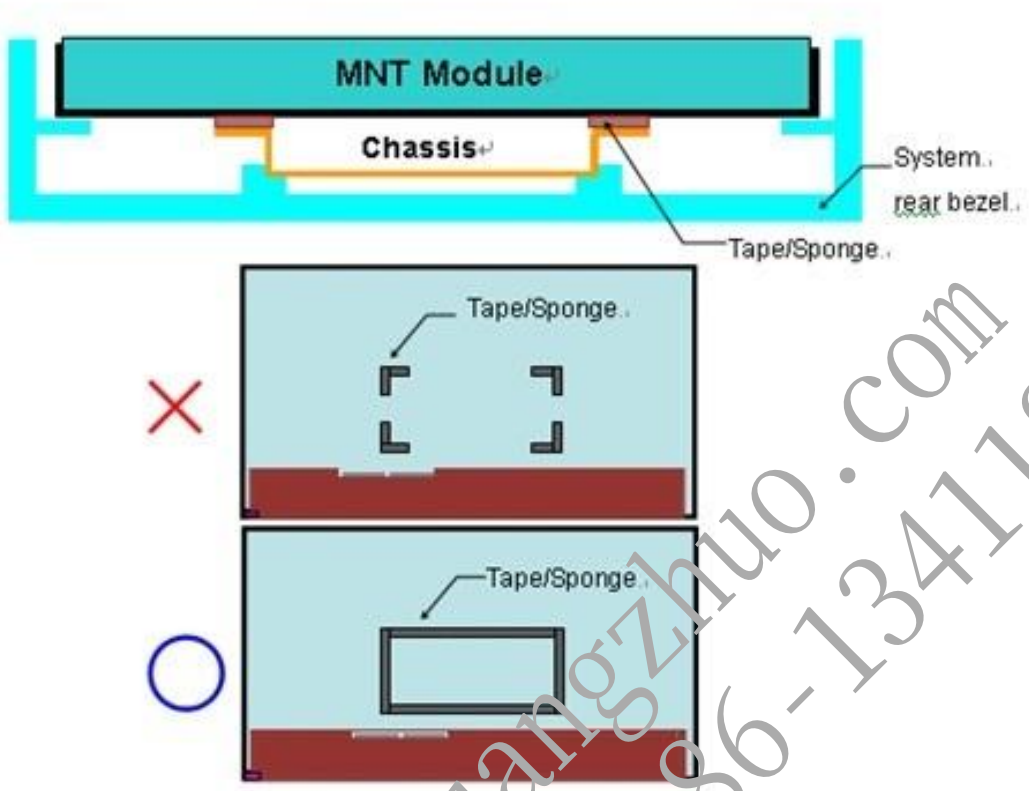
(2) IEC60950-1 or updated standard.

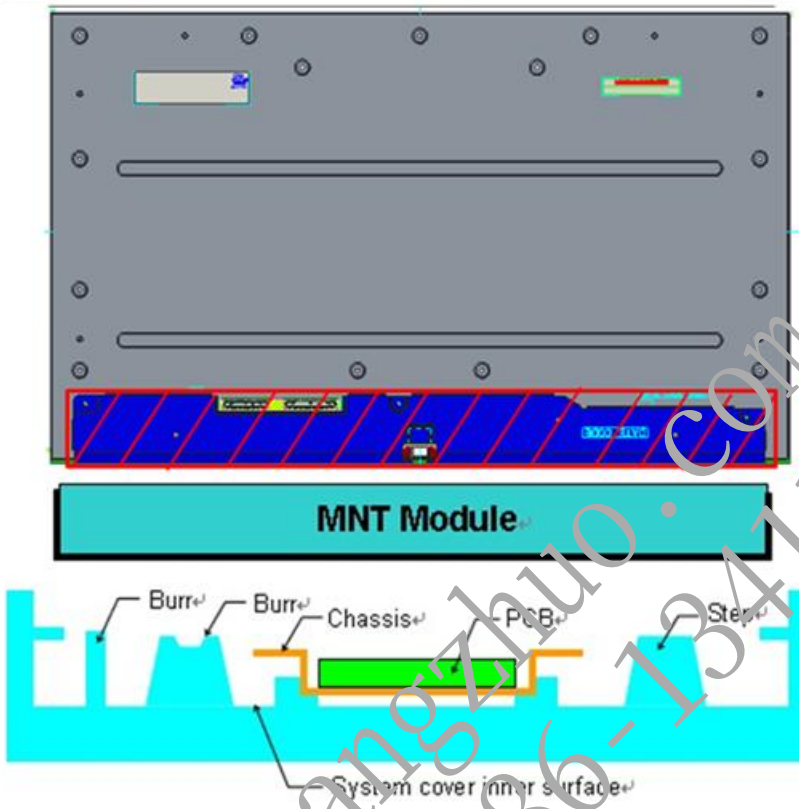
## 10.6 OTHER

When fixed patterns are displayed for a long time, remnant image is likely to occur.

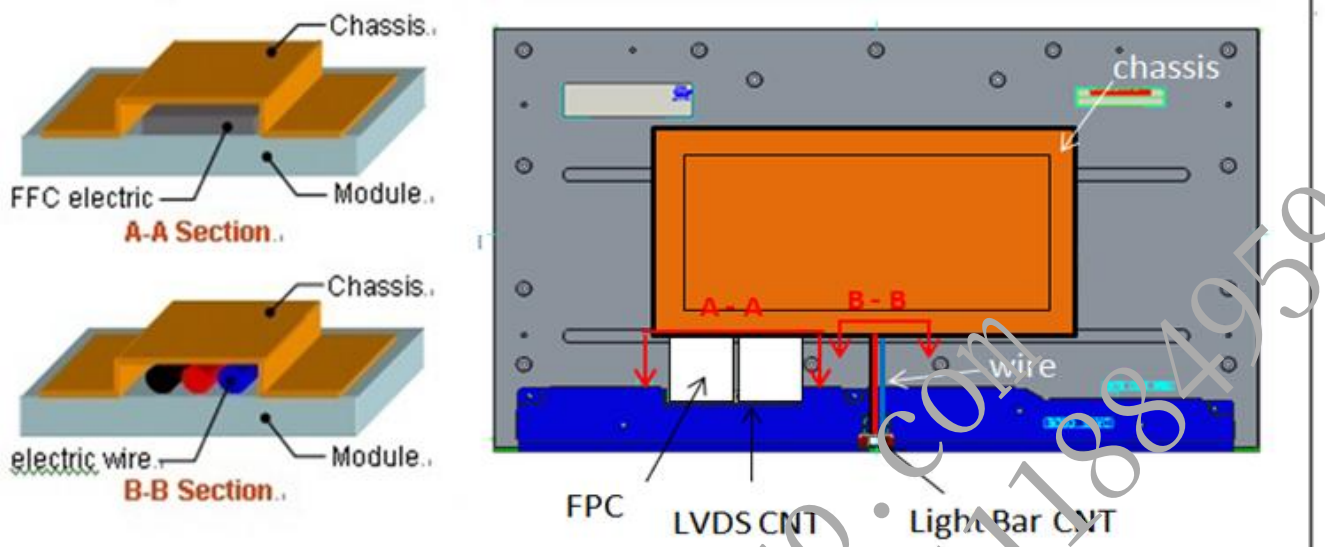
## Appendix 1. SYSTEM COVER DESIGN NOTICE

| 1. | Set Chassis and MNT Module touching Mode |
|---|---|
| |  |
| Definition | a) To prevent from abnormal display & white spot after Mechanical test, it is not recommended to used spring type chassis.<br>b) We suggest the contact mode between Chassis and Module rear cover is Tape/Sponge, sencond is Flat sheetmetal type chassis. |

| 2 | Tape/sponge design on system inner surface |
|---|---|
| |  |
| Definition | a) To prevent from abnormal display & white spot after Mechanical test, We suggest using Tape/Sponge as medium between chassis and Module rear cover could reduce the occurrence of white spot.<br>b) When using the Tape/Sponge, suggest it be lay over between set chassis and module rear cover. it is not recommended to add tape/sponge in separate location. Since each tape/sponge may act as pressure concentration location. |

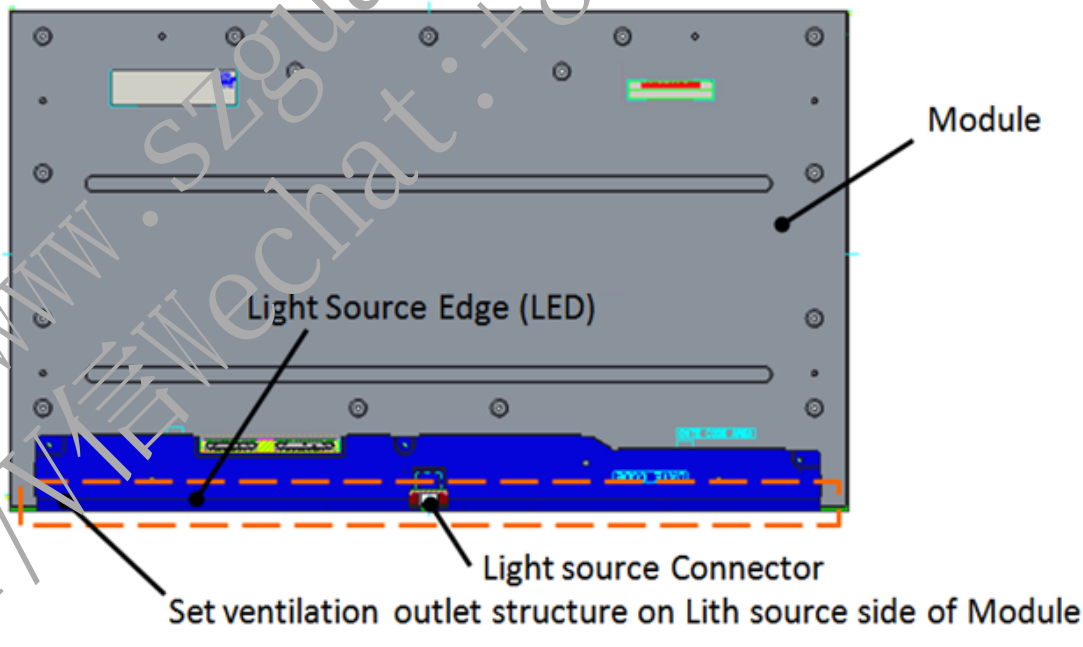
| 3 | System inner surface examination |
|---|---|
| |  |
| Definition | a). Burr at logo edge, step, protrusion or PCB board will easily cause white spot.<br>b). Keeping flat surface underneath module is recommended.<br>c). The area ( ) on Module PCBA and Light bar connector should keep at least 1mm gap to any structure with System cover inner surface. |

| 4 | The overlapping part on System's Chassis and electric wire needs gap structure. |
|---|---|

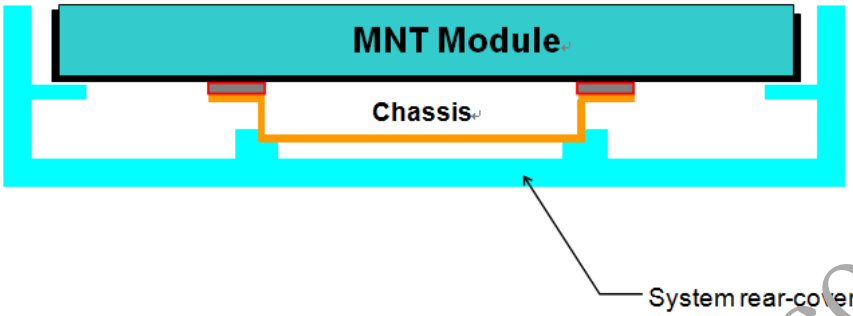


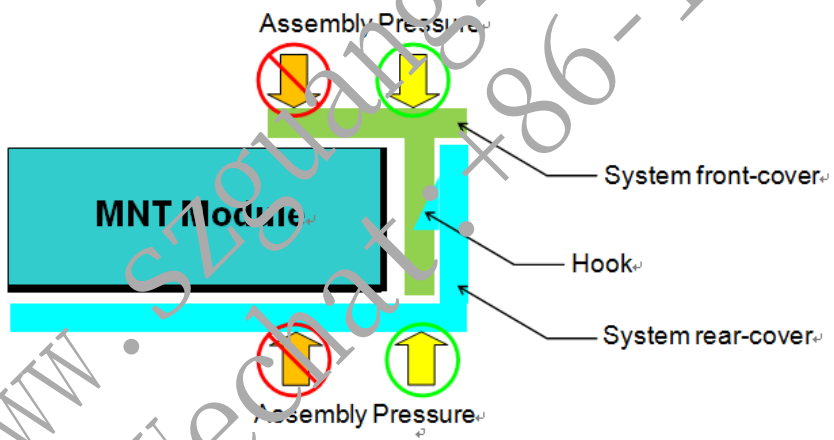

| Definition | The overlapping part on System's Chassis and electric wire (FPC、FFC and wire) needs gap structure to avoid display of white spot by pressing overlapping part cause interference. |
|---|---|

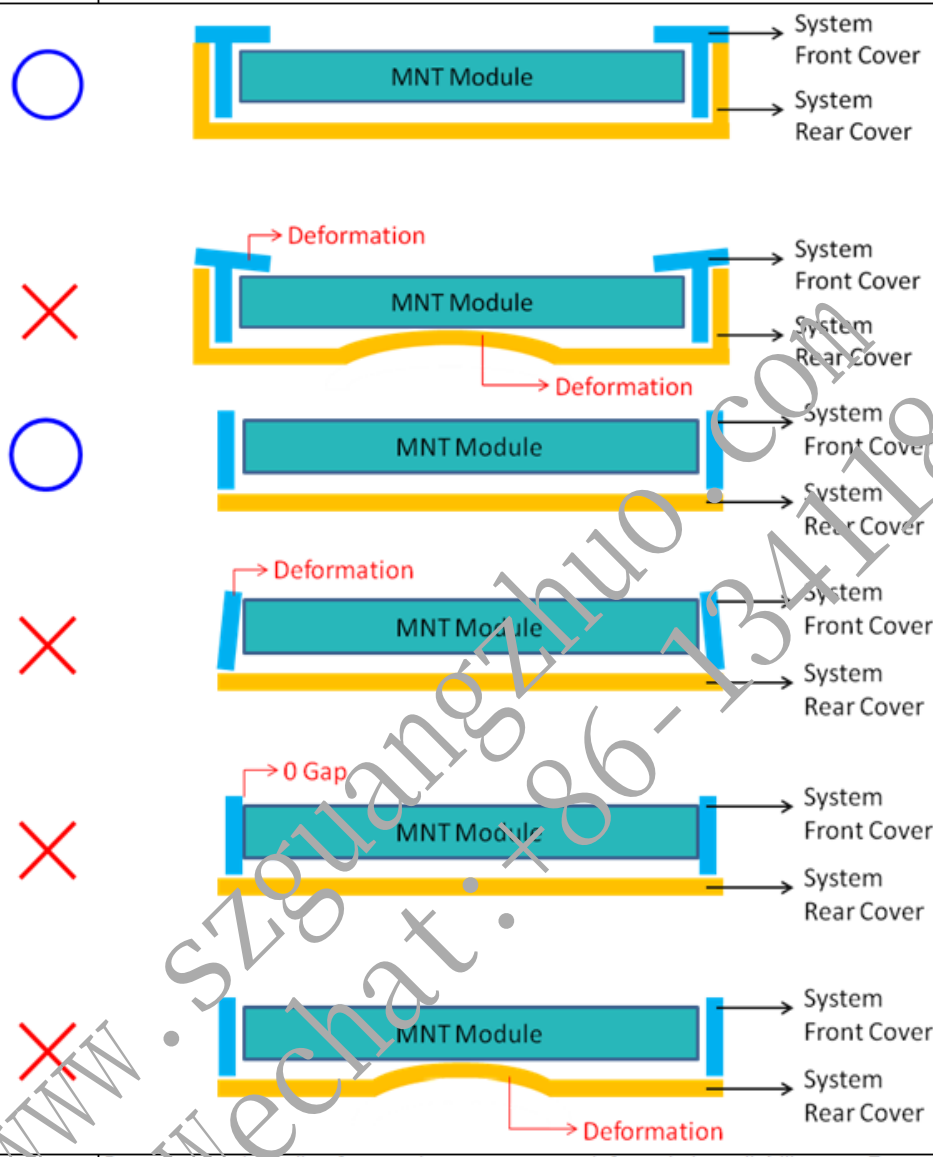
| 5 | System cover's ventilation outlet structure |
|---|---|

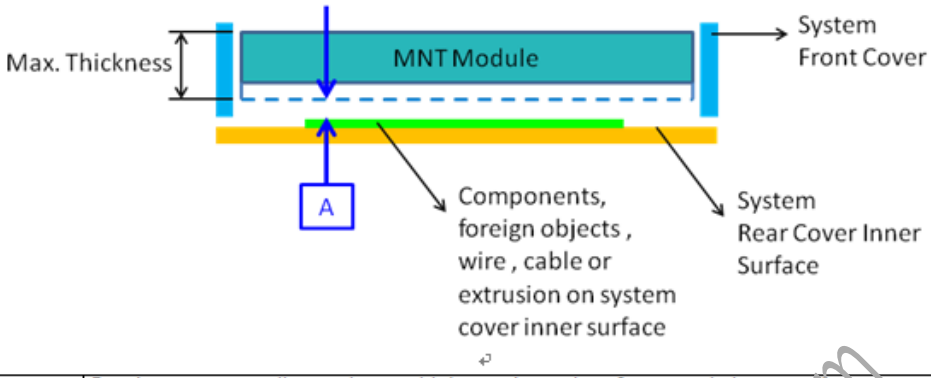


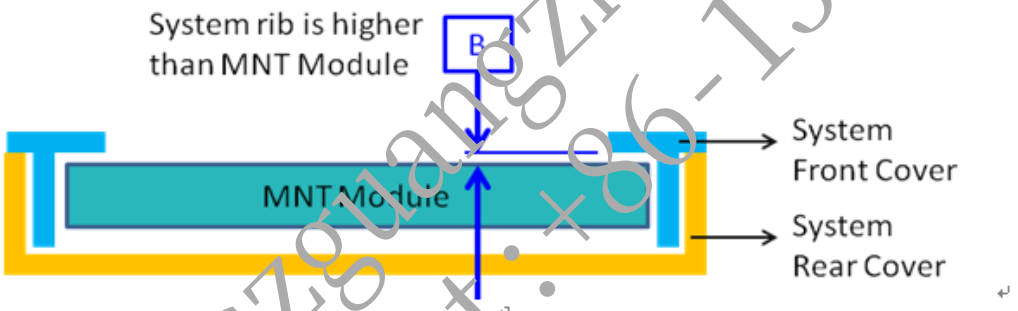

| Definition | To prevent from abnormal display of light leakage, We suggest to set ventilation outlet structure on side of Module Light bar in system cover inner surface. |
|---|---|

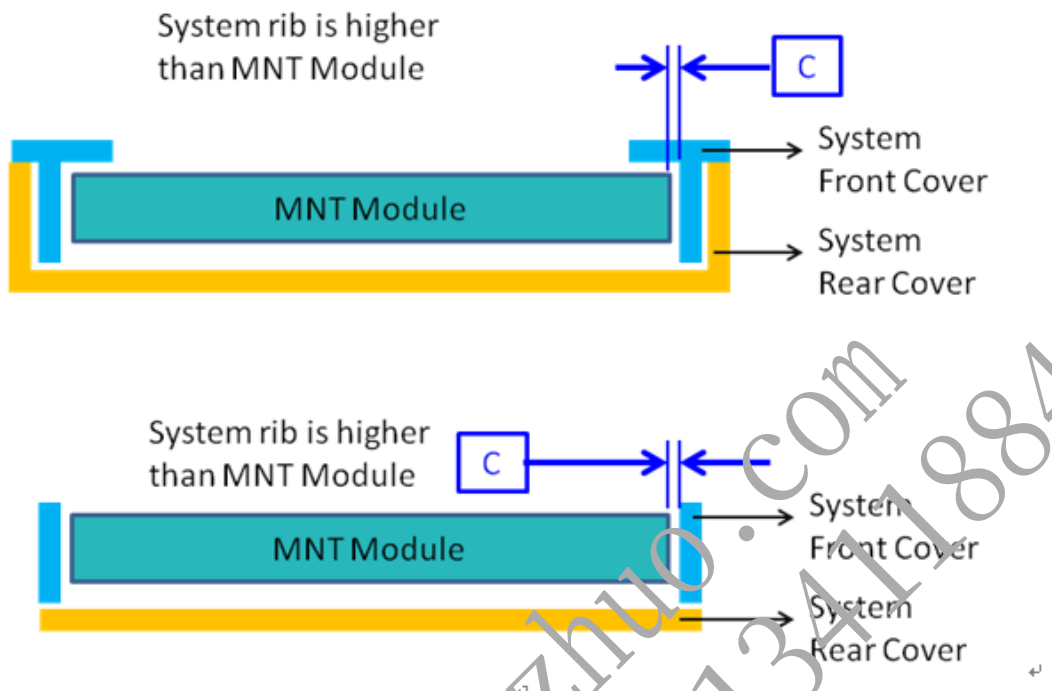
| 6 | Material used for system rear-cover |
|---|---|
| |  |
| Definition | System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw's boss positioning for module's bracket are deformed during open-close test. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference. |

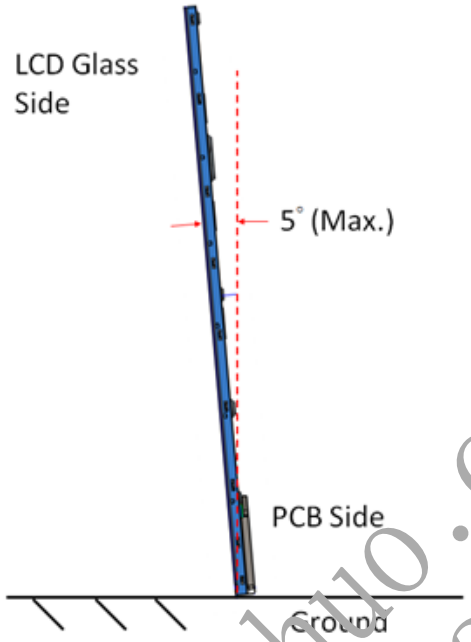
| 7 | Assembly SOP examination for system front-cover with Hook design |
|---|---|
| |  |
| Definition | To prevent panel crack during system front-cover assembly process with hook design, it is not recommended to press panel or any location that related directly to the panel. |

| 8 | Permanent deformation of system cover after reliability test |
|---|---|
| |  |
| Definition | System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack.<br>Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference. |

| 9 | Design gap A between panel & any components on system rear-cover |
|---|---|
| |  |
| Definition | Gap between panel's maximum thickness boundary & system's inner surface components such as wire, cable, extrusion is needed for preventing from backpack or pogo test fail. Because zero gap or interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur.<br>Maximum flatness of panel and system rear-cover should be taken into account for gap design.<br>Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference. |

| 10 | Design gap B between system front-cover & panel surface |
|---|---|
| |  |
| Definition | Gap between system front-cover & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system front-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test, or during pooling inspection procedure.<br>To remain sufficient gap, design with system rib higher than maximum panel thickness is recommended.<br>Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference. |

| 11 | Design gap C between panel & system front-cover or protrusions |
|---|---|
| |  |
| Definition | Gap between panel & system front-cover or protrusions is needed to prevent shock test failure. Because system front-cover or protrusions with small gap may hit panel during the test. Issue such as cell crack, abnormal display may occur.<br>The gap should be large enough to absorb the maximum displacement during the test.<br>Note: If the interference cannot be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference. |

| 12 | For MNT borderless module usage, forward tilt angle limitation is 5° maximum. |
|---|---|
| |  |
| Definition | For MNT borderless module usage, forward tilt angle limitation is 5° maximum.<br>MNT borderless module LCD glass and blacklight unit are bonded by tape, to avoid tape peeling issue, we suggest for MNT borderless module usage, forward tilt angle limitation is 5° maximum.<br>Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference. |

## Appendix 2. OUTLINE DRAWING