SPECIFICATION
FOR
APPROVAL

( ) **Preliminary Specification**
(◆) **Final Specification**

Title	14.0" FHD TFT LCD

Customer	
MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	LP140WF9
Suffix	SPR1

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE
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Contents

Record of Revisions

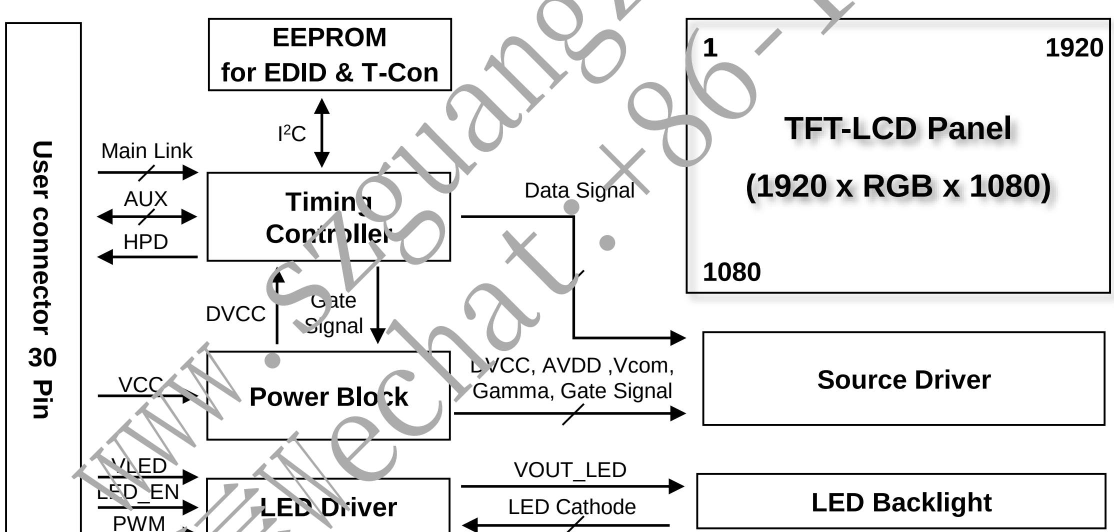
Revision No	Revision Date	Page	Before	After	EDID version
0.0	Aug. 11. 2021	All	First Draft (Preliminary Specification)	-	-
0.1	Aug. 30. 2021	26	-	LCM Label update	-
0.2	Sep. 08. 2021	55-60	-	Add E-EDID Table (Checksum: D5 / 90)	0.0
0.3	Oct. 07. 2021	55-60	E-EDID Table (Checksum: D5 / 90)	E-EDID Table (Checksum: 76 / 90)	0.1
0.4	Oct. 29. 2021	5, 21	Weight: 285g max.	Weight: 260g max.	0.1
0.5	Dec.28.2021	26~28	-	Packing update	0.1
0.6	Jan. 06. 2022	17	Power sequence T9: - (min.) / - (max.) T10: 0 (min.)	Power sequence T9: 1ms (min.) / 5ms (max.) T10: 35ms (min.)	0.1
0.7	Jan. 18. 2022	17	Power sequence T9: 1ms (min.) / 5ms (max.)	Power sequence T9: 0ms (min.) / - ms (max.)	0.2
		55-60	E-EDID Table (Checksum: 76 / 90)	E-EDID Table (Checksum: 2B / 90)	-
1.0	Feb. 18, 2022	-	Final		

LG Display

1. General Description

1-1. Introduction

The LP140WF9 is a Color Active Matrix Liquid Crystal Display with an integral LED backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. This TFT-LCD has 14.0 inches diagonally measured active display area with FHD resolution (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 8-bit gray scale signal for each dot, thus, presenting a palette of more than 16,777,216 colors. The LP140WF9 has been designed to apply the interface method that enables low power, high speed, low EMI. The LP140WF9 is intended to support applications where thin thickness, low power are critical factors and graphic displays are important. In combination with the vertical arrangement of the sub-pixels, the LP140WF9 characteristics provide an excellent flat display for office automation products such as Notebook PC.



1-2. General Feature

Active Screen Size		14.0 inches diagonal
Outline Dimension		315.81(H, Typ.) × 186.07(V, Typ.) × 3.0(D, Max.) [mm] without PCB
Pixel Pitch		0.1611 mm X 0.1611 mm
Pixel Format		1920 horiz. by 1080 vert. Pixels RGB strip arrangement
Color Depth		8bit, 16,777,216 colors
Luminance, White		400 cd/m^2(Typ.)
Power Consumption		Total 3.54W (Max.) Logic: 0.44W (Max. @ Mosaic), B/L: 3.10W (Max.)
Weight		260g (Max.)
Display Operating Mode		Normally black
Surface Treatment		Anti-Glare treatment (3H) of the front Polarizer
Color Gamut		sRGB 100%
LED Dimming Control mode		DC Dimming
RoHS Compliance		Yes
BFR / PVC / As Free		Yes for all
eDP version(Tcon)		eDP1.4
DPCD version		Ver1.4
Function	PSR	PSR2
	sDRRS	sDRRS 40Hz
	DMRRS	Support
	Adaptive sync	Freesync support
	NVSR	Not support
	SSC	Support

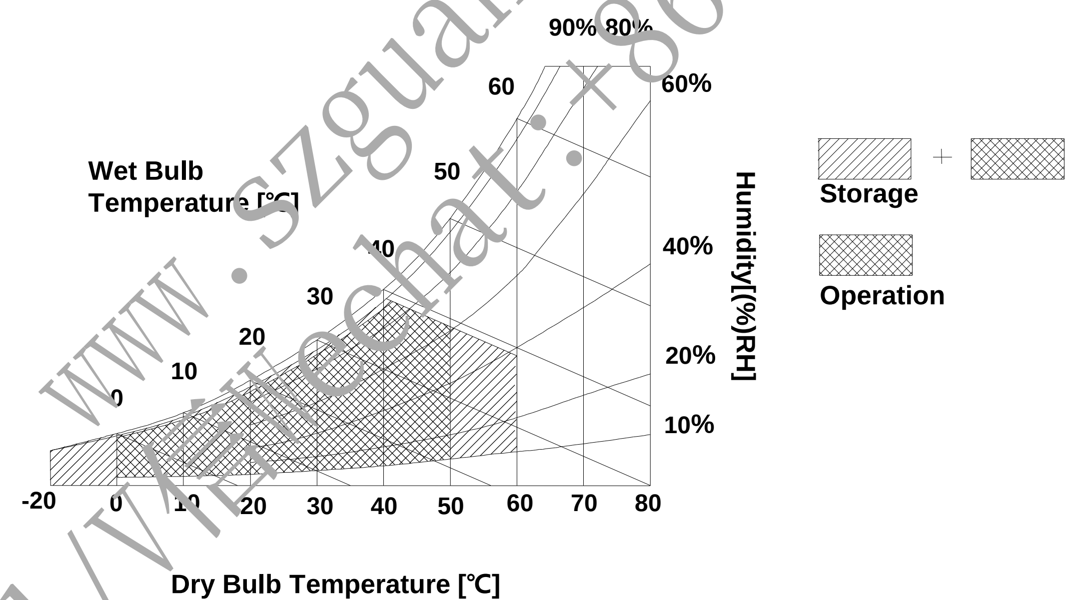
2. Absolute Maximum Ratings

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Values		Units	Notes
		Min	Max		
Power Input Voltage	VCC	-0.3	4.0	V_{DC}	at 25 ± 2°C
Operating Temperature	T_{OP}	0	50	°C	1
Storage Temperature	T_{ST}	-20	60	°C	1,2
Operating Ambient Humidity	H_{OP}	10	90	%RH	1
Storage Humidity	H_{ST}	10	90	%RH	1,2

Note : 1. Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39°C Max, and no condensation of water.
Note : 2. Storage Condition is guaranteed under packing condition.



3. Electrical Specifications

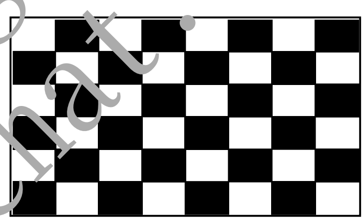
3-1. LCD Electrical Characteristics

Table 2. LCD ELECTRICAL CHARACTERISTICS

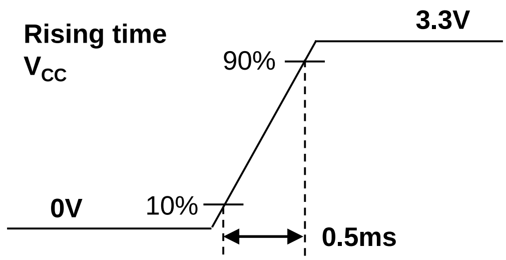
Parameter		Symbol	Values			Unit	Notes
			Min	Typ	Max		
Power Supply Input Voltage		Vcc	3.0	3.3	3.6	V	1
Permissive Power Supply Input Ripple		VCCrp	-	-	100	mV_{p-p}	
Power Supply Input Current	Mosaic	Icc	-	121	134	mA	2
Power Consumption	Mosaic	Pcc	-	0.40	0.44	W	
Power Supply Inrush Current		Icc_P	-	-	1.5	A	3
Differential Impedance		ZLVDS	90	100	110	Ω	

Note)

1. The measuring position is the connector of LCM and the test conditions are under 25℃, fv = 60Hz
2. The specified I_{CC} current and power consumption are under the V_{CC} = 3.3V , 25℃, fv = 60Hz condition and Mosaic pattern.



3. The V_{CC} rising time is same as the minimum of T1 at Power on sequence.

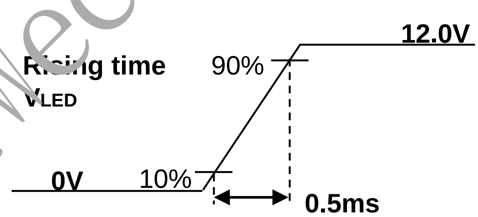


3-2. LED Backlight Electrical Characteristics

Table 3. LED B/L ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Values			Unit	Notes
			Min	Typ	Max		
LED Power Input Voltage		V_{LED}	5.0	12.0	21.0	V	1
LED Power Input Current		I_{LED}	-	250	258	mA	2
LED Power Consumption		P_{LED}	-	3.0	3.1	W	
LED Power Inrush Current		I_{LED_P}	-	-	1.5	A	3
PWM Duty Ratio			5	-	100	%	4
PWM Resolution				10		Bit	5
PWM Jitter			0	-	0.05	%	6
PWM Frequency		F_{PWM}	200	-	2000	Hz	7
PWM	High Level Voltage	V_{PWM_H}	2.5	-	3.6	V	
	Low Level Voltage	V_{PWM_L}	0	-	0.3	V	
	Rising Time	Tr_{PWM}	-	-	500	us	
	Falling Time	Tf_{PWM}	-	-	500	us	
LED_EN	High Voltage	$V_{LED\_EN\_H}$	2.5	-	3.6	V	
	Low Voltage	$V_{LED\_EN\_L}$	0	-	0.3	V	
Life Time			15,000	-	-	Hrs	9

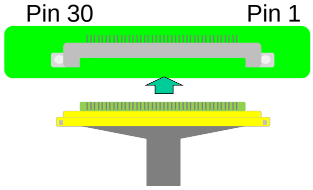
Note)
1. The measuring position is the connector of LCM and the test conditions are under 25℃.
2. The current and power consumption with LED Driver are under the V_{LED} = 12.0V , 25℃, PWM Duty 100% and White pattern with the normal frame frequency operated(60Hz).
3. The V_{LED} rising time is same as the minimum of T13 at Power on sequence.



4. The operation of LED Driver below minimum dimming ratio may cause flickering or reliability issue.
5. 10bit resolution means it's possible to change PWM duty by 0.1% step. (8bit operated by 0.4% step)
6. If Jitter of PWM is bigger than maximum, it may induce flickering.
7. This Spec is not effective at 100% dimming ratio as an exception because it has DC level equivalent to 0Hz. In spite of acceptable range as defined, the PWM Frequency should be fixed and stable for more consistent brightness control at any specific level desired.
8. The life time is determined as the time at which brightness of LCD is 50% compare to that of minimum value specified in table 7. under general user condition.

3-3. Interface Connections

Table 4. MODULE CONNECTOR PIN CONFIGURATION (CN1)

Pin	Symbol	Description	Notes
1	NC Reserved	Reserved for LCD manufacturer's use	
2	GND	High Speed Ground	
3	Lane1_N	Complement Signal Link Lane 1	
4	Lane1_P	True Signal Link Lane 1	
5	GND	High Speed Ground	
6	Lane0_N	Complement Signal Link Lane 0	
7	Lane0_P	True Signal Link Lane 0	
8	GND	High Speed Ground	
9	AUX_CH_P	True Signal Auxiliary Channel	[Connector]
10	AUX_CH_N	Complement Signal Auxiliary Channel	HIROSE, IKN38B-30S-0.5H
11	GND	High Speed Ground	(30pin, 0.5pitch) or equivalent
12	VCC	LCD logic and driver power	
13	VCC	LCD logic and driver power	[Connector pin arrangement]
14	LCD Self Test or NC	LCD Panel Self Test Enable (Optional)	Pin 30 Pin 1
15	GND	LCD logic and driver ground	
16	GND	LCD logic and driver ground	
17	HPD	HPD signal pin	
18	BL_GND	LED Backlight ground	
19	BL_GND	LED Backlight ground	
20	BL_GND	LED Backlight ground	
21	BL_GND	LED Backlight ground	[LGD P-Vcom using information]
22	BL ENABLE	LED Backlight control on/off control	1. Pin for P-Vcom : #24, #25
23	BL PWM	System PWM signal input for dimming	2. P-Vcom Address : 0101000x
24	NC Reserved	Reserved for LCD manufacture's use	
25	NC Reserved	Reserved for LCD manufacture's use	
26	VLED	LED Backlight power (12V Typical)	
27	VLED	LED Backlight power (12V Typical)	
28	VLED	LED Backlight power (12V Typical)	
29	VLED	LED Backlight power (12V Typical)	
30	NC Reserved	Reserved for LCD manufacture's use	

3-3-1. Input/output signal circuit

Figure1.HPD Output circuit is as below

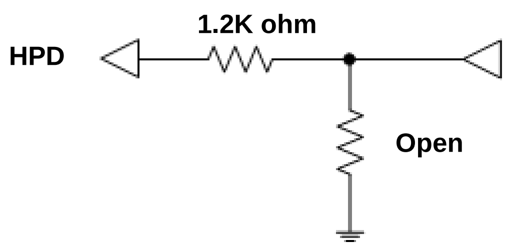


Figure2.BL PWM input circuit is as below

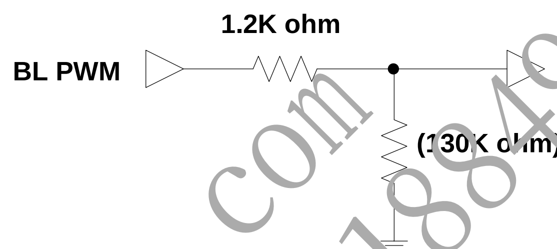


Figure3.BL Enable input circuit is as below

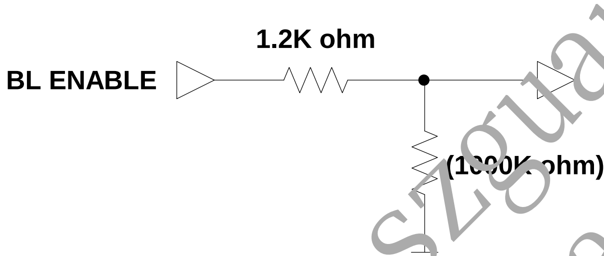
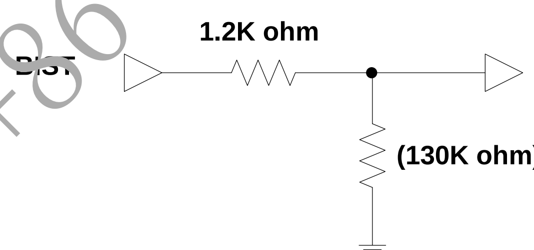
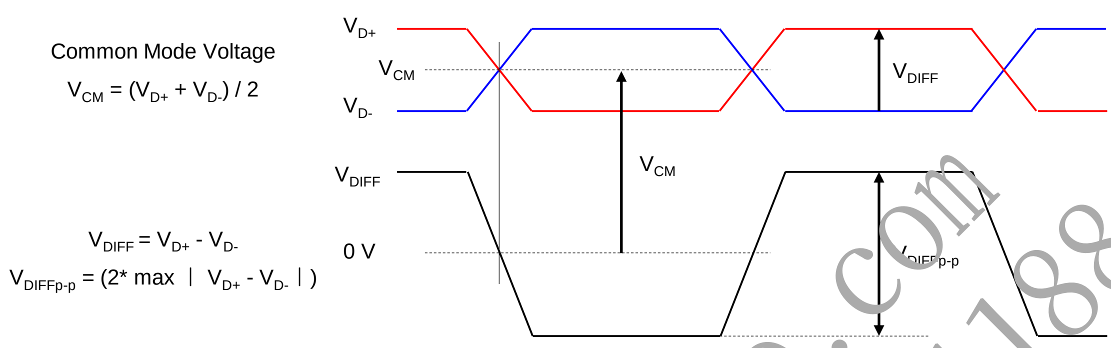


Figure4.BIST input circuit is as below



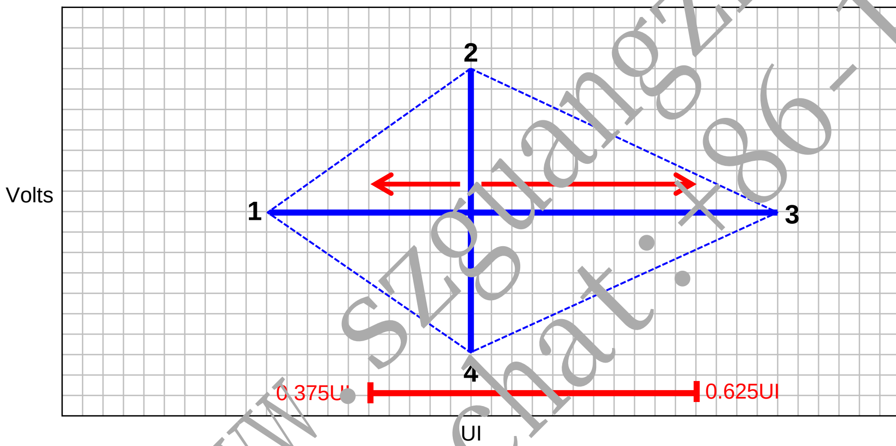
3-4. eDP Signal Timing Specifications

3-4-1. Definition of Differential Voltage



[Definition of Differential Voltage]

3-4-2. Main Link EYE Diagram



[EYE Mask at TP3_EQ/RX_EQ]

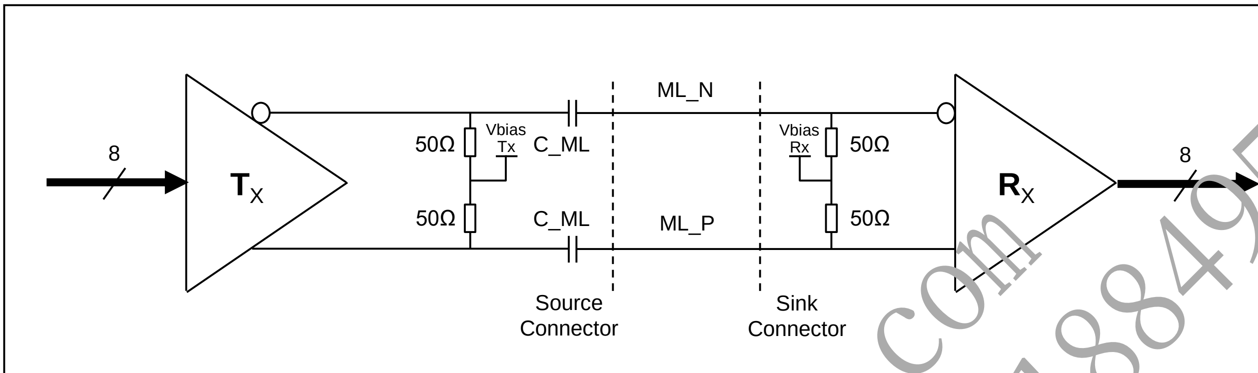
Point	Time(UI)	Voltage(V)
1	Any UI location (0mV)	0.000
2	0.375<point2<0.625	0.0375
3	Point1 + 0.5UI	0.000
4	0.375<point4<0.625	-0.0375

[eDP TP3_EQ EYE Mask Vertices]

Point	Time(UI)	Voltage(V)
1	Any UI location (0mV)	0.000
2	0.375<point2<0.625	0.035
3	Point1 + 0.45UI	0.000
4	0.375<point2<0.625	-0.035

[eDP RX_EQ EYE Mask Vertices]

3-4-3. eDP Main Link Signal

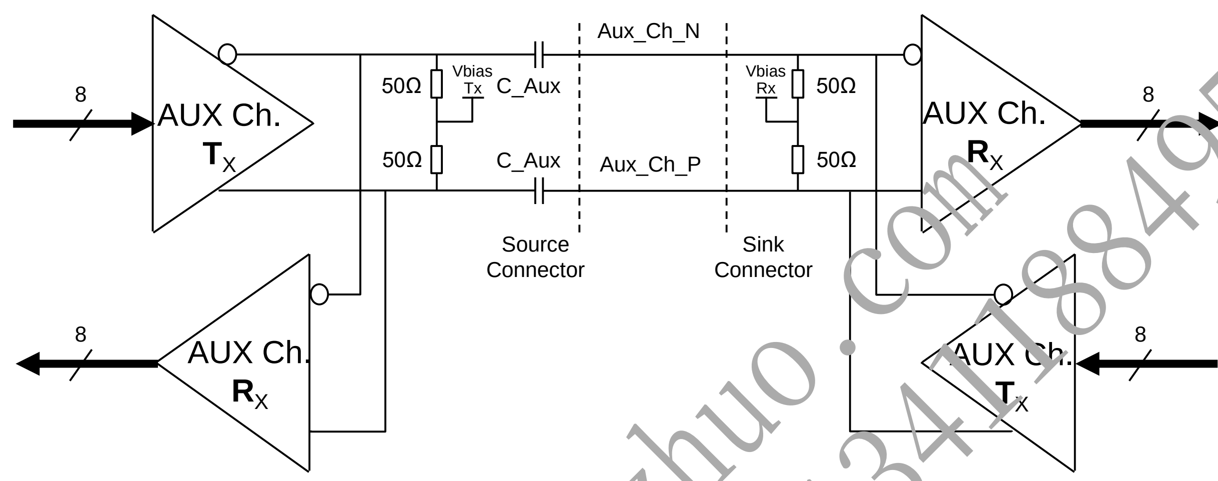


[Main Link Differential Pair]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval for high bit rate (2.7Gbps / lane)	UI_HBR	-	370	-	ps	
Unit Interval for reduced bit rate (2.43Gbps / lane)	UI_2.16	-	412	-	ps	
Unit Interval for reduced bit rate (2.16Gbps / lane)	UI_2.16	-	463	-	ps	
Unit Interval for reduced bit rate (1.62Gbps / lane)	UI_RBR	-	617	-	ps	
Link Clock Down Spreading	Amplitude	0	-	0.5	%	
	Frequency	30	-	33	kHz	
Differential peak-to-peak Voltage at Sink side connector	$V_{TX-DIFFp-p}$	75	-	-	mV	TP3_EQ
EYE width at Sink side connector	$T_{TX-EYE-CONN}$	0.5	-	-	UI	TP3_EQ
Differential peak-to-peak voltage at RX package pin	$V_{RX-DIFFp-p}$	70	-	-	mV	TP4_EQ
EYE width at RX package pin	$T_{RX-EYE-CONN}$	0.45	-	-	UI	TP4_EQ
Rx DC common mode voltage	$V_{RX\ CM}$	0	-	1.0	V	
AC Coupling Capacitor	C_{SOURCE_ML}	75		200	nF	Source side

Note)
1. Termination resistor is typically integrated into the transmitter and receiver implementations.
2. AC Coupling Capacitor is not placed at the sink side.
3. In cabled embedded system, it is recommended the system designer ensure that EYE width and voltage are met at the sink side connector pins.

3-4-4. eDP AUX Channel Signal

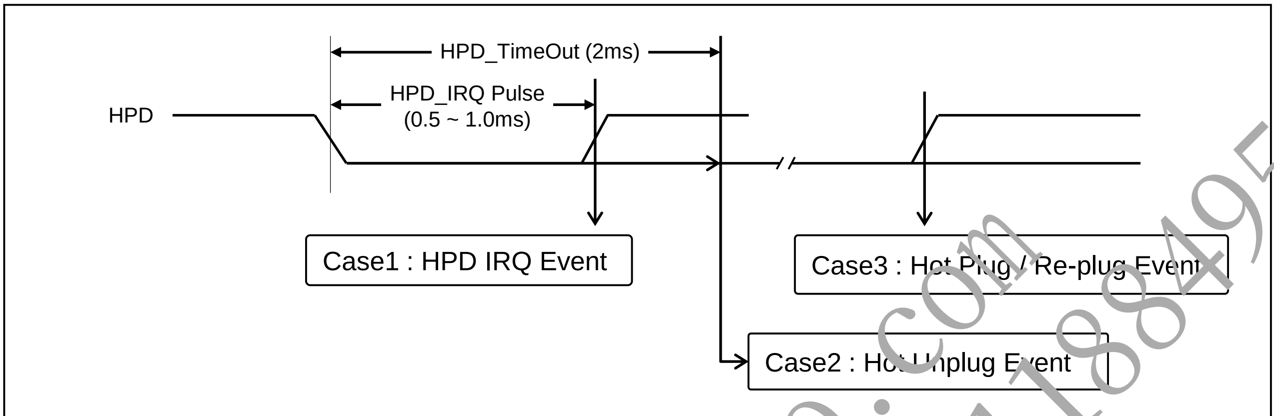


[Recommended eDP AUX Channel Differential Pair]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
AUX Unit Interval	UI	0.4	-	0.6	us	
AUX Jitter at Tx IC Package Pins	T_{jitter}	-	-	0.04	UI	Equal to 24ns
AUX Jitter at Rx IC Package Pins		-	-	0.05	UI	Equal to 30ns
AUX Peak-to-peak voltage at TX package pins (TP1)	$V_{AUX\_DIFFp\text{-}p}$	0.18	0.20	1.38	V	
AUX Peak-to-peak voltage at TP3		0.14	-	1.36	V	
AUX EYE width at Connector Pins of Tx and Rx		0.98	-	-	UI	
AUX DC common mode voltage	$V_{AUX\text{-}CM}$	0	-	1.0	V	
AUX AC Coupling Capacitor	$C_{SOURCE\text{-}AUX}$	75		200	nF	Source side

Note)
1. Termination resistor is typically integrated into the transmitter and receiver implementations.
2. AC Coupling Capacitor is not placed at the sink side.
3. $V_{AUX\_DIFFp\text{-}p} = 2^* \mid V_{AUXP} - V_{AUXN} \mid$
4. If Vaux-cm does not satisfy the specification, there could be problem at Aux ch. Rx and Tx communication.

3-4-5. eDP HPD Signal



[HPD Events]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
HPD Voltage	HPD	2.25	-	3.6	V	Sink side Driving
Hot Plug Detection Threshold		2.0	-	-	V	Source side Detecting
Hot Unplug Detection Threshold		-	-	0.8	V	
HPD_IRQ Pulse Width	HPD_IRQ	0.5	-	1.0	ms	
HPD_TimeOut		2.0	-	-	ms	HPD Unplug Event

Note)

1. HPD IRQ : Sink device wants to notify the Source device that Sink's status has changed so it toggles HPD line, forcing the Source device to read its Link / Sink Receiver DPCD field via the AUX-CH
2. HPD Unplug : The Sink device is no longer attached to the Source device and the Source device may then disable its Main Link as a power saving mode
3. Plug / Re-plug : The Sink device is now attached to the Source device, forcing the Source device to read its Receiver capabilities and Link / Sink status Receiver DPCD fields via the AUX-CH

3-5. Signal Timing Specifications

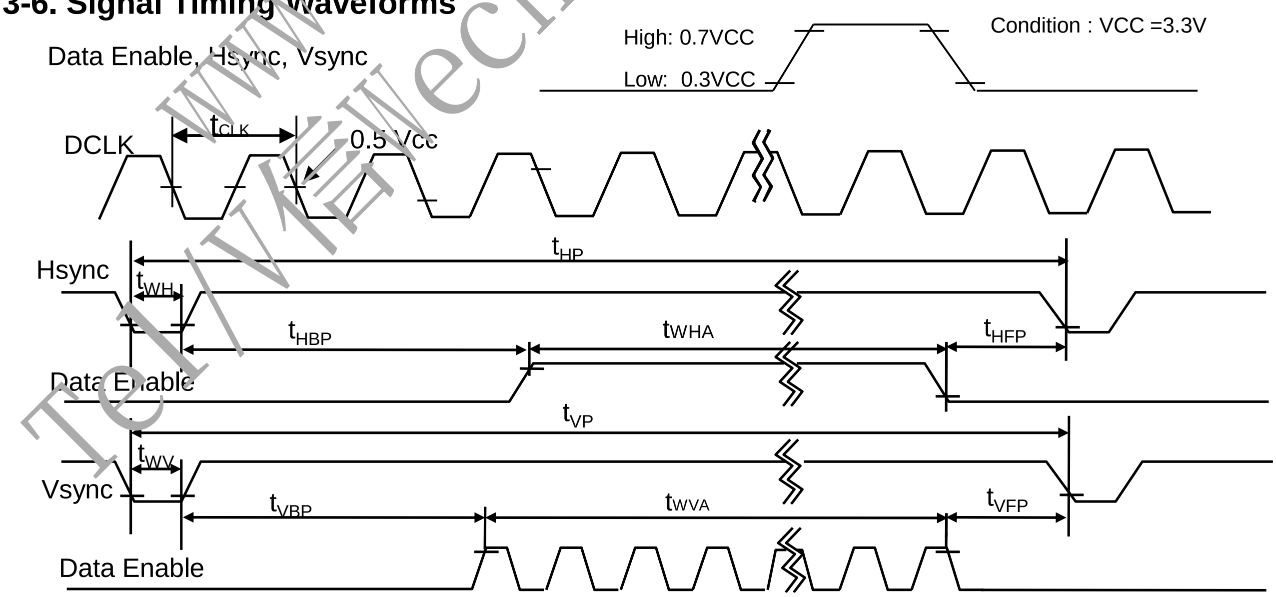
This is the signal timing required at the input of the User connector. All of the interface signal timing should be satisfied with the following specifications and specifications of eDP Tx/Rx for its proper operation.

Table 4. TIMING TABLE

ITEM	Symbol		Min	Typ	Max	Unit	Note
DCLK	Frequency	f_{CLK}	-	138.7	-	MHz	
Hsync	Period	t_{HP}	2072	2080	2088	t_{CLK}	
	Width	t_{WH}	32	32	32		
	Width-Active	t_{WHA}		1920			
Vsync	Period	t_{VP}	1108	1111	1114	t_{HP}	
	Width	t_{WV}	5	5	5		
	Width-Active	t_{WVA}		1080			
Data Enable	Horizontal back porch	t_{HBP}	72	80	88	t_{CLK}	
	Horizontal front porch	t_{HFP}	48	48	48		
	Vertical back porch	t_{VBP}	20	23	24	t_{HP}	
	Vertical front porch	t_{VFP}	3	3	5		
Refresh rate		Hz	-	60	-		

Notice. all reliabilities are specified for timing specification based on refresh rate of 60Hz. However, LP140WF9 has a good actual performance even at lower refresh rate (e.g. 40Hz or 50Hz) for power saving Mode, whereas LP140WF9 is secured only for function under lower refresh rate. 60Hz at Normal mode, 50Hz, 40Hz at Power save mode. Don't care Flicker level (Power save mode).

3-6. Signal Timing Waveforms



3-7. Color Input Data Reference

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color ; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Table 5. COLOR DATA REFERENCE

Color		Input Color Data																							
		RED MSB							RED LSB	GREEN MSB							GREEN LSB	BLUE MSB							BLUE LSB
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED (0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	...	...								...								...							
	RED (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN (0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	...	...								...								...							
	GREEN (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	GREEN (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
BLUE	BLUE (0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	...	...								...								...							
	BLUE (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	BLUE (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

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3-8. Power Sequence

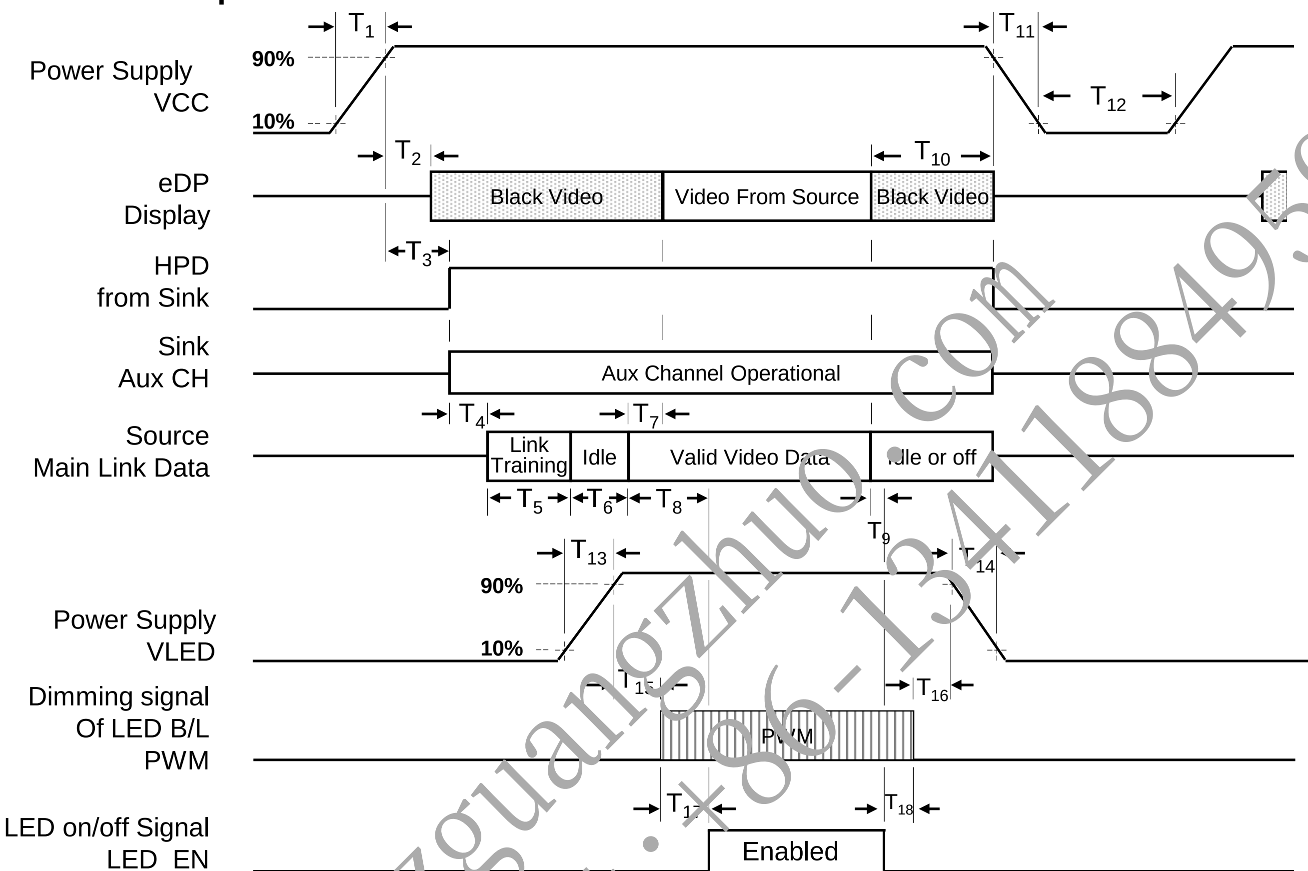


Table 6. POWER SEQUENCE TABLE

Symbol	Required By	Limits Min	Limits Max	Units	Notes	Symbol	Required By	Limits Min	Limits Max	Units	Notes
T_1	Source	0.5	10	ms	-	T_{10}	Source	35	500	ms	7
T_2	Sink	0	80	ms	-	T_{11}	Source	-	10	ms	-
T_3	Sink	0	80	ms	-	T_{12}	Source	500	-	ms	
T_4	Source	-	-	ms	-	T_{13}	Source	0.5	10	ms	-
T_5	Source	-	-	ms	-	T_{14}	Source	0.5	10	ms	-
T_6	Source	-	-	ms	-	T_{15}	Source	10	-	ms	-
T_7	Sink	0	50	ms	-	T_{16}	Source	10	-	ms	-
T_8	Source	-	-	ms	5	T_{17}	Source	0	-	ms	-
T_9	Source	0	-	ms	6	T_{18}	Source	0	-	ms	-

Note) 1. Do not insert the mating cable when system turn on.
2. Valid Data have to meet "3-3. eDP Signal Timing Specifications"
3. Video Signal, LED_EN and PWM need to be on pull-down condition on invalid status.
4. LGD recommend the rising sequence of VLED after the Vcc and valid status of Video Signal turn on.
5. Driving signal of B/L must be "On" after normal video signal (Normal operating data from source) input.
6. When VCC off, LED EN must be dropped to low level within black video data.
7. For stable operation of BL, Black video data have to meet min 35ms.

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 20 minutes in a dark environment at 25°C. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and Θ equal to 0°.
FIG. 1 presents additional information concerning the measurement equipment and method.

FIG. 1 Optical Characteristic Measurement Equipment and Method

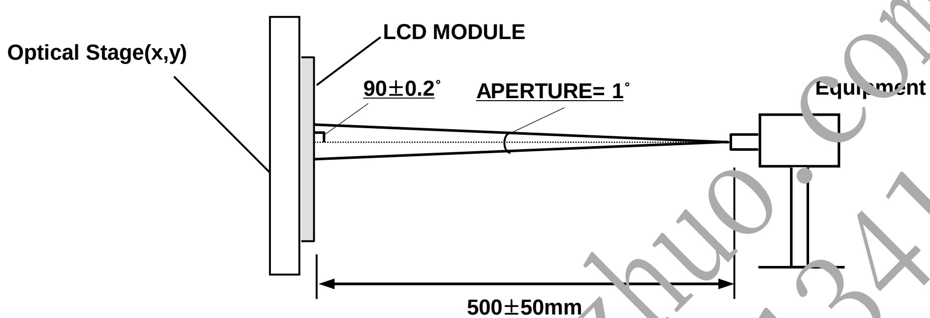


Table 7. OPTICAL CHARACTERISTICS

Ta=25°C, VCC=3.3V, fv=60Hz

Parameter		Symbol	Values Min	Values Typ	Values Max	Units	Notes
Contrast Ratio		CR	800	1000	-		1
Surface Luminance, white		L_{WH}	340	400	-	cd/m²	2
Luminance Variation		$\delta_{WHITE (5P)}$	-	1.2	1.4	-	3
		$\delta_{WHITE(13P)}$	-	1.4	1.6		
Response Time		Tr + Tf	-	30	35	ms	4
Color Coordinates	RED	Rx	Typical - 0.03	0.653	Typical + 0.03		5
		Ry		0.333			
	GREEN	Gx		0.300			
		Gy		0.592			
	BLUE	Bx		0.143			
		By		0.059			
	WHITE	Wx		0.313			
		Wy		0.329			
Viewing Angle	x axis, right(Φ=0°)	Θr	80	85	-	Degree	6
	x axis, left (Φ=180°)	Θl	80	85	-		
	y axis, up (Φ=90°)	Θu	80	85	-		
	y axis, down (Φ=270°)	Θd	80	85	-		
Gray Scale							7

Note)

1. It should be measured in the center of screen(1 Point). Contrast Ratio(CR) is defined mathematically as

$$\text{Contrast Ratio(1 Point)} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

2. Surface luminance is the average of 5 point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see FIG 2.

$$L_{WH} = \text{Average(1,2, … 5 Point)}$$

3. The variation in surface luminance , The panel total variation (δ WHITE) is determined by measuring N at each test position 1 through 13 and then defined as following numerical formula.
   For more information see FIG 2.

$$\delta\ \text{WHITE (5P)} = \frac{\text{Maximum (1,2, … 5 Point)}}{\text{Minimum (1,2, … 5 Point)}} \qquad \delta\ \text{WHITE (13P)} = \frac{\text{Maximum (1,2, … 13 Point)}}{\text{Minimum (1,2, … 13 Point)}}$$

4. Response time is the time required for the display to transition from black to white (rise time, Tr) and from white to black (falling time, Tf). For additional information see FIG 3.

5. It should be measured in the center of screen (1 Point).
   Color coordination must be measured with the equipment which has optical wavelength resolution of under 2㎚. (ex. PR670, PR680, CS2000. ..)

6. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 4.

7. Gray scale specification

Gray Level	Luminance [%] (Typ)
L0	0.04
L31	0.49
L63	2.94
L95	8.10
L127	17.83
L159	33.66
L191	52.78
L223	74.62
L255	100.00

FIG. 2 Luminance

<Measuring point for Average Luminance & measuring point for Luminance variation>

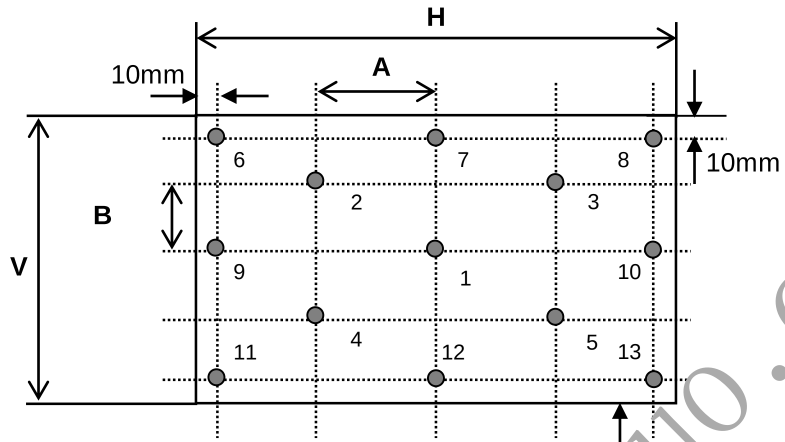


FIG. 3 Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white”.

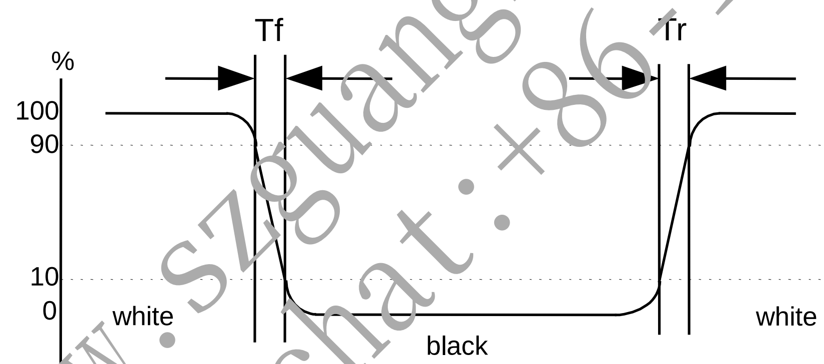
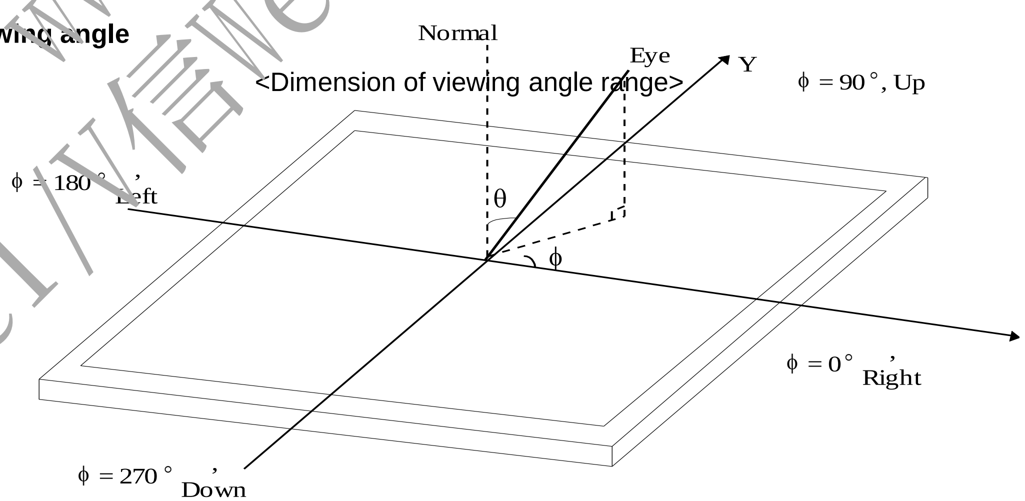


FIG. 4 Viewing angle

<Dimension of viewing angle range>



5. Mechanical Characteristics

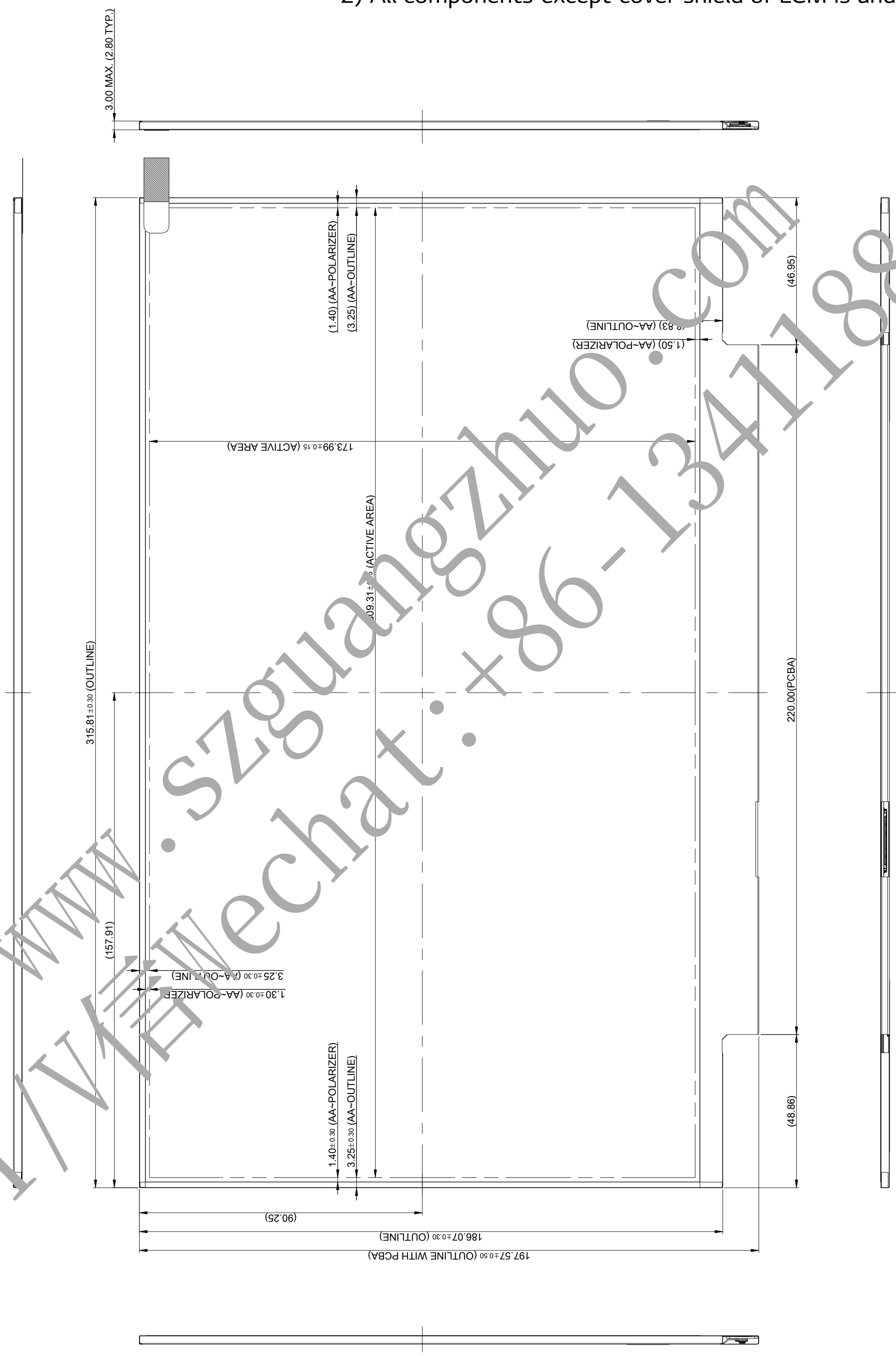
The contents provide general mechanical characteristics for the model LP140WF9. In addition the figures in the next page are detailed mechanical drawing of the LCD.

Outline Dimension	Horizontal	315.81± 0.3 mm
	Vertical	186.07± 0.3 mm
	Thickness	3.0mm (max.)(Without PCBA)
Upper Polarizer Dimension	Horizontal	312.11 ± 0.2 mm
	Vertical	176.79 ± 0.2 mm
Active Display Area	Horizontal	309.31 ± 0.15 mm
	Vertical	173.99 ± 0.15 mm
Weight	260g (Max.)	
Surface Treatment	Anti-Glare treatment of the front polarizer	

Product Specification

<FRONT VIEW>

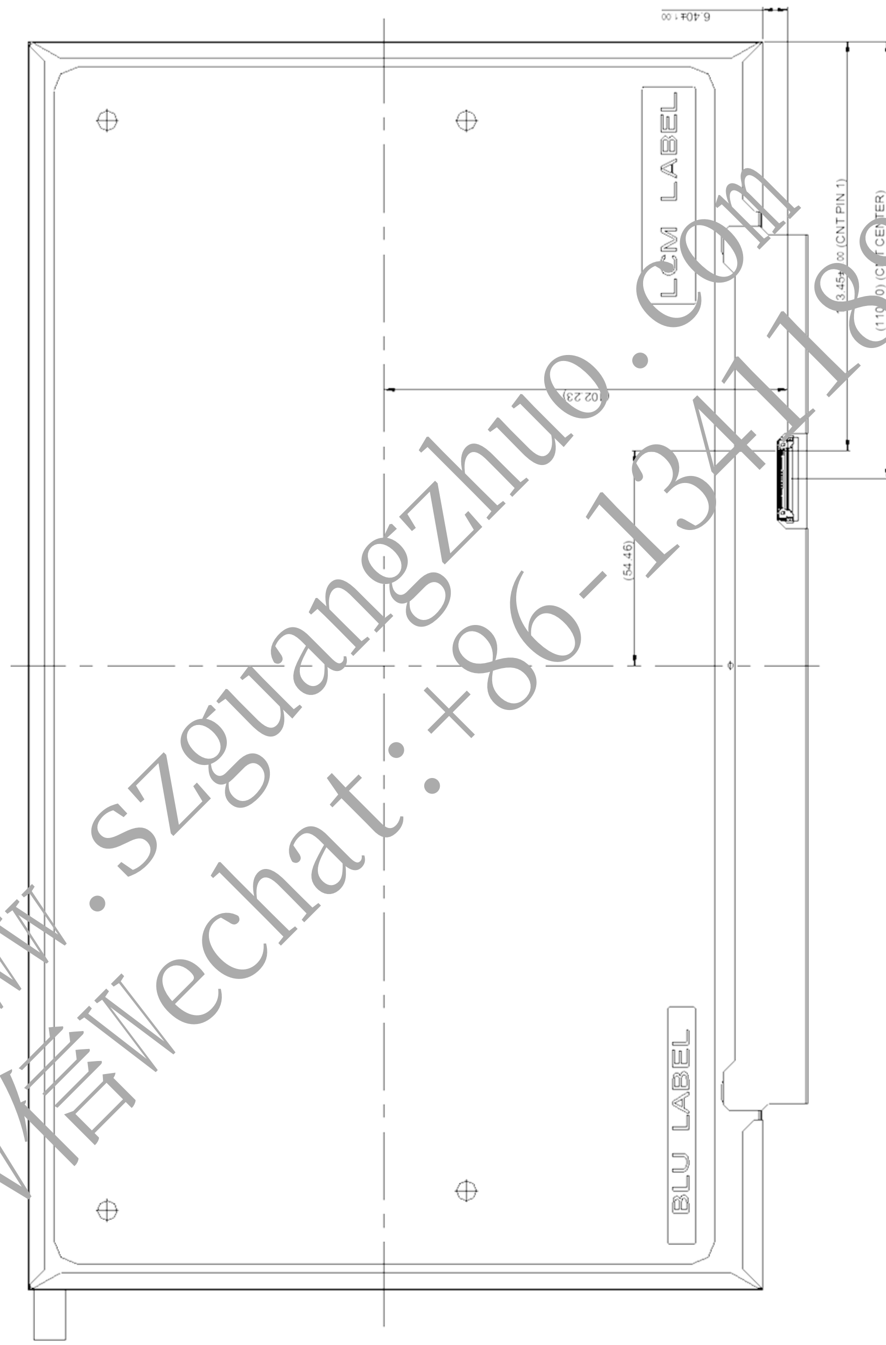
Notes (Measurement method refer to the Appendix D)
1) Unit[mm], General tolerance : ± 0.5mm
2) All components except cover shield of LCM is under upper POL.



Product Specification

<REAR VIEW>

Notes
1) Unit[mm], General tolerance : ± 0.5mm
2) LCM Label Information refer to the page 26.



6. Reliability

Environment test condition

No.	Test Item	Conditions
1	High temperature storage test	Ta= 60°C, 240h
2	Low temperature storage test	Ta= -20°C, 240h
3	High temperature operation test	Ta= 50°C, 50%RH, 240h
4	Low temperature operation test	Ta= 0°C, 240h
5	Vibration test (non-operating)	Random, 1.0Grms, 10 ~ 300Hz(PSD 0.0035) 3 axis, 30min/axis
6	Shock test (non-operating)	- No functional or cosmetic defects following a shock to all 6 sides delivering at least 180 G in a half sine pulse no longer than 2 ms to the display module - No functional defects following a shock delivering at least 200 g in a half sine pulse no longer than 2 ms to each of 6 sides. Each of the 6 sides will be shock tested with one each display, for a total of 6 displays
7	Altitude operating storage / shipment	0 ~ 10,000 feet (3,048m) 24Hr 0 ~ 40,000 feet (12,192m) 24Hr
8	ESD	± 8kV for contact discharge ± 15kV for air discharge

[Result Evaluation Criteria]

1. Comparing the initial functional FOS status, there should be no major change which might affect the practical display function when the display reliability test is conducted.

2. After conduct reliability tests, LGD guarantees only functional FOS quality.

3. In the Reliability Test, Confirm performance after leaving in room temp.

4. In the standard condition, there shall be no practical problems that may affect the display function 24 hours later after reliability test. After the reliability test, we can guarantee the product only when the corrosion is causing its malfunction. The corrosion causing no functional defect can not be guaranteed.

7. International Standards

7-1. Safety

a) IEC 62368-1, The International Electro-technical Commission(IEC).
Audio/video, Information and Communication Technology Equipment - Safety - Safety Requirements.
b) EN 62368-1, European Committee for Electro-technical Standardization (CENELEC)
Audio/video, Information and Communication Technology Equipment - Safety Requirements
c) UL 62368-1, UL LLC.
Audio/video, Information and Communication Technology Equipment - Safety Requirements
d) CAN/CSA C22.2 No.62368-1, Canadian Standards Association (CSA).
Audio/video, Information and Communication Technology Equipment - Safety Requirements
e) IEC 60950-1, The International Electro technical Commission (IEC).
Information Technology Equipment - Safety - Part 1 : General Requirements

7-2. Environment

a) RoHS, Directive 2011/65/EU of the European Parliament and of the council of 8 June 2011

8. Packing

8-1. Designation of Lot Mark

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M

A,B,C : SIZE(INCH)
D : YEAR
E : MONTH
F ~ M : SERIAL NO.

Note

1. YEAR

Year	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029
Mark	K	L	M	N	P	R	S	T	U	V

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

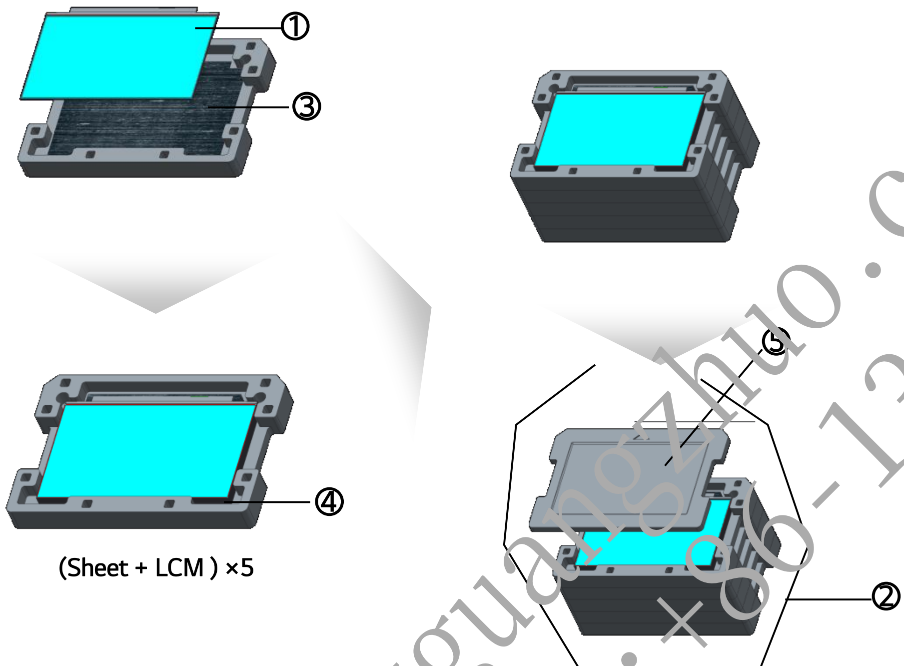
Serial No. is printed on the label. The label is attached to the backside of the LCD module.
This is subject to change without prior notice.

8-2. Packing Form

a) Package quantity in one box : 35 pcs

b) Box Size : 410 x 278 x 328

8-3. Packing Assembly

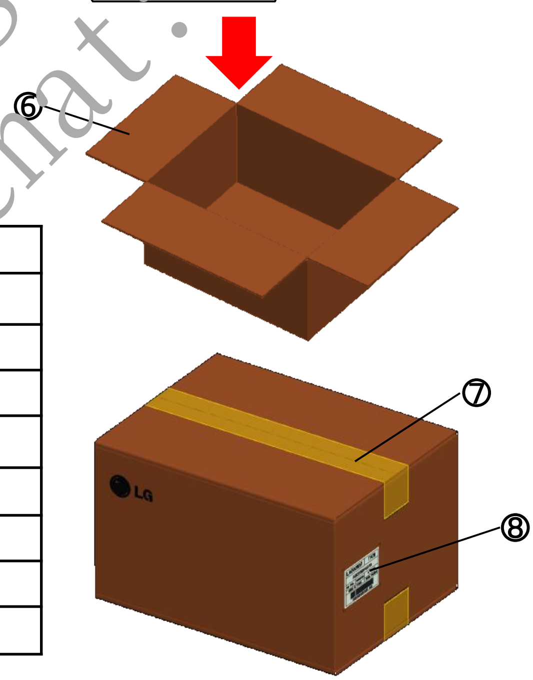


5 LCM / Tray

7 Tray / Box

35LCM/Box

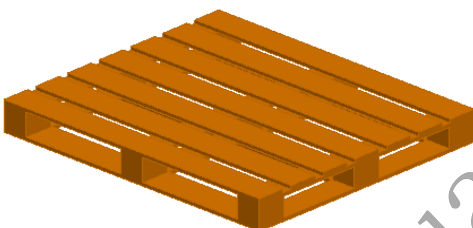
2EA Desiccant in the box



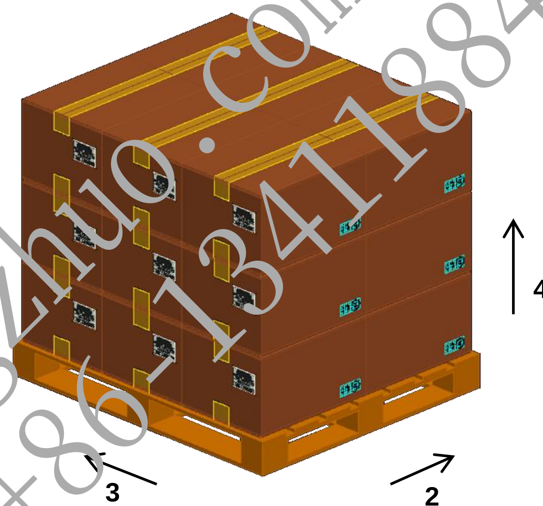
NO.	DESCRIPTION	MATERIAL
1	LCD Module	
2	BAG	AL
3	Sheet	PE
4	Bottom Tray	EPO
5	Top Tray	EPO
6	BOX	SWR4
7	TAPE	OPP 70MMX300M
8	LABEL	ART 100X70

8-4. Pallet Assembly

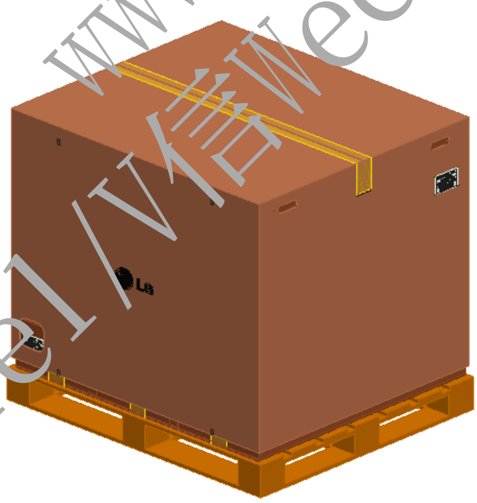
1. Pallet Ready



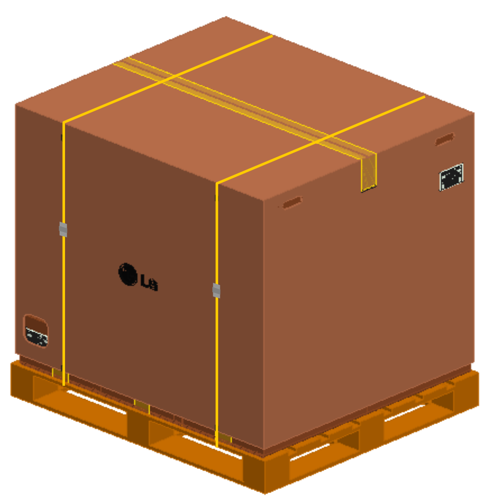
2. 3 x 2 x 4 Box Pattern



3. Angle Packing & Taping

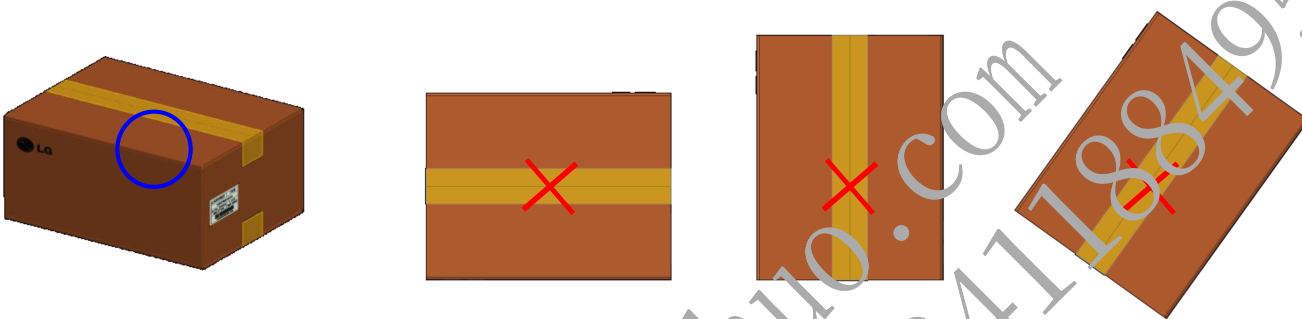


4. Banding

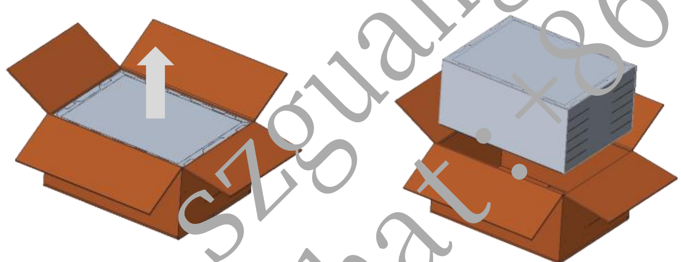


8-5. Precautions for unpacking the Box

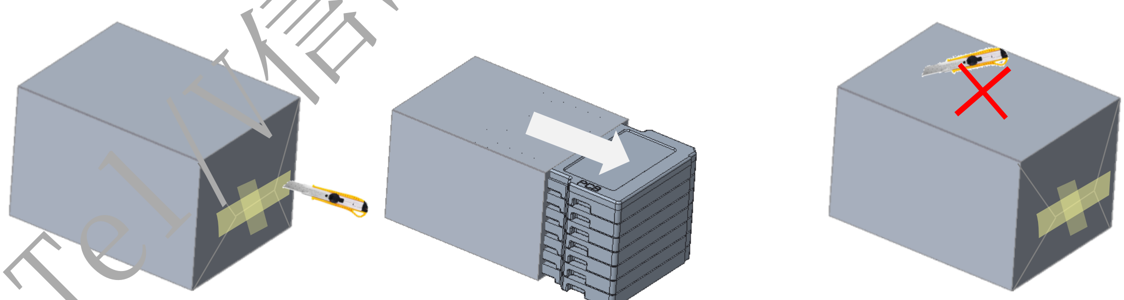
a.) Don't throw or tilt the box and put it on a flat surface.



b.) Place the box on a flat floor and Take out the AL bag vertically.



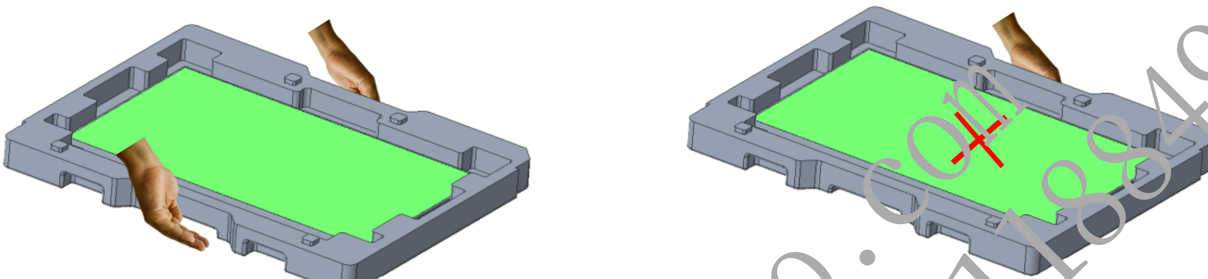
c.) Cut the tape on the side of the bag with a knife and Take out the tray horizontally.



**Caution : Do not cut the top of the bag with a knife.
(The Knife can damage product)**

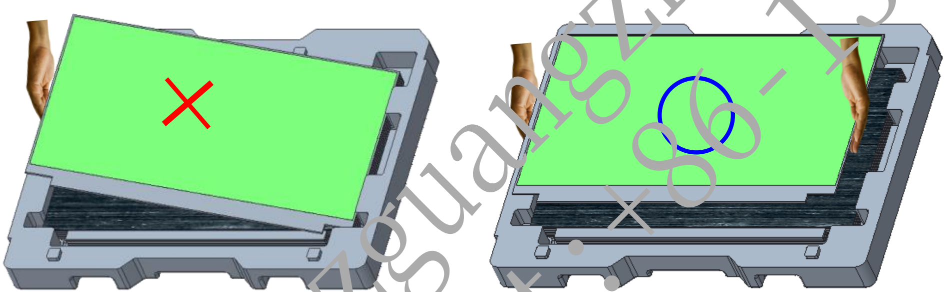
8-6. Precautions for Handling tray

a.) Hold center of short or long side of the tray with both hands when handling one or more trays.

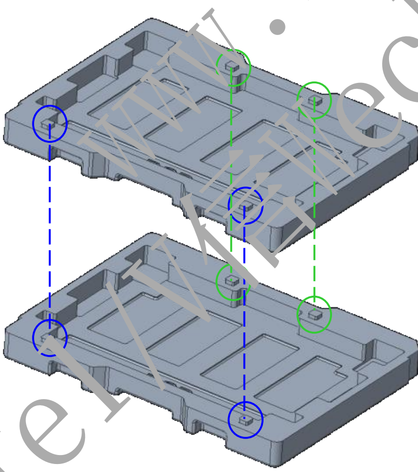


Caution : Do not handle with only one hand.

b.) Always place tray on flat surface and Don't tilt with one hand to take out.



c.) When stacking trays, Please align same position of the protrusion of each tray.



If not Aligned,
The tray may slip without being loaded.

d.) The maximum stacking quantity is equal to the number of loads per box.

- Recommended as above because heavier weight can cause muscular skeletal disease and operator handling errors.

9. PRECAUTIONS

Please pay attention to the followings when you use this TFT LCD module.

9-1. MOUNTING PRECAUTIONS

(1) You must mount a module using holes arranged in four corners or four sides.
(2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(4) You should adopt radiation structure to satisfy the temperature specification.
(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(9) Do not open the case because inside circuits do not have sufficient strength.
(10) When handling the LCD module, it needs to handle with care not to give mechanical stress to the PCB and Mounting Hole area.

9-2. OPERATING PRECAUTIONS

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage : V=± 200mV(Over and under shoot voltage)

(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.) And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
(4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.

9-3. ELECTROSTATIC DISCHARGE CONTROL

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-4. PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter.

9-5. STORAGE

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

9-6. HANDLING PRECAUTIONS FOR PROTECTION FILM

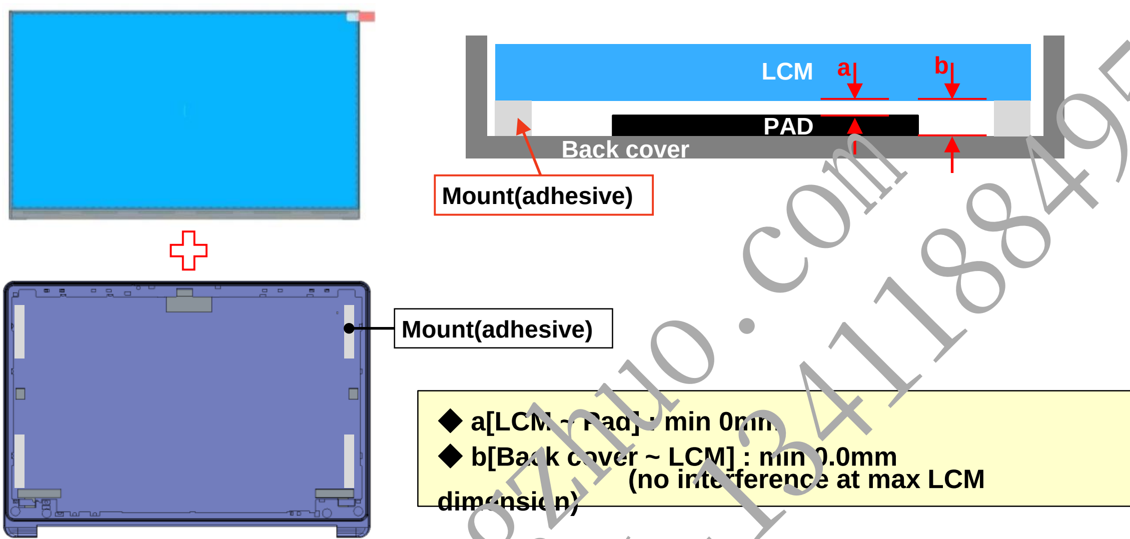
(1) When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) The protection film is attached to the polarizer with a small amount of glue. If some stress is applied to rub the protection film against the polarizer during the time you peel off the film, the glue is apt to remain on the polarizer.
Please carefully peel off the protection film without rubbing it against the polarizer.
(3) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.
(4) You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

9-7. THE LGD QA RESPONSIBILITY WILL BE AVOIDED IN CASE OF BELOW

(1) When the customer attaches TSM(Touch Sensor Module) on LCM without Supplier's approval.
(2) When the customer attaches cover glass on LCM without Supplier's approval.
(3) When the LCMs were repaired by 3rd party without Supplier's approval.
(4) When the LCMs were treated like Disassemble and Rework by the Customer and/or Customer's representatives without supplier's approval.

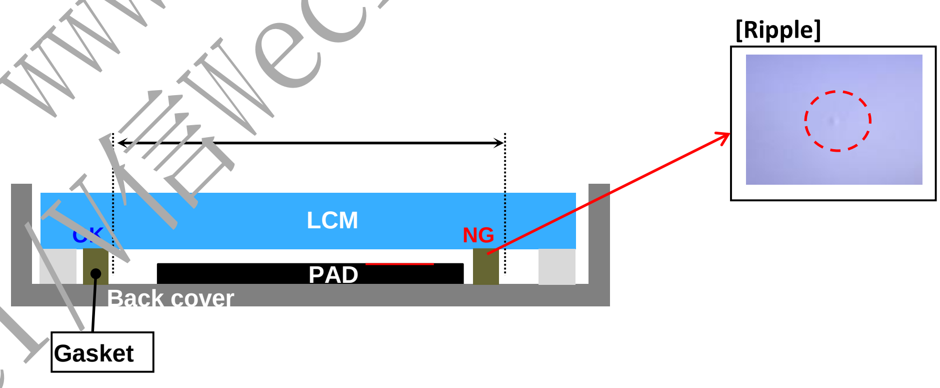
APPENDIX A. LGD Proposal for system cover design.

1	**Gap check for securing the enough gap between LCM and System back cover.**



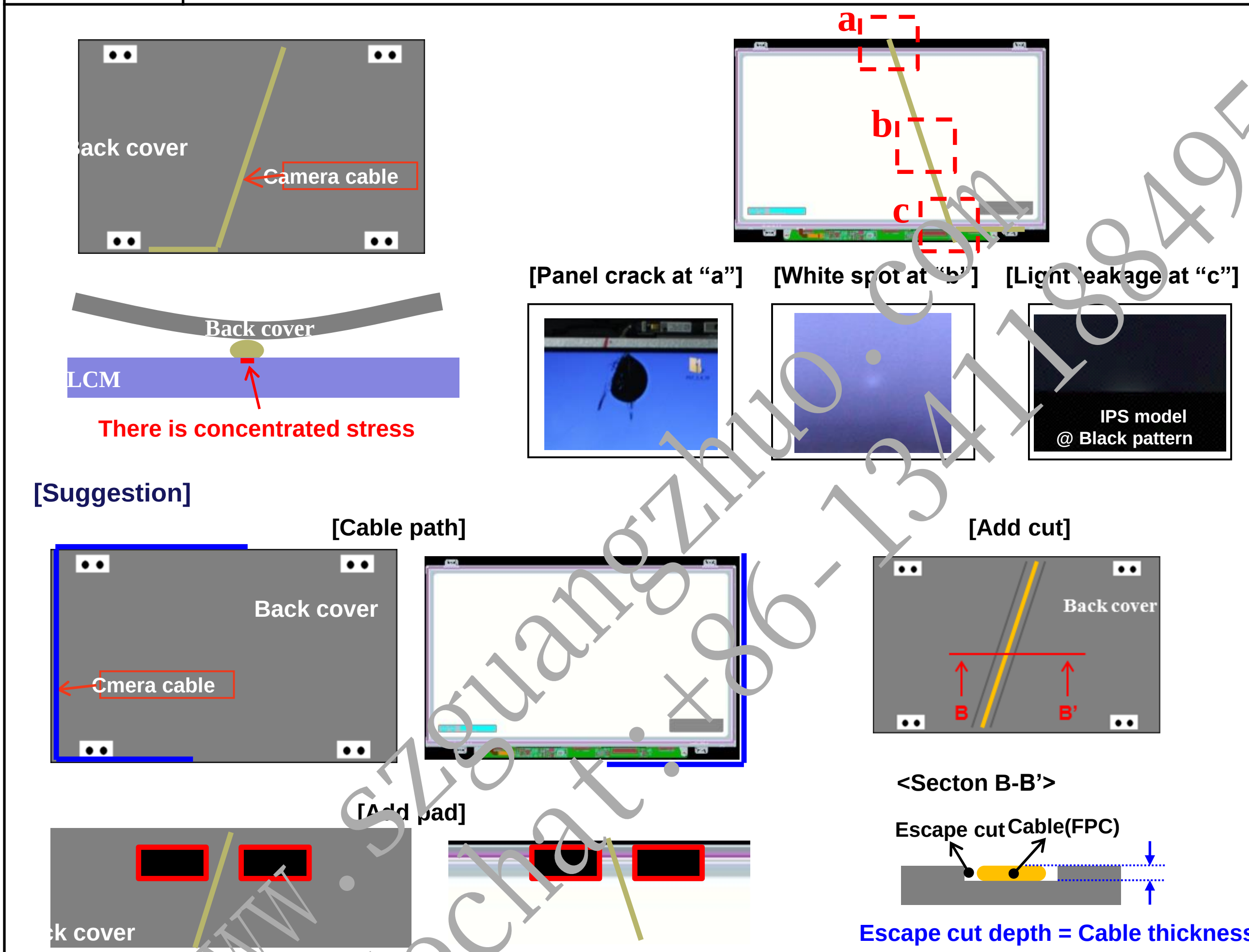
Risk point	Rear side of LCM is sensitive against external stress, and previous check about interference is highly needed.
Suggestion	In case there is something from system cover comes into the boundary above,mechanical interference may cause the FOS defects. (ex: Ripple, White spot..)

2	**Gasket position**



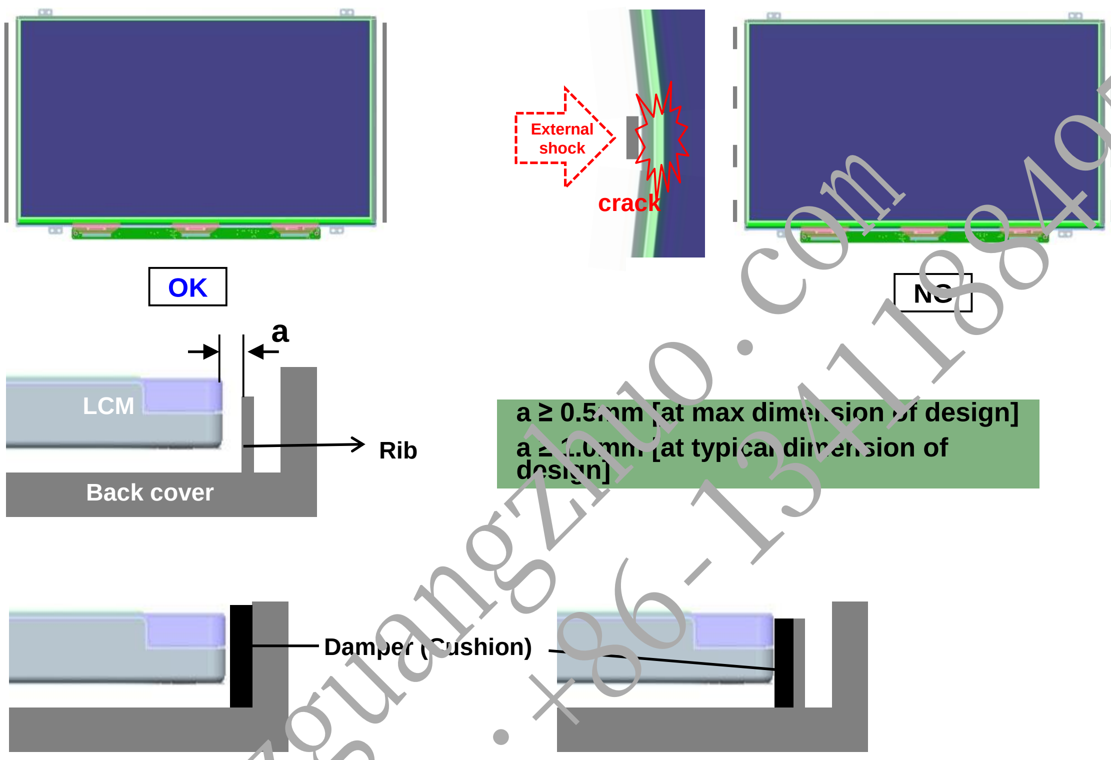
Risk point	Ripple or white spot can be happened by interference between pad and LCM when gap is not enough.
Suggestion	It is recommended that gasket is posited out of active area .

APPENDIX A. LGD Proposal for system cover design.

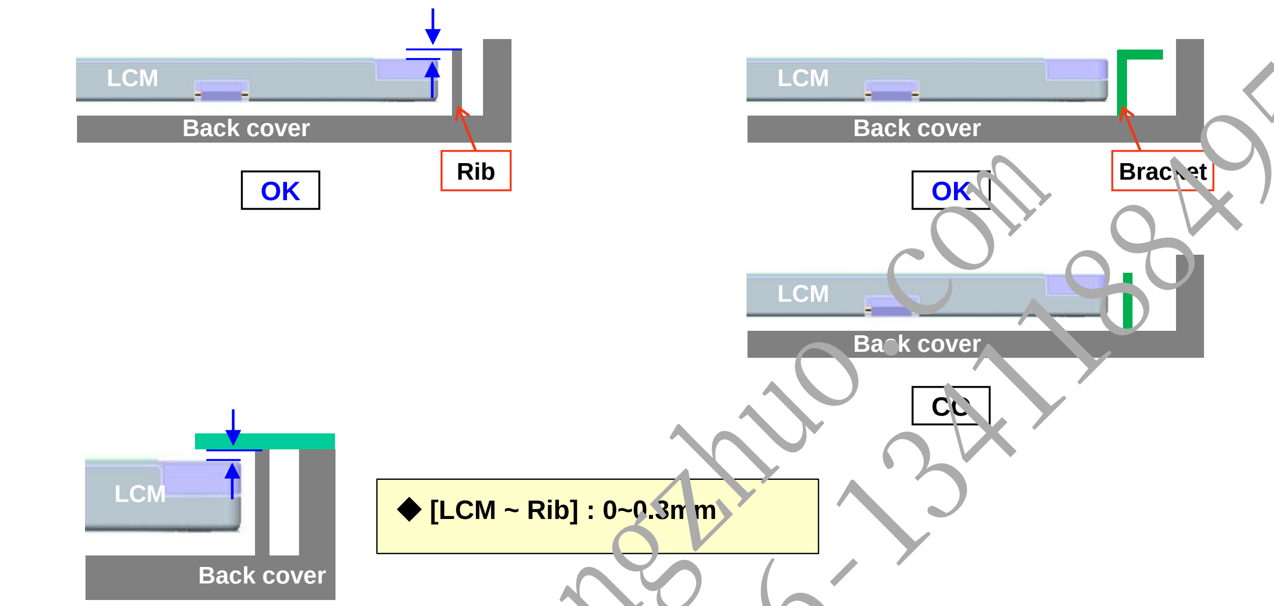
3	Checking the path of the System cables
	
Risk point	LCM is easily damage by camera cable when cable is protruded from back cover. It is caused panel crack or white spot by concentrated stress and light leakage by panel bending at IPS model.
Suggestion	It is recommended that camera cable path put outside of LCM. It is recommended that pad is added at both side of cable. If cable path must be cross middle area of system,@slim & narrow bezel 1) Cable type is recommended to use flexible (Use FPC type). 2) Add escape cut on back cover and add round at the edge of cut Depth of escape cut recommended to set the same as FPC thickness.

Product Specification

APPENDIX A. LGD Proposal for system cover design.

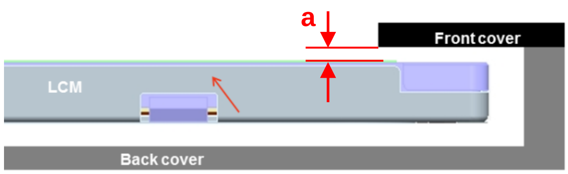
4	System rib (on A cover)
	
Risk point	Gap is too small and rib is too short, panel is easily cracked by external stress.
Suggestion	Gap is must be kept more than 0.5mm(max dim.) and 1.0mm(typ dim.) .
	The figure of rib is continuous or fully long.
	“a” is not enough as narrow bezel type, add damper between LCM and system rib/wall

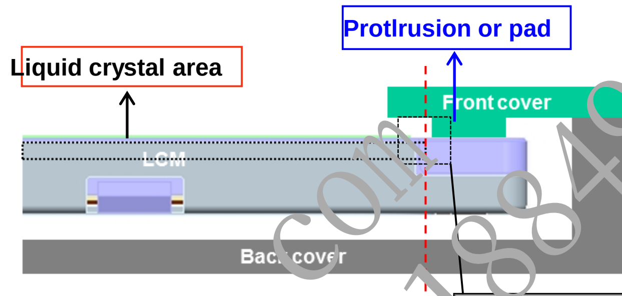
APPENDIX A. LGD Proposal for system cover design.

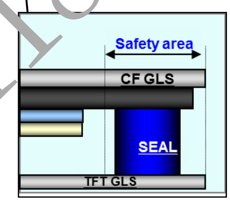
<table>
<tr><td>5</td><td>Check the rib or Bracket on back cover</td></tr>
<tr><td colspan="2">
</td></tr>
<tr><td>Risk point</td><td>It is necessary that the height of back cover rib or bracket is higher than LCM height. It can prevent direct compression of panel at LCM edge.</td></tr>
<tr><td rowspan="3">Suggestion</td><td>"¬" shape bracket is stronger than "I" shape one.</td></tr>
<tr><td>It is recommended that rib height is same or more with LCM height.</td></tr>
<tr><td>In this case it must be considered light leakage at front cover, too.</td></tr>
</table>

APPENDIX A. LGD Proposal for system cover design.

6	**Check the gap between front cover and LCM(glass)**
Risk point	Ripple can be happened by little gap between glass and front cover.
Suggestion	Keep the gap between front cover and LCM from 0.1 to 0.3mm Ripple is prevented by add protrusion shape at the back side of front cover. In this case, protrusion must be created outside of liquid crystal area



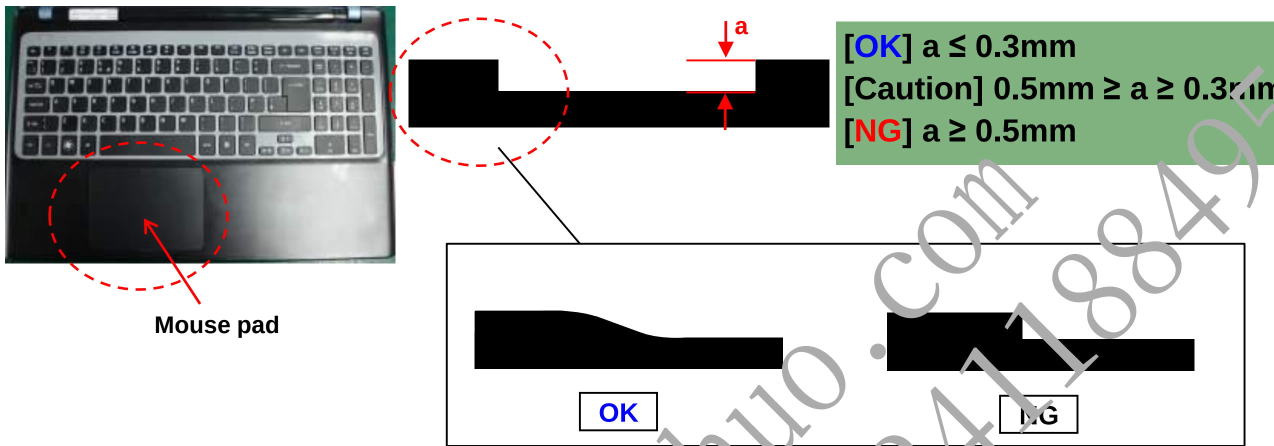




[OK] 0.1mm ≤ a ≤ 0.3mm
[Caution] 0.0mm ≤ a < 0.1mm, 0.3mm < a ≤ 0.5mm
[NG] a ≤ 0mm (overlap), a>0.5mm (leakage)

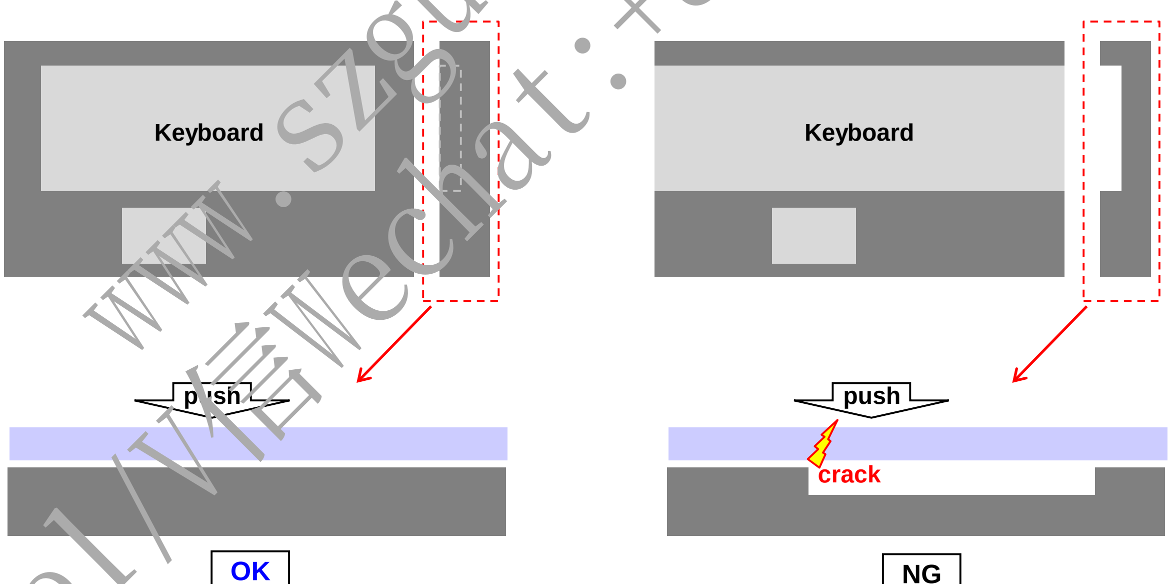
APPENDIX A. LGD Proposal for system cover design.

7	**Check mouse pad (touch pad) depth and shape of edge**



Risk point	Mouse pad step is deep, it is caused panel crack by external load.
Suggestion	The edge shape must be smooth.

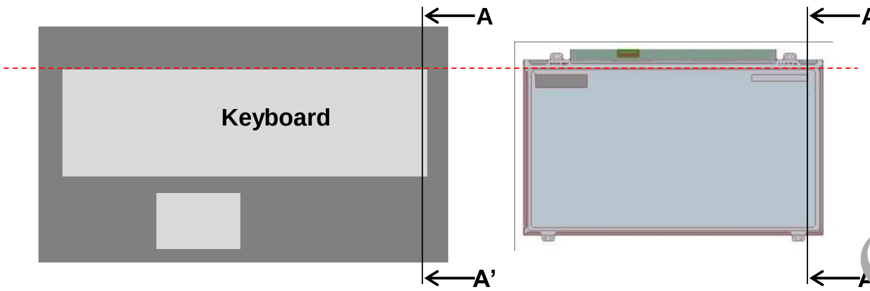
8	**Check the step of keyboard area**

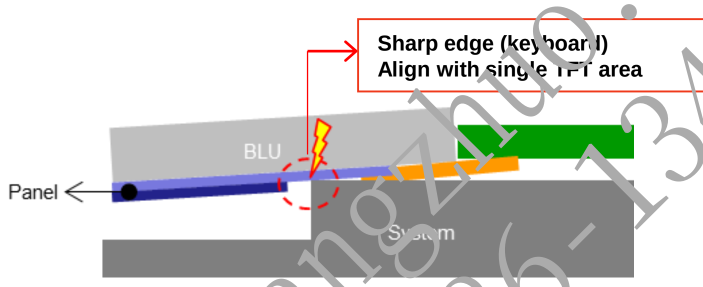


Risk point	The step of keyboard at the side edge of main body, it is caused panel crack
Suggestion	Keep to flat out side of keyboard.

APPENDIX A. LGD Proposal for system cover design.

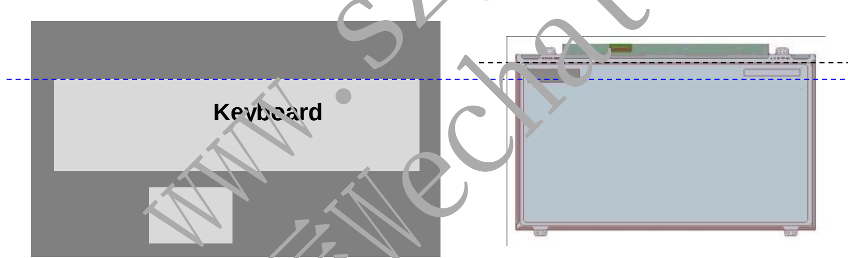
9	The position and shape of keyboard step





<Section A-A'>

[Suggestion]

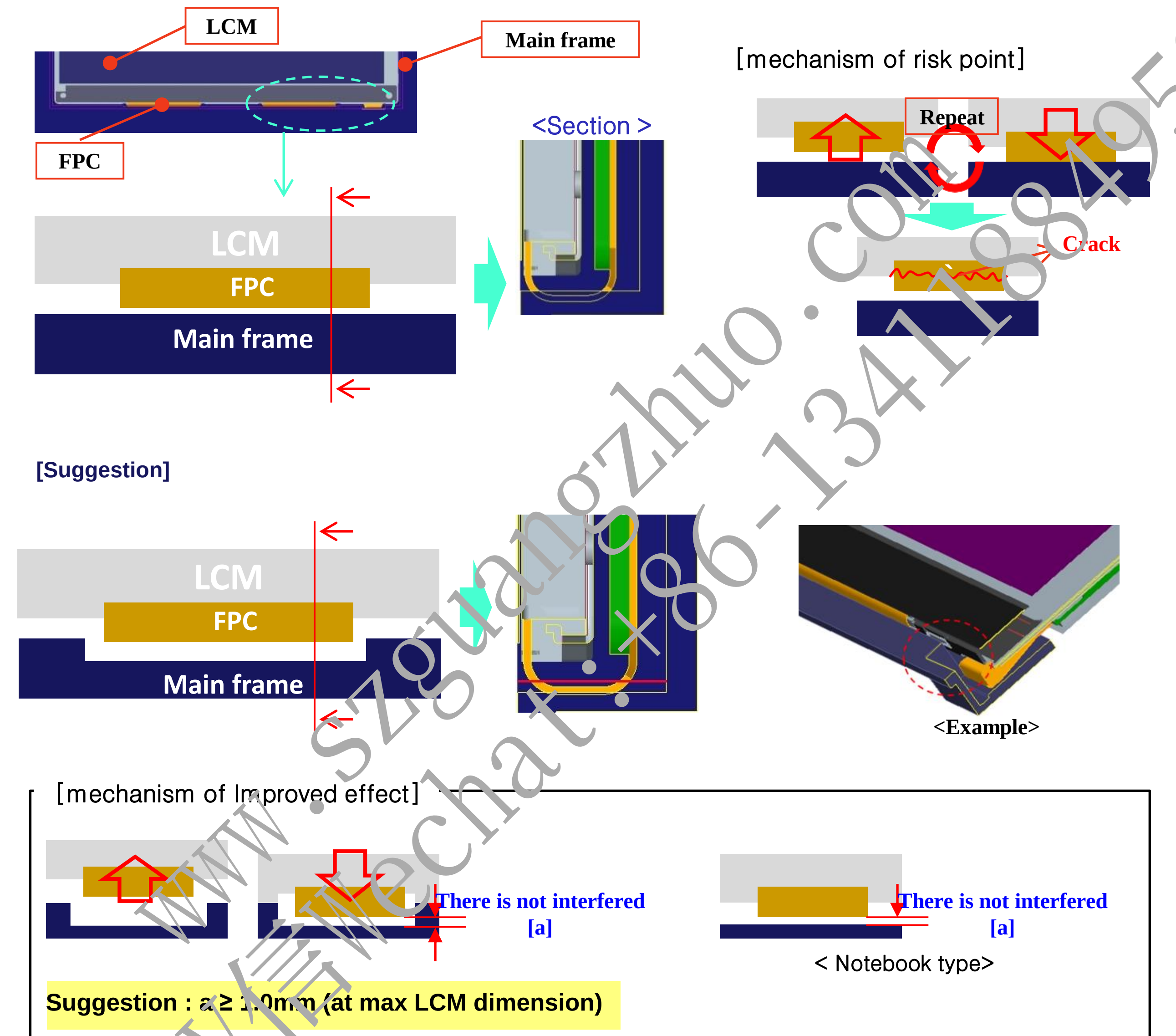


<Section A-A'>

Risk point	Keyboard edge is sharp (a right angle), panel is get concentrated stress, by external force at this edge.
	Especially, keyboard edge is aligned with panel edge (single-TFT area), crack risk is seriously increase.
Suggestion	It is recommended that keyboard edge is posited to avoid single-TFT area.
	It is recommended that edge shape of touch pad is rounded.

APPENDIX A. LGD Proposal for system cover design.

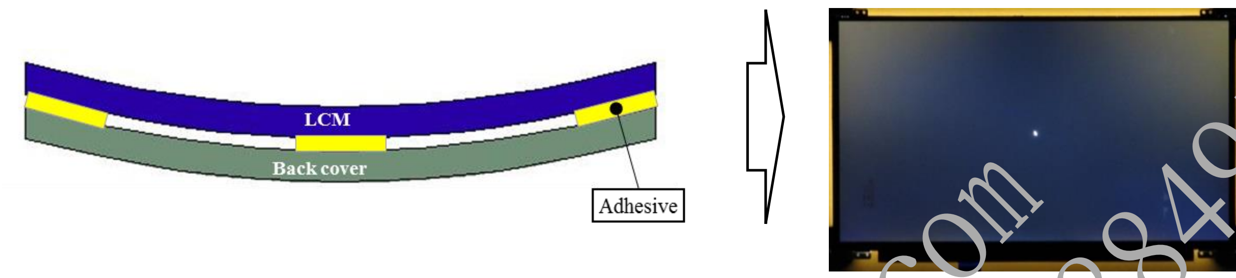
10	FPC escape figure



Risk point	FPC is easily cracked by interference between FPC and frame during repetitive external shock or vibration. It is also happened when gap between is exist.
Suggestion	FPC crack can be improved by add escape figure at middle frame
	The gap is recommended to keep more than 1.0mm

APPENDIX A. LGD Proposal for system cover design.

11-1 LCM fixing (no flange model)

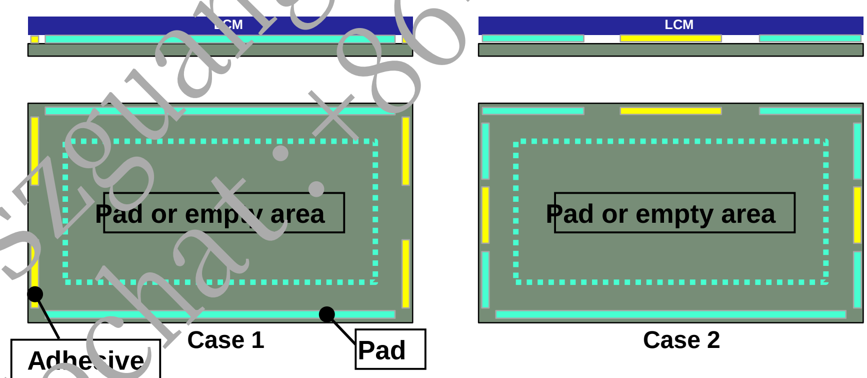


[Suggestion]

Flat

Adhesive width

Position of pad & adhesive



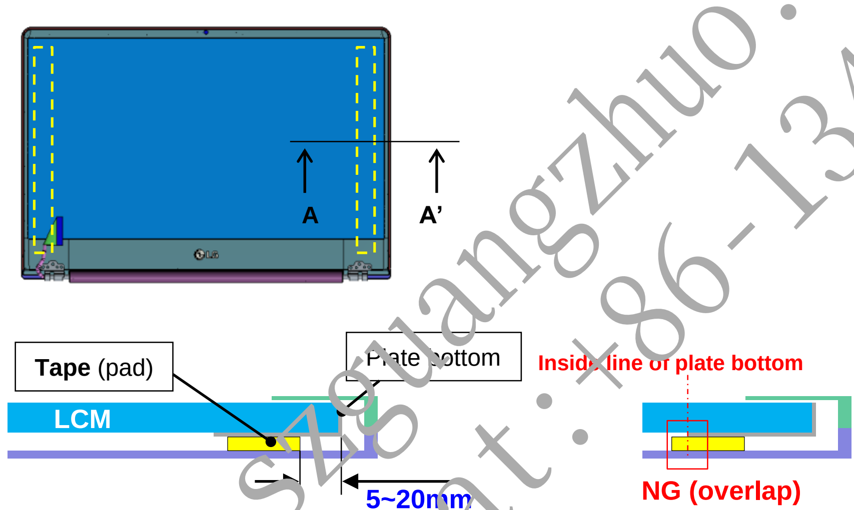
[Mapping on back cover]

Risk point	In IPS model, bended LCM, light leakage of IPS (mura) is happened. LCM is bended by below condition. 1. Back cover is not flat or distorted. 2. LCM is fixed by adhesive at center area. 3. Adhesive width is too large.
Suggestion	It is recommended that back cover is flat type. Adhesive width need to be minimized if adhesive strength is enough. It is recommended that adhesive is posited at outside on back-cover. Pad is recommended to apply at other area.

APPENDIX A. LGD Proposal for system cover design.

11-2	LCM fixing (no flange model)

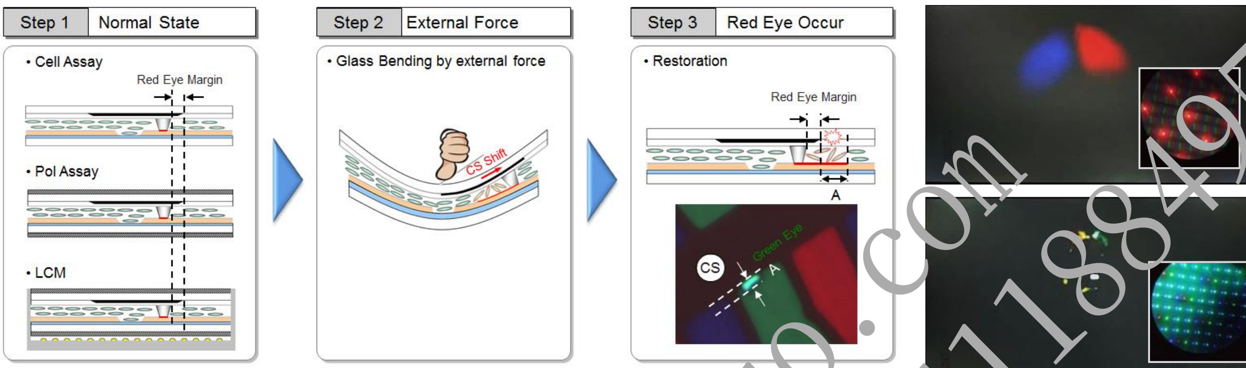
[Suggestion]



Risk point	In IPS model, bended LCM, light leakage of IPS (mura) is happened. LCM is bended by below condition. 1. Back cover is not flat or distorted. 2. LCM is fixed by adhesive at center area. 3. Adhesive width is too large.
Suggestion	It is recommended to attach LCM fixing tape to the inside with reference to the outside (5~20mm). But do not overlap the pad with the inside line of the plate bottom

APPENDIX A. LGD Proposal for system cover design.

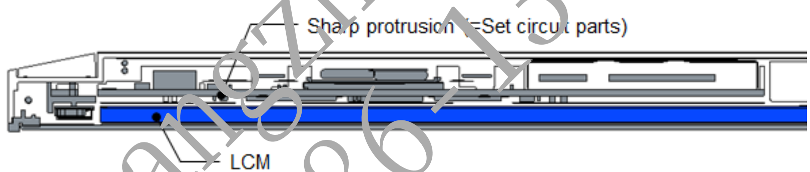
12-1	System protrusion and step for RGB eye



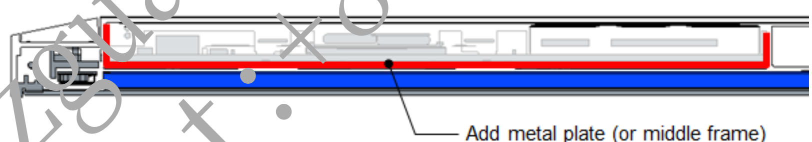
[Suggestion]

Middle frame

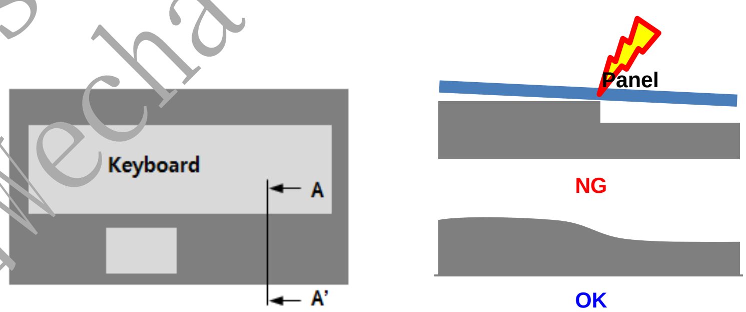
NG



Suggestion



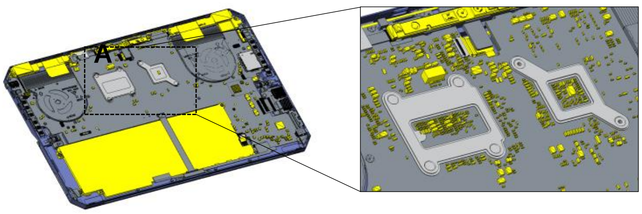
Keyboard step

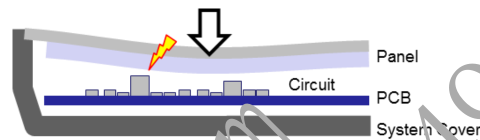


Risk point	When abnormally strong external force is given to LCM, CF CS push the PI and make a scratch, which have the light leak happen. This light leak comes out as Red Eye.
Suggestion	Minimize the height of protrusion and add metal plate on main board. (Tablet type) It is recommended to make a round edge at keyboard step area to prevent stress concentration by external force.

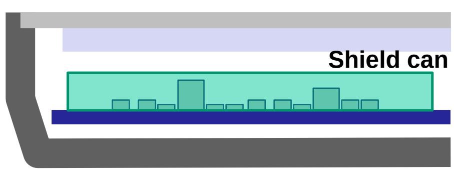
APPENDIX A. LGD Proposal for system cover design.

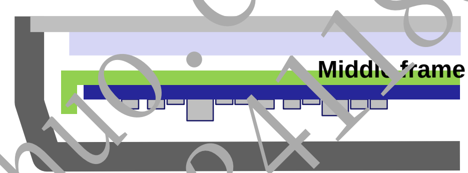
12-2	System protrusion and step for RGB eye





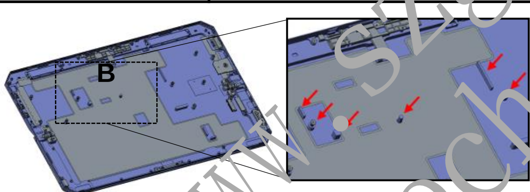
[Suggestion]

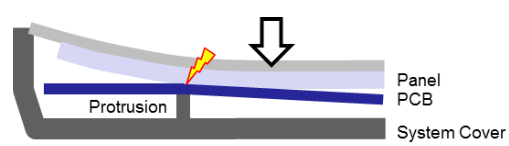




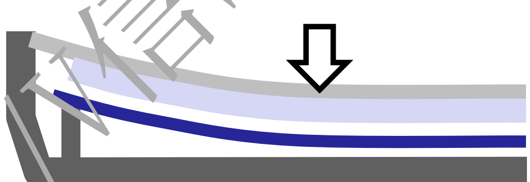
Risk point	The system PCB circuit is exposed at the front side, and LCM damage occurs due to direct contact with the back of the LCM
Suggestion	Apply shield can to circuit open area of PCB.
	Apply Middle frame to avoid LCM backside interference.

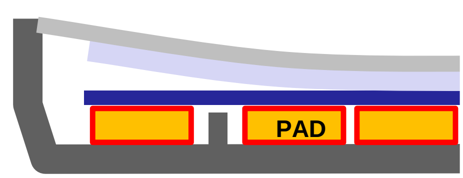
12-3	System protrusion and step for RGB eye





[Suggestion]





Risk point	System A-Cover ribs and screw bosses cause LCM damage due to stress concentration and bending inflection point.
Suggestion	Protrusions should be located outside the LCM.
	Apply level compensation structure around protrusions

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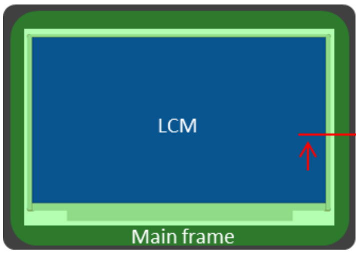
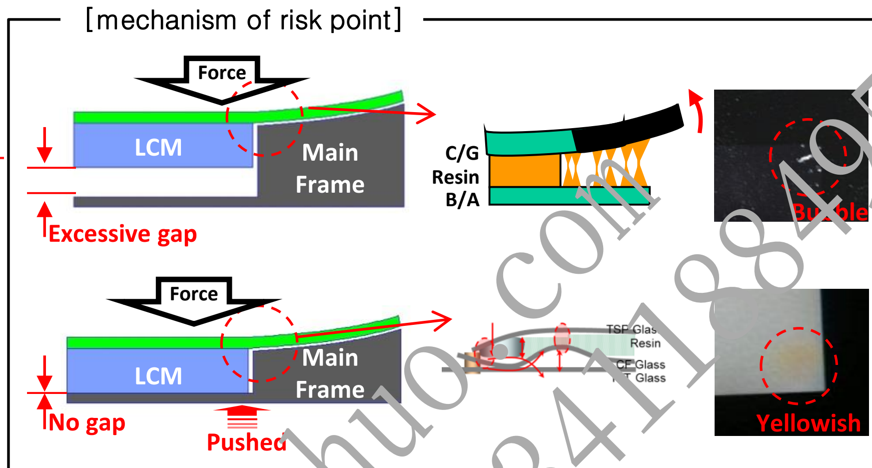
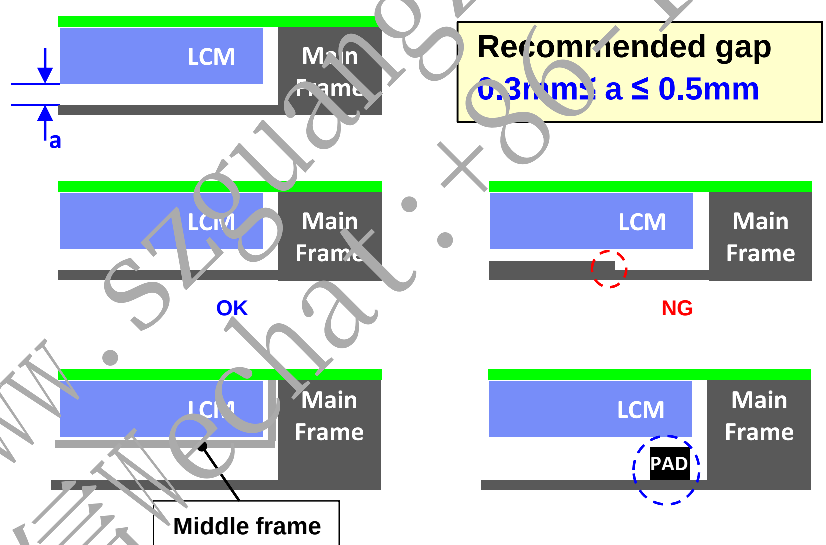
APPENDIX A. LGD Proposal for system cover design.

13	Gap[System ~ LCM] at corner





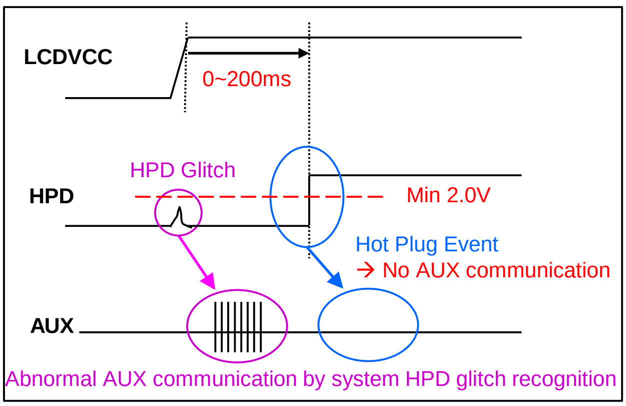
[Suggestion]



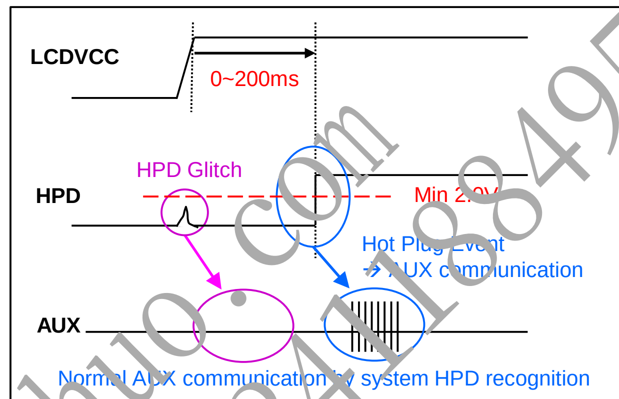
Risk point	If there is no gap, too large gap or not flat between LCM and system main body, it is easily caused ripple, yellowish, bubble and so on.
Suggestion	It is recommended to keep 0.3~0.5mm gap between LCM and system main keep at LCM corner
	It is recommended to keep flatness of system frame
	If there is not frame between LCM and system, add frame at LCM edge or add pad on back cover (LCM edge position).
	Use good strength material against bending

APPENDIX B. LGD Proposal for eDP Interface Design Guide

1	HPD Signal recognition



[Abnormal Communication By HPD Glitch]

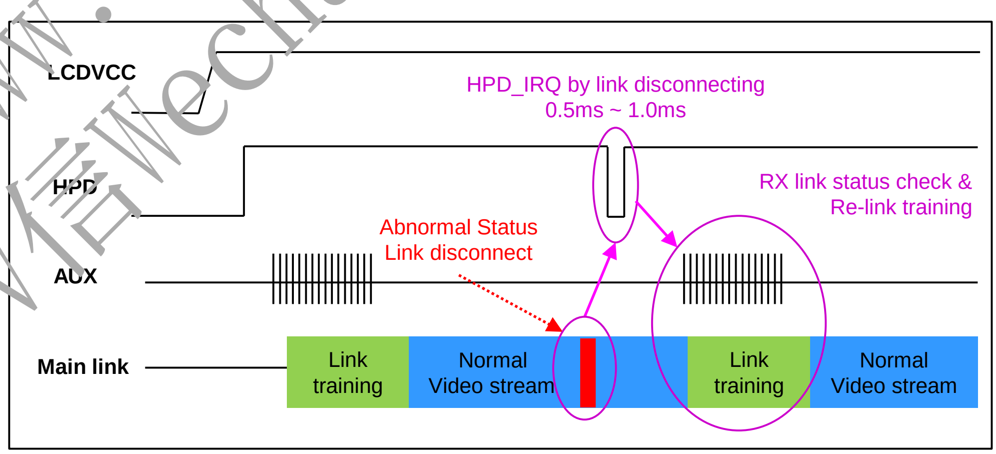


[Normal Communication By HPD Signal]

Define	1. Hot Plug Detection (HPD) Threshold level of Source Device is minimum 2.0V
	2. HPD Unplug : HPD pulse stays low longer than 2ms. DP Tx shall wait for HPD signal to go high again.
	3. “HPD High” is confirmed only after HPD has been asserted continuously for 100msec.

2	IRQ (Interrupt Request) HPD Pulse Definition

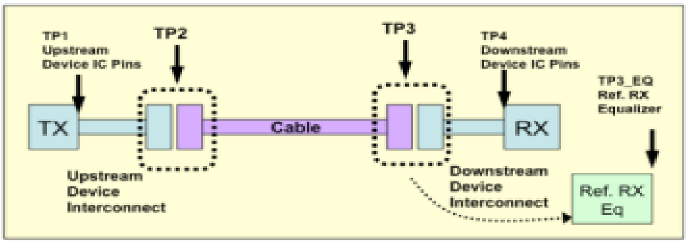
Ex) HPD Pulse



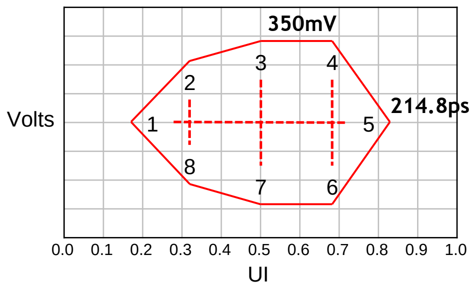
Define	Upon detection this “HPD IRQ Event”(0.5ms ~ 1ms) ,the source device must read the link / sink status field of the DPCD and take corrective action.

APPENDIX B. LGD Proposal for eDP Interface Design Guide

3 Main Link EYE Diagram

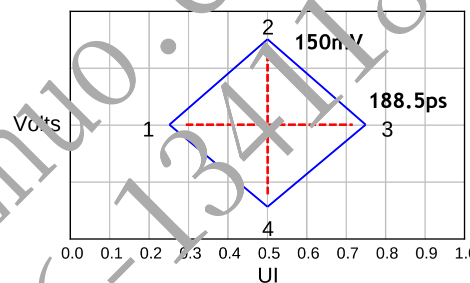


[EYE Diagram]



Point	UI	Voltage (Volts)
1	0.210	0.000
2	0.355	0.140
3	0.500	0.175
4	0.645	0.175
5	0.790	0.000
6	0.645	-0.175
7	0.500	-0.175
8	0.355	-0.140

[EYE Vertices for TP2 at HBR]



Point	UI	Voltage (Volts)
1	0.246	0.000
2	0.500	0.075
3	0.755	0.000
4	0.500	-0.075

[EYE Vertices for TP3 at HBR]

Define: Main Link EYE Diagram should meet TP2 and TP3 point

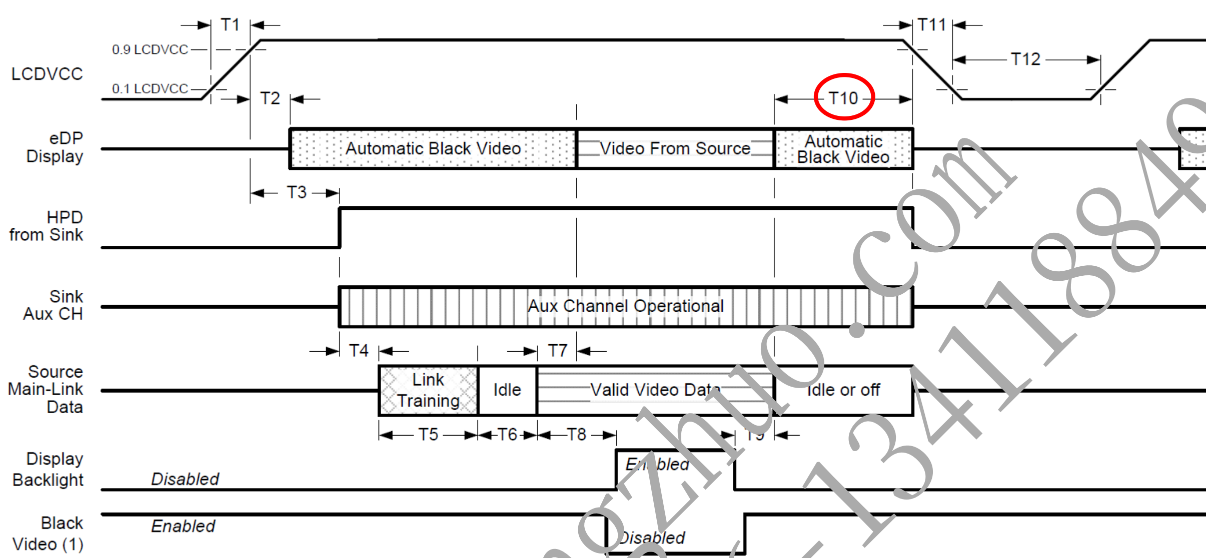
4 Cable Impedance management

Segment	Differential Impedance	Maximum Tolerance
Fixture	100 Ω	+/- 10%
Connector	100 Ω	
Wire management	100 Ω	
Cable	100 Ω	+/- 5%

Define: Cable Impedance 100 Ω +/- 5% (95Ω ~ 105Ω)

APPENDIX B. LGD Proposal for eDP Interface Design Guide

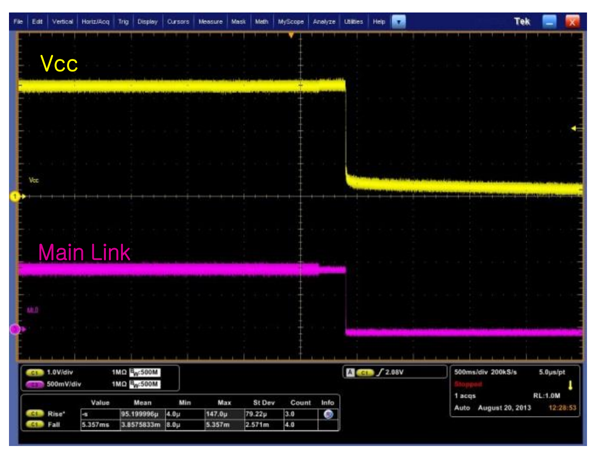
5	Main Link Off vs. LCD Power Off at Non-PSR



Timing Parameter	Description	Required By	Min	Max
T10	Delay from end of valid video from Source to Power Off	Source	0ms	500ms

* LGD recommend that Source must power off the LCDVCC in Main Link off like below.

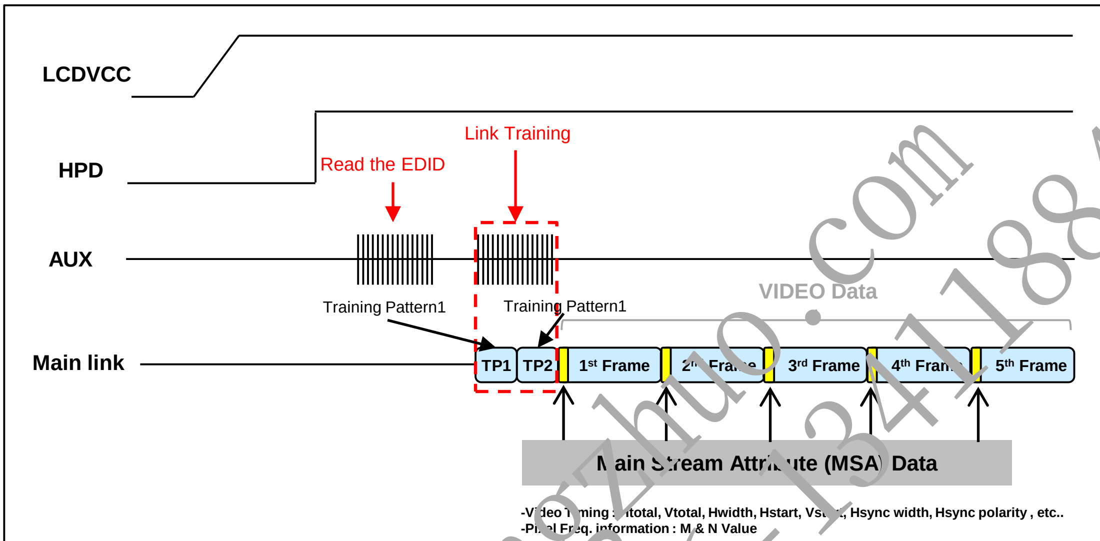
[Case1. Resolution Change]



[Case2. Close the Lid]

Define	If Main Link off signal from Source, then LCDVCC must be Power Off within T10 period at Non-PSR mode

APPENDIX B. LGD Proposal for eDP Interface Design Guide

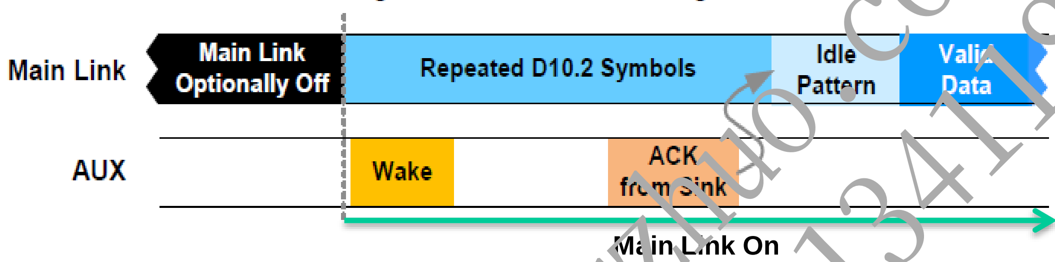
6	Main Link M & N value of MSA data
	
Define	It need to fix M& N value of MSA data output to prevent the initial abnormal M& N Value from incoming after power on.

APPENDIX B. LGD Proposal for eDP Interface Design Guide

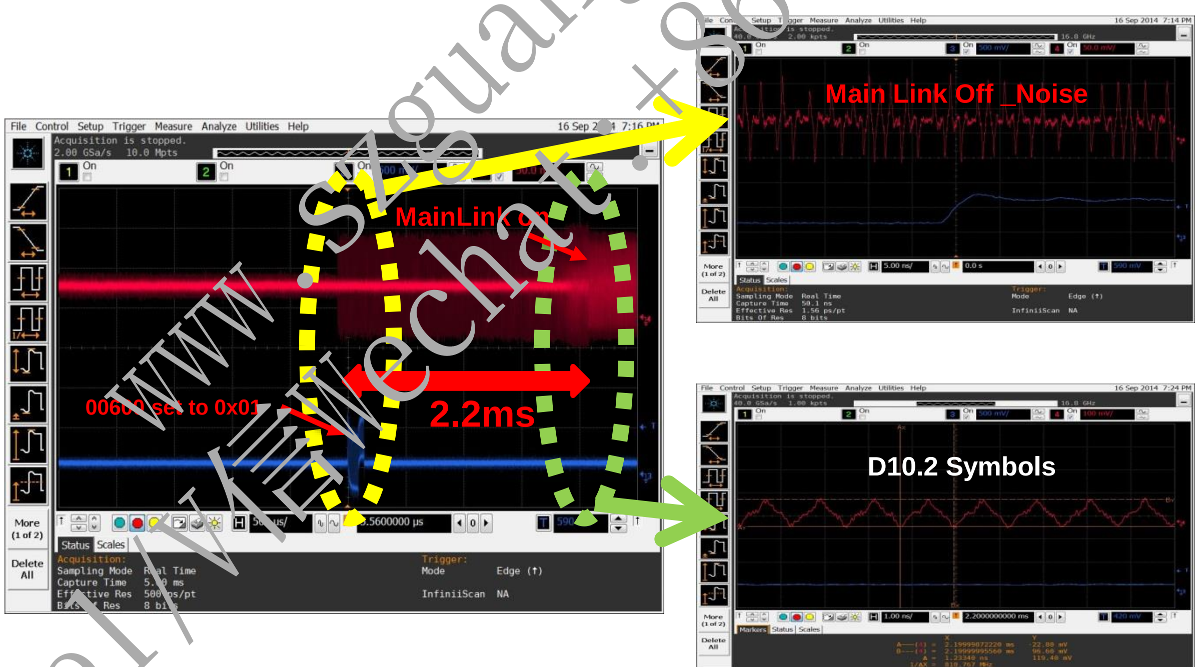
7	PSR Exit

If link training is not required, the Source must begin transmitting data on the Main Link prior to the wake AUX command which occurs through writing 01h to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h; see *DP v1.2a*), as illustrated in the upper portion of Figure 6-9. This transmitted data must be a repetition of D10.2 symbols (which is the same as Link Training Pattern 1). Note the requirement above to transmit five repeats of the Idle Pattern after receiving ACK from the Sink.

PSR Exit Link Management with No Link Training



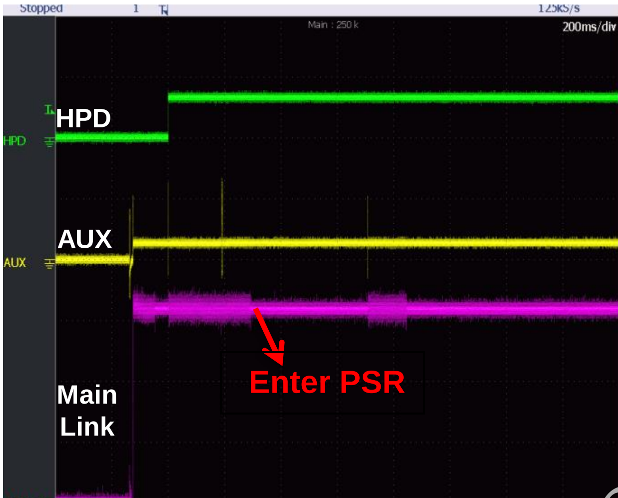
-. The below waveform is the issued case.



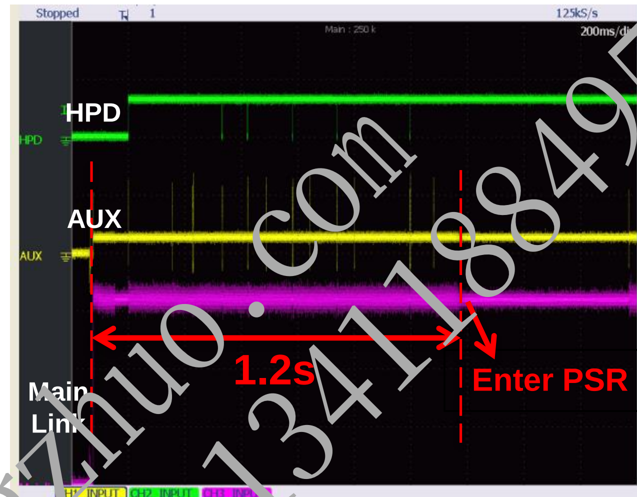
Define	If link training is not required, the source must begin transmitting data on the ML prior to the wake AUX wake-up command.

APPENDIX B. LGD Proposal for eDP Interface Design Guide

8	1st time PSR Entry after Power on



< Issue waveform >



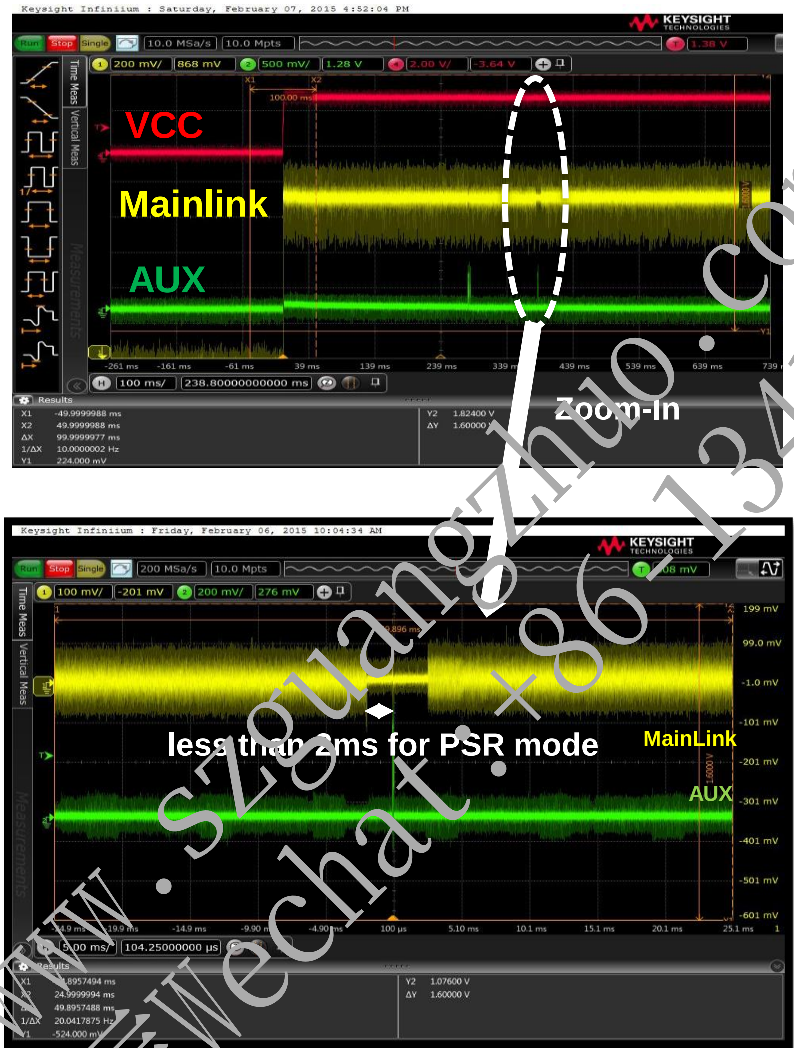
< solution waveform >

1. It is found that with solution , the TCON enter the PSR timing is 1.2s delay from VCC on which avoid TCON capture the wrong data from DP link(poor link quality) and enter the BIST mode + PSR mode(black screen).
2. **According to test, link is stable 800ms after VCC on.**

Define	After power(Vcc) on, the DP link is not stable, so the source try to PSR entry at 800ms after Power(Vcc) on..

APPENDIX B. LGD Proposal for eDP Interface Design Guide

9	PSR Period Issue

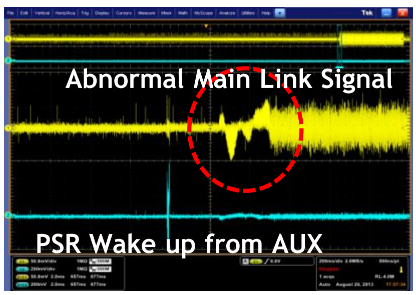


1. When issue is happened, system go to PSR mode for very short time.
2. If PSR active period is shorter than 1frame(16.67ms), T-Con can not go to the standby mode for PSR exit.

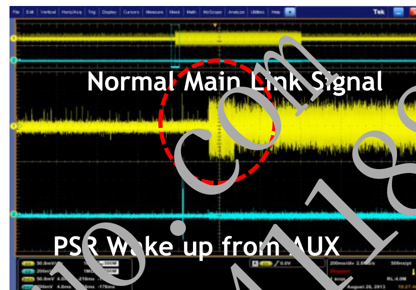
Define	When GPU go to the PSR mode, the source must hold the main link off over than 1frame.

APPENDIX B. LGD Proposal for eDP Interface Design Guide

10	**Main Link Noise at PSR Exit**



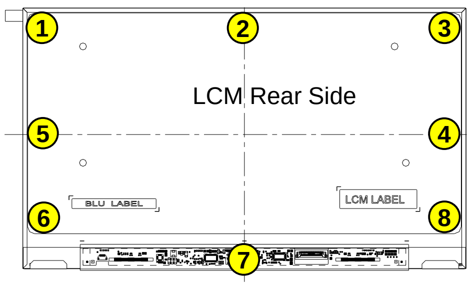
[Abnormal Main Link Noise]

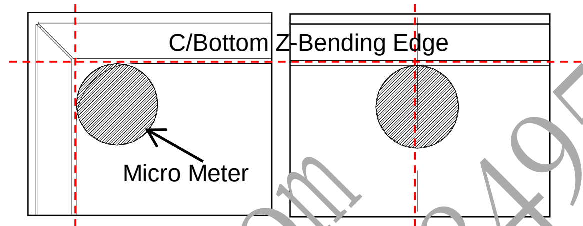


[Normal Main Link Signal]

Define	Main Link Noise at PSR Exit mode can be a cause abnormal display.

APPENDIX C. LGD Proposal for Measurement Method

<table>
<tr><th>1</th><th>LCM Thickness</th></tr>
<tr><td>Point</td><td>



C/Bottom Z-Bending Edge (①,③,⑥,⑧)
LCM Center (②,④,⑤)</td></tr>
<tr><td>Measure Tool</td><td>Micro Meter

</td></tr>
<tr><td>Guide</td><td>✓ Measure the thickness between Polarizer surface and M/Chassis on the rear of LCM
✓ Subtract Pol. protect film thickness from LCM thickness</td></tr>
</table>

APPENDIX D. Enhanced Extended Display Identification Data (EEDID™) 1/6

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
Header	0	00	Header	00	00000000
	1	01	Header	FF	11111111
	2	02	Header	FF	11111111
	3	03	Header	FF	11111111
	4	04	Header	FF	11111111
	5	05	Header	FF	11111111
	6	06	Header	FF	11111111
	7	07	Header	00	00000000
Vendor / Product EDID Version	8	08	ID Manufacture Name LGD	30	00110000
	9	09	ID Manufacture Name	E4	11100100
	10	0A	ID Product Code 0726h	26	00100110
	11	0B	(Hex. LSB first)	07	00000111
	12	0C	ID Serial No. - Optional ("00h" If not used, Number Only and LSB First)	00	00000000
	13	0D	ID Serial No. - Optional ("00h" If not used, Number Only and LSB First)	00	00000000
	14	0E	ID Serial No. - Optional ("00h" If not used, Number Only and LSB First)	00	00000000
	15	0F	ID Serial No. - Optional ("00h" If not used, Number Only and LSB First)	00	00000000
	16	10	Week of Manufacture - Optinal 00 weeks	00	00000000
	17	11	Year of Manufacture 2021 years	1F	00011111
	18	12	EDID structure version # = 1	01	00000001
	19	13	EDID revision # = 4	04	00000100
Display Parameters	20	14	Video input Definition = Input is a Digital Video signal Interface , Color Bit Depth : 8 Bits per Primary Color , Digital Video Interface Standard Supported: DisplayPort is supported	A5	10100101
	21	15	Horizontal Screen Size (Rounded cm) = 31 cm	1F	00011111
	22	16	Vertical Screen Size (Rounded cm) = 17 cm	11	00010001
	23	17	Display Transfer Characteristic (Gamma) = (gamma*100)-100 = Example:(2.2*100)-100=120	78	01111000
	24	18	Feature Support [Display Power Management(DPM) : Standby Mode is not supported, Suspend Mode is not supported, Active Off = Very Low Power is not supported ,Supportted Color Encoding Formats : RGB 4:4:4 ,Other Feature Support Flags : sRGB, Preferred Timing Mode, Display is continuous frequency (Display Range Limits Descriptor is required).]	07	00000111
Panel Color Coordinates	25	19	Red/Green Low Bits (RxRy/GxGy)	5E	01011110
	26	1A	Blue/White Low Bits (BxBy/WxWy)	85	10000101
	27	1B	Red X Rx = 0.653	A7	10100111
	28	1C	Red Y Ry = 0.333	55	01010101
	29	1D	Green X Gx = 0.30	4C	01001100
	30	1E	Green Y Gy = 0.592	97	10010111
	31	1F	Blue X Bx = 0.143	24	00100100
	32	20	Blue Y By = 0.059	0F	00001111
	33	21	White X Wx = 0.313	50	01010000
	34	22	White Y Wy = 0.329	54	01010100
Established Timings	35	23	Established timing 1 (Optional_00h if not used)	00	00000000
	36	24	Established timing 2 (Optional_00h if not used)	00	00000000
	37	25	Manufacturer's timings (Optional_00h if not used)	00	00000000
Standard Timing ID	38	26	Standard timing ID1 (Optional_01h if not used)	01	00000001
	39	27	Standard timing ID1 (Optional_01h if not used)	01	00000001
	40	28	Standard timing ID2 (Optional_01h if not used)	01	00000001
	41	29	Standard timing ID2 (Optional_01h if not used)	01	00000001
	42	2A	Standard timing ID3 (Optional_01h if not used)	01	00000001
	43	2B	Standard timing ID3 (Optional_01h if not used)	01	00000001
	44	2C	Standard timing ID4 (Optional_01h if not used)	01	00000001
	45	2D	Standard timing ID4 (Optional_01h if not used)	01	00000001
	46	2E	Standard timing ID5 (Optional_01h if not used)	01	00000001
	47	2F	Standard timing ID5 (Optional_01h if not used)	01	00000001
	48	30	Standard timing ID6 (Optional_01h if not used)	01	00000001
	49	31	Standard timing ID6 (Optional_01h if not used)	01	00000001
	50	32	Standard timing ID7 (Optional_01h if not used)	01	00000001
	51	33	Standard timing ID7 (Optional_01h if not used)	01	00000001
	52	34	Standard timing ID8 (Optional_01h if not used)	01	00000001
	53	35	Standard timing ID8 (Optional_01h if not used)	01	00000001

APPENDIX D. Enhanced Extended Display Identification Data (EEDID^{TM}) 2/6

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
Timing Descriptor #1	54	36	Pixel Clock/10,000 (LSB) 138.7 MHz @ 60 Hz	2E	00101110
	55	37	Pixel Clock/10,000 (MSB)	36	00110110
	56	38	Horizontal Active (HA) (lower 8 bits) 1920 pixels	80	10000000
	57	39	Horizontal Blanking (HB) (lower 8 bits) 160 pixels	A0	10100000
	58	3A	Horizontal Active (HA) / Horizontal Blanking (HB) (upper 4:4bits)	70	01110000
	59	3B	Vertical Avtive (VA) 1080 lines	38	00111000
	60	3C	Vertical Blanking (VB) (DE Blanking typ.for DE only panels) 31 lines	1F	00011111
	61	3D	Vertical Active (VA) / Vertical Blanking (VB) (upper 4:4bits)	40	01000000
	62	3E	Horizontal Front Porch in pixels (HF) (lower 8 bits) 48 pixels	30	00110000
	63	3F	Horizontal Sync Pulse Width in pixels (HS) (lower 8 bits) 32 pixels	20	00100000
	64	40	Vertical Front Porch in lines (VF) : Vertical Sync Pluse Width in lines (VS) (lower 4 bits) 3 lines : 5 lines	35	00110101
	65	41	Horizontal Front Porch/ Sync Pulse Width/ Vertical Front Porch/ Sync Pulse Width (upper 2bits)	00	00000000
	66	42	Horizontal Vedio Image Size (mm) (lower 8 bits) 309 mm	35	00110101
	67	43	Vertical Vedio Image Size (mm) (lower 8 bits) 174 mm	AE	10101110
	68	44	Horizontal Image Size / Vertical Image Size (upper 4 bits)	10	00010000
	69	45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000
	70	46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000
	71	47	Non-Interlace, Normal display, no stereo, Digital Separate [Vsync_NEG, Hsync_POS (outside of V-sync)]	1A	00011010
Timing Descriptor #2	72	48	Pixel Clock/10,000 (LSB) 92.5 MHz @ 40 Hz	1F	00011111
	73	49	Pixel Clock/10,000 (MSB)	24	00100100
	74	4A	Horizontal Active (HA) (lower 8 bits) 1920 pixels	80	10000000
	75	4B	Horizontal Blanking (HB) (lower 8 bits) 160 pixels	A0	10100000
	76	4C	Horizontal Active (HA) / Horizontal Blanking (HB) (upper 4:4bits)	70	01110000
	77	4D	Vertical Avtive (VA) 1080 lines	38	00111000
	78	4E	Vertical Blanking (VB) (DE Blanking typ.for DE only panels) 31 lines	1F	00011111
	79	4F	Vertical Active (VA) / Vertical Blanking (VB) (upper 4:4bits)	40	01000000
	80	50	Horizontal Front Porch in pixels (HF) (lower 8 bits) 48 pixels	30	00110000
	81	51	Horizontal Sync Pulse Width in pixels (HS) (lower 8 bits) 32 pixels	20	00100000
	82	52	Vertical Front Porch in lines (VF) : Vertical Sync Pluse Width in lines (VS) (lower 4 bits) 3 lines : 5 lines	35	00110101
	83	53	Horizontal Front Porch/ Sync Pulse Width/ Vertical Front Porch/ Sync Pulse Width (upper 2bits)	00	00000000
	84	54	Horizontal Vedio Image Size (mm) (lower 8 bits) 309 mm	35	00110101
	85	55	Vertical Vedio Image Size (mm) (lower 8 bits) 174 mm	AE	10101110
	86	56	Horizontal Image Size / Vertical Image Size (upper 4 bits)	10	00010000
	87	57	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000
	88	58	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000
	89	59	Non-Interlace, Normal display, no stereo, Digital Separate [Vsync_NEG, Hsync_POS (outside of V-sync)]	1A	00011010
Timing Descriptor #3	90	5A	Reserved	00	00000000
	91	5B	Reserved	00	00000000
	92	5C	Reserved	00	00000000
	93	5D	Reserved	00	00000000
	94	5E	Reserved	00	00000000
	95	5F	Reserved	00	00000000
	96	60	Reserved	00	00000000
	97	61	Reserved	00	00000000
	98	62	Reserved	00	00000000
	99	63	Reserved	00	00000000
	100	64	Reserved	00	00000000
	101	65	Reserved	00	00000000
	102	66	Reserved	00	00000000
	103	67	Reserved	00	00000000
	104	68	Reserved	00	00000000
	105	69	Reserved	00	00000000
	106	6A	Reserved	00	00000000
	107	6B	Reserved	00	00000000

APPENDIX D. Enhanced Extended Display Identification Data (EEDID™) 3/6

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
Timing Descriptor #4	108	6C	Detailed Timing Descriptions #4	00	00000000
	109	6D	Flag	00	00000000
	110	6E	Reserved	00	00000000
	111	6F	For Brightness Table and Power consumption	02	00000010
	112	70	Flag	00	00000000
	113	71	PWM % [7:0] @ Step 0 5 % @ 20 nit	0C	00001100
	114	72	PWM % [7:0] @ Step 5 15 % @ 60 nit	26	00100110
	115	73	PWM % [7:0] @ Step 10 100 % @ 400 nit	FF	11111111
	116	74	Nits [7:0] @ Step 0	14	00010100
	117	75	Nits [7:0] @ Step 5	3C	00111100
	118	76	Nits [7:0] @ Step 10	C8	11001000
	119	77	Panel Electronicx Power @ 32 x 32 Chess Pattern = 440 mW	0B	00001011
	120	78	Backlight Power @ 60 nits = 1040 mW	1A	00011010
	121	79	Backlight Power @ Step 10 = 3100 mW	27	00100111
	122	7A	Nits @ 100% PWM Duty = 400 nit	C8	11001000
	123	7B	Flag	00	00000000
	124	7C	Flag	00	00000000
	125	7D	Flag	00	00000000
Checksum	126	7E	Extension flag (# of optional 128 panel ID extension block to follow, Typ = 0)	01	00000001
	127	7F	Check Sum (The 1-byte sum of all 128 bytes in this panel ID block shall = 0)	2B	00101011

APPENDIX D. Enhanced Extended Display Identification Data (EEDID™) 4/6

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
DID Extension Header	128	80	DisplayID EDID Extension Block tag	70	01110000
	129	81	DisplayID Version/Revsion = 2.0	20	00100000
	130	82	Section Size (byte) = 121 bytes	79	01111001
	131	83	Display Product Primary Use Case	00	00000000
	132	84	Extension count	00	00000000
DID Block #1 Header	133	85	DID2.0 Data block tag[25h] = Dynamic Video Timing Range Limits	25	00100101
	134	86	Block revision = Revision 1	01	00000001
	135	87	Number of Payload Bytes in block= 9 Bytes	09	00001001
DID DATA Block #1	136	88	Minimum Pixel Clock (Low bit, Range = 0.001Mhz (000000h) ~ 16,777.216Mhz (FFFFFFh)) 92.435 MHz @ 40 Hz	12	00010010
	137	89	Minium Pixel Clock (Middle bit)	69	01101001
	138	8A	Minium Pixel Clock (High bit)	01	00000001
	139	8B	Maximum Pixel Clock (Low bit, Range = 0.001Mhz (000000h) ~ 16,777.216Mhz (FFFFFFh)) 138.7 MHz @ 60 Hz	CA	11001010
	140	8C	Maximum Pixel Clock (Middle bit)	1D	00011101
	141	8D	Maximum Pixel Clock (High bit)	02	00000010
	142	8E	Min. Vertical Rate : 40 Hz (Range : 0Hz (00h) ~ 255Hz (FFh))	28	00101000
	143	8F	Max. Vertical Rate : 60 Hz (Range : 0Hz (000h) ~ 1023Hz (3FFh))	3C	00111100
	144	90	Seamless Dynamic Video Timing Support : Seamless Dynamic Video Timing change shall be supported with a fixed horizont	80	10000000
DID Block #2 Header	145	91	DID2.0 Data block tag[81h] = CTA DisplayID	81	10000001
	146	92	Block revision = Revision 0	00	00000000
	147	93	Number of Payload Bytes in block= 19 Bytes	13	00010011
DID DATA Block #2	148	94	CTA Block1 Tag Code and Block1 Length = Vendor Specific Data Block(03h), Size(byte) = 18 bytes	72	01110010
	149	95	AMD IEEE OUI value (0x00001A)	1A	00011010
	150	96	(Hex LSB first)	00	00000000
	151	97	(Hex MSB first)	00	00000000
	152	98	AMD VSDB Version 3	03	00000011
	153	99	Freesync Capability : Seamless Local Dimming Disable Control Not Supported , Seamless Native Color Space & Transfer Sw	01	00000001
	154	9A	Min Refresh Rate = 40 Hz	28	00101000
	155	9B	Max Refresh Rate = 60 Hz	3C	00111100
	156	9C	Freesync MCCS VCP Code	00	00000000
	157	9D	Support WCG and HDR features : Seamless Gamma 2.2 EOTF Not Supported , Seamless PQ EOTF Not Supported	00	00000000
	158	9E	Max Luminance 1 (for HDR) = 400 Cd/m2	60	01100000
	159	9F	Min Luminance 1 (for HDR) = 0.4 Cd/m2	50	01010000
	160	A0	Max Luminance 2 (for HDR) = 400 Cd/m2	60	01100000
	161	A1	Min Luminance 2 (for HDR) = 0.4 Cd/m2	50	01010000
	162	A2	Freesync Maximum Refresh Rate (LSB) : 60 Hz (Range : 0Hz (000h) ~ 1023Hz (3FFh), for VSDB v3)	3C	00111100
	163	A3	Freesync Maximum Refresh Rate (MSB)	00	00000000
	164	A4	Reseved	00	00000000
	165	A5	Reseved	00	00000000
	166	A6	Reseved	00	00000000

APPENDIX D. Enhanced Extended Display Identification Data (EEDID™) 5/6

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
Fill Data	167	A7	Reseved	00	00000000
	168	A8	Reseved	00	00000000
	169	A9	Reseved	00	00000000
	170	AA	Reseved	00	00000000
	171	AB	Reseved	00	00000000
	172	AC	Reseved	00	00000000
	173	AD	Reseved	00	00000000
	174	AE	Reseved	00	00000000
	175	AF	Reseved	00	00000000
	176	B0	Reseved	00	00000000
	177	B1	Reseved	00	00000000
	178	B2	Reseved	00	00000000
	179	B3	Reseved	00	00000000
	180	B4	Reseved	00	00000000
	181	B5	Reseved	00	00000000
	182	B6	Reseved	00	00000000
	183	B7	Reseved	00	00000000
	184	B8	Reseved	00	00000000
	185	B9	Reseved	00	00000000
	186	BA	Reseved	00	00000000
	187	BB	Reseved	00	00000000
	188	BC	Reseved	00	00000000
	189	BD	Reseved	00	00000000
	190	BE	Reseved	00	00000000
	191	BF	Reseved	00	00000000
	192	C0	Reseved	00	00000000
	193	C1	Reseved	00	00000000
	194	C2	Reseved	00	00000000
	195	C3	Reseved	00	00000000
	196	C4	Reseved	00	00000000
	197	C5	Reseved	00	00000000
	198	C6	Reseved	00	00000000
	199	C7	Reseved	00	00000000
	200	C8	Reseved	00	00000000
	201	C9	Reseved	00	00000000
	202	CA	Reseved	00	00000000
	203	CB	Reseved	00	00000000
	204	CC	Reseved	00	00000000
	205	CD	Reseved	00	00000000
	206	CE	Reseved	00	00000000
	207	CF	Reseved	00	00000000
	208	D0	Reseved	00	00000000
	209	D1	Reseved	00	00000000
	210	D2	Reseved	00	00000000
	211	D3	Reseved	00	00000000
	212	D4	Reseved	00	00000000
	213	D5	Reseved	00	00000000
	214	D6	Reseved	00	00000000
	215	D7	Reseved	00	00000000
	216	D8	Reseved	00	00000000

APPENDIX D. Enhanced Extended Display Identification Data (EEDID™) 6/6

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
Fill Data	217	D9	Reseved	00	00000000
	218	DA	Reseved	00	00000000
	219	DB	Reseved	00	00000000
	220	DC	Reseved	00	00000000
	221	DD	Reseved	00	00000000
	222	DE	Reseved	00	00000000
	223	DF	Reseved	00	00000000
	224	E0	Reseved	00	00000000
	225	E1	Reseved	00	00000000
	226	E2	Reseved	00	00000000
	227	E3	Reseved	00	00000000
	228	E4	Reseved	00	00000000
	229	E5	Reseved	00	00000000
	230	E6	Reseved	00	00000000
	231	E7	Reseved	00	00000000
	232	E8	Reseved	00	00000000
	233	E9	Reseved	00	00000000
	234	EA	Reseved	00	00000000
	235	EB	Reseved	00	00000000
	236	EC	Reseved	00	00000000
	237	ED	Reseved	00	00000000
	238	EE	Reseved	00	00000000
	239	EF	Reseved	00	00000000
	240	F0	Reseved	00	00000000
	241	F1	Reseved	00	00000000
	242	F2	Reseved	00	00000000
	243	F3	Reseved	00	00000000
	244	F4	Reseved	00	00000000
	245	F5	Reseved	00	00000000
	246	F6	Reseved	00	00000000
	247	F7	Reseved	00	00000000
	248	F8	Reseved	00	00000000
	249	F9	Reseved	00	00000000
	250	FA	Reseved	00	00000000
	251	FB	Reseved	00	00000000
	252	FC	Reseved	00	00000000
	253	FD	Reseved	00	00000000
checksum	254	FE	DisplayID section checksum (81h~FDh)	CB	11001011
	255	FF	Extended block checksum (80h~FEh)	90	10010000