Product Specification

AUO CORPORATION

( ) Preliminary Specifications
(V) Final Specifications

Module	**17.3”(17.26”) FHD 16:9 Color TFT-LCD with LED Backlight design**
Model Name	**B173HANAA.0**
H/W	**0A**
Note ( )	***LED Backlight with driving circuit design***

Customer	**Date**	**Approved by**	**Date**
		Eric CW Tseng	5/6/2025
Checked & Approved by	**Date**	**Prepared by**	**Date**
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Note: This Specification is subject to change without notice.		**AUO corporation**	

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Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2024/10/10	All	First Edition for Customer		
0.2 2024/12/5	All	H/W , EDID, label		
0.3 2025/6/5	All	Packing		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turnoff power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
10) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
11) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
12) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B173HANA**A**.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 FHD, 1920(H) x 1080(V) screen and 16.7M colors (RGB 8-bit) with LED backlight driving circuit. All input signals are eDP interface compatible.

B173HANA**A**.0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃condition:

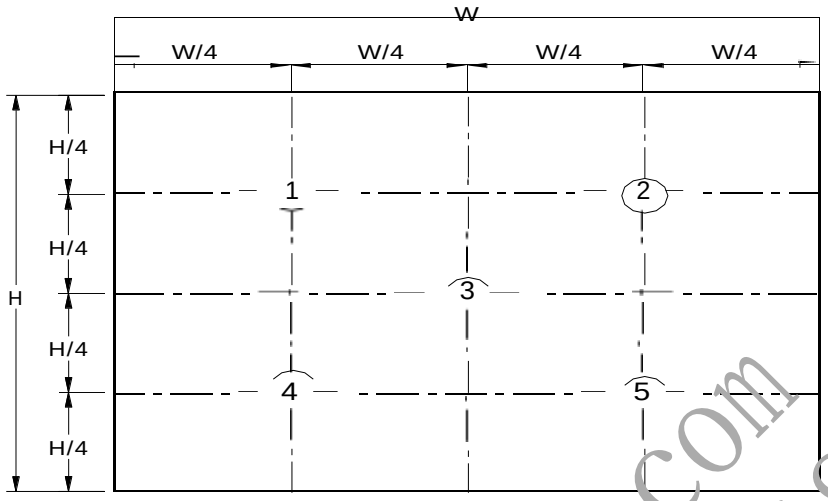
Items	Unit	Specifications			
Screen Diagonal	[mm]	17.3”(17.26)			
Active Area	[mm]	381.888 x 214.812			
Pixels H x V		1920 x 3 (RGB) x 1080			
Pixel Pitch	[mm]	0.1989 x 0.1989			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black			
White Luminance (I_{LED}=14.5mA) (Note: I_{LED} is LED current)	[cd/m^2]	250 typ. (5 points average) 212.5 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		800 typ			
Response Time	[ms]	25 typ.			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	5.0W (max: inculd Logic@mosaic & BL power)			
Weight	[Grams]	500g max			
Physical Size	[mm]		Min.	Typ.	Max.
		Length	389.59	389.89	390.19
		Width	226.71	227.01	227.31
		Thickness	-	-	3.5
Electrical Interface		4 Lane eDP 1.3			
Glass Thickness	[mm]	0.4			
Surface Treatment		Anti-Glare, Hardness 3H			
Support Color		16.7M colors (RGB 8-bit)			
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +60 -20 to +60			
RoHS Compliance		RoHS Compliance			

2.2 Optical Characteristics

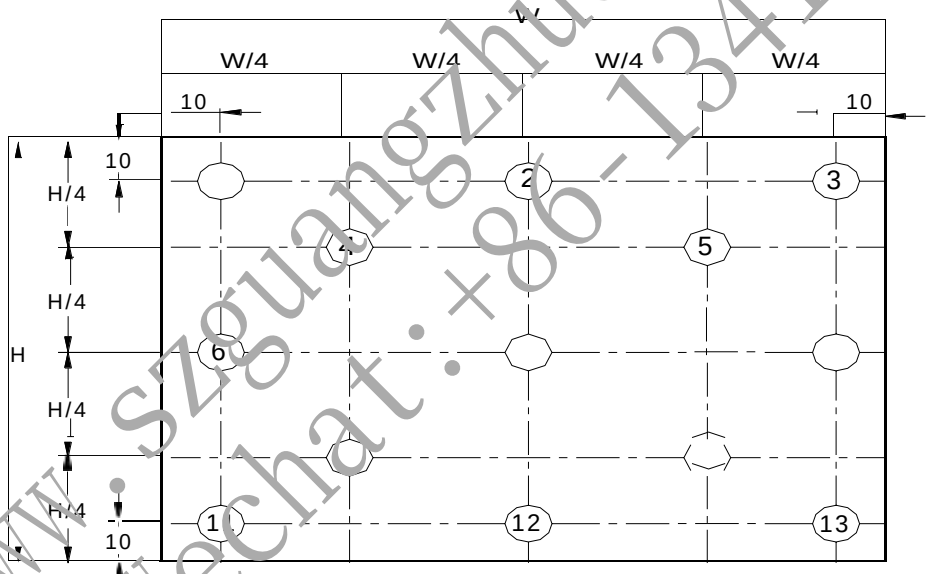
The optical characteristics are measured under stable conditions at 25℃(Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED} = 14.5mA (Base Panel Only)			5 points average	212.5	250	-	cd/m²	1, 4, 5
Viewing Angle		θ_R θ_L	Horizontal (Right) CR = 10 (Left)	80 80	85 85	89 89	degree	4, 9
		ψ_H ψ_L	Vertical (Upper) CR = 10 (Lower)	80 80	85 85	89 89		
Luminance Uniformity		δ_{5P}	5 Points	-		1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.6		2, 3, 4
Contrast Ratio		CR		600	800	-		4, 6
Cross talk		%				4		4, 7
Response Time		T_{RT}	Rising + Falling	-	25	35	msec	4, 8
Color / Chromaticity Coodinates	White	Wx	CIE 1931	0.283	0.313	0.343		4
		Wy		0.299	0.329	0.359		
	Red	Rx		0.545	0.575	0.605		
		Ry		0.317	0.347	0.377		
	Green	Gx		0.322	0.352	0.382		
		Gy		0.548	0.578	0.608		
	Blue	Bx		0.131	0.161	0.191		
		By		0.098	0.128	0.158		
NTSC		%		35	45	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

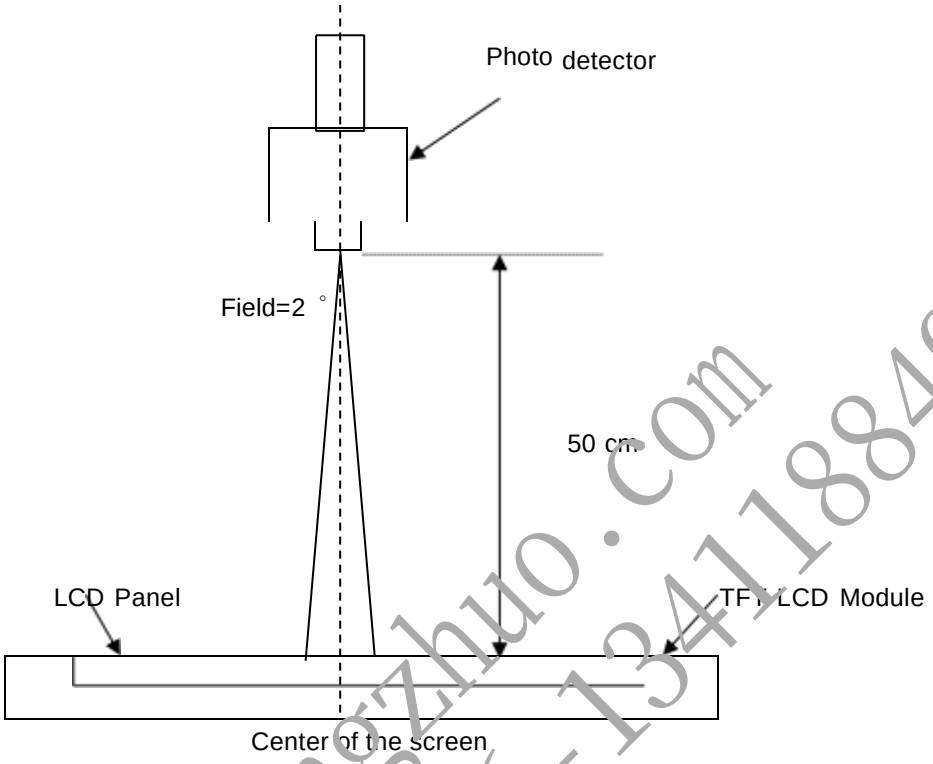
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable,windless and dark room, and it should be measured in the center of

screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

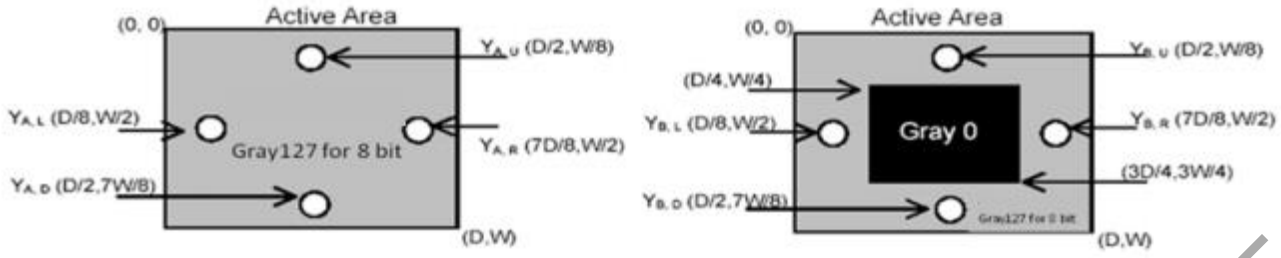
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B – Y_A | / Y_A \times 100\ (\%)$

Where

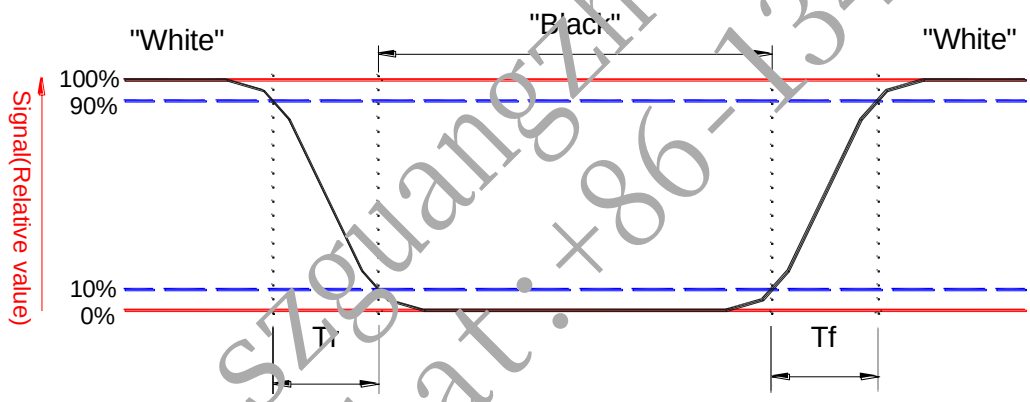
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



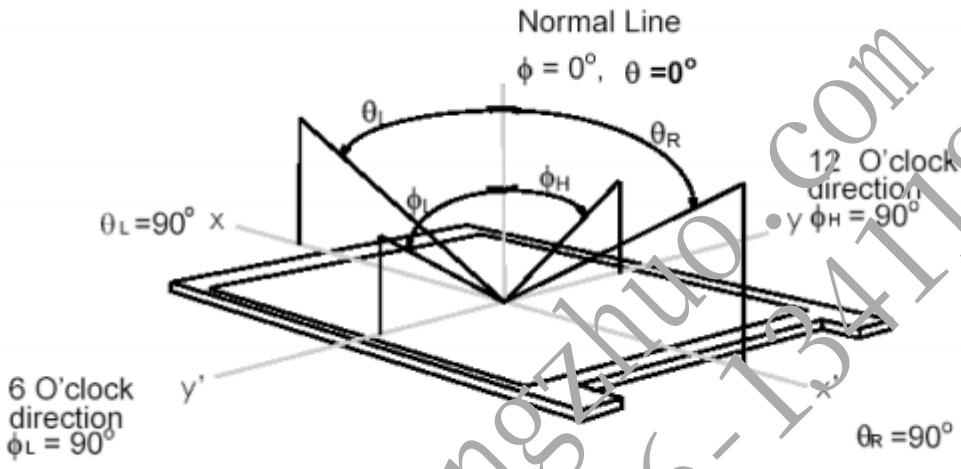
Note 8： Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



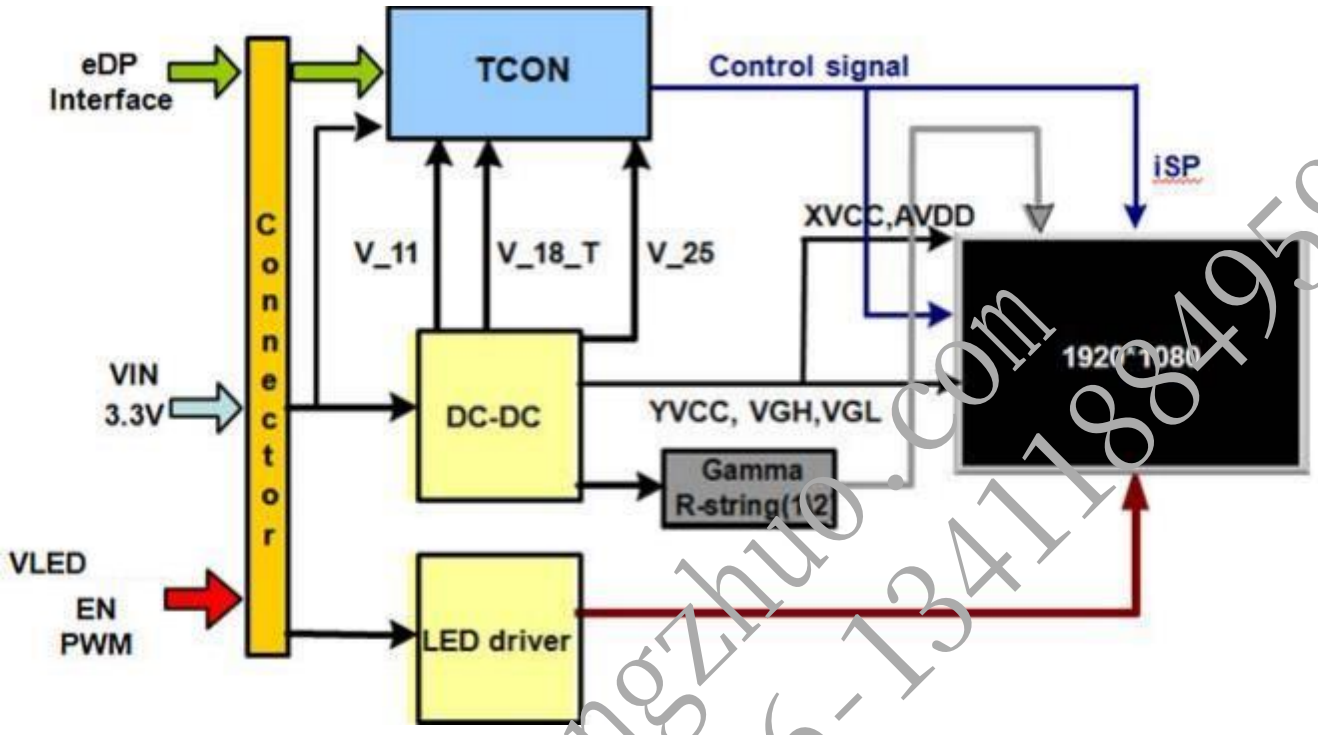
Note 9： Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 17.3 inches wide Color TFT/LCD 40 Pin



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

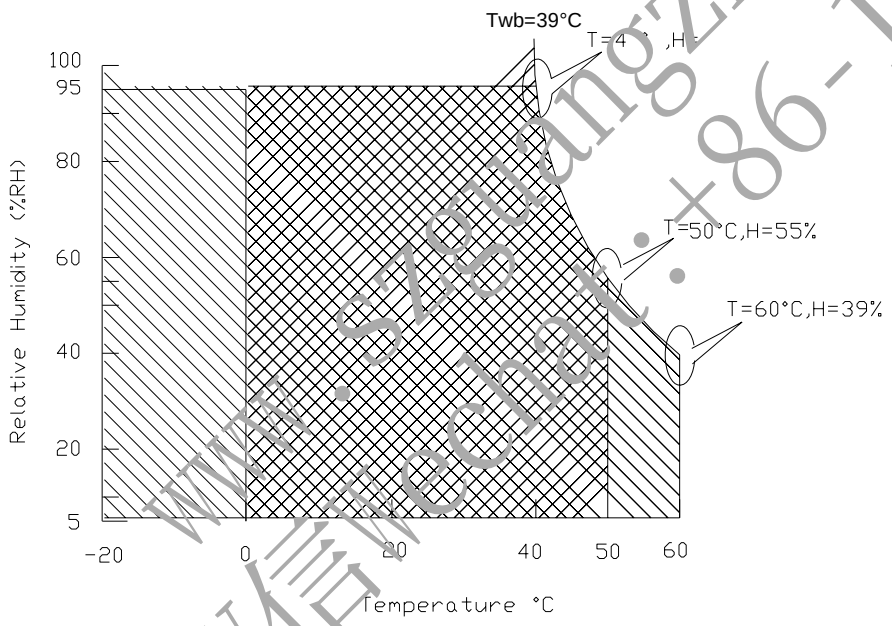
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	10	90	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

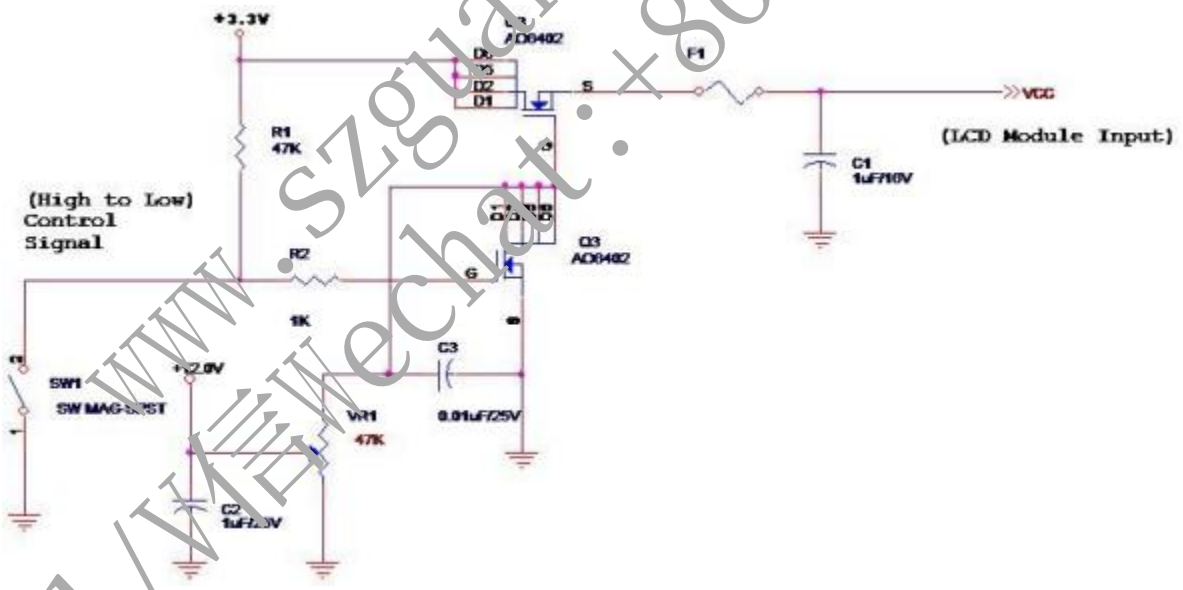
The power specification are measured under 25℃ and frame frenquency under 144Hz

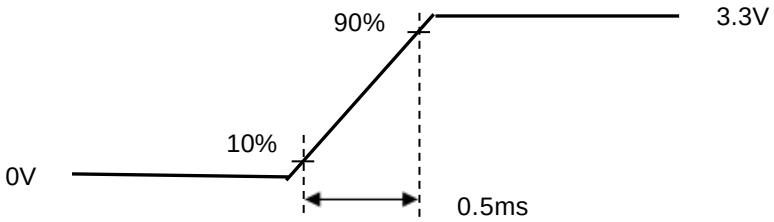
Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	2.0	3.1	[Watt]	Note 1
IDD	IDD Current	-	-	1033	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : PDD(typ)@ mosaic pattern Maximum Power ; PDD(Max)@ R/G/B pattern Maximum Power

IDD(Max)=PDD(Max) / VDD(Min)

Note 2： Measure Condition



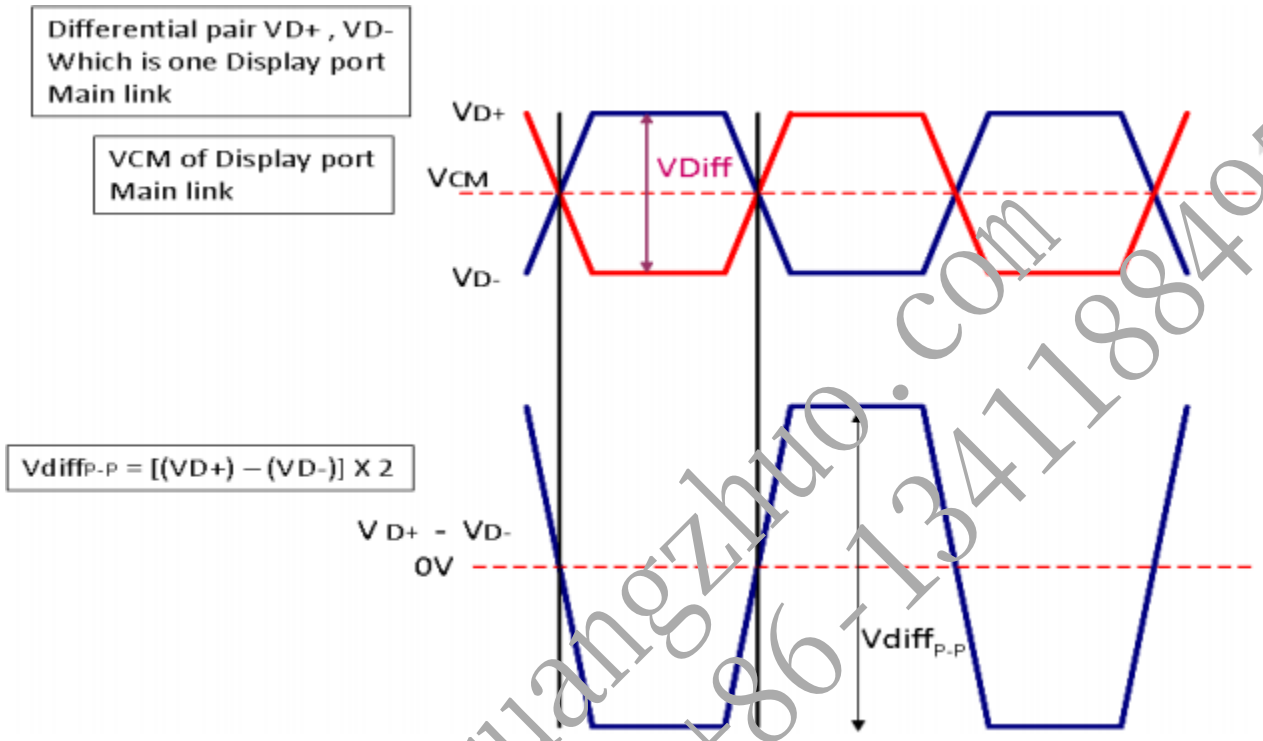


Vin rising time

5.1.2 Signal Electrical Characteristics

Signal electrical characteristics are as follows;

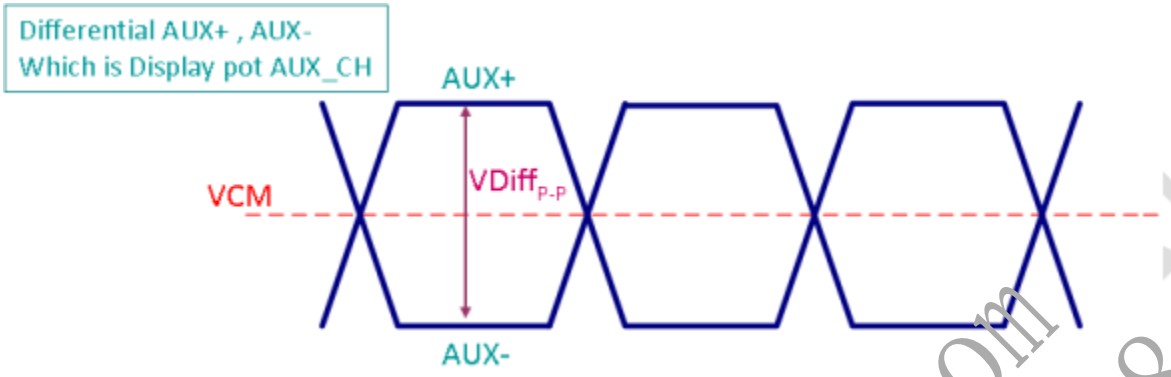
Display Port main link signal:



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
VDiffP-P	Peak-to peak Voltage at a receiving Device	75		1320	mV

Follow as VESA eDP1.4 Standard

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiffP-P	AUX Peak-to-peak Voltage at a receiving Device	270		800	V

Follow as VESA display port standard V1.4

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25	--	3.6	V

Follow as VESA display port standard V1.4

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	3	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-		(Ta=25℃), Note 2 IF=14.5 mA

Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED (Note 1)	6.0 Note 2	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2.5	--	3.6	[Volt]	
LED Enable Input Low Level		--	--	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	--	3.6	[Volt]	
PWM Logic Input Low Level		--	--	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

Note 1 : Recommend system pull up/down resistor no bigger than 10kohm

Note 2 : measured in panel VLED at PWM duty ratio 100%

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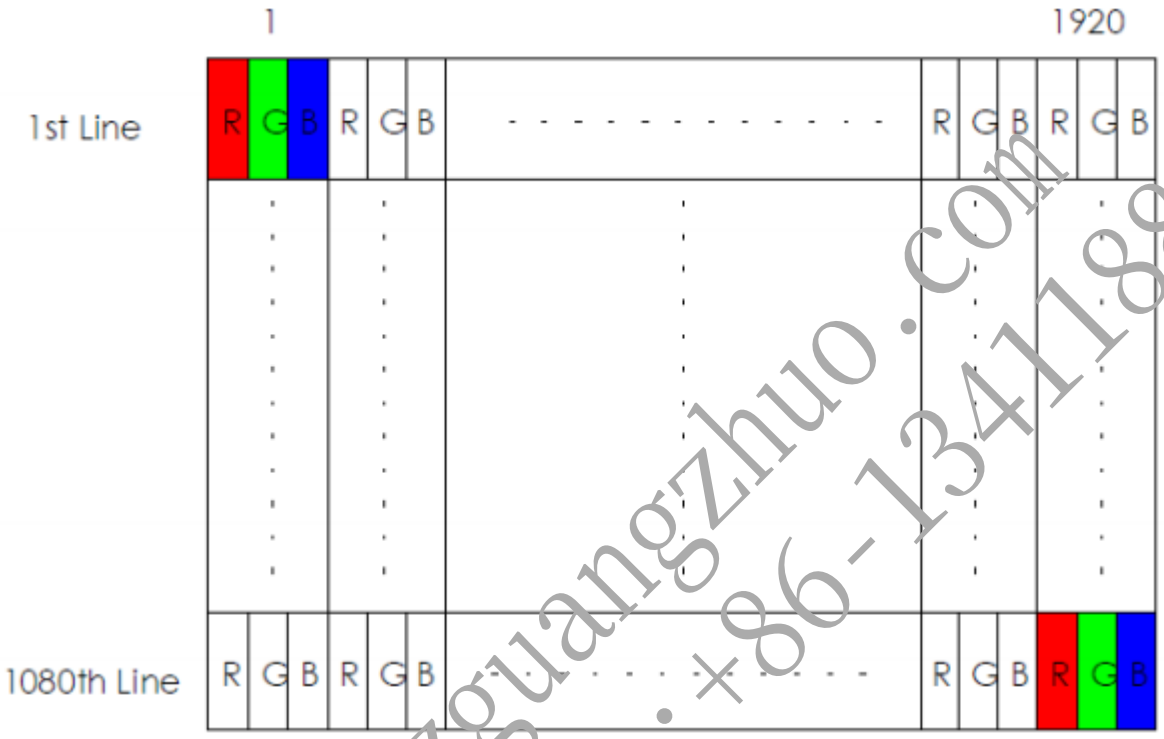
6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	STM

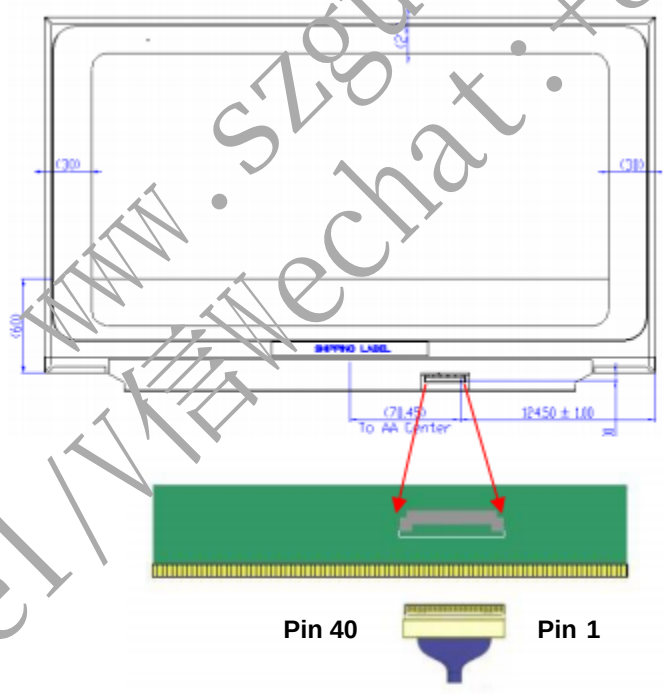
Type / Part Number	STM / MSAK24025P40M
Mating Housing/Part Number	I-PEX / 20704-040T-13 or compatible

6.2.2 Pin Assignment

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN No	Symbol	Function
1	NC	DCR or NC
2	H_GND	High Speed Ground
3	Lane3_N	Comp Signal Lane 3
4	Lane3_P	True Signal Link Lane 3
5	H_GND	High Speed Ground
6	Lane2_N	Comp Signal Lane 2
7	Lane2_P	True Signal Link Lane 2
8	H_GND	High Speed Ground
9	Lane1_N	Comp Signal Lane 1
10	Lane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12	Lane0_N	Comp Signal Link Lane 0
13	Lane0_P	True Signal Link Lane 0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Ch.
16	AUX_CH_N	Comp Signal Auxiliary Ch.
17	H_GND	High Speed Ground
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	LCD_Self_Test or NC	LCD Panel Self Test Enable (Optional)
23	LCD GND	LCD logic and driver ground
24	LCD GND	LCD logic and driver ground
25	LCD GND	LCD logic and driver ground
26	LCD GND	LCD logic and driver ground
27	HPD	HPD signale pin

28	BL_GND	Backlight_ground
29	BL_GND	Backlight_ground
30	BL_GND	Backlight_ground
31	BL_GND	Backlight_ground
32	BL_Enable	Backlight On / Off
33	BL PWM DIM	System PWM signal Input
34	NC	NC
35	NC	NC
36	BL_PWR	Backlight power (6V~21V)
37	BL_PWR	Backlight power (6V~21V)
38	BL_PWR	Backlight power (6V~21V)
39	BL_PWR	Backlight power (6V~21V)
40	NC	NC



Pin 40 **Pin 1**

Note1: Start from right side.
Note2: Input signals shall be low or High-impedance state when VDD is off.

Internal circuit of **eDP inputs** are as following.

6.3 Interface Timing

6.3.1 Timing Characteristics

Basically, interface timings should match the 1920x1080 / 144Hz manufacturing guide line timing.

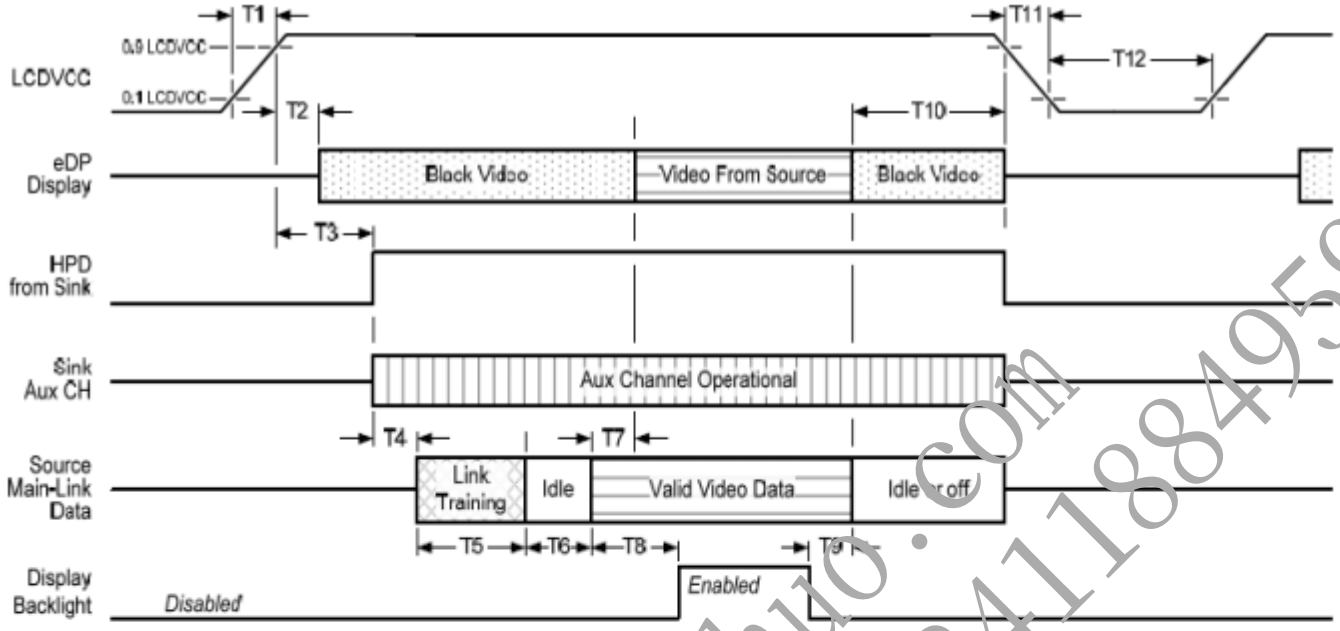
Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	60	-	144	Hz
Clock frequency		1/ T_{Clock}	148.83	-	357.13	MHz
Vertical Section	Period	T_V	1180	-	1180	T_{Line}
	Active	T_{VD}	1080			
	Blanking	T_{VB}	100	-	100	
Horizontal Section	Period	T_H	2102	-	2102	T_{Clock}
	Active	T_{HD}	1920			
	Blanking	T_{HB}	182	-	182	

Note 1 : The above is as optimized setting

6.4 Power ON/OFF Sequence

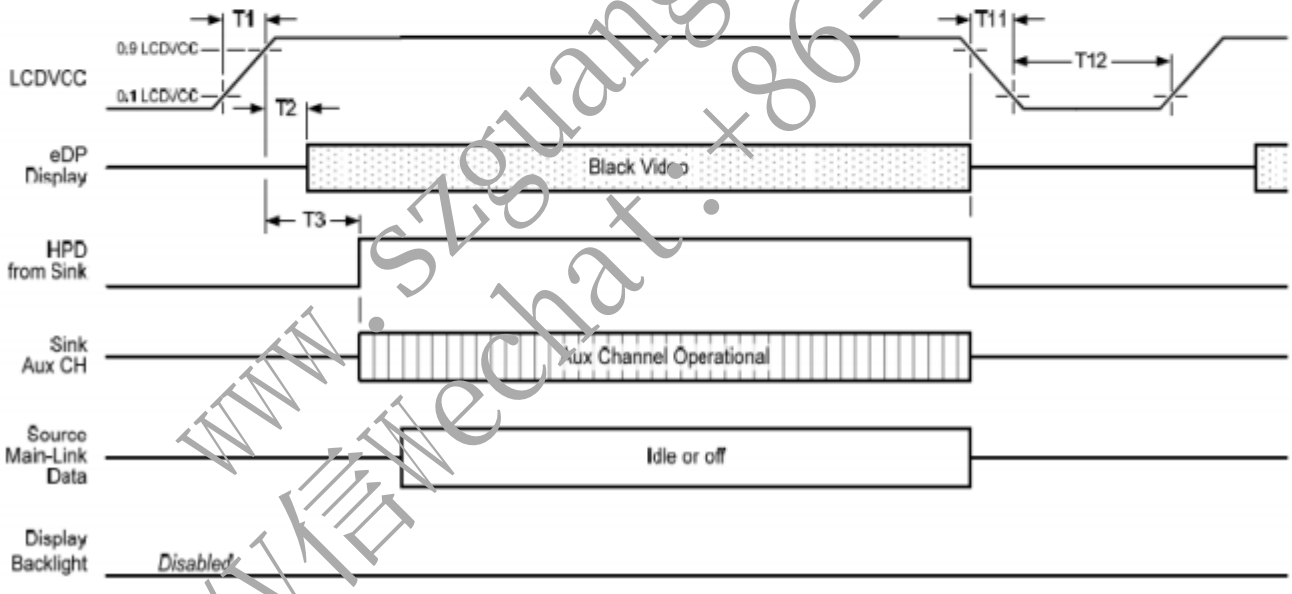
Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port Panel Power Sequence Timing Parameters

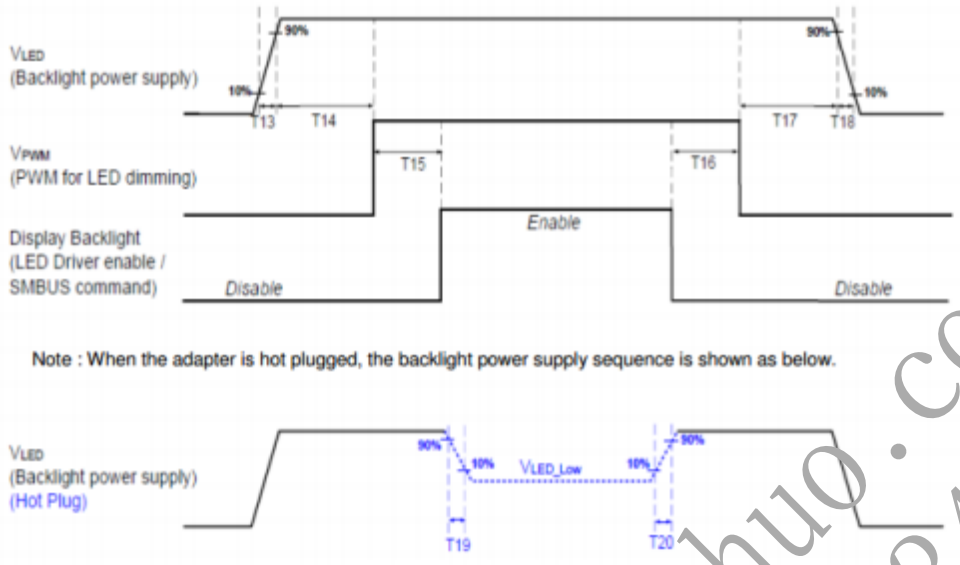
Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	50ms		500ms	
T11	power rail fall time, 90% to 10%	source			10ms	
T12	power off time	source	500ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCD VDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	0	-
T16	0	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM} = 1/PWM Frequency

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G，Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

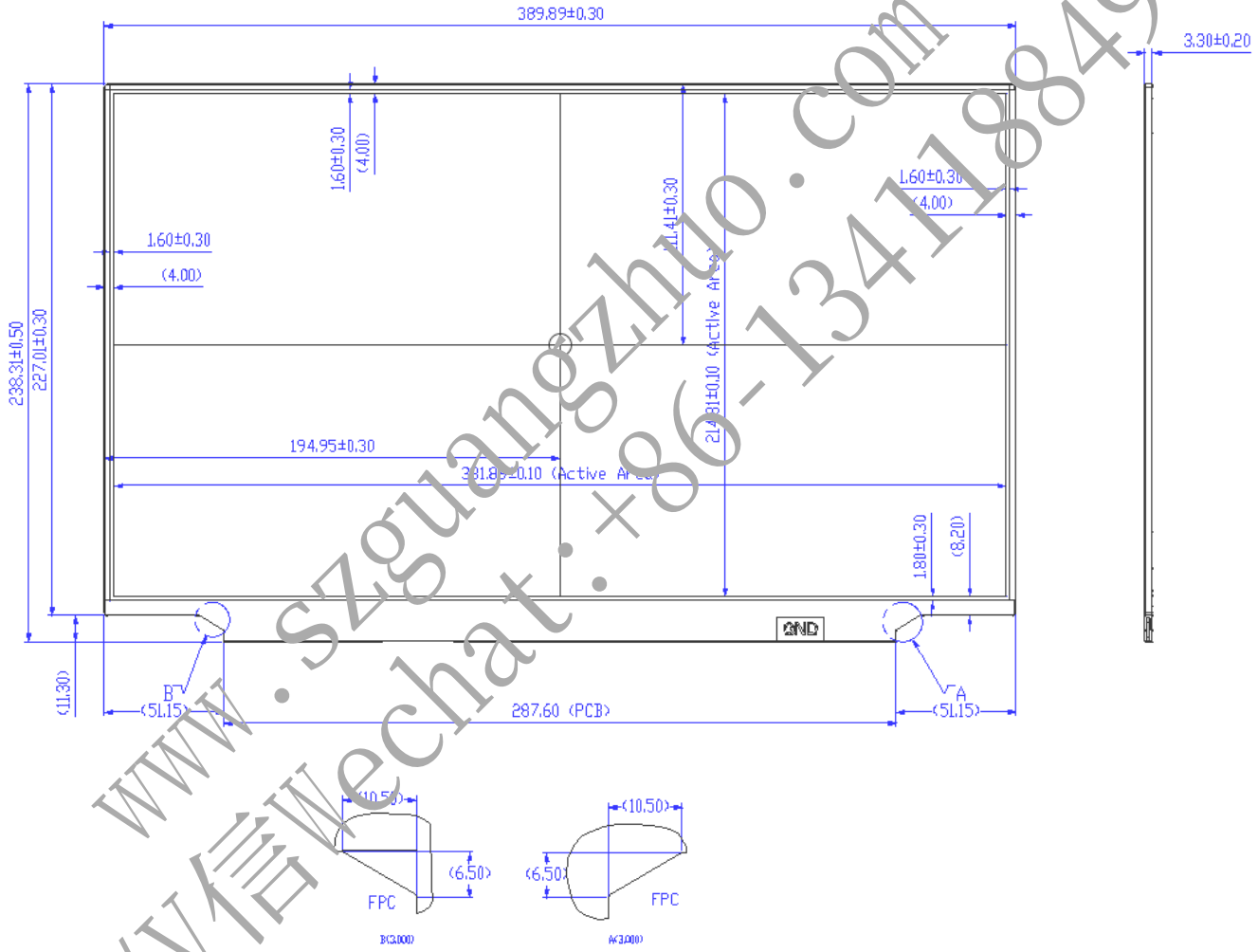
Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 240h	
High Temperature Operation	Ta= 60℃, 240h	
Low Temperature Operation	Ta= 0℃, 240h	
High Temperature Storage	Ta= 60℃, 240h	
Low Temperature Storage	Ta= -20℃, 240h	
Thermal Shock Test	Ta=-20℃ to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact：±8 KV Air：±15 KV	Note 1

Note1: According to EN 61000-4-2，ESD class B: Some performance degradation allowed. No data lost Self-recoverable. No hardware failures.

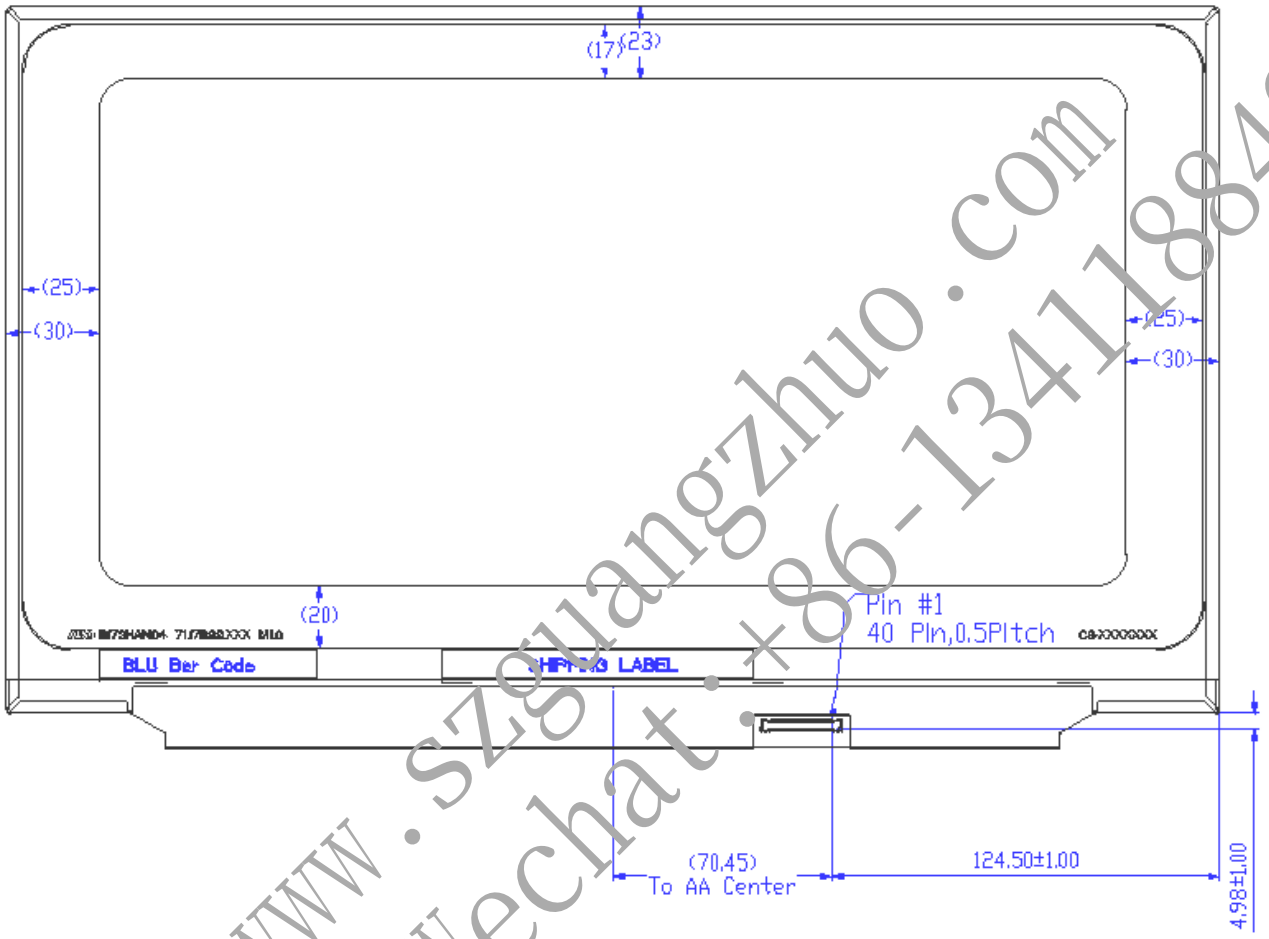
Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

8.1 LCM Outline Dimension



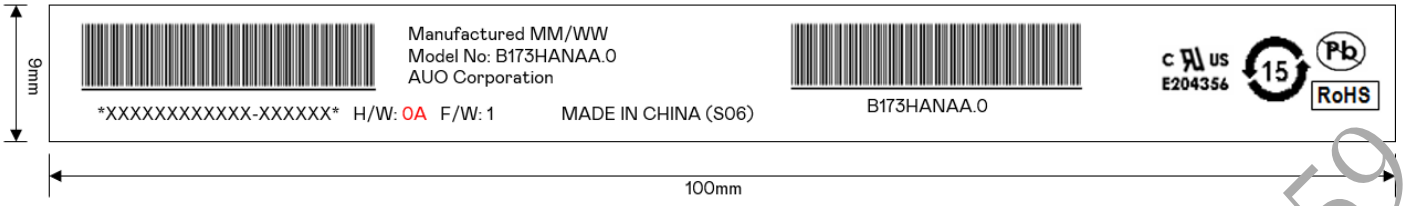
NOTE:
1.MEASURED METHOD IS VERNIER CALIPER.



Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

9. Shipping and Package

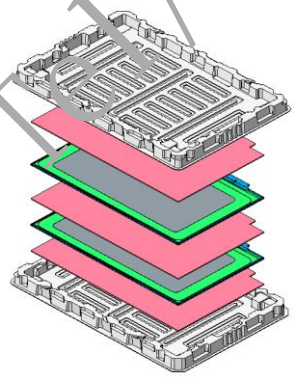
9.1 Shipping Label Format

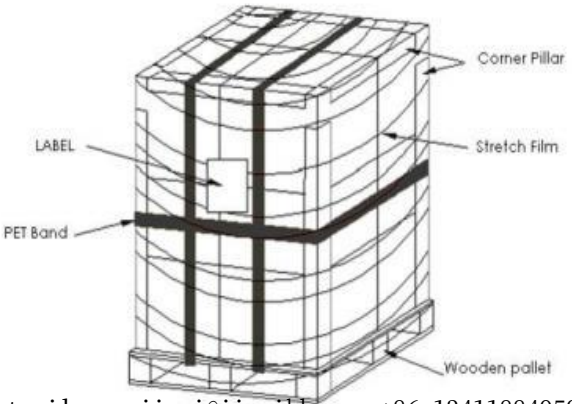


9.2 Carton Package

9.3 Shipping Package of Palletizing Sequence

3PCS Spacer + 2PCS Panel / Tray
28PCS/箱





10. Appendix

10.1 EDID Description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01	Header	FF	11111111	255	
02	Header	FF	11111111	255	
03	Header	FF	11111111	255	
04	Header	FF	11111111	255	
05	Header	FF	11111111	255	
06	Header	FF	11111111	255	
07	Header	00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	B8	10111000	184	
0B	Product Code	4A	01001010	74	
0C	32-bit ser #	00	00000000	0	
0D	ID S/N - option	00	00000000	0	
0E	ID S/N - option	00	00000000	0	
0F	ID S/N - option	00	00000000	0	
10	Week of manufacture	2D	00101101	45	
11	Year of manufacture	22	00100010	34	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	04	00000100	4	
14	**Video input def. (digital I/P, non-TMDS, CRGB)**	A5	10100101	165	
15	**Max H image size (rounded to cm)**	26	00100110	38	
16	**Max V image size (rounded to cm)**	16	00010110	22	
17	**Display Gamma (= gamma*100)-100**	78	01111000	120	
18	**Feature support (no DPMS, Active OFF, RGB, tmg Blk#1)**	03	00000011	3	
19	Red/green low bits (Lower 2:2:2:2 bits)	70	01110000	112	
1A	Blue/white low bits (Lower 2:2:2:2 bits)	75	01110101	117	
1B	Red x (Upper 8 bits)	93	10010011	147	
1C	Red y (Upper 8 bits)	58	01011000	88	
1D	Green x	5A	01011010	90	
1E	Green y	94	10010100	148	
1F	Blue x	29	00101001	41	
20	Blue y	20	00100000	32	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27	Standard timing #1	01	00000001	1	
28	Standard timing #2	01	00000001	1	
29	Standard timing #2	01	00000001	1	

2A	Standard timing #3	01	00000001	1	
2B	Standard timing #3	01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D	Standard timing #4	01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F	Standard timing #5	01	00000001	1	
30	Standard timing #6	01	00000001	1	
31	Standard timing #6	01	00000001	1	
32	Standard timing #7	01	00000001	1	
33	Standard timing #7	01	00000001	1	
34	Standard timing #8	01	00000001	1	
35	Standard timing #8	01	00000001	1	
36	Pixel Clock/10000 LSB	86	10000110	134	
37	Pixel Clock/10000 USB	8B	10001011	139	
38	Horz active Lower 8bits	80	10000000	128	
39	Horz blanking Lower 8bits	B6	10110110	182	
3A	HorzAct:HorzBlnk Upper 4:4 bits	70	01110000	112	
3B	Vertical Active Lower 8bits	38	00111000	56	
3C	Vertical Blanking Lower 8bits	64	01100100	100	
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	40	01000000	64	
3E	HorzSync. Offset	30	00110000	48	
3F	HorzSync.Width	20	00100000	32	
40	VertSync.Offset : VertSync.Width	A5	10100101	165	
41	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0	
42	Horizontal Image Size Lower 8bits	7E	01111110	126	
43	Vertical Image Size Lower 8bits	D7	11010111	215	
44	Horizontal & Vertical Image Size (upper 4:4 bits)	10	00010000	16	
45	Horizontal Border (zero for internal LCD)	00	00000000	0	
46	Vertical Border (zero for internal LCD)	00	00000000	0	
47	Signal (non-intr, norm, no stero, sep sync, neg pol)	18	00011000	24	
48	Pixel Clock/10000 LSB	23	00100011	35	
49	Pixel Clock/10000 USB	3A	00111010	58	
4A	Horz active Lower 8bits	80	10000000	128	
4B	Horz blanking Lower 8bits	B6	10110110	182	
4C	HorzAct:HorzBlnk Upper 4:4 bits	70	01110000	112	
4D	Vertical Active Lower 8bits	38	00111000	56	
4E	Vertical Blanking Lower 8bits	64	01100100	100	
4F	Vert Act : Vertical Blanking (upper 4:4 bit)	40	01000000	64	
50	HorzSync. Offset	30	00110000	48	
51	HorzSync.Width	20	00100000	32	
52	VertSync.Offset : VertSync.Width	A5	10100101	165	
53	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0	
54	Horizontal Image Size Lower 8bits	7E	01111110	126	
55	Vertical Image Size Lower 8bits	D7	11010111	215	
56	Horizontal & Vertical Image Size (upper 4:4 bits)	10	00010000	16	
57	Horizontal Border (zero for internal LCD)	00	00000000	0	
58	Vertical Border (zero for internal LCD)	00	00000000	0	
59	Signal (non-intr, norm, no stero, sep sync, neg pol)	18	00011000	24	
5A	descriptor #3	00	00000000	0	
5B	Reserved for definition	00	00000000	0	
5C	Reserved for definition	00	00000000	0	
5D	ASCII String	FD	11111101	253	
5E	Reserved for definition	00	00000000	0	
5F	Manufacture	30	00110000	48	0

60	Manufacture	90	10010000	144	
61	Manufacture	AA	10101010	170	
62	Reserved for definition	AA	10101010	170	
63	Reserved for definition	24	00100100	36	
64	Reserved for definition	01	00000001	1	
65	Reserved for definition	0A	00001010	10	
66	Reserved for definition	20	00100000	32	
67	Reserved for definition	20	00100000	32	
68	Reserved for definition	20	00100000	32	
69	Reserved for definition	20	00100000	32	
6A	Reserved for definition	20	00100000	32	
6B	Reserved for definition	20	00100000	32	
6C	Reserved for definition	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E	Reserved for definition	00	00000000	0	
6F	Reserved for definition	FC	11111100	252	
70	Reserved for definition	00	00000000	0	
71	Manufacture P/N	42	01000010	66	B
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	37	00110111	55	7
74	Manufacture P/N	33	00110011	51	3
75	Manufacture P/N	48	01001000	72	H
76	Manufacture P/N	41	01000001	65	A
77	Manufacture P/N	4E	01001110	78	N
78	Manufacture P/N	41	01000001	65	A
79	Manufacture P/N	41	01000001	65	A
7A	Manufacture P/N	2E	00101110	46	.
7B	Manufacture P/N	30	00110000	48	0
7C	Reserved for definition	20	00100000	32	
7D	Reserved for definition	0A	00001010	10	
7E	Extension Flag	01	00000001	1	
7F	Checksum	D3	11010011	211	
			SUM	8448	
			SUM to HEX	2100	

Extend EDID Code

Hex Address	Field Name	Value Hex	Value (dec)	Value (bin)
80	**EDID extension block tag**	70	112	01110000
81	DisplayID Version/Revsion = 2.0	20	32	00100000
82	Section Size (byte) =	79	121	01111001
83	Display Product Primary Use Case	02	2	00000010
84	Extension count	00	0	00000000
85	**DID2.0 Data block tag[22h] =Type VII Timing – Detailed Timing Data Block**	22	34	00100010
86	Block Revision and Other Data	00	0	00000000
87	Number of Payload Bytes in Block	14	20	00010100
88	Timing 1 Pixel Clock (in kHz) Rate range is defined as 0.001 through 16,777.216MP/s.	3B	59	00111011
89		73	115	01110011
8A		05	5	00000101
8B	Timing Options	84	32	10000100
8C	Horizontal Active Image Pixels Number of pixels ranges from 1 through 65,536.	7F	127	01111111
8D		07	7	00000111
8E	Horizontal Blank Pixels Number of pixels ranges from 1 through 65,536.	B5	181	10110101
8F		00	0	00000000
90	Horizontal Offset (Front Porch) Number of pixels ranges from 1 through 32,768.	2F	47	00101111
91		80	128	10000000
92	Horizontal Sync Width Number of pixels ranges from 1 through 65,536.	1F	31	00011111
93		00	0	00000000
94	Vertical Active Image Lines Number of lines ranges from 1 through 65,536.	37	55	00110111
95		04	4	00000100
96	Vertical Blank Lines Number of lines ranges from 1 through 65,536.	63	99	01100011
97		00	0	00000000
98	Vertical Sync Offset (Front Porch) Number of lines ranges from 1 through 32,768.	09	9	00001001
99		00	0	00000000
9A	Vertical Sync Width Number of lines ranges from 1 through 65,536.	04	4	00000100
9B		00	0	00000000
9C	**DID2.0 Data block tag[25h] = Dynamic Video Timing Range Limits**	25	37	00100101
9D	Block revision = Revision 1	01	1	00000001
9E	Number of Payload Bytes in block=	09	9	00001001
9F	Minimum Pixel Clock (Low bit, Range = 0.001Mhz (000000h) ~ 16,777.216Mhz (FFFFFFh))	3B	59	00111011
A0	Minium Pixel Clock (Middle bit)	73	115	01110011
A1	Minium Pixel Clock (High bit)	05	5	00000101
A2	Maximum Pixel Clock (Low bit, Range = 0.001Mhz (000000h) ~ 16,777.216Mhz (FFFFFFh))	3B	59	00111011
A3	Maximum Pixel Clock (Middle bit)	73	115	01110011
A4	Maximum Pixel Clock (High bit)	05	5	00000101
A5	Min. Vertical Rate : ?? Hz (Range : 0Hz (00h) ~ 255Hz (FFh)	30	48	00110000
A6	Max. Vertical Rate : ?? Hz (Range : 0Hz (000h) ~ 1023Hz (3FFh))	90	144	10010000
A7	Seamless Dynamic Video Timing Support : Seamless Dynamic Video Timing change shall be supported with a fixed horizontal pixel rate and dynamic vertical blanking.	80	128	10000000
A8	**Adaptive-Sync Data Block** **2Bh.**	2B	43	00101011
A9	Block Revision and Other Data Revision 0	00	0	00000000
AA	Number of Payload Bytes in Block	0C	12	00001100
AB	Adaptive-Sync Operationand Range Information	27	39	00100111
AC	Maximum Single Frame Duration Increase Allowed for Meeting VESA Adaptive Sync Flicker Performance 00h = Flicker performance is met in any duration increase within the refresh rate range without jitter impact	00	0	00000000
AD	Minimum Refresh Rate Minimum refresh rate ranges from 0 through 255 Hz, divided by 1.001.	3C	60	00111100
AE	Maximum Refresh Rate7:0 Maximum refresh rate ranges from 1 through 1,024 Hz, plus 350 ppm	8F	143	10001111
AF	Maximum Refresh Rate9:8 Maximum refresh rate ranges from 1 through 1,024 Hz, plus 350 ppm	00	0	00000000

B0	Maximum Single Frame Duration Decrease Allowed for Meeting VESA Adaptive Sync Flicker Performance 00h = Flicker performance is met in any duration decrease within the refresh rate range without jitter impact.	00	0	00000000
B1	Adaptive-Sync Operationand Range Information	27	39	00100111
B2	Maximum Single Frame Duration Increase Allowed for Meeting VESA Adaptive Sync Flicker Performance 00h = Flicker performance is met in any duration increase within the refresh rate range without jitter impact	00	0	00000000
B3	Minimum Refresh Rate Minimum refresh rate ranges from 0 through 255 Hz, divided by 1.001.	30	48	00110000
B4	Maximum Refresh Rate7:0 Maximum refresh rate ranges from 1 through 1,024 Hz, plus 350 ppm	3B	59	00111011
B5	Maximum Refresh Rate9:8 Maximum refresh rate ranges from 1 through 1,024 Hz, plus 350 ppm	00	0	00000000
B6	Maximum Single Frame Duration Decrease Allowed for Meeting VESA Adaptive Sync Flicker Performance 00h = Flicker performance is met in any duration decrease within the refresh rate range without jitter impact.	00	0	00000000
B7	**DID2.0 Data block tag[81h] = CTA DisplayID**	81	129	10000001
B8	Block revision	00	0	00000000
B9	Number of Payload Bytes in block=	15	21	00010101
BA	CTA Block Tag Code and Block Length = Vendor Specific Data Block(03h) +Length of following data block (in bytes)	74	16	01110100
BB	IEEE OUI of AMD -- Predefined field in VSDB (0x00001A)	1A	26	00011010
BC	(Hex. LSB first)	00	0	00000000
BD	(Hex. LSB first)	00	0	00000000
BE	AMD VSDB Version = 0x03	03	3	00000011
BF	Bit 0 = FreeSync supported by panel Bit 1 = Native Color Space Set Supported Bit 2 = Reserved Bit 3 = Local Dimming Control Supported Bit 4 = Replay/PSR Switch Supported Bit 5 = SPRS Supported Bit 6 = Replay Mode Supported Bit 7 = Fast Transport Supported	01	1	00000001
C0	FreeSync Min Refresh Rate [Hz] - bits 7:0	30	48	00110000
C1	FreeSync Max Refresh Rate [Hz] - bits 7:0 (Up to 255 for source device supporting legacy v2 definition)	90	144	10010000
C2	FreeSync MCCS VCP Code Required if EDID update not possible to indicate current state of FreeSync support. 00h or MCCS code to query current state of FreeSync	00	0	00000000
C3	Bit 2 = Gamma 2.2 EOTF Supported Bit 5 = PQ EOTF Supported Bit 7:6 = Panel Type 00 = Not Specified 01 = miniLED 10 = OLED 11 = Reserved	00	0	00000000
C4	Max Luminance 1 (Peak luminance - Maximum luminance (10% white patch)) Max Luminance value = 50 x 2^(CV/32)	4B	75	01001011
C5	Min Luminance 1 (Minimum luminance with 100% full black pattern) Min Luminance = Max Luminance 1 x (CV/255)^2/ 100	59	89	01011001
C6	Max Luminance 2 (Min Backlight) (If Seamless LD Disable Control supported, Average luminance (100% full white pattern)) Max Luminance value = 50 x 2^(CV/32)	4B	75	01001011
C7	Min Luminance (Min Backlight) (If Seamless LD Disable Control supported, Minimum luminance with corner white pattern (2.5% per corner)) Min Luminance = Max Luminance 2 x (CV/255)^2/ 100	59	89	01011001
C8	LSB FreeSync Maximum refresh rate [Hz] - bits 7:0	90	144	10010000
C9	MSB FreeSync Maximum refresh rate [Hz] - bits 9:8	00	0	00000000
CA	Maximum Fast Transport Input Pixel Rate [kHz] - bits 7:0	00	0	00000000
CB	Maximum Fast Transport Input Pixel Rate [kHz] - bits 15:8	00	0	00000000
CC	Maximum Fast Transport Input Pixel Rate [kHz] - bits 23:16	00	0	00000000
CD	Bit7 = 1, additional sink info offset supported Additional sink information offset DP/eDP Port: offset from DPCD 0x403	00	0	00000000
CE	Bit7 = 1, eDP features offset B91supported eDP Display Features Handshake DPCD offset eDP Port: offset from DPCD 0x380	00	0	00000000
CF		00	0	00000000

D0		00	0	00000000
D1		00	0	00000000
D2		00	0	00000000
D3		00	0	00000000
D4		00	0	00000000
D5		00	0	00000000
D6		00	0	00000000
D7		00	0	00000000
D8		00	0	00000000
D9		00	0	00000000
DA		00	0	00000000
DB		00	0	00000000
DC		00	0	00000000
DD		00	0	00000000
DE		00	0	00000000
DF		00	0	00000000
E0		00	0	00000000
E1		00	0	00000000
E2		00	0	00000000
E3		00	0	00000000
E4		00	0	00000000
E5		00	0	00000000
E6		00	0	00000000
E7		00	0	00000000
E8		00	0	00000000
E9		00	0	00000000
EA		00	0	00000000
EB		00	0	00000000
EC		00	0	00000000
ED		00	0	00000000
EE		00	0	00000000
EF		00	0	00000000
F0		00	0	00000000
F1		00	0	00000000
F2		00	0	00000000
F3		00	0	00000000
F4		00	0	00000000
F5		00	0	00000000
F6		00	0	00000000
F7		00	0	00000000
F8		00	0	00000000
F9		00	0	00000000
FA		00	0	00000000
FB		00	0	00000000
FC		00	0	00000000
FD		00	0	00000000
FE	Section Checksum (Mandatory)	F4	244	11110100
FF	EDID Extension Block Checksum (Mandatory)	90	144	10010000

10.2 Note

Item	DPCD Ver.	eDP	LRR	DRRS (Static DRRS)	sDRRS (Seamless DRRS)	DCR	DMRRS	PSR	MBO	VESA DSC	MSO	Free-Sync	HDR	Dimming
Panel setting	1.3	1.3	N/A	Off	Off	Off	Off	PSR1	Off	Off		Yes	N/A	No HDR Global