



Product Specification

AU OPTRONICS CORPORATION

- (V) Preliminary Specifications
- () Final Specifications

Module	17.3”(17.26”) FHD 16:9 Color TFT-LCD with LED Backlight design
Model Name	B173HANAA.K
H/W	0A
Note ()	<i>LED Backlight with driving circuit design</i>

Customer	Date
Checked & Approved by	Date
<p>Note: This Specification is subject to change without notice.</p>	

Approved by	Date
<u>Eric Tseng</u>	<u>24/07/2025</u>
Prepared by	Date
<u>LiqiangBai</u>	<u>24/07/2025</u>
<p>NBBU Marketing Division AU Optronics corporation</p>	



Product Specification

AU OPTRONICS CORPORATION

Contents

1. Handling Precautions	4
2. General Description	5
2.1 General Specification	5
2.2 Optical Characteristics	6
3. Functional Block Diagram	11
4. Absolute Maximum Ratings	12
4.1 Absolute Ratings of TFT LCD Module	12
4.2 Absolute Ratings of Environment	12
5. Electrical Characteristics	13
5.1 TFT LCD Module	13
5.2 Backlight Unit	17
6. Signal Interface Characteristic	18
6.1 Pixel Format Image	18
6.2 Integration Interface Requirement	19
6.3 Interface Timing	23
6.4 Power ON/OFF Sequence	23
7. Panel Reliability Test	26
7.1 Vibration Test	26
7.2 Shock Test	26
7.3 Reliability Test	27
8. Mechanical Characteristics	28
8.1 LCM Outline Dimension	28
9. Shipping and Package	31
9.1 Shipping Label Format	31
9.2 Carton Package	31
9.3 Shipping Package of Palletizing Sequence	32
10. Appendix	33
10.1 EDID Description	33
10.2 Note	33



Product Specification

AU OPTRONICS CORPORATION

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2025/07/24	All	First Edition for Customer		

www.szguangzhuo.com
 Wechat: +86-13411884959



Product Specification

AU OPTRONICS CORPORATION

1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 10) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 11) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 12) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.



Product Specification

AU OPTRONICS CORPORATION

2. General Description

B173HANAA.K is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 FHD, 1920(H) x 1080(V) screen and 16.7M colors (RGB 8-bit) with LED backlight driving

circuit. All input signals are eDP interface compatible.

B173HANAA.K is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	17.3"(17.26)			
Active Area	[mm]	381.838 x 214.812			
Pixels H x V		1920 x 3 (RGB) x 1080			
Pixel Pitch	[mm]	0.1989 x 0.1989			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black			
White Luminance (ILED=24mA) (Note: ILED is LED current)	[cd/m ²]	300 typ. (5 points average) 255 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		1200:1 typ/ 1000 : 1 (min)			
Response Time	[ms]	25 typ.			
Nominal Input Voltage /VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	4.25W max (max: includ Logic@mosaic & BL power)			
Weight	[Grams]	480g max			
Physical Size	[mm]		Min.	Typ.	Max.
		Length	389.59	389.89	390.19
		Width	226.71	227.01	227.31
		Thickness (panel side)		3.3	3.5
		Thickness (PCBA side)	-	3.3	3.5
Electrical Interface		2 Lane eDP 1.2			
Glass Thickness	[mm]	0.4			
Surface Treatment		Anti-Glare, Hardness 3H			
Support Color		16.7M colors (RGB 8-bit)			



Product Specification

AU OPTRONICS CORPORATION

Temperature Range Operating	[°C]	0 to +50
Storage (Non-Operating)	[°C]	-20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25°C(Room Temperature) :

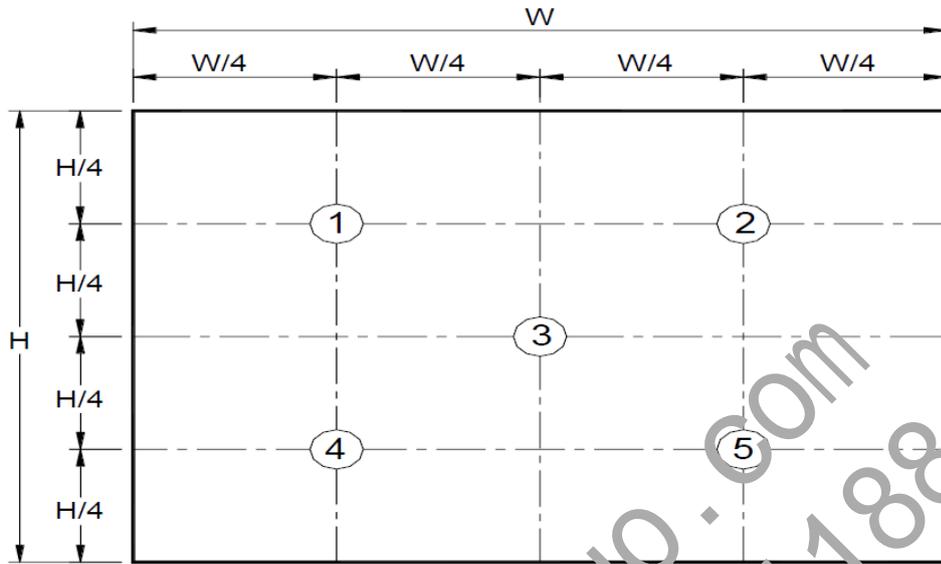
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Notes
White Luminance $I_{LED} = 17.3mA$ (Base Panel Only)		5 points average	255	300	-	cd/m ²	1, 4, 5
Viewing Angle	θ_R θ_L	Horizontal (Right) CR = 10 (Left)	80	89	-	degree	4, 9
	ψ_H ψ_L	Vertical (Upper) CR = 10 (Lower)	80	89	-		
Luminance Uniformity	δ_P	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity	δ_{13P}	13 Points	-	-	1.6		2, 3, 4
Contrast Ratio	CR		1000	1200	-		4, 6
Cross talk	%		-	-	4		4, 7
Response Time	T_{RT}	Rising + Falling	-	25	35	msec	4, 8
Color / Chromaticity Coordinates	White	W_x	0.270	0.300	0.330	CIE 1931	4
		W_y	0.291	0.321	0.351		
	Red	R_x	0.545	0.575	0.605		
		R_y	0.317	0.347	0.377		
	Green	G_x	0.322	0.352	0.382		
		G_y	0.542	0.572	0.602		
	Blue	B_x	0.126	0.161	0.186		
		B_y	0.098	0.128	0.158		
sRGB	%		NTSC 45%	-			
Gamma Value			2.2				



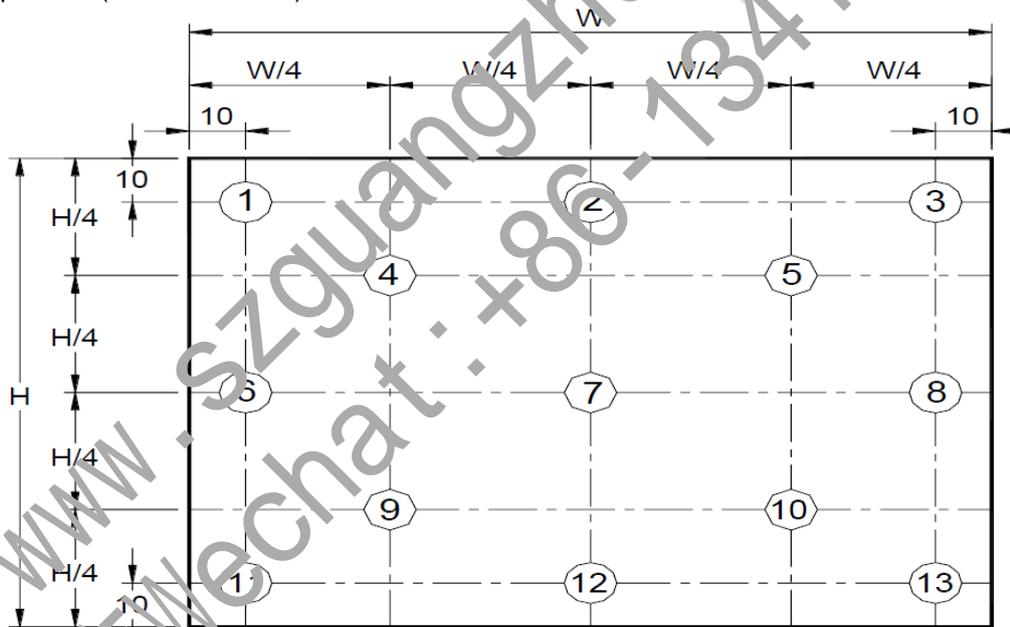
Product Specification

AU OPTRONICS CORPORATION

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{w5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{w13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

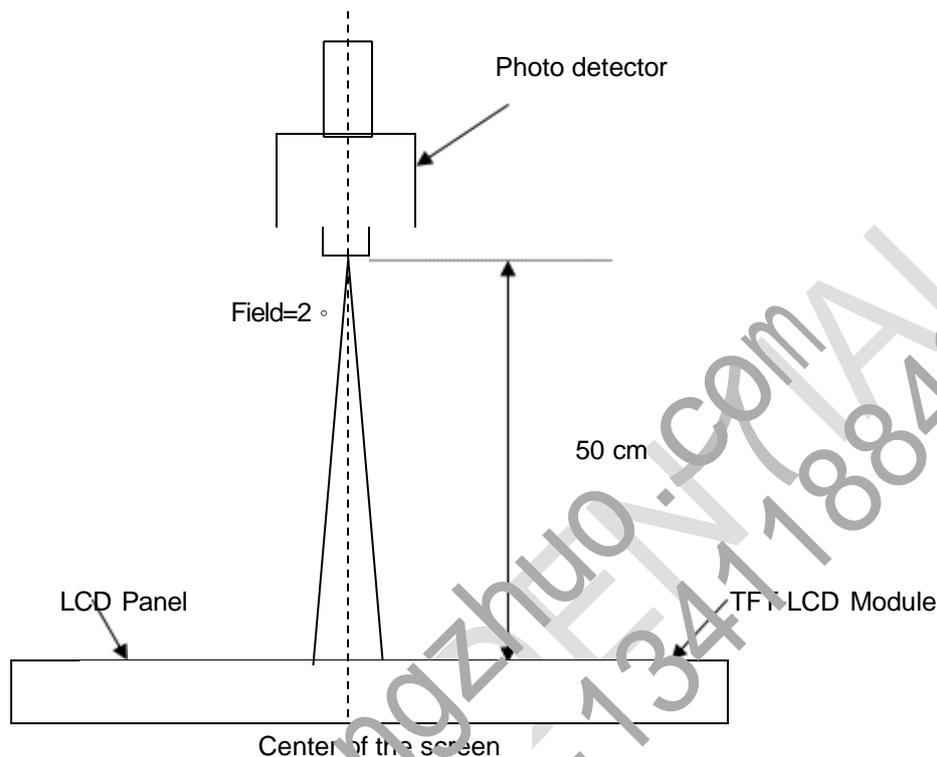
The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of



Product Specification

AU OPTRONICS CORPORATION

screen.



Note 5: Definition of Average Luminance of White (YL):

Measure the luminance of gray level 3 at 5 points, $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

L(x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6: Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

Note 7: Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

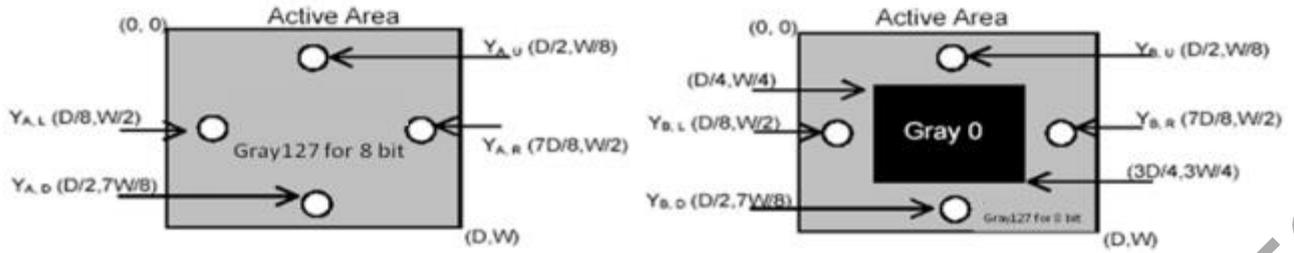
Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



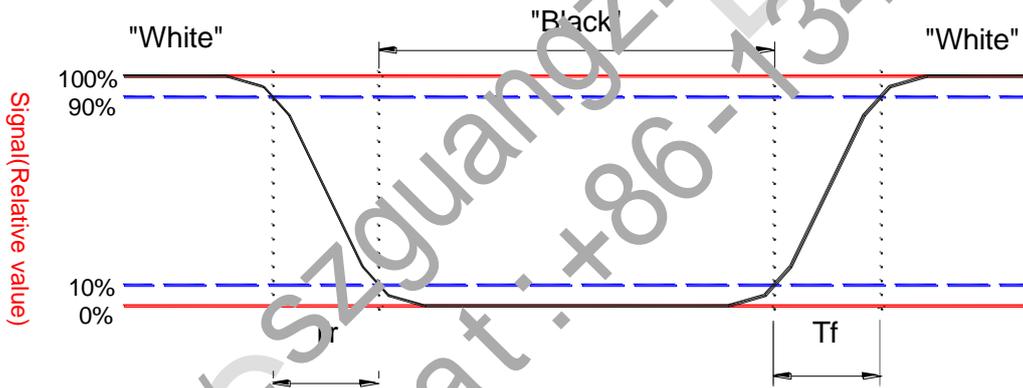
Product Specification

AU OPTRONICS CORPORATION



Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



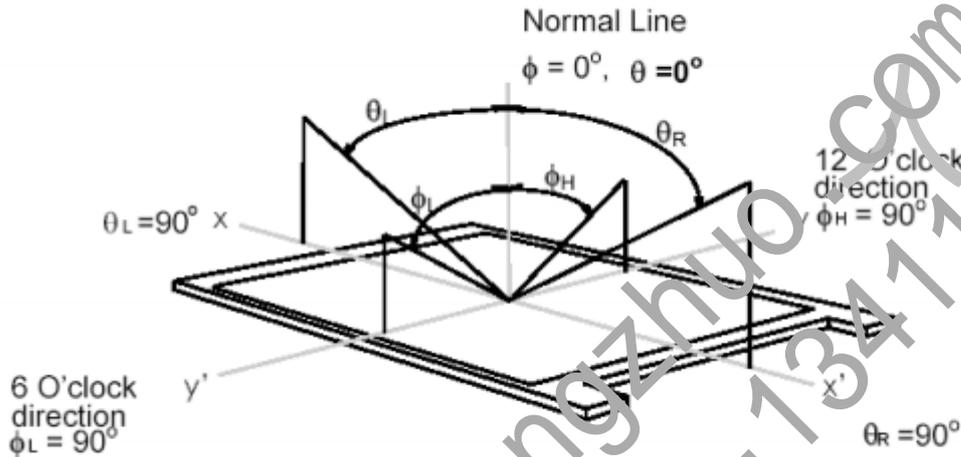


Product Specification

AU OPTRONICS CORPORATION

Note 9: Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



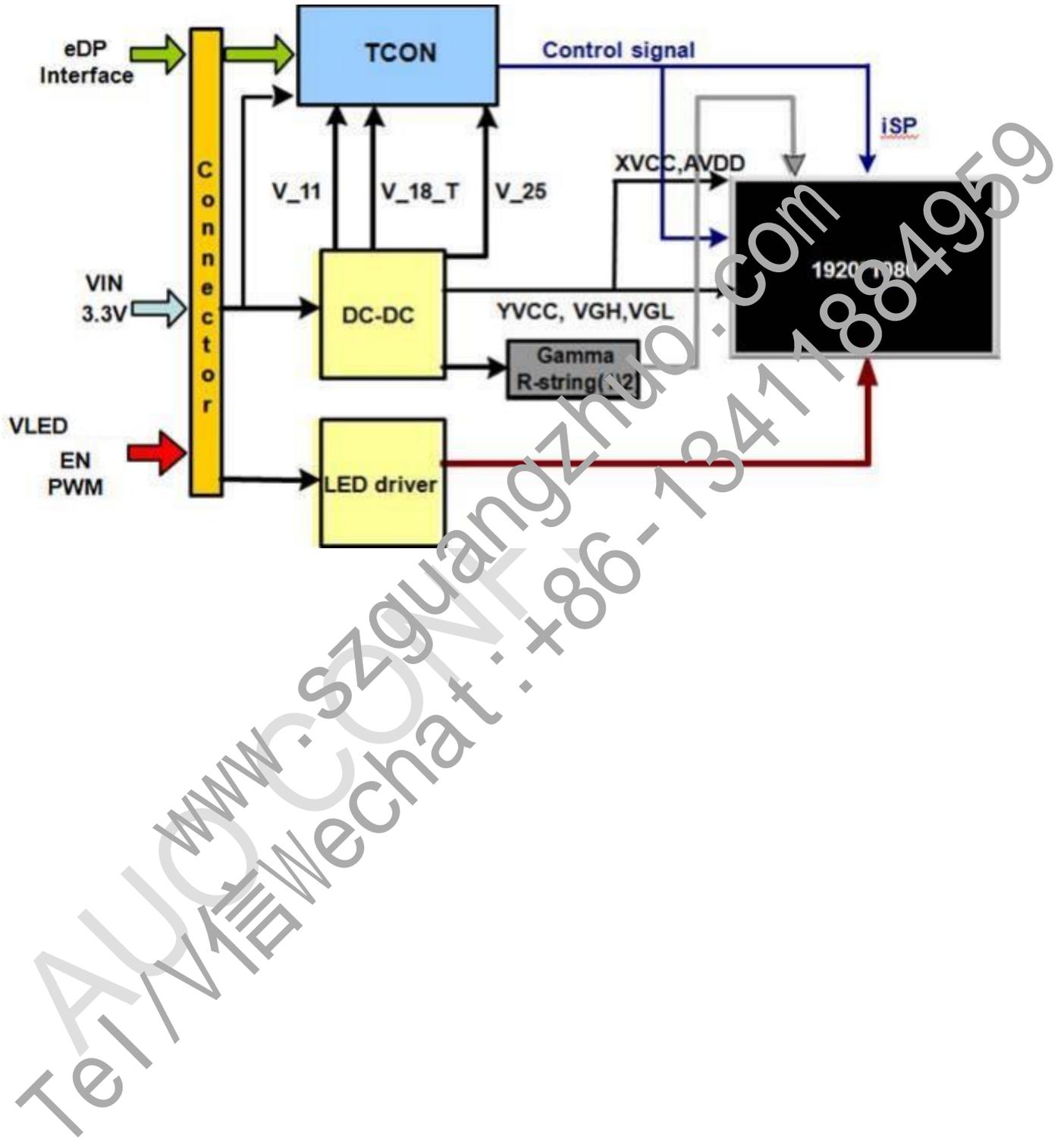


Product Specification

AU OPTRONICS CORPORATION

3. Functional Block Diagram

The following diagram shows the functional block of the 17.3 inches wide Color TFT/LCD 30 Pin





Product Specification

AU OPTRONICS CORPORATION

4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 1
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	10	90	[%RH]	Note 4

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

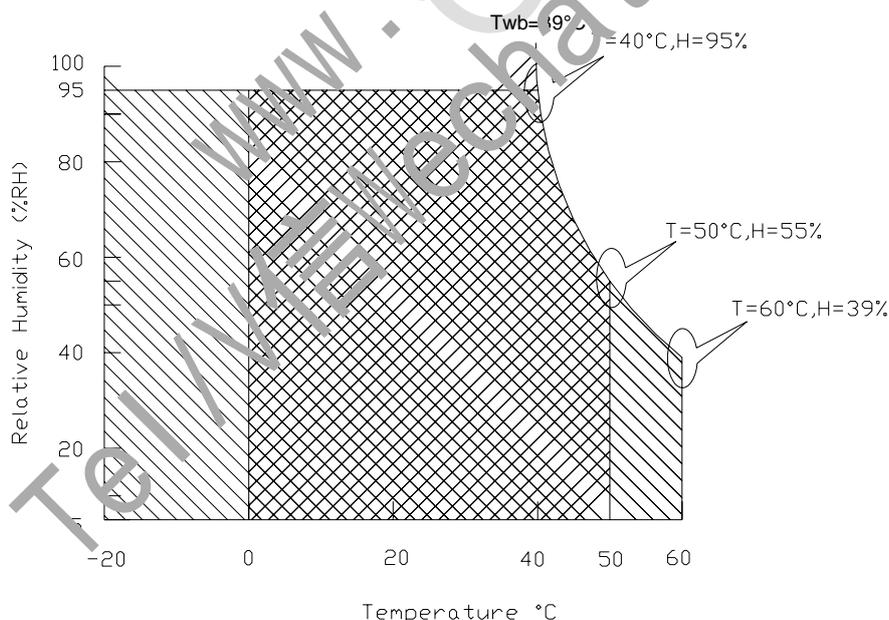
Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO II's Incoming Inspection Standard).

Note 5: The packing material of system forbid to involve ammonium component

Note 6: The reliability test conditions do not exceed the verified conditions of TFT module that refer to section 7.3

Note 7: Be sure the panel test condition do not exceed the component limitation of TFT module(TN Liquid crystal , for example)





Product Specification

AU OPTRONICS CORPORATION

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

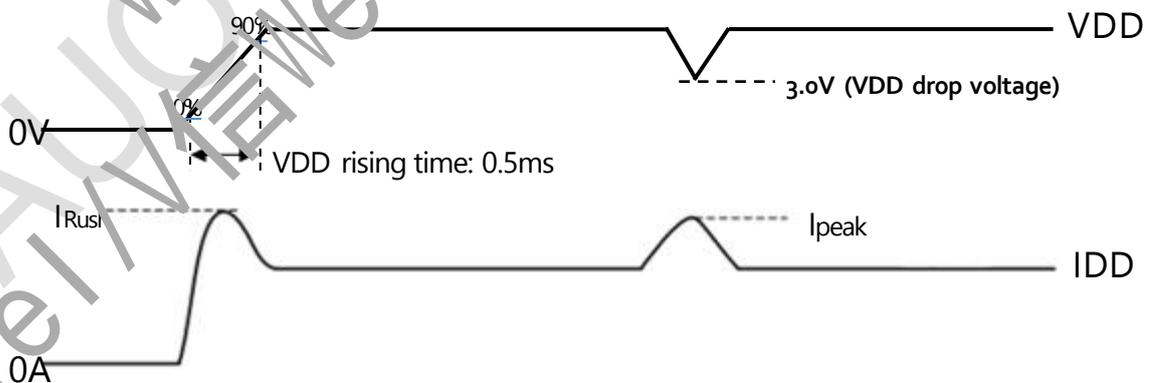
The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	1.0	1.4	[Watt]	Note 1
PDD(worst pattern)	VDD Power	-	-	3.0	[Watt]	Note 1
IDD	IDD Current(RMS)	-	-	470	[mA]	Note 1
IDD(worst pattern)	IDD Current(RMS)	-	-	1000	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
Ipeak	Peak Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Driver Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : PDD(typ)@ mosaic pattern Maximum Power; PDD(Max)@ R/G/B pattern Maximum Power

$$IDD(Max)=PDD(Max) / VDD(Min)$$

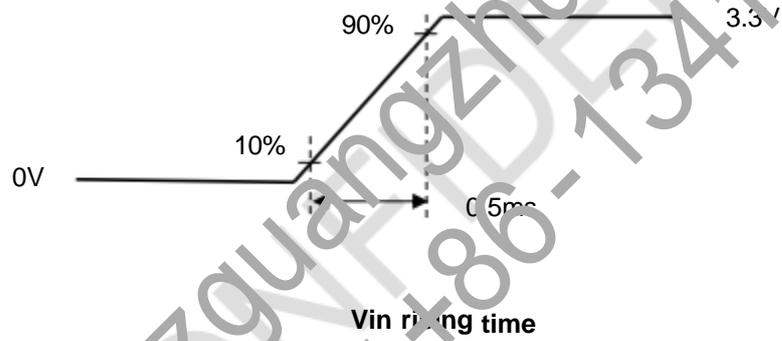
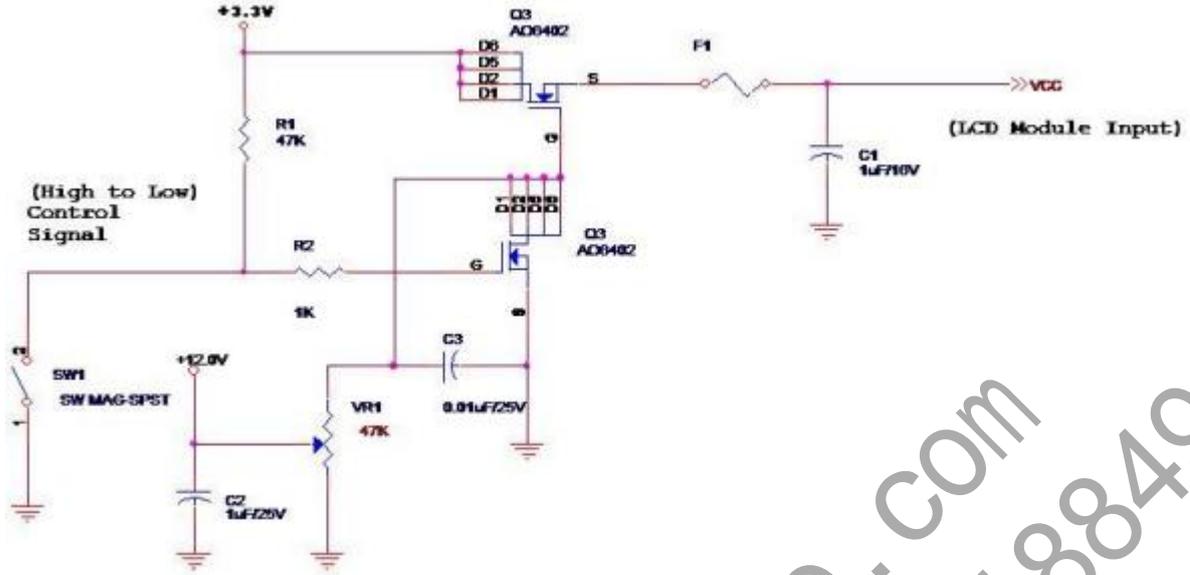
Worst pattern: H-stripe pattern





Product Specification

AU OPTRONICS CORPORATION





Product Specification

AU OPTRONICS CORPORATION

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

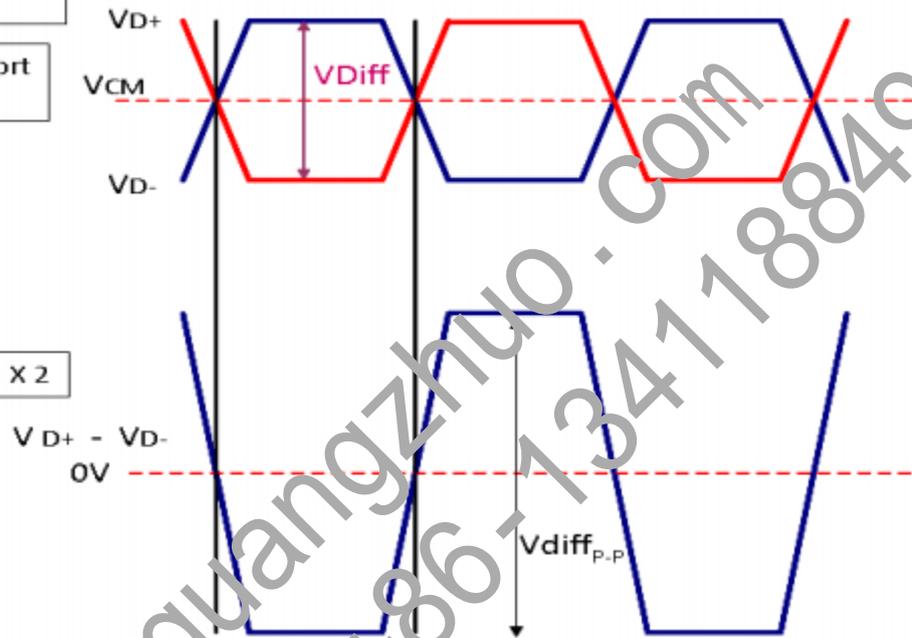
Signal electrical characteristics are as follows;

Display Port main link signal:

Differential pair VD+ , VD-
Which is one Display port
Main link

VCM of Display port
Main link

$$V_{diffP-P} = [(VD+) - (VD-)] \times 2$$



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
VDiffP-P	Peak-to-peak Voltage at a receiving Device	150		1320	mV

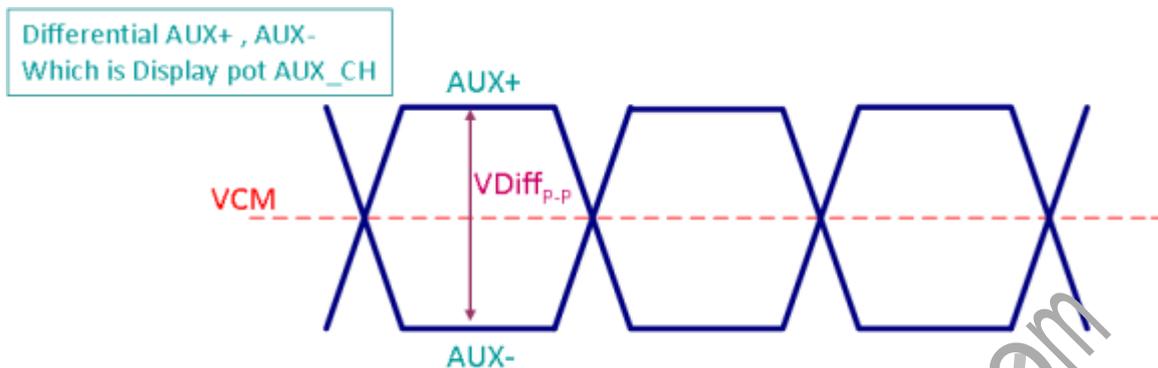
Follow as VESA eDP1.3 Standard



Product Specification

AU OPTRONICS CORPORATION

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff _{P-P}	AUX Peak-to-peak Voltage at TX package pins (TP1)	0.18	0.2	1.38	V
VDiff _{P-P}	AUX Peak-to-peak Voltage at TP3	0.14		1.36	V

Follow as VESA Embedded DisplayPort (eDP) Standard V1.4a

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25	--	3.6	V

Follow as VESA display port standard V1.3



Product Specification

AU OPTRONICS CORPORATION

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	5.2	[Watt]	(Ta=25°C), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25°C), Note 2 If=23.1 mA
Inrush Current	VLED	-	-	2000	mA	VLED = 6V/White pattern, Note 4

Note 1: Calculator value for reference $P_{LED} = VF$ (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

Note 4: VLED measured rising timing to BL enable load current (T13+T14+T15) / VLED input 6V / test pattern : White pattern / PWM 100%

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED (Note 1)	6.0 Note 2	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25°C) *Note 3
LED Enable Input High Level	VLED_EN	3.0	--	3.3	[Volt]	
LED Enable Input Low Level		--	--	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	3.0	--	3.3	[Volt]	
PWM Logic Input Low Level		--	--	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5 *Note 2	--	100	%	



Product Specification

AU OPTRONICS CORPORATION

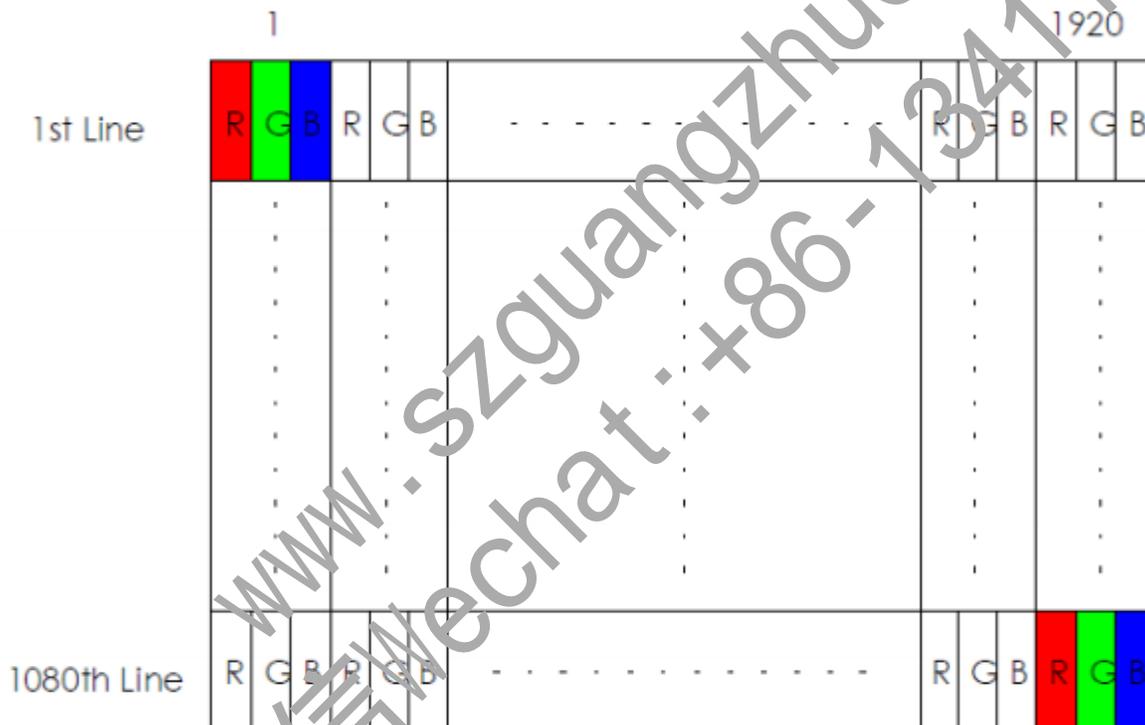
Note 2: If the PWM duty ratio(min) is set between 5% to 1%, the PWM input frequency should be set below 1KHz . The brightness-duty characteristic might not be able to keep in it's linearity if the dimming control is operated in 1% to 5% range.

Note 3: BL Control Mode is DC diming mode.

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.





Product Specification

AU OPTRONICS CORPORATION

6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX
Type / Part Number	eDP / 20765-030E-11A
Mating Housing/Part Number	I-PEX / 20453-030T-01

6.2.2 Pin Assignment

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

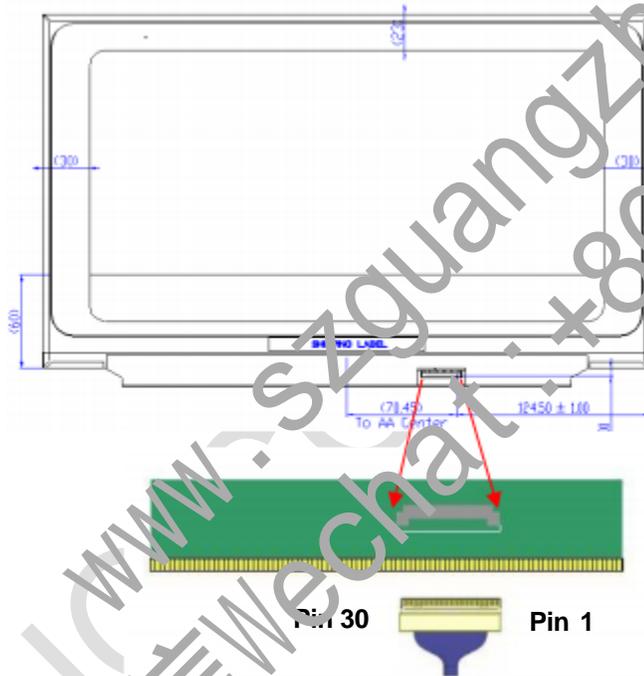
PIN NO	Symbol	Function
1	NC	NC
2	H_GND	High Speed Ground
3	Lane1_N	Complement Signal Link Lane 1
4	Lane1_P	True Signal Link Lane 1
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	LCD_Self_Test	LCD Panel Self Test Enable
15	LCD_GND	LCD logic and driver ground
16	LCD_GND	LCD logic and driver ground
17	HPD	HPD signale pin
18	BL_GND	Backlight_ground
19	BL_GND	Backlight_ground
20	BL_GND	Backlight_ground



Product Specification

AU OPTRONICS CORPORATION

21	BL_GND	Backlight_ground
22	BL_Enable	Backlight On / Off
23	BL PWM DIM	System PWM signal Input
24	NC	NC
25	NC	NC
26	BL_PWR	Backlight power (6V~21V)
27	BL_PWR	Backlight power (6V~21V)
28	BL_PWR	Backlight power (6V~21V)
29	BL_PWR	Backlight power (6V~21V)
30	NC	NC



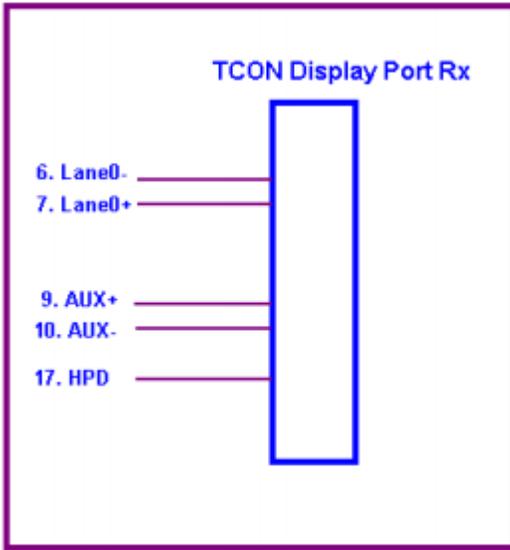
Note1: Start from right side.

Note2: Input signals shall be low or High-impedance state when VDD is off.
Internal circuit of **eDP inputs** are as following.



Product Specification

AU OPTRONICS CORPORATION



www.szguangzhuo.com
Tel/Wechat: +86-13411884959



Product Specification

AU OPTRONICS CORPORATION

Note3. Pin I/O resistor & voltage remark

Update after DVT1

Pin No	Resistor(ohm)		Voltage(V)		Schematic remark (Y/N) _ H/L EN
	R1	R2 to GND Or R2 to Power	Min	Max	
14_BIST					
17_HPDP					
22_BL EN					
23_BL PWM					

Update after DVT1

circuit	Pin14 LCD Self Test (Aging/BIST)	Pin 7 HPDP	Pin22 BL_EN	Pin23 BL PWM
Schematic				



Product Specification

AU OPTRONICS CORPORATION

6.3 Interface Timing

6.3.1 Timing Characteristics

Basically, interface timings should match the 1920x1080 / 60Hz manufacturing guide line timing.

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Frame Rate	-	48	-	60	Hz	
Clock frequency	$1/ T_{\text{Clock}}$	94	-	141	MHz	
Vertical Section	Period	T_V	1118	-	1118	T_{Line}
	Active	T_{VD}	1080			
	Blanking	T_{VB}	38	-	38	
Horizontal Section	Period	T_H	2100	-	2100	T_{Clock}
	Active	T_{HD}	1920			
	Blanking	T_{HB}	180	-	180	

Note 1 : The above is as optimized setting

Note 2 : The maximum clock frequency = $(1920+B)*(1080+A)*50 < 141$ MHz

6.4 Power ON/OFF Sequence

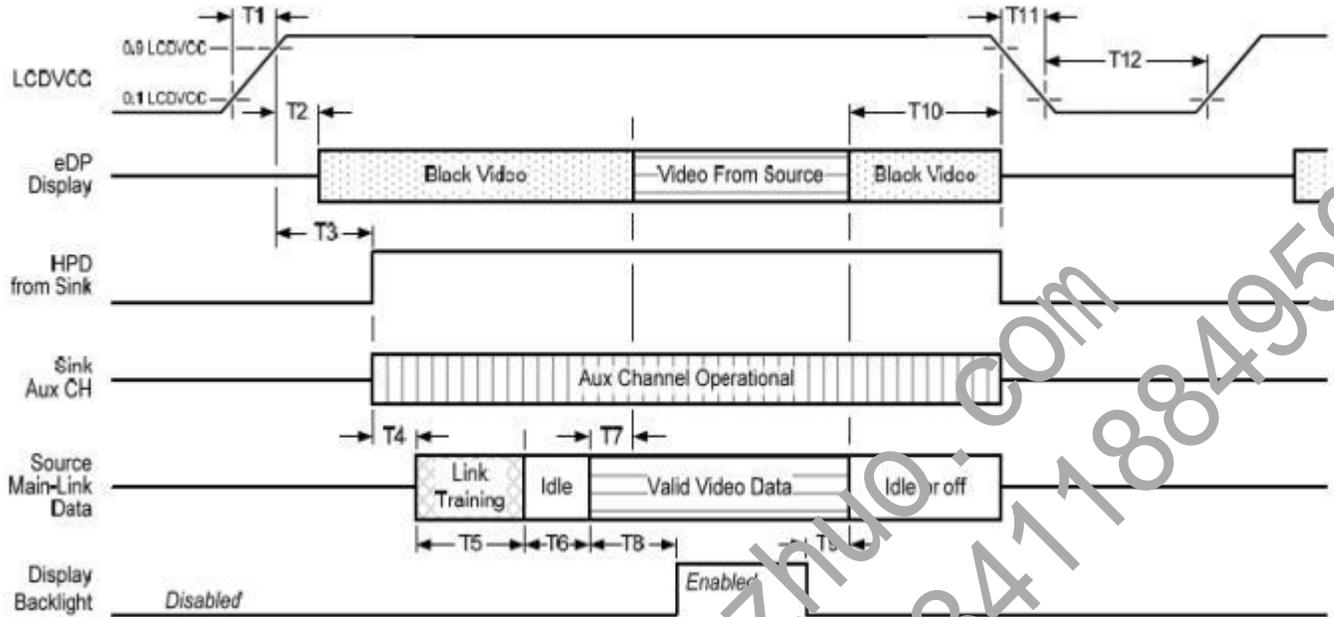
Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Product Specification

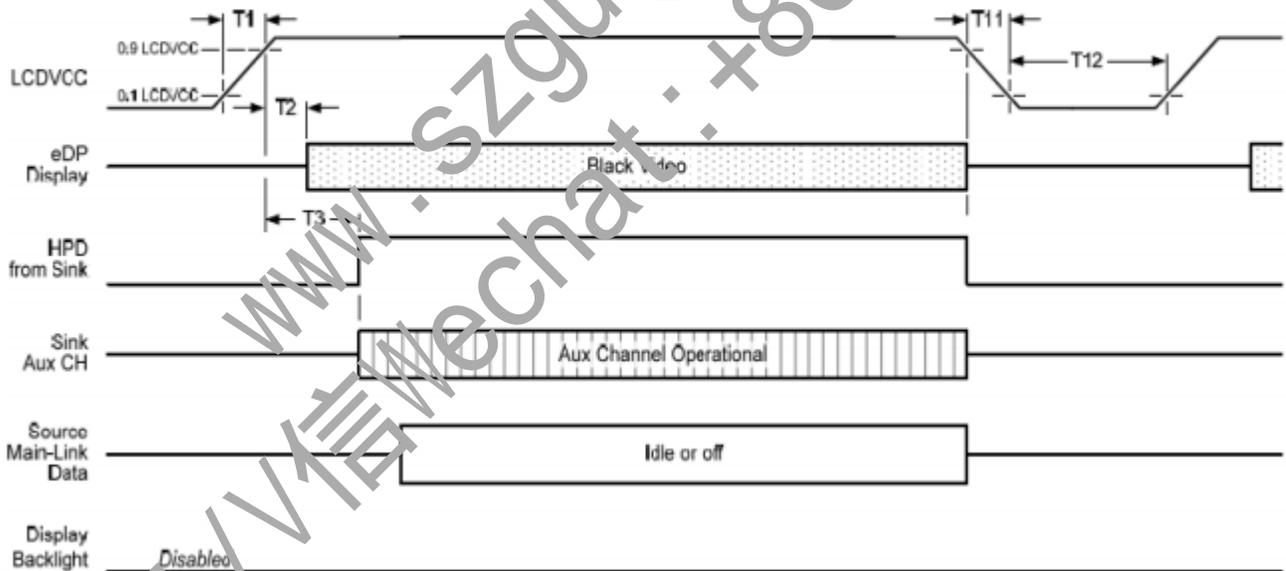
AU OPTRONICS CORPORATION

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only



Product Specification

AU OPTRONICS CORPORATION

Display Port Panel Power Sequence Timing Parameters

Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read sink capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	50ms		500ms	
T11	power rail fall time, 90% to 10%	source			10ms	
T12	power off time	source	500ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:

- upon LCDVDD power on (with in T2 max) when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T3).

- when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

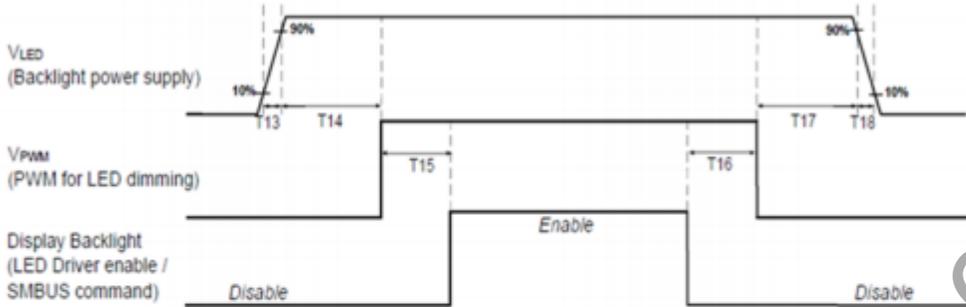
Note 3: The sink must support AUX_CH polling by the source immediately following LCD VDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.



Product Specification

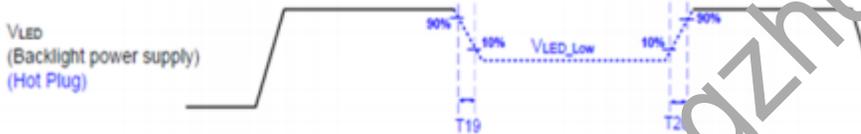
AU OPTRONICS CORPORATION

Display Port panel B/L power sequence timing parameter:



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



Seamless change: $T19/T20 = 5 \times T_{PWM}^*$
 $*T_{PWM} = 1/PWM \text{ Frequency}$

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500 Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side



Product Specification

AU OPTRONICS CORPORATION

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C, 90%RH, 240h	
High Temperature Operation	Ta= 50°C, Dry, 240h	
Low Temperature Operation	Ta= 0°C, 240h	
High Temperature Storage	Ta= 60°C, 240h	
Low Temperature Storage	Ta= -20°C, 240h	
Thermal Shock Test	Ta=-20°C to 60°C, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV Class B	Note 1

Note1: According to EN 61000-4-2 , ESD class B. Some performance degradation allowed. No data lost

. Self-recoverable. No hardware failures.

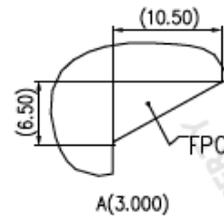
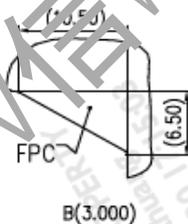
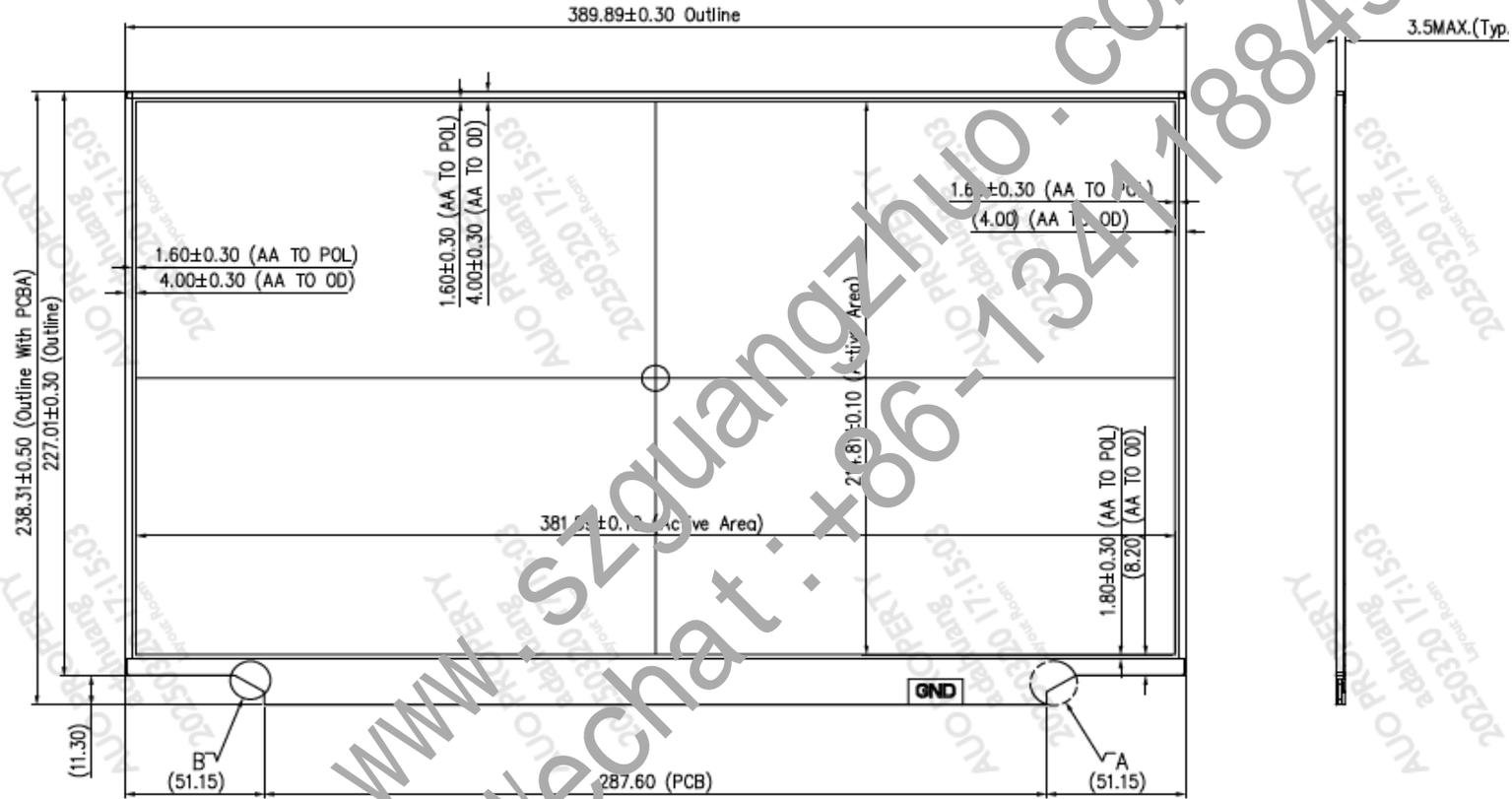
Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

Product Specification

AU OPTRONICS CORPORATION

8. Mechanical Characteristics

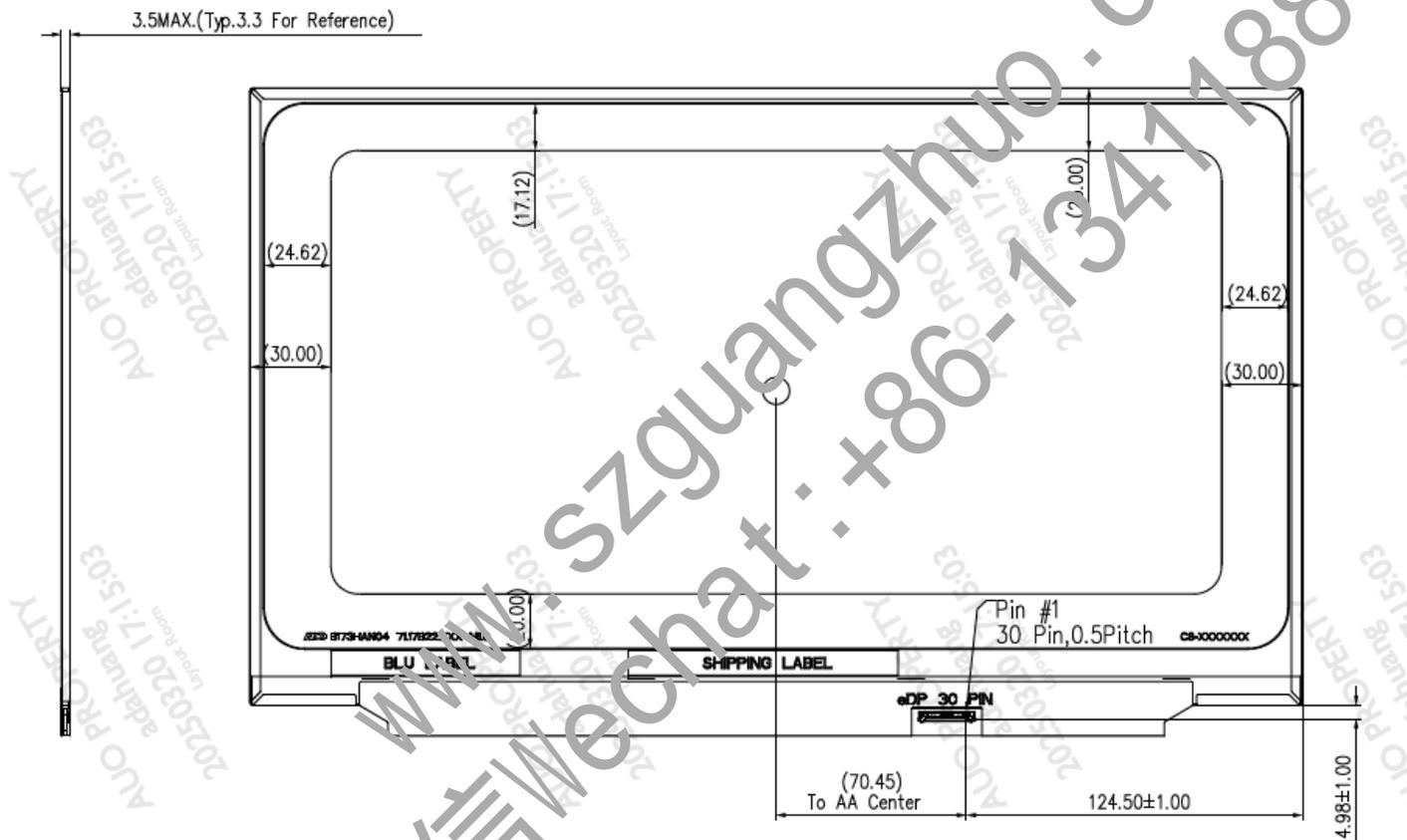
8.1 LCM Outline Dimension





Product Specification

AU OPTRONICS CORPORATION

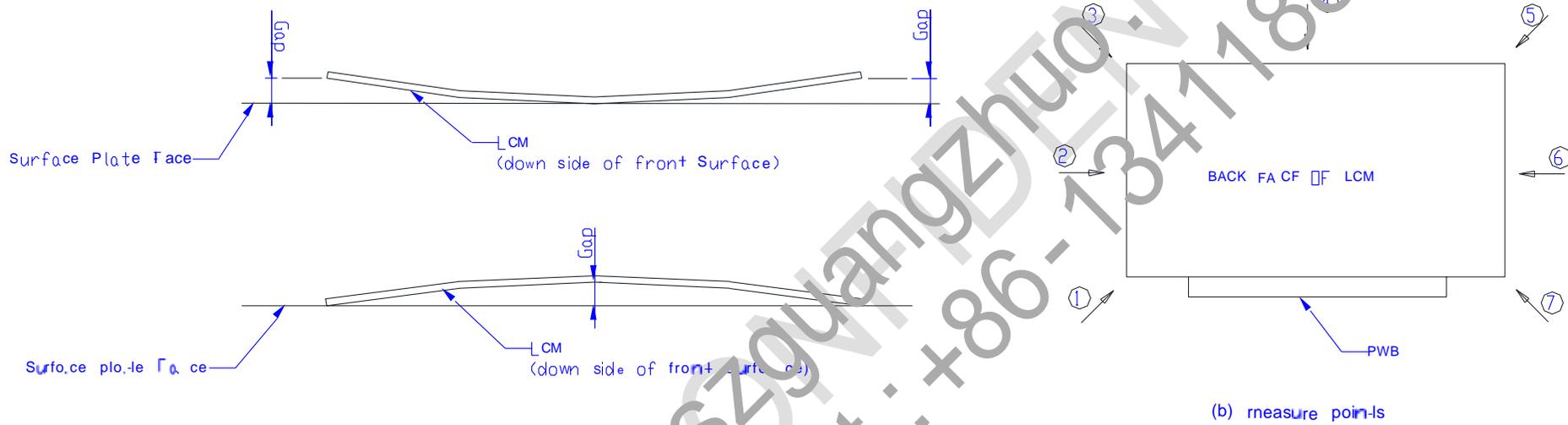


Note: Prevention IC damage, IC positions not allowed any overlap over these are

Note: Warpage Measurement Method

Put LCM on surface plate (display front surface downside) and measure the gap between module and surface plate by clearance gauge.

7 measure points are set as bellow (b)





Product Specification

AU OPTRONICS CORPORATION

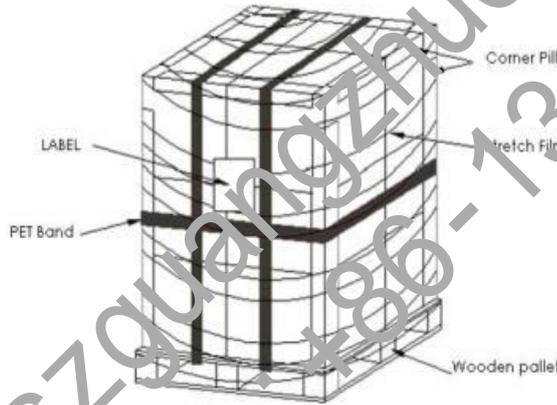
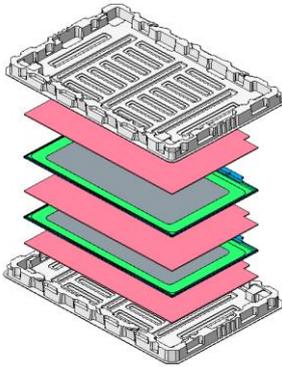
9. Shipping and Package

9.1 Shipping Label Format

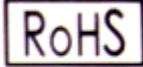
	Manufactured MM/WW Model No: B173HANAA.K AUO Corporation		c  15 
XXXXXXXXXXXX-XXXXXX	H/W: OA F/W: 1	MADE IN CHINA (S06)	B173HANAA.K

9.2 Carton Package

3PCS Spacer + 2PCS Panel / Tray
28PCS/箱



Carton Label Format

AUC Corporation	QTY :		
MODEL NO : B173HANAA.K			
PART NO : 97.17B33.K01			
CUSTOMER NO			
CARTON NO :			
Made In China	*XXXXXXXXXXXX-XXXXXX*		



Product Specification

AU OPTRONICS CORPORATION

10. Appendix

10.1 EDID Description

Update after DVT1

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01	Header	FF	11111111	255	
02	Header	FF	11111111	255	
03	Header	FF	11111111	255	
04	Header	FF	11111111	255	
05	Header	FF	11111111	255	
06	Header	FF	11111111	255	
07	Header	00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	BC	10111100	188	
0B	Product Code	67	01100111	103	
0C	32-bit ser #	00	00000000	0	
0D	ID S/N - option	00	00000000	0	
0E	ID S/N - option	00	00000000	0	
0F	ID S/N - option	00	00000000	0	
10	Week of manufacture	21	00100001	33	
11	Year of manufacture	23	00100011	35	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	04	00000100	4	
14	Video input def. (digital I/P, nor TMDS, CRGB)	A5	10100101	165	
15	Max H image size (rounded to cm)	36	00100110	38	
16	Max V image size (rounded to cm)	15	00010101	21	
17	Display Gamma (γ gamma*100, 100)	78	01111000	120	
18	Feature support (no DPMS, Active OFF, RGB, tmg Blk#1)	03	00000011	3	
19	Red/green low bits (Lower 2:2:2 bits)	72	01110010	114	
1A	Blue/white low bits (Lower 2:2:2 bits)	7D	01111101	125	
1B	Red x (Upper 8 bits)	93	10010011	147	
1C	Red y, high LR 8 bits	58	01011000	88	
1D	Green x	5A	01011010	90	
1E	Green y	92	10010010	146	
1F	Blue x	29	00101001	41	
20	Blue y	20	00100000	32	
21	White x	4C	01001100	76	
22	White y	52	01010010	82	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27	Standard timing #1	01	00000001	1	
28	Standard timing #2	01	00000001	1	
29	Standard timing #2	01	00000001	1	

2A	Standard timing #3	01	00000001	1
2B	Standard timing #3	01	00000001	1
2C	Standard timing #4	01	00000001	1
2D	Standard timing #4	01	00000001	1
2E	Standard timing #5	01	00000001	1
2F	Standard timing #5	01	00000001	1
30	Standard timing #6	01	00000001	1
31	Standard timing #6	01	00000001	1
32	Standard timing #7	01	00000001	1
33	Standard timing #7	01	00000001	1
34	Standard timing #8	01	00000001	1
35	Standard timing #8	01	00000001	1
36	Pixel Clock/10000 LSB	20	00100000	32
37	Pixel Clock/10000 USB	37	00110111	55
38	Horz active Lower 8bits	80	10000000	128
39	Horz blanking Lower 8bits	B4	10110100	180
3A	HorzAct:HorzBlnk Upper 4:4 bits	70	01110000	112
3B	Vertical Active Lower 8bits	38	00111000	56
3C	Vertical Blanking Lower 8bits	28	00101000	40
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	40	01000000	64
3E	HorzSync. Offset	6C	01101100	108
3F	HorzSync.Width	30	00110000	48
40	VertSync.Offset : VertSync.Width	AA	10010100	170
41	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0
42	Horizontal Image Size Lower 8bits	7D	01111101	125
43	Vertical Image Size Lower 8bits	76	11010110	214
44	Horizontal & Vertical Image Size (upper 4:4 bits)	70	00000000	16
45	Horizontal Border (zero for internal LCD)	00	00000000	0
46	Vertical Border (zero for internal LCD)	00	00000000	0
47	Signal (non-intr, norm, no stereo, sep sync, neg pol)	18	00011000	24
48	Pixel Clock/10000 LSB	00	00000000	0
49	Pixel Clock/10000 USB	00	00000000	0
4A	Horz active Lower 8bits	00	00000000	0
4B	Horz Blanking Lower 8bits	0F	00001111	15
4C	HorzAct:HorzBlnk Upper 4:4 bits	00	00000000	0
4D	Vertical Active Lower 8bits	00	00000000	0
4E	Vertical Blanking Lower 8bits	00	00000000	0
4F	Vert Act : Vertical Blanking (upper 4:4 bit)	00	00000000	0
50	HorzSync. Offset	00	00000000	0
51	HorzSync.Width	00	00000000	0
52	VertSync.Offset : VertSync.Width	00	00000000	0
53	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0
54	Horizontal Image Size Lower 8bits	00	00000000	0
55	Vertical Image Size Lower 8bits	00	00000000	0
56	Horizontal & Vertical Image Size (upper 4:4 bits)	00	00000000	0
57	Horizontal Border (zero for internal LCD)	00	00000000	0
58	Vertical Border (zero for internal LCD)	00	00000000	0
59	Signal (non-intr, norm, no stereo, sep sync, neg pol)	20	00100000	32
5A	descriptor #3	00	00000000	0
5B	Reserved for definition	00	00000000	0

5C	Reserved for definition	00	00000000	0	
5D	ASCII String	FD	11111101	253	
5E	Reserved for definition	00	00000000	0	
5F	Manufacture	28	00101000	40	(
60	Manufacture	3C	00111100	60	<
61	Manufacture	44	01000100	68	D
62	Reserved for definition	44	01000100	68	D
63	Reserved for definition	0E	00001110	14	
64	Reserved for definition	01	00000001	1	
65	Reserved for definition	0A	00001010	10	
66	Reserved for definition	20	00100000	32	
67	Reserved for definition	20	00100000	32	
68	Reserved for definition	20	00100000	32	
69	Reserved for definition	20	00100000	32	
6A	Reserved for definition	20	00100000	32	
6B	Reserved for definition	20	00100000	32	
6C	Reserved for definition	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E	Reserved for definition	00	00000000	0	
6F	Reserved for definition	FC	11111100	252	
70	Reserved for definition	00	00000000	0	
71	Manufacture P/N	42	01000100	66	B
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	37	00110111	55	7
74	Manufacture P/N	33	00110011	51	3
75	Manufacture P/N	43	01001000	72	H
76	Manufacture P/N	41	01000001	65	A
77	Manufacture P/N	4E	01001110	78	N
78	Manufacture P/N	41	01000001	65	A
79	Manufacture P/N	41	01000001	65	A
7A	Manufacture P/N	2E	00101110	46	.
7B	Manufacture P/N	4B	01001011	75	K
7C	Reserved for definition	20	00100000	32	
7D	Reserved for definition	0A	00001010	10	
7E	Extension flag	01	00000001	1	
7F	Checksum	AA	10101010	170	
			SUM	6656	
			SUM to HEX	1A00	

10.2 Note

DPCD Ver.	sDRRS	DCR	DMRRS	PSR	MBO	VESA DSC	MSO	Free-Sync	HDR	Dimming
1.2	On	Off	On	Off	Off	Off	Off	Off	NA	No HDR Global