Product Specification

AU OPTRONICS CORPORATION

( ) Preliminary Specifications
(V) Final Specifications

Module	**17.3”(17.26”) FHD 16:9 Color TFT-LCD with LED Backlight design**
Model Name	**B173HAN05.4**
HW	**1B**
Note ( )	***LED Backlight with driving circuit design***

Customer	**Date**	**Approved by**	**Date**
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Checked & Approved by	**Date**	**Prepared by**	**Date**
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Note: This Specification is subject to change without notice.		**NBBU Marketing Division AU Optronics corporation**	

Contents

Product Specification

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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2020/09/08	All	First Edition for Customer		
0.2 2020/11/12	P6 P27-P37		Add Chromaticity Coodinates、LCM OD、Shipping Label Format、EDID、Notes	
1.0 2021/01/08	All	Final Edition for Customer		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
10) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
11) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
12) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B173HAN05.4 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 FHD, 1920(H) x 1080(V) screen and 16.7M colors (RGB 8-bits data driver) with LED backlight driving circuit. All input signals are eDP interface compatible.

B173HAN05.4 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	17.3”(17.26)			
Active Area	[mm]	381.888 x 214.812			
Pixels H x V		1920 x 3 (RGB) x 1080			
Pixel Pitch	[mm]	0.1989 x 0.1989			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black			
White Luminance (I_{LED}=12.4mA) (Note: I_{LED} is LED current)	[cd/m²]	300 typ. (5 points average) 255 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		1000:1 typ			
Response Time	[ms]	Tr+Tf 8 typ. OD GTG 3 typ.			
Nominal Input Voltage VDD	[Volt]	+3.3V min			
Power Consumption	[Watt]	5.6W max. (include Logic@mosaic and BLU power)			
Weight	[Grams]	510g max			
Physical Size	[mm]		Min.	Typ.	Max.
		Length	389.59	389.89	390.19
		Width	226.71	227.01	227.31
		Thickness	-	-	3.5
Electrical Interface		4 Lane eDP1.4			
Glass Thickness	[mm]	0.4			
Surface Treatment		Anti-Glare, Hardness 3H			
Support Color		16.7M colors (RGB 8-bit)			

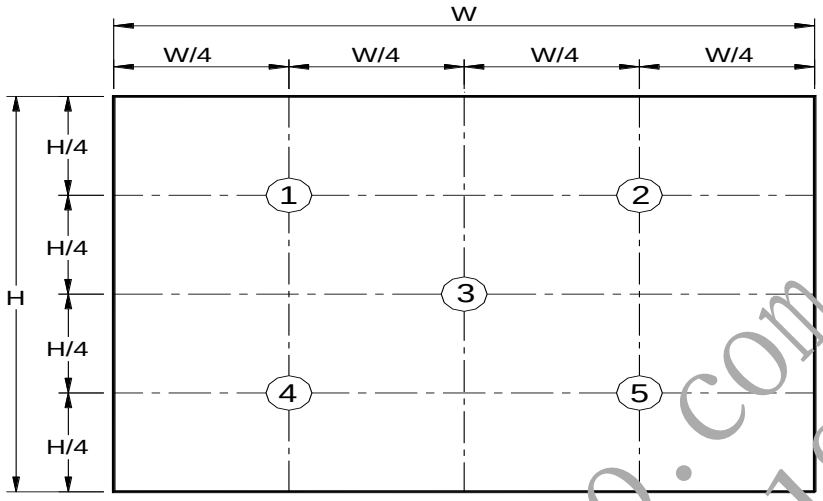
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

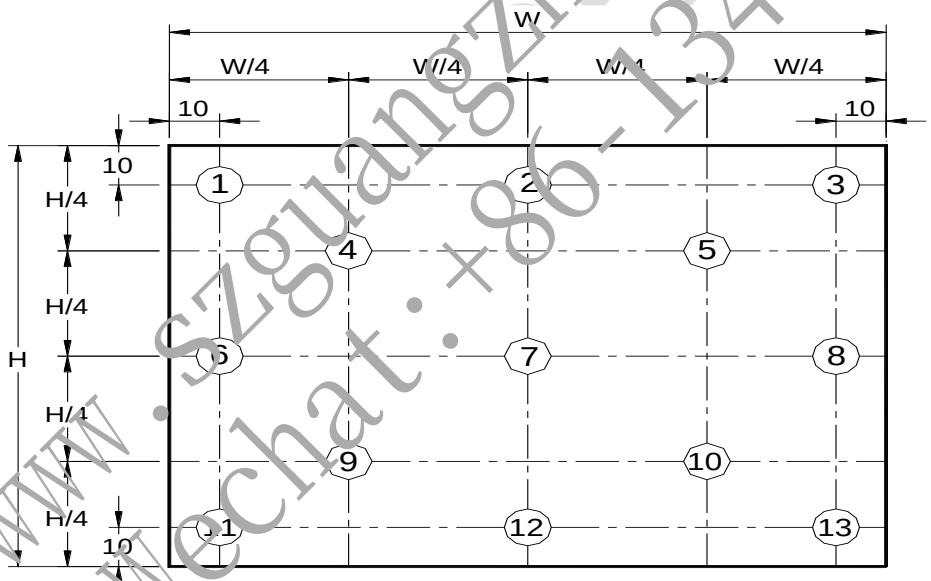
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED} = 12.4mA			5 points average	255	300	-	cd/m²	1, 4, 5
Viewing Angle		θ_R θ_L	Horizontal (Right) CR = 10 (Left)	80 80	85 85	-	degree	4, 9
		ψ_H ψ_L	Vertical (Upper) CR = 10 (Lower)	80 80	85 85	-		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.6		2, 3, 4
Contrast Ratio		CR			1000	-		4, 6
Cross talk		%		-	-	4		4, 7
Response Time		T_{RT}	Rising + Falling	-	8	-	msec	4, 8
Response Time		$T_{G\ To\ G}$		-	5	-	msec	8
Response Time		$T_{OD\ G\ To\ G}$		-	3	-	msec	8
Color / Chromaticity Coodinates	White	Wx	CIE 1931	0.283	0.313	0.343		4
		Wy		0.299	0.329	0.359		
	Red	Rx		0.620	0.650	0.680		
		Ry		0.296	0.326	0.356		
	Green	Gx		0.259	0.289	0.319		
		Gy		0.582	0.612	0.642		
	Blue	Bx		0.122	0.152	0.182		
		By		0.035	0.065	0.095		
sRGB		%		-	100	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

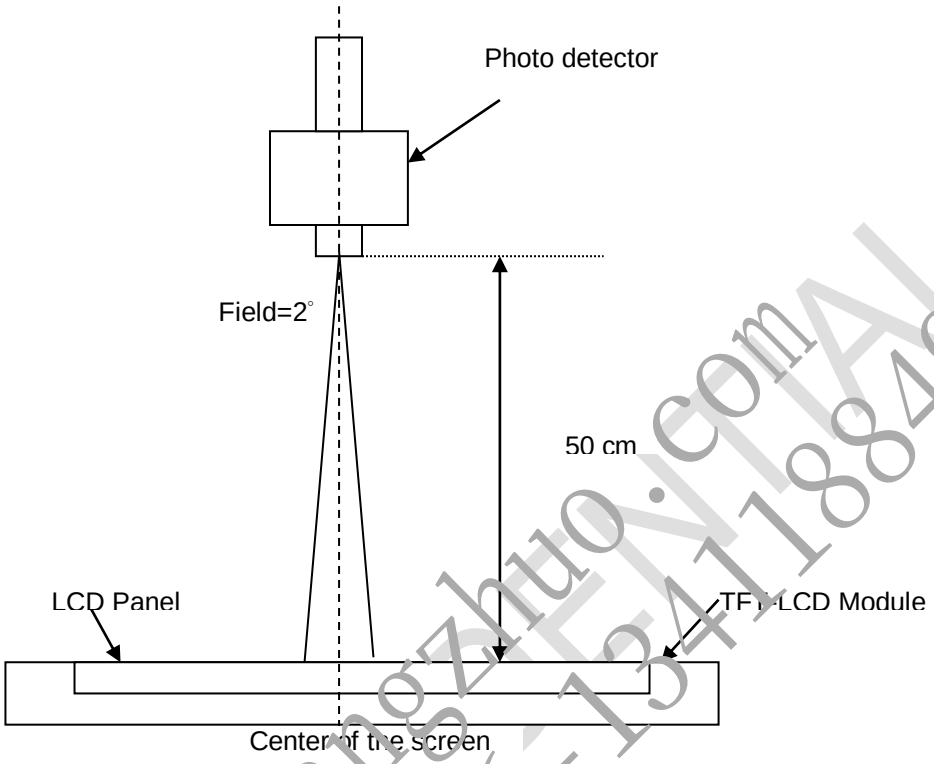
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

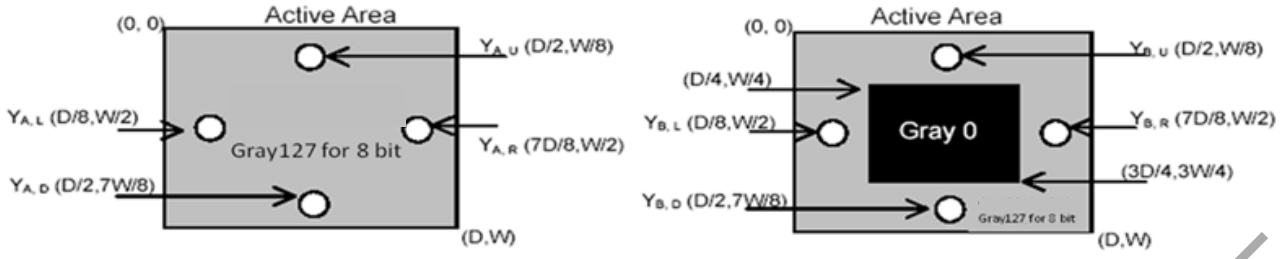
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where

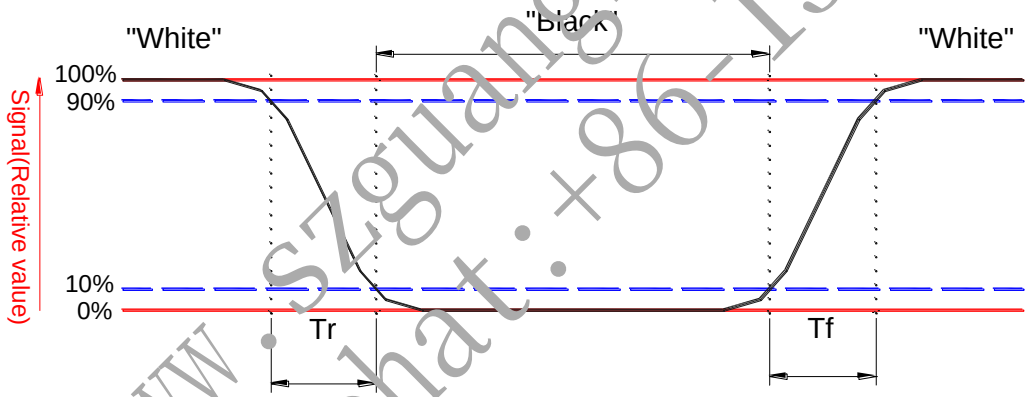
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



Note 8： Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.

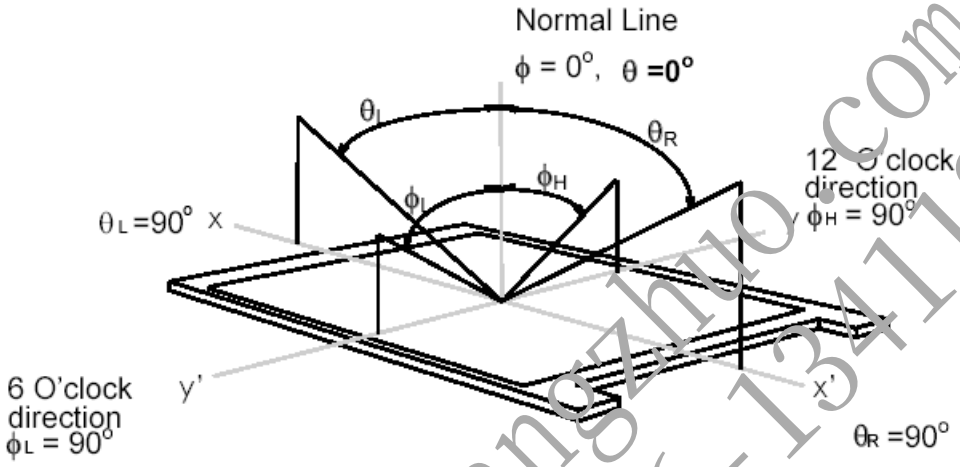


The gray to gray response time is defined as the following table.

Response Time9*9 matrix										
Response Time		To								
		L0	L32	L64	L96	L128	L160	L192	L224	L255
From	L0									
	L32									
	L64									
	L96									
	L128									
	L160									
	L192									
	L224									
	L255									
Response time (Tr+Tf)=L0 to L255+L255 to L0										
Response time (Gray to Gray) average = average time in 9*9 matrix										

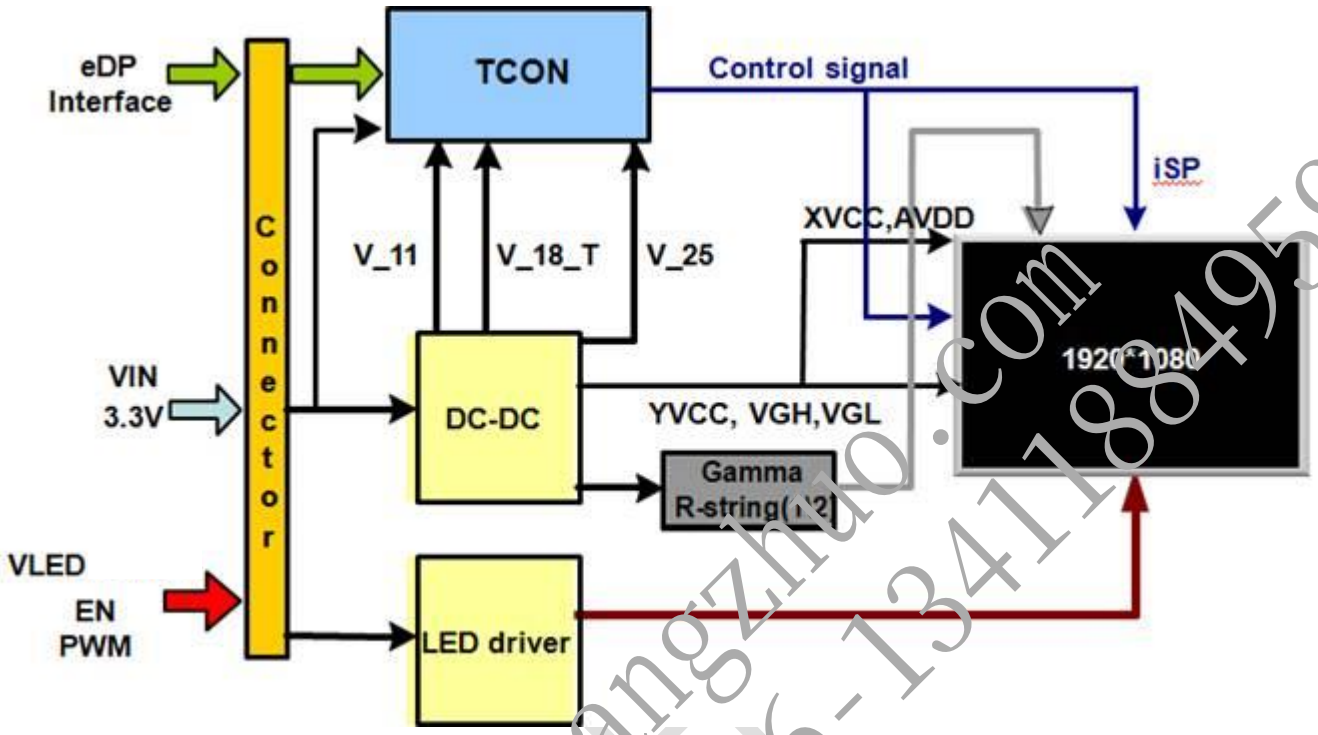
Note 9： Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧ 10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 17.3 inches wide Color TFT/LCD 40 Pin



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operating Humidity	HOP	5	90	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	90	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

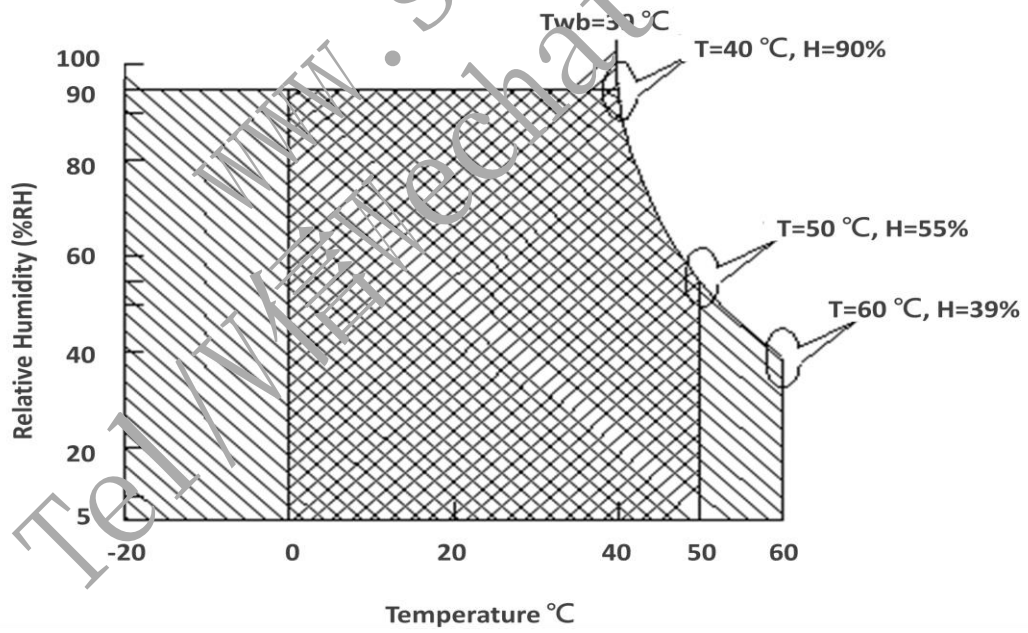
Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).

Note 5: The packing material of system forbid to involve ammonium component

Note 6: The reliability test conditions of system do not exceed the verified conditions of TFT module

Note 7: Be sure the panel test condition do not exceed the component limitation of TFT module(TN Liquid crystal , for example)



Operating Range Storage Range +

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

The power specification are measured under 25℃ and frame frenquency under 360Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	-	3.6	[Volt]	
PDD	VDD Power	-	2.35	2.6	[Watt]	Note 1
IDD	IDD Current	-	-	866	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
IPeak	Peak Current	-	-	1500	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1: PDD(Max)@ mosaic pattern Maximum Power

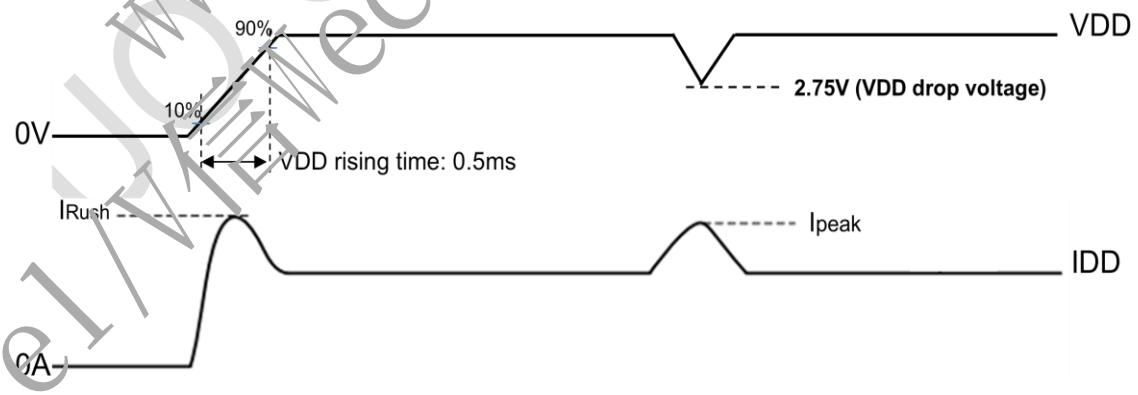
PDD(Max)@ R/G/B pattern Maximum Power

IDD(Max)=PDD(Max) / VDD(Min)

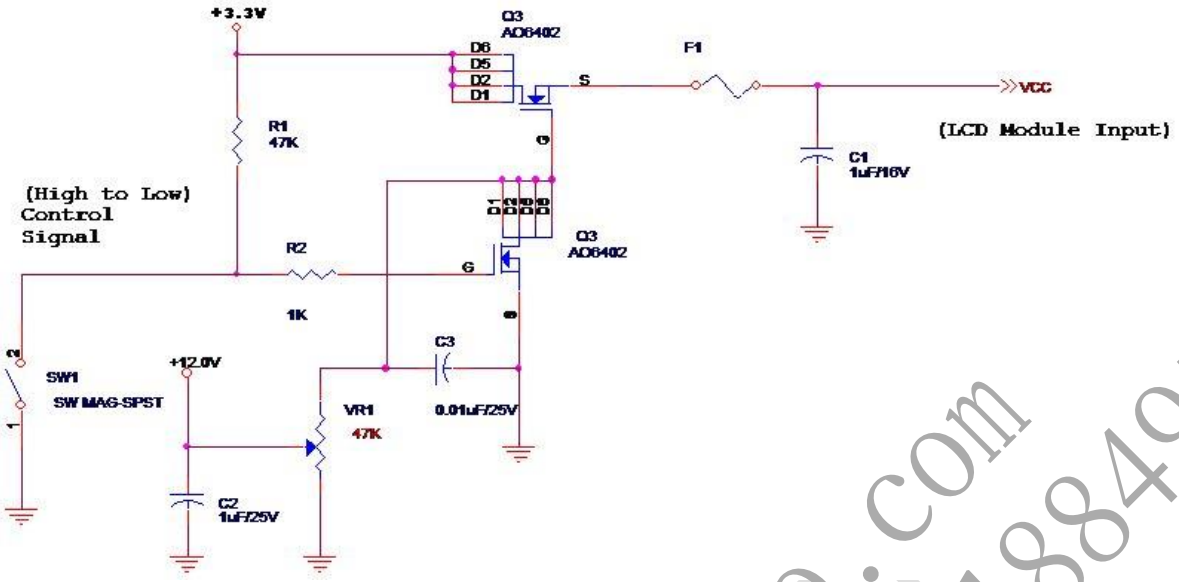
Note 2：

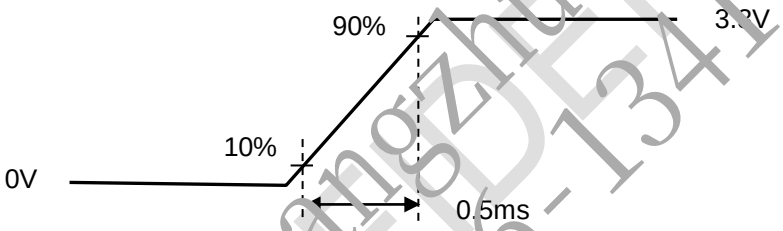
a. IRush: VDD measured rising timing @ 0.5ms

b. IPeak: VDD drop Voltage ≧ 2.75V at this Ipeak current



c. IRush Measure Condition



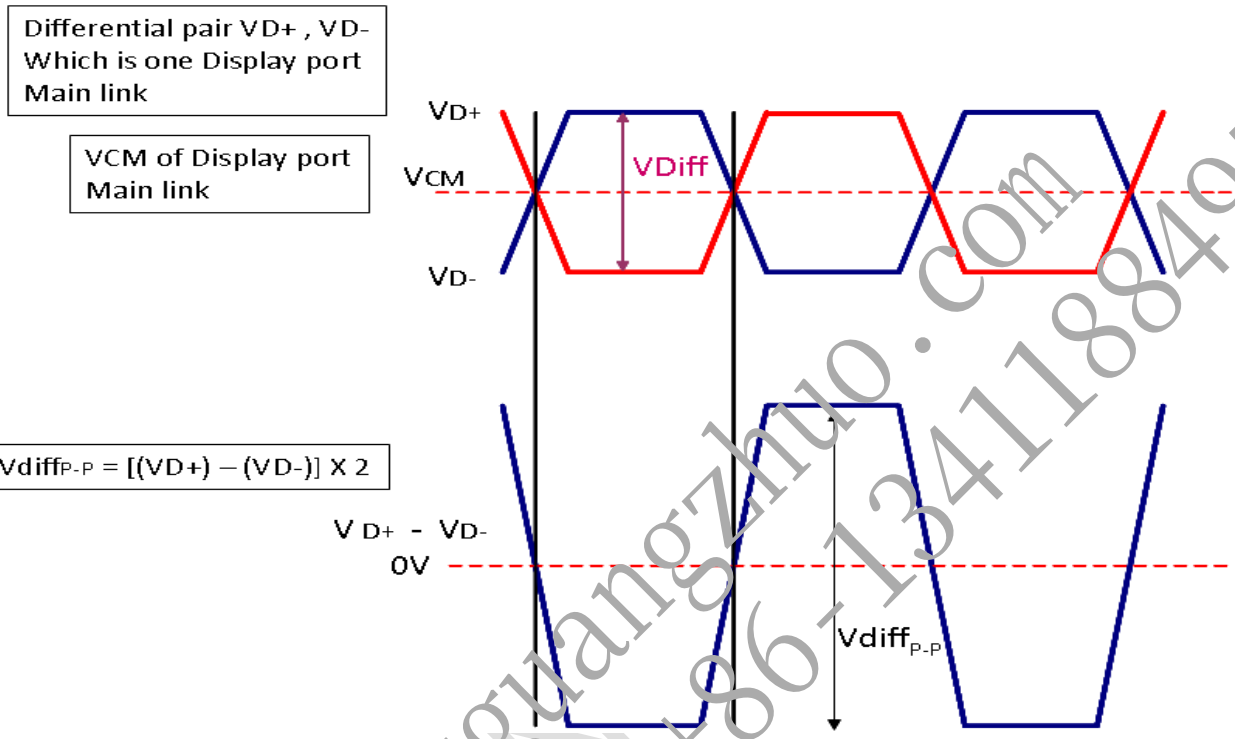


Vin rising time

5.1.2 Signal Electrical Characteristics

Signal electrical characteristics are as follows;

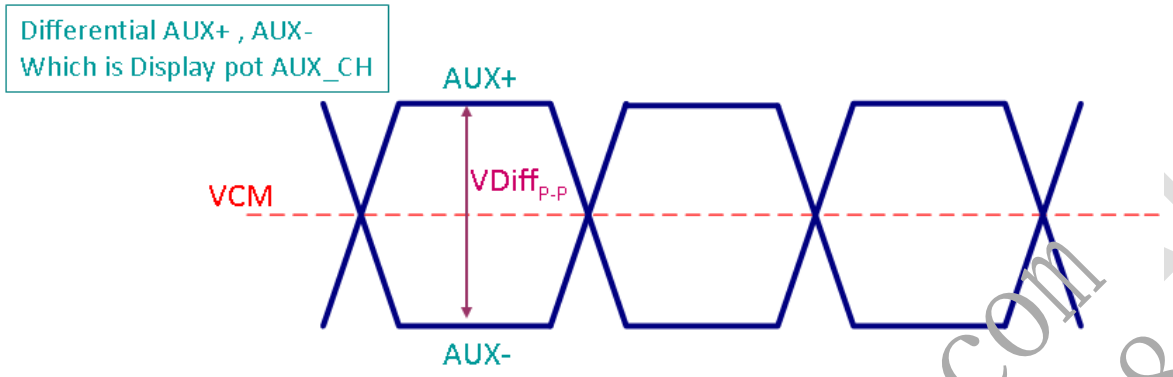
Display Port main link signal:



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	75		1320	mV

Follow as VESA display port standard V1.4

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff P-P	AUX Peak-to-peak Voltage at a receiving Device	270		800	V

Follow as VESA display port standard V1.3

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25	--	3.6	V

Follow as VESA display port standard V1.3

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	3.0	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25℃), Note 2 I_F=12.4mA

Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED (Note 1)	6	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	3.0	--	3.6	[Volt]	
LED Enable Input Low Level		--	--	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	3.0	--	3.6	[Volt]	
PWM Logic Input Low Level		--	--	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

Note 1 : Recommend system pull up/down resistor no bigger than 10kohm

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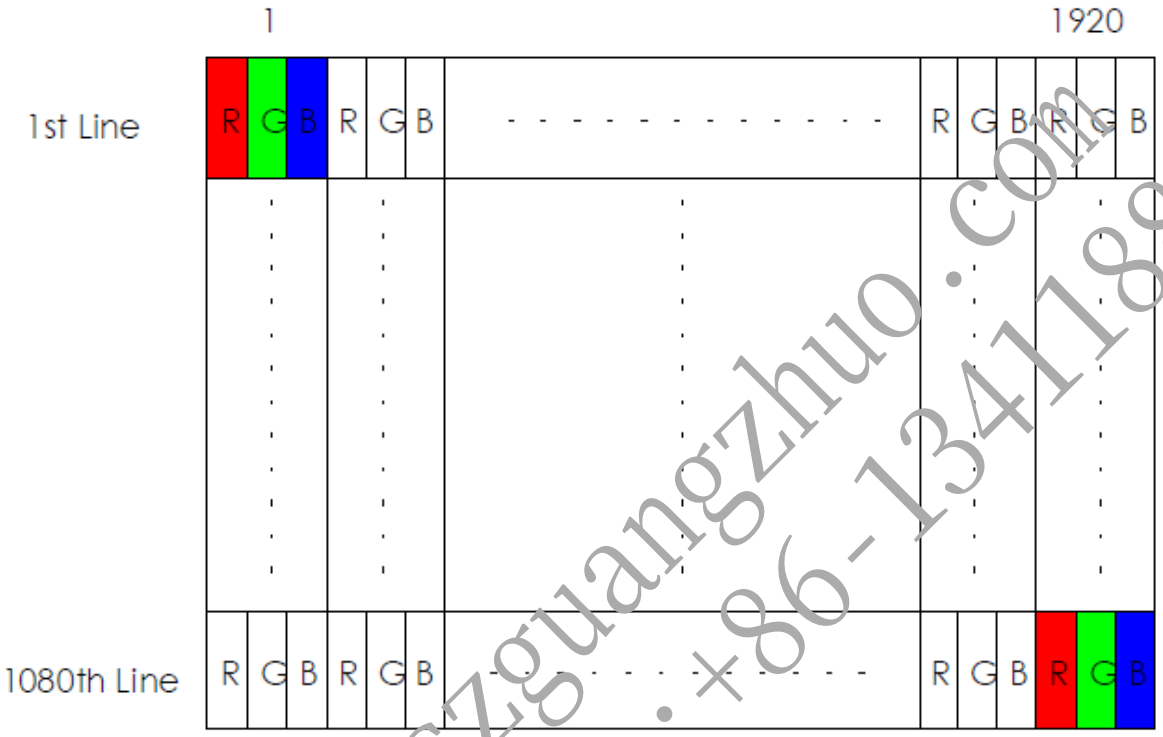
6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

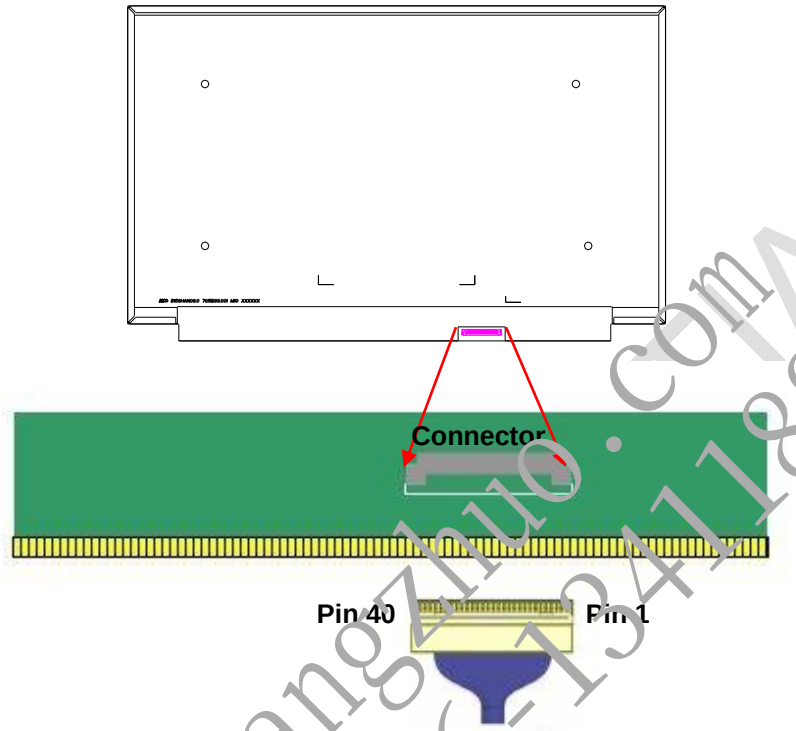
Connector Name / Designation	For Signal Connector
Manufacturer	IPEX
Type / Part Number	20682-040E-02
Mating Housing/Part Number	20679-040T-01

6.2.2 Pin Assignment (4 Lane)

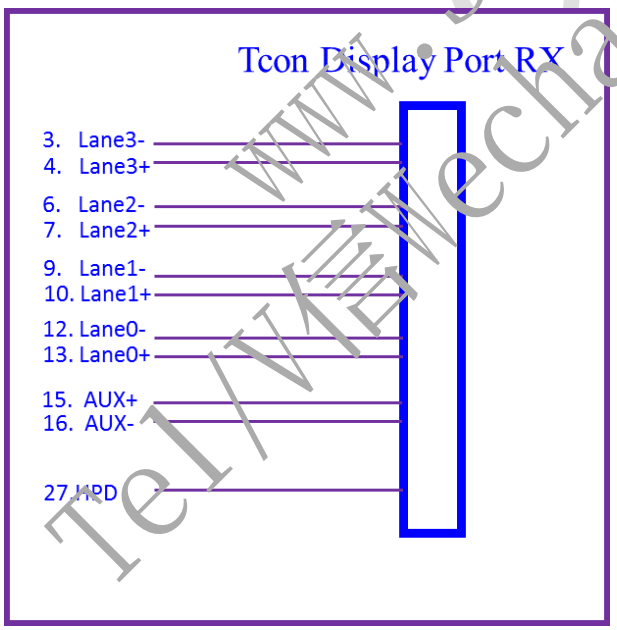
eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN No	Symbol	Function
1	NC	NC
2	H_GND	High Speed Ground
3	Lane3_N	Comp Signal Lane3
4	Lane3_P	True Signal Link Lane 3
5	H_GND	High Speed Ground
6	Lane2_N	Comp Signal Link Lane 2
7	Lane2_P	True Signal Link Lane 2
8	H_GND	High Speed Ground
9	Lane1_N	Comp Signal Lane 1
10	Lane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12	Lane0_N	Comp Signal Link Lane 0
13	Lane0_P	True Signal Link Lane 0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Ch.
16	AUX_CH_N	Comp Signal Auxiliary Ch.
17	H_GND	High Speed Ground
18	LCD_VCC	LCD logic and driver power

19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	LCD_Self_Test or NC	LCD Panel Self Test Enable (Optional)
23	LCD GND	LCD logic and driver ground
24	LCD GND	LCD logic and driver ground
25	LCD GND	LCD logic and driver ground
26	LCD GND	LCD logic and driver ground
27	HPD	HPD signal pin
28	BL_GND	Backlight_ground
29	BL_GND	Backlight_ground
30	BL_GND	Backlight_ground
31	BL_GND	Backlight_ground
32	BL_Enable	Backlight On / Off
33	BL PWM DIM	System PWM signal Input
34	NC	NC
35	NC	NC
36	BL_PWR	Backlight power (6V~21V)
37	BL_PWR	Backlight power (6V~21V)
38	BL_PWR	Backlight power (6V~21V)
39	BL_PWR	Backlight power (6V~21V)
40	OD_EN	OD function default off which can be enable by pull low



Note1: Start from right side.
Note2: Input signals shall be low or High-impedance state when VDD is off.
Internal circuit of **eDP inputs** are as following.



6.3 Interface Timing

6.3.1 Timing Characteristics

Basically, interface timings should match the 1920x1080 / 360Hz manufacturing guide line timing.

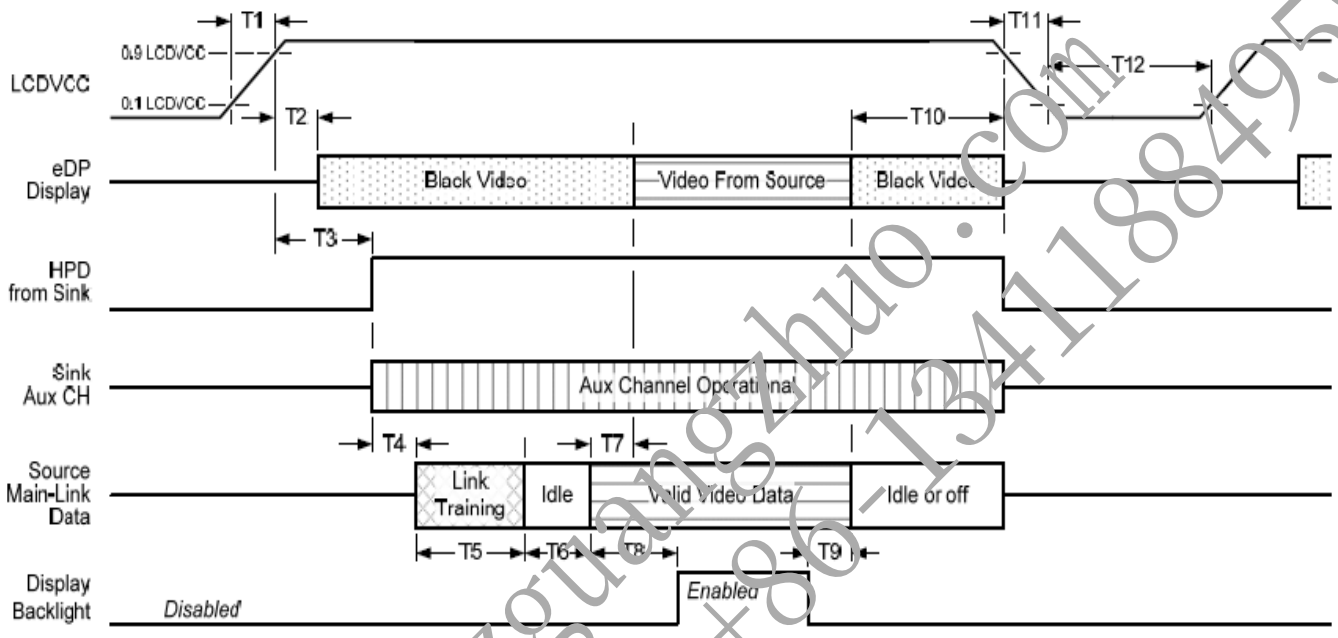
Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	60	-	360	Hz
Clock frequency		1/ T_{Clock}	533.28	-	800	MHz
Vertical Section	Period	T_V	1111	-	4440	T_{Line}
	Active	T_{VD}	1080			
	Blanking	T_{VB}	31	-	3360	
Horizontal Section	Period	T_H	2000	-	2000	T_{Clock}
	Active	T_{HD}	1920			
	Blanking	T_{HB}	80	-	80	

Note 1 : The above is as optimized setting

6.4 Power ON/OFF Sequence

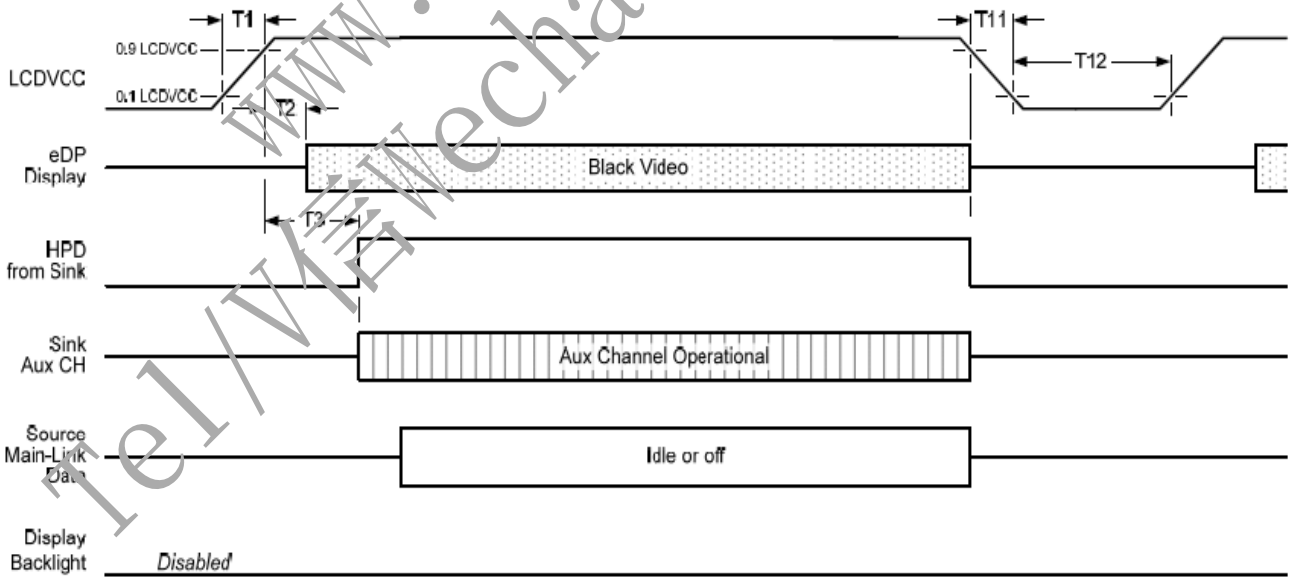
Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port Panel Power Sequence Timing Parameters

Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				Dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	50ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

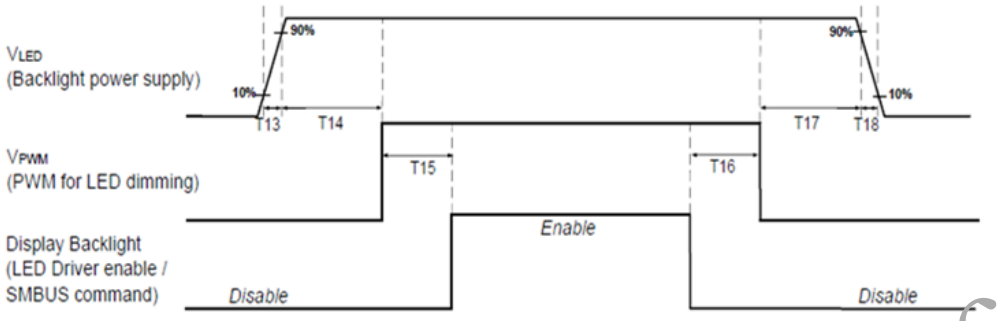
Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max) when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Note 4:T8>T7

Display Port panel B/L power sequence timing parameter:

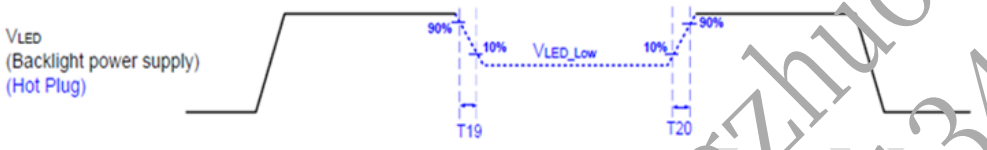


	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM} = 1/PWM Frequency

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

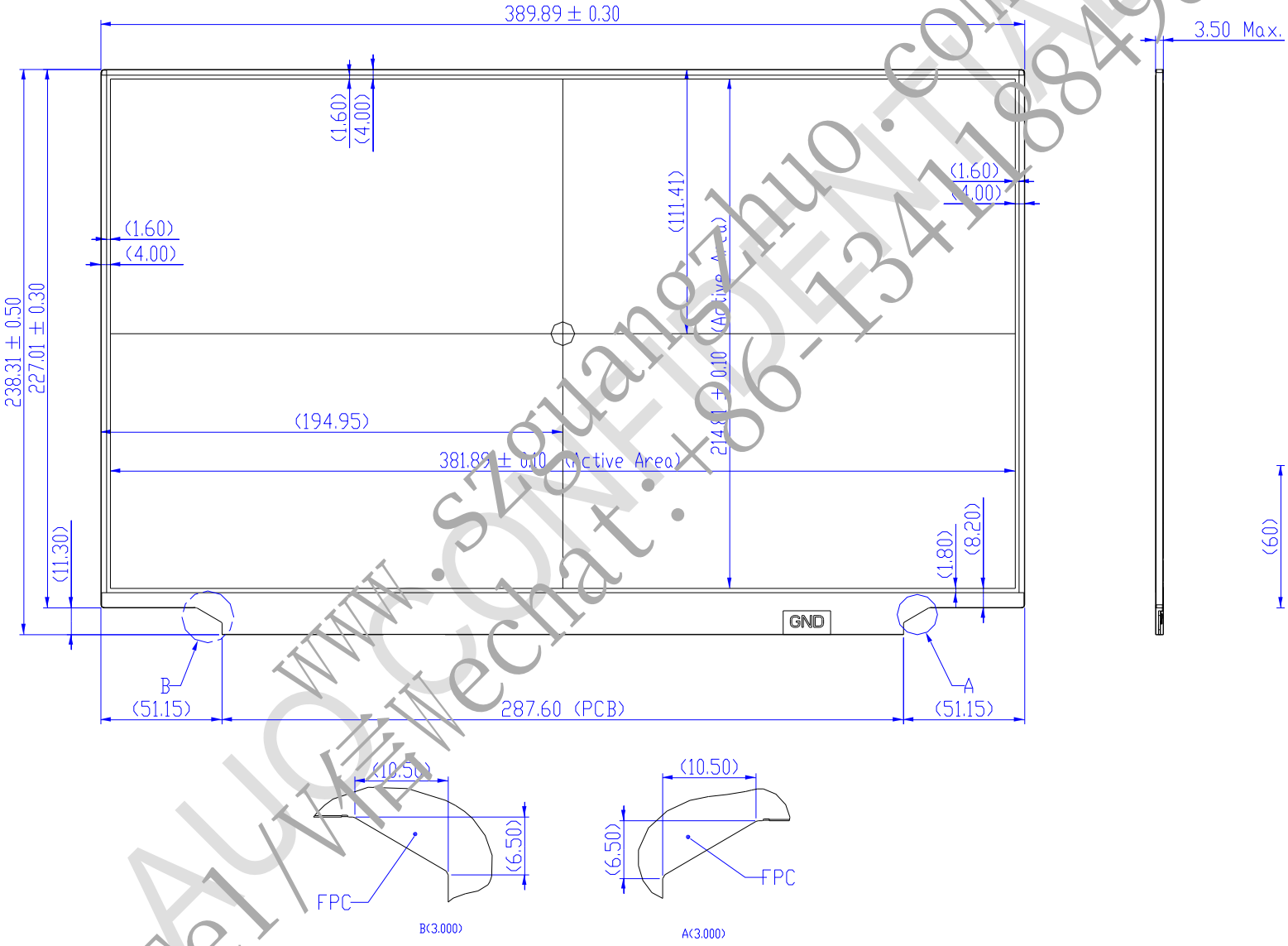
Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 35%RH, 300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 300h	
Thermal Shock Test	Ta=-20℃ to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

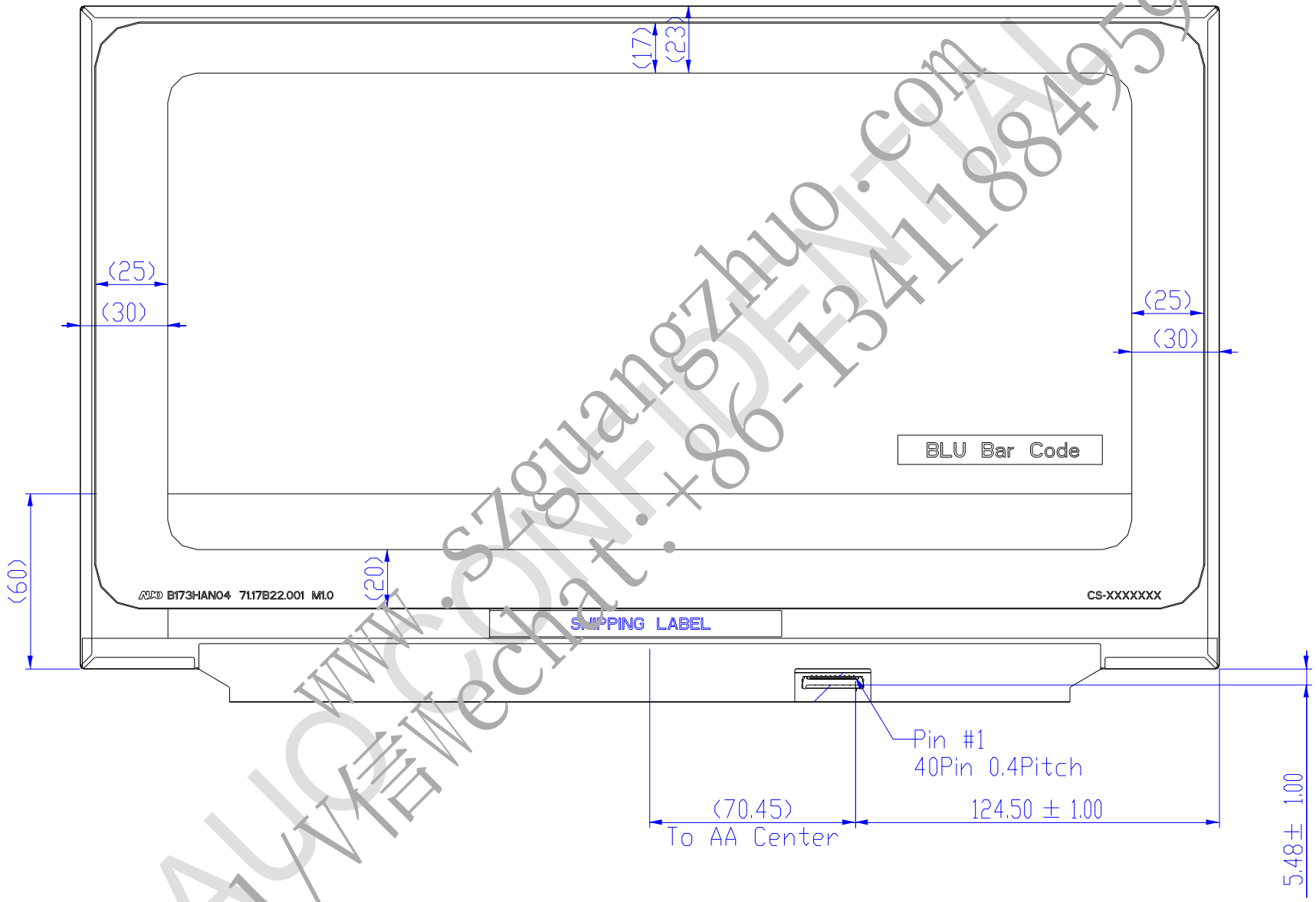
Note 1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

8.1 LCM Outline Dimension

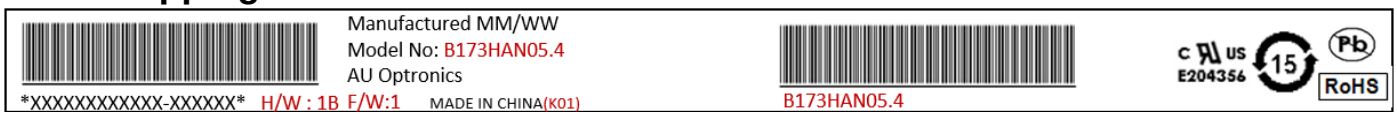




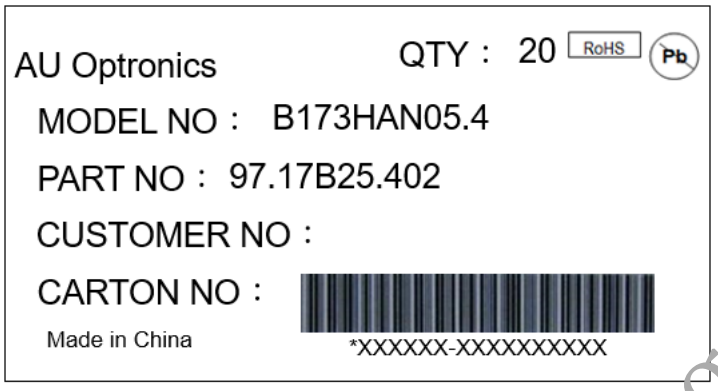
Note. Prevention IC damage, IC positions not allowed any overlap over these areas.

9. Shipping and Package

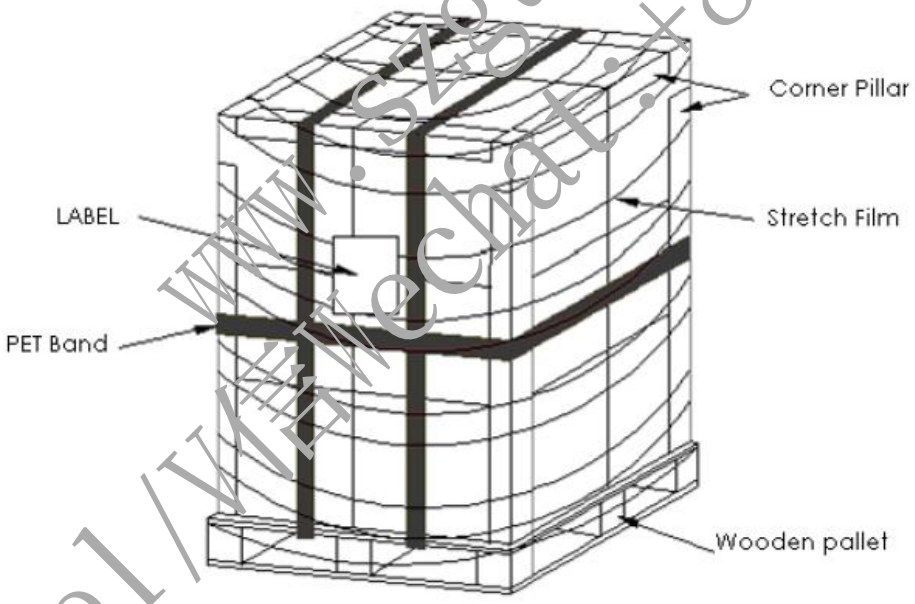
9.1 Shipping Label Format



9.2 Carton Package



9.3 Shipping Package of Palletizing Sequence



10. Appendix:

10.1 EDID Description

Address	FUNCTION	Value	Value	Value
HEX		HEX	BIN	DEC
00	Header	00	00000000	0
01	Header	FF	11111111	255
02	Header	FF	11111111	255
03	Header	FF	11111111	255
04	Header	FF	11111111	255
05	Header	FF	11111111	255
06	Header	FF	11111111	255
07	Header	00	00000000	0
08	EISA Manuf. Code LSB	06	00000110	6
09	Compressed ASCII	AF	10101111	175
0A	Product Code	95	10010101	149
0B	Product Code	E2	11100010	226
0C	32-bit ser #	00	00000000	0
0D	ID S/N - option	00	00000000	0
0E	ID S/N - option	00	00000000	0
0F	ID S/N - option	00	00000000	0
10	Week of manufacture	29	00101001	41
11	Year of manufacture	1E	00011110	30
12	EDID Structure Ver.	01	00000001	1
13	EDID revision #	04	00000100	4
14	**Video input def.** *(digital I/P, non TMDS, CRGB)*	A5	10100101	165
15	**Max H image size** *(rounded to cm)*	26	00100110	38
16	**Max V image size** *(rounded to cm)*	16	00010110	22
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	03	00000011	3
19	Red/green low bits **(Lower 2:2:2:2 bits)**	A3	10100011	163
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	35	00110101	53
1B	Red x **(Upper 8 bits)**	A6	10100110	166
1C	Red y/ highER 8 bits	53	01010011	83
1D	Green x	4A	01001010	74
1E	Green y	9C	10011100	156
1F	Blue x	27	00100111	39
20	Blue y	10	00010000	16
21	White x	50	01010000	80

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22	White y	54	01010100	84
23	Established timing 1	00	00000000	0
24	Established timing 2	00	00000000	0
25	Established timing 3	00	00000000	0
26	Standard timing #1	01	00000001	1
27	Standard timing #1	01	00000001	1
28	Standard timing #2	01	00000001	1
29	Standard timing #2	01	00000001	1
2A	Standard timing #3	01	00000001	1
2B	Standard timing #3	01	00000001	1
2C	Standard timing #4	01	00000001	1
2D	Standard timing #4	01	00000001	1
2E	Standard timing #5	01	00000001	1
2F	Standard timing #5	01	00000001	1
30	Standard timing #6	01	00000001	1
31	Standard timing #6	01	00000001	1
32	Standard timing #7	01	00000001	1
33	Standard timing #7	01	00000001	1
34	Standard timing #8	01	00000001	1
35	Standard timing #8	01	00000001	1
36	Pixel Clock/10000 LSB	1C	00011100	28
37	Pixel Clock/10000 USB	34	00110100	52
38	Horz active **Lower 8bits**	80	10000000	128
39	Horz blanking **Lower 8bits**	50	01010000	80
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	70	01110000	112
3B	Vertical Active **Lower 8bits**	38	00111000	56
3C	Vertical Blanking **Lower 8bits**	1F	00011111	31
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	40	01000000	64
3E	HorzSync. Offset	30	00110000	48
3F	HorzSync.Width	20	00100000	32
40	VertSync.Offset : VertSync.Width	A5	10100101	165
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0
42	Horizontal Image Size **Lower 8bits**	7E	01111110	126
43	Vertical Image Size **Lower 8bits**	D7	11010111	215
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	10	00010000	16
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0
46	Vertical Border *(zero for internal LCD)*	00	00000000	0
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24
48	Pixel Clock/10000 LSB	00	00000000	0

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49	Pixel Clock/10000 USB	00	00000000	0
4A	Horz active **Lower 8bits**	00	00000000	0
4B	Horz blanking **Lower 8bits**	0F	00001111	15
4C	HorzAct:HorzBlnk **Upper 4:4 bits**	00	00000000	0
4D	Vertical Active **Lower 8bits**	00	00000000	0
4E	Vertical Blanking **Lower 8bits**	00	00000000	0
4F	Vert Act : Vertical Blanking **(upper 4:4 bit)**	00	00000000	0
50	HorzSync. Offset	00	00000000	0
51	HorzSync.Width	00	00000000	0
52	VertSync.Offset : VertSync.Width	00	00000000	0
53	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0
54	Horizontal Image Size **Lower 8bits**	00	00000000	0
55	Vertical Image Size **Lower 8bits**	00	00000000	0
56	Horizontal & Vertical Image Size **(upper 4:4 bits)**	00	00000000	0
57	Horizontal Border *(zero for internal LCD)*	00	00000000	0
58	Vertical Border *(zero for internal LCD)*	00	00000000	0
59	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	20	00100000	32
5A	descriptor #3	00	00000000	0
5B	Reserved for definition	00	00000000	0
5C	Reserved for definition	00	00000000	0
5D	ASCII String	FD	11111101	253
5E	Reserved for definition	0E	00001110	14
5F	Manufacture	3C	00111100	60
60	Manufacture	69	01101001	105
61	Manufacture	91	10010001	145
62	Reserved for definition	91	10010001	145
63	Reserved for definition	50	01010000	80
64	Reserved for definition	01	00000001	1
65	Reserved for definition	0A	00001010	10
66	Reserved for definition	20	00100000	32
67	Reserved for definition	20	00100000	32
68	Reserved for definition	20	00100000	32
69	Reserved for definition	20	00100000	32
6A	Reserved for definition	20	00100000	32
6B	Reserved for definition	20	00100000	32
6C	Reserved for definition	00	00000000	0
6D	descriptor #4	00	00000000	0
6E	Reserved for definition	00	00000000	0
6F	Reserved for definition	FE	11111110	254

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70	Reserved for definition	00	00000000	0
71	Manufacture P/N	42	01000010	66
72	Manufacture P/N	31	00110001	49
73	Manufacture P/N	37	00110111	55
74	Manufacture P/N	33	00110011	51
75	Manufacture P/N	48	01001000	72
76	Manufacture P/N	41	01000001	65
77	Manufacture P/N	4E	01001110	78
78	Manufacture P/N	30	00110000	48
79	Manufacture P/N	35	00110101	53
7A	Manufacture P/N	2E	00101110	46
7B	Manufacture P/N	34	00110100	52
7C	Reserved for definition	20	00100000	32
7D	Reserved for definition	0A	00001010	10
7E	Extension Flag	01	00000001	1
7F	Checksum	37	00110111	55

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Extend-EDID

Address	FUNCTION	Value	Value	Value
HEX		HEX	BIN	DEC
80		70	01110000	112
81	Display ID Version	13	00010011	19
82	Block Size	79	01111001	121
83		00	00000000	0
84		00	00000000	0
85	Type I timing	03	00000011	3
86	Revision '1'	01	00000001	1
87	Number of Payload Bytes in Block	14	00010100	20
88	Pixel clock	80	10000000	128
89	Pixel clock	38	00111000	56
8A	Pixel clock	01	00000001	1
8B	Preferred timing	84	10000100	132
8C	H-AA	7F	01111111	127
8D	H-AA	07	00000111	7
8E	H-BK	4F	01001111	79
8F	H-BK	00	00000000	0
90	H-offset	2F	00101111	47
91	H-offset	00	00000000	0
92	H-Sync	1F	00011111	31
93	H-Sync	00	00000000	0
94	V-AA	37	00110111	55
95	V-AA	04	00000100	4
96	V-BK	1E	00011110	30
97	V-BK	00	00000000	0
98	V-offset	09	00001001	9
99	V-offset	00	00000000	0
9A	V-Sync	04	00000100	4
9B	V-Sync	00	00000000	0
9C		00	00000000	0
9D		00	00000000	0
9E		00	00000000	0
9F		00	00000000	0
A0		00	00000000	0
A1		00	00000000	0
A2		00	00000000	0
A3		00	00000000	0

Product Specification

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A4		00	00000000	0
A5		00	00000000	0
A6		00	00000000	0
A7		00	00000000	0
A8		00	00000000	0
A9		00	00000000	0
AA		00	00000000	0
AB		00	00000000	0
AC		00	00000000	0
AD		00	00000000	0
AE		00	00000000	0
AF		00	00000000	0
B0		00	00000000	0
B1		00	00000000	0
B2		00	00000000	0
B3		00	00000000	0
B4		00	00000000	0
B5		00	00000000	0
B6		00	00000000	0
B7		00	00000000	0
B8		00	00000000	0
B9		00	00000000	0
BA		00	00000000	0
BB		00	00000000	0
BC		00	00000000	0
BD		00	00000000	0
BE		00	00000000	0
BF		00	00000000	0
C0		00	00000000	0
C1		00	00000000	0
C2		00	00000000	0
C3		00	00000000	0
C4		00	00000000	0
C5		00	00000000	0
C6		00	00000000	0
C7		00	00000000	0
C8		00	00000000	0
C9		00	00000000	0
CA		00	00000000	0

CB		00	00000000	0
CC		00	00000000	0
CD		00	00000000	0
CE		00	00000000	0
CF		00	00000000	0
D0		00	00000000	0
D1		00	00000000	0
D2		00	00000000	0
D3		00	00000000	0
D4		00	00000000	0
D5		00	00000000	0
D6		00	00000000	0
D7		00	00000000	0
D8		00	00000000	0
D9		00	00000000	0
DA		00	00000000	0
DB		00	00000000	0
DC		00	00000000	0
DD		00	00000000	0
DE		00	00000000	0
DF		00	00000000	0
E0		00	00000000	0
E1		00	00000000	0
E2		00	00000000	0
E3		00	00000000	0
E4		00	00000000	0
E5		00	00000000	0
E6		00	00000000	0
E7		00	00000000	0
E8		00	00000000	0
E9		00	00000000	0
EA		00	00000000	0
EB		00	00000000	0
EC		00	00000000	0
ED		00	00000000	0
EE		00	00000000	0
EF		00	00000000	0
F0		00	00000000	0
F1		00	00000000	0

F2		00	00000000	0
F3		00	00000000	0
F4		00	00000000	0
F5		00	00000000	0
F6		00	00000000	0
F7		00	00000000	0
F8		00	00000000	0
F9		00	00000000	0
FA		00	00000000	0
FB		00	00000000	0
FC		00	00000000	0
FD		00	00000000	0
FE	Section Checksum (81~FE)	96	10010110	150
FF	EDID Extension Block Checksum (80~FF)	90	10010000	144

10.2 Notes

DPCD Ver.	eDP	LRR	DRRS (Static DRRS)	sDRRS (Seamless DRRS)	DCR	DMRRS	PSR	MBO
1.4	1.4a	NA	Off	Off	Off	Off	PSR1	Off

VESA DSC	MSO	AMD Free-Sync	Intel Adaptive Sync	NVidia G-Sync	HDR	Dimming
Off	Off	On	On	On	NA	PWN