Product Specification

AU OPTRONICS CORPORATION

( ) Preliminary Specifications
(V) Final Specifications

Module	**17.3”(17.26”) FHD 16:9 Color TFT-LCD with LED Backlight design**
Model Name	**B173HAN05.2 (H/W:0A) DPN:TNCHH**
Note ( )	***LED Backlight with driving circuit design***

Customer	**Date**	**Approved by**	**Date**
		YW Lee	04/18/2021
Checked & Approved by	**Date**	**Prepared by**	**Date**
		CraigWu	04/18/2021
Note: This Specification is subject to change without notice.		**NBBU Marketing Division AU Optronics corporation**	

www.szguangzhuo.com 广卓液晶屏 echodeng61@hotmail.com jimei@jimeihk.com +86-13411884959

Classify:AUO-General

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www.szguangzhuo.com 广卓液晶屏 echodeng61@hotmail.com jimei@jimeihk.com +86-13411884959

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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2020/04/15	All	First Edition for Customer		
0.2 2020/10/18	30-37	EDID update	Update EDID X11	
0.3 2021/01/22	29-37	Label Format & EDID update	Update Label Format & EDID X20	
1.0 2021/04/18	All	Final Edition for Customer		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
10) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
11) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
12) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B173HAN05.2 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 FHD, 1920(H) x 1080(V) screen and 16.7M colors (RGB 8-bits data driver) with LED backlight driving circuit. All input signals are eDP interface compatible.

B173HAN05.2 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	17.3”(17.26)			
Active Area	[mm]	381.888 x 214.812			
Pixels H x V		1920 x 3 (RGB) x 1080			
Pixel Pitch	[mm]	0.1989 x 0.1989			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black			
White Luminance (I_{LED}=20mA) (Note: I_{LED} is LED current)	[cd/m^2]	300 typ. (5 points average) 255 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		1000 typ			
Response Time	[ms]	Tr+Tf 5 typ. GTG w/o OD 3 typ. GTG w/ OD 1 typ			
Nominal Input Voltage VDD	[Volt]	+3.3V min			
Power Consumption	[Watt]	7.2W Max (with OD) (Max: inculd Logic@mosaic & BL power)			
Weight	[Grams]	600g max			
Physical Size	[mm]		Min.	Typ.	Max.
		Length	389.59	389.89	390.19
		Width	226.71	227.01	227.31
		Thickness	-	-	3.0
Electrical Interface		4 Lane eDP1.4			
Glass Thickness	[mm]	0.4			
Surface Treatment		Anti-Glare, Hardness 3H			
Support Color		16.7M colors (RGB 8-bit)			
Temperature Range Operating Storage (Non-Operating)	[ºC] [ºC]	0 to +50 -20 to +60			

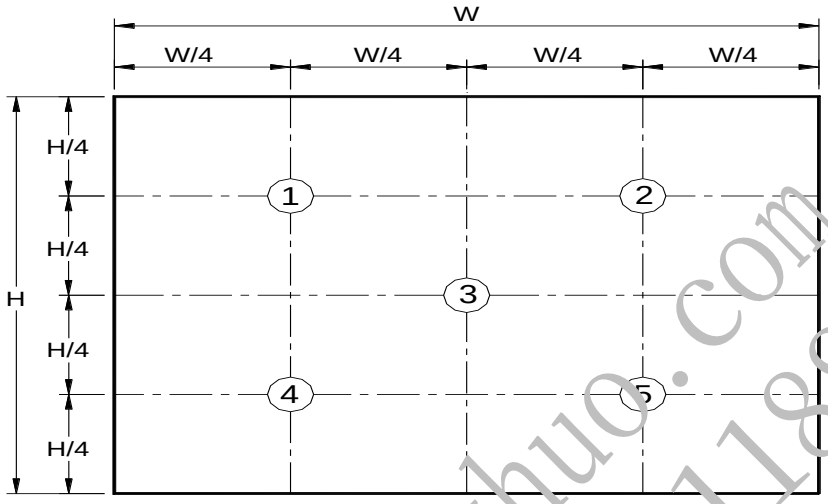
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

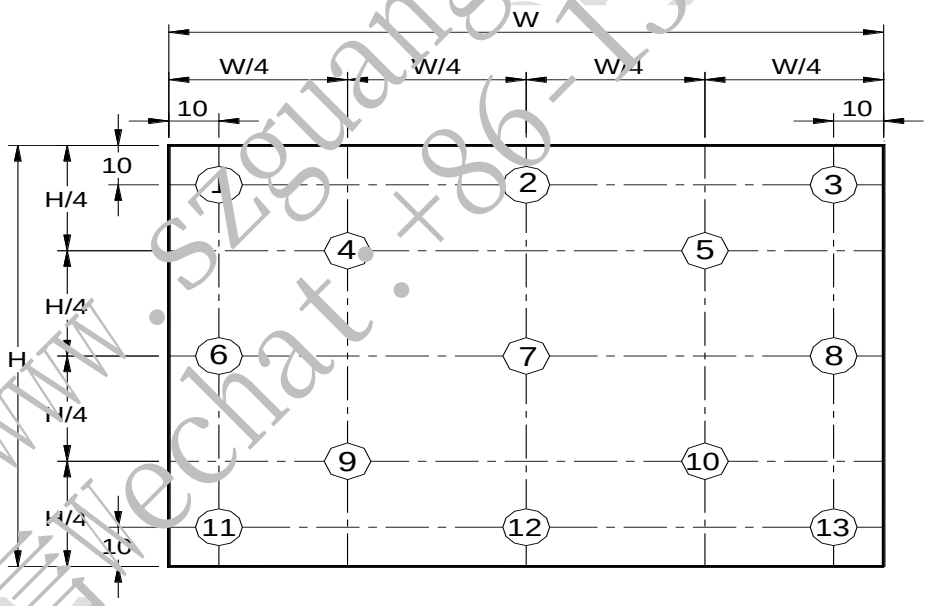
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED} = 20mA			5 points average	255	300	-	cd/m²	1, 4, 5
Viewing Angle		θ_R θ_L	Horizontal (Right) CR = 10 (Left)	80 80	85 85	-	degree	4, 9
		ϕ_H ϕ_L	Vertical (Upper) CR = 10 (Lower)	80 80	85 85	-		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.6		2, 3, 4
Contrast Ratio		CR		700	1000	-		4, 6
Cross talk		%				4		4, 7
Response Time		T_{RT}	Rising + Falling	-	5	-	msec	4, 8
Response Time		$T_{G\ To\ G}$		-	3	-	msec	8
Response Time		$T_{OD\ G\ To\ G}$		-	1	-	msec	8
Color / Chromaticity Coordinates	White	Wx	CIE 1931	0.283	0.313	0.343		4
		Wy		0.299	0.329	0.359		
	Red	Rx		0.630	0.660	0.690		
		Ry		0.300	0.330	0.360		
	Green	Gx		0.248	0.278	0.308		
		Gy		0.597	0.627	0.657		
	Blue	Bx		0.114	0.144	0.174		
		By		0.032	0.062	0.092		
sRGB		%		95	100	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

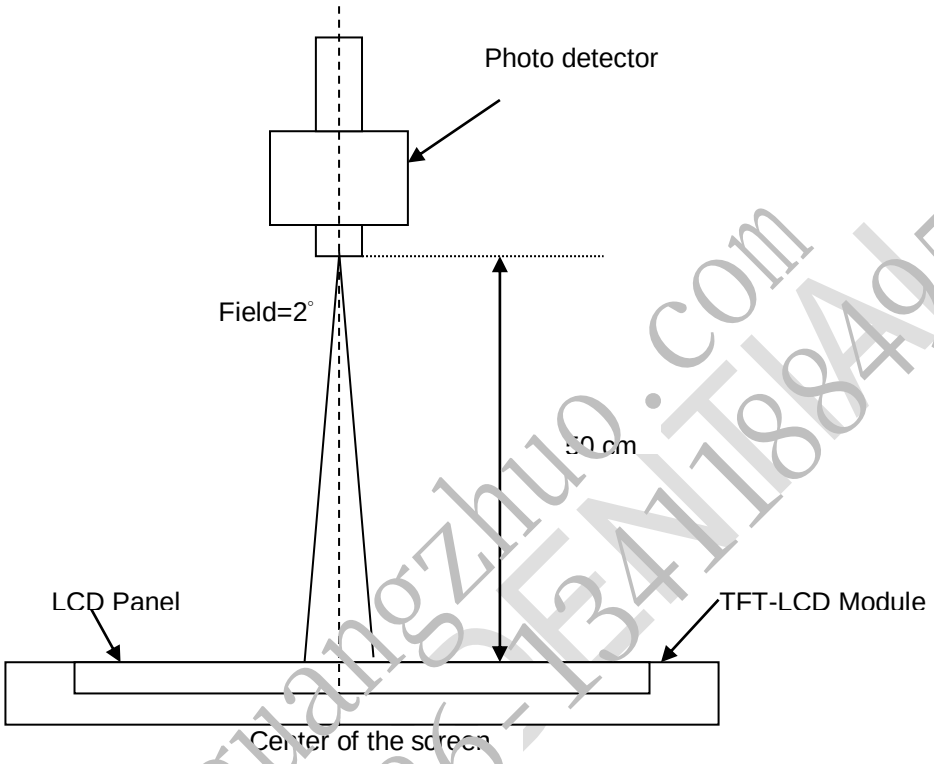
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

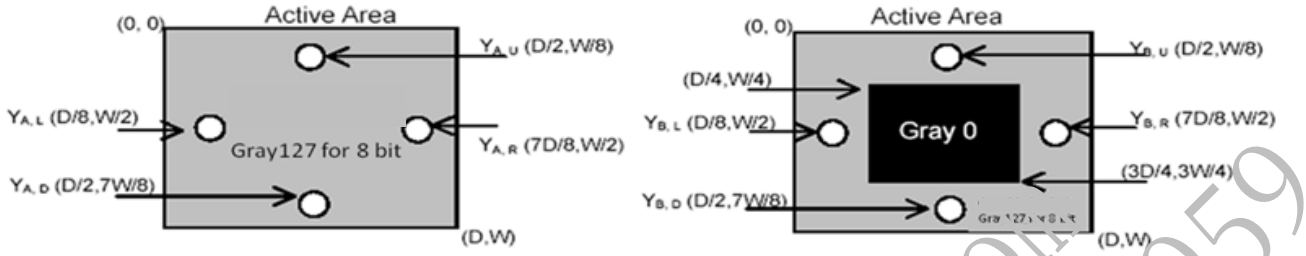
Note 7： Definition of Cross Talk (CT)

$CT = |Y_B - Y_A| / Y_A \times 100$ (%)

Where

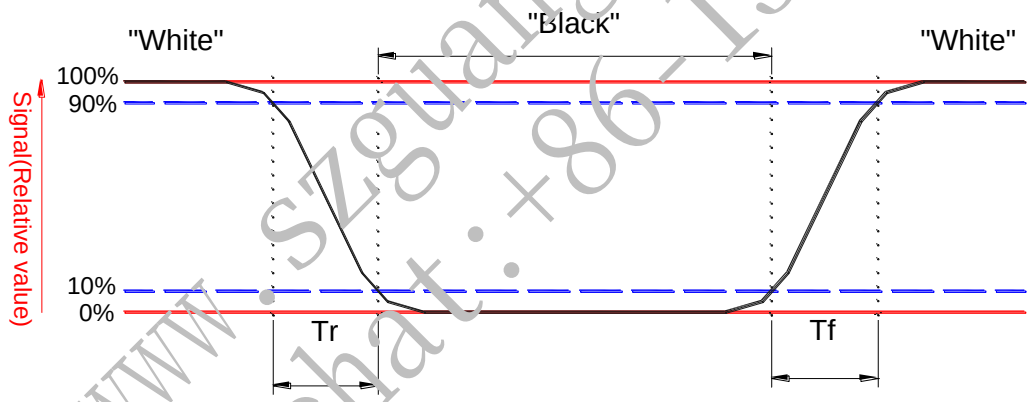
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



Note 8： Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.

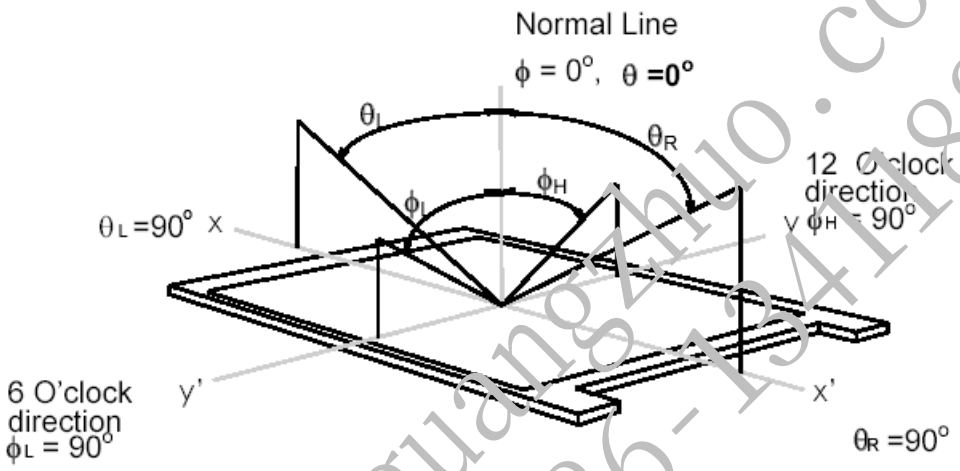


The gray to gray response time is defined as the following table.

Response Time9*9 matrix										
Response Time		To								
		L0	L32	L64	L96	L128	L160	L192	L224	L255
From	L0									
	L32									
	L64									
	L96									
	L128									
	L160									
	L192									
	L224									
	L255									
Response time (Tr+Tf)=L0 to L255+L255 to L0										
Response time (Gray to Gray) average = average time in 9*9 matrix										

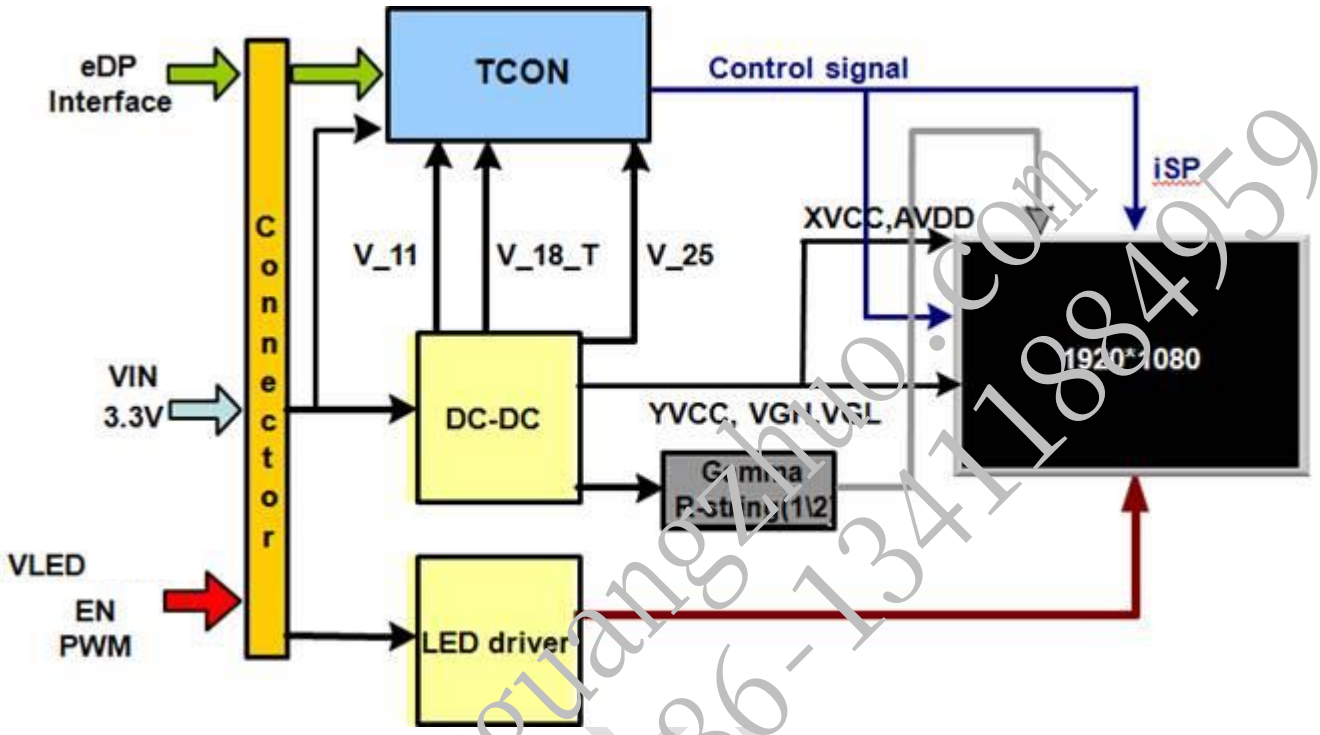
Note 9： Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧ 10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 17.3 inches wide Color TFT/LCD 40 Pin



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

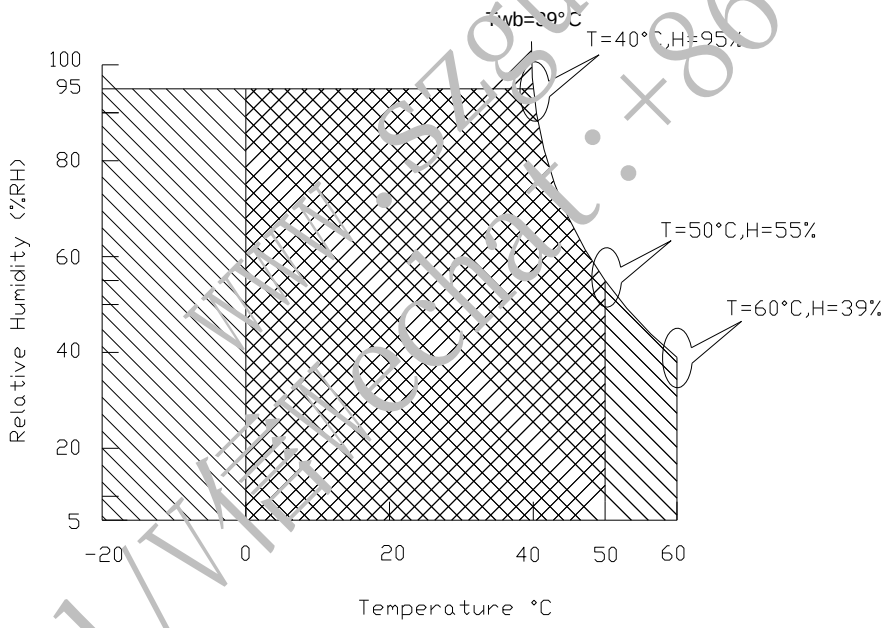
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range +

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

The power specification are measured under 25℃ and frame frenquency under 360Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power @ mosaic pattern	-	-	2.6	[Watt]	Note 1
IDD	IDD Current(RMS) @ mosaic pattern	-	-	866	[mA]	Note 1
PDD	VDD Power @ R/G/B pattern	-	-	3.7	[Watt]	Note 1
IDD	IDD Current(RMS) @ R/G/B pattern	-	-	1233	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
Ipeak	Peak Current	-	-	1500	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	
CDD	VDD Capacitance	-	-	TBD	[uF]	Note3

Note 1 : PDD(Max)@ mosaic pattern Maximum Power

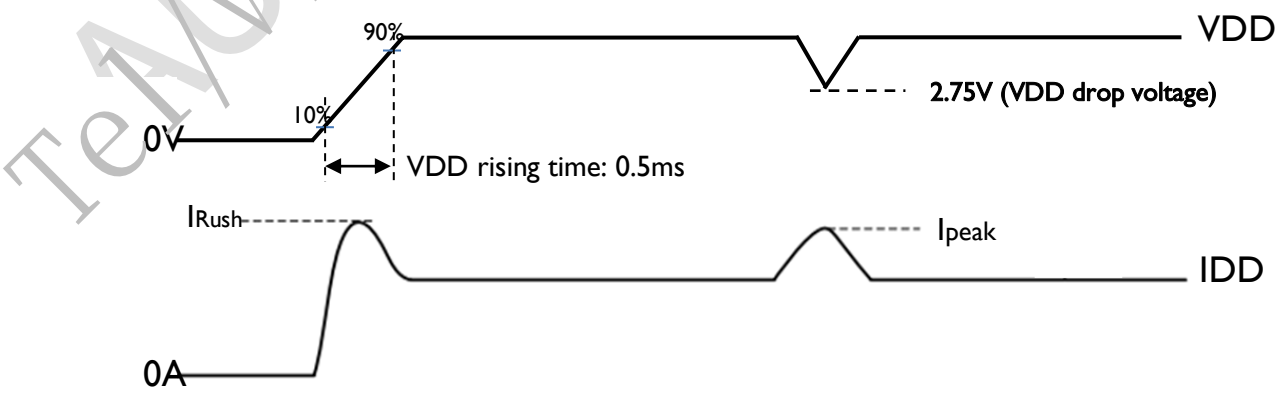
PDD(Max)@ R/G/B pattern Maximum Power

IDD(Max)=PDD(Max) / VDD(Min)

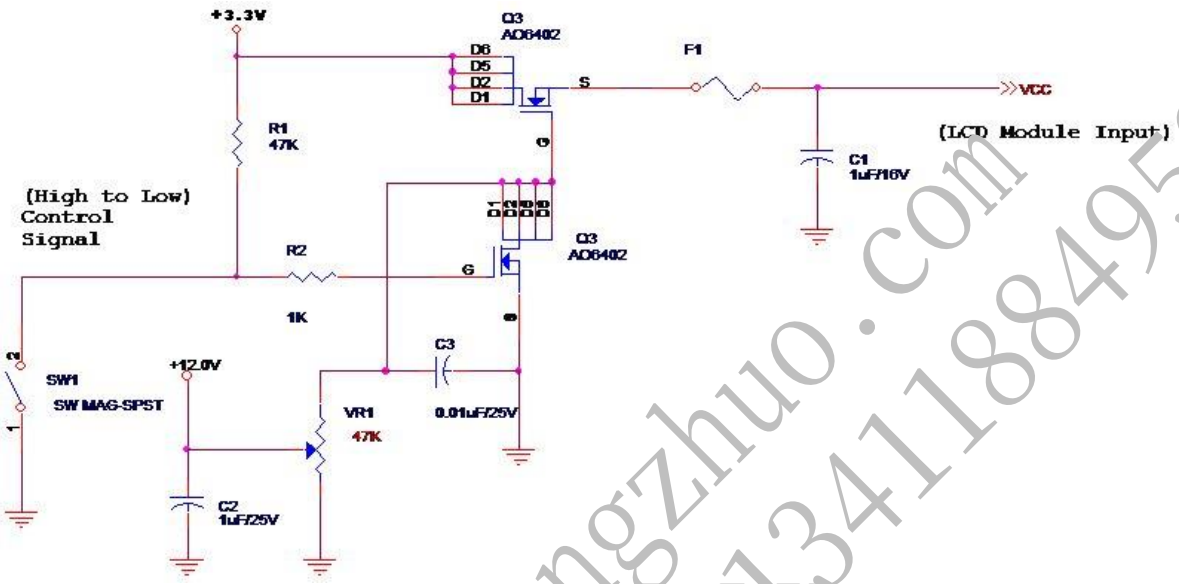
Note 2：

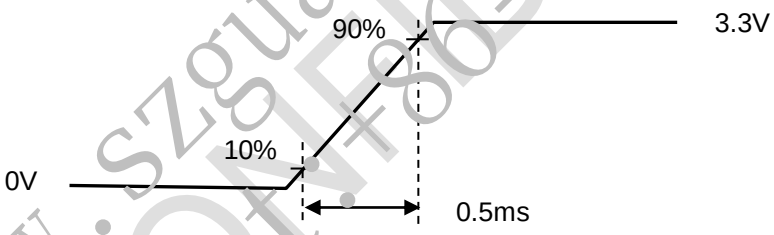
a. IRush: VDD measured rising timing @ 0.5ms

b. IPeak: VDD drop Voltage ≥ 2.75V at this Ipeak current



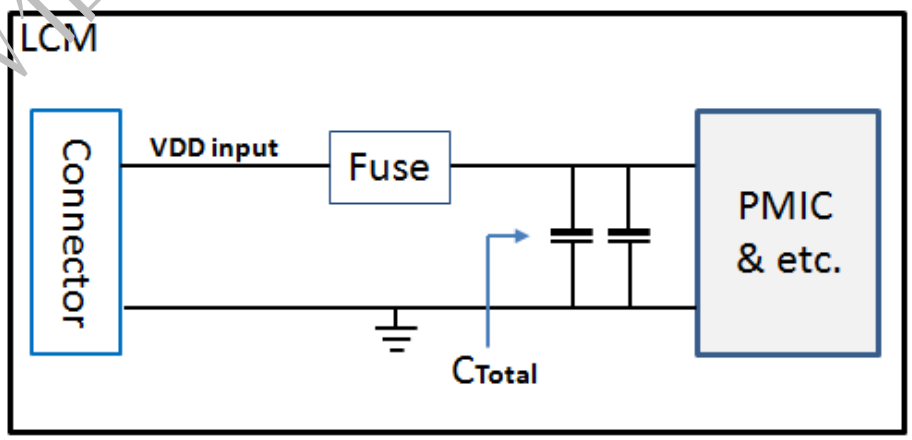
c. IRush Measure Condition:





Vin rising time

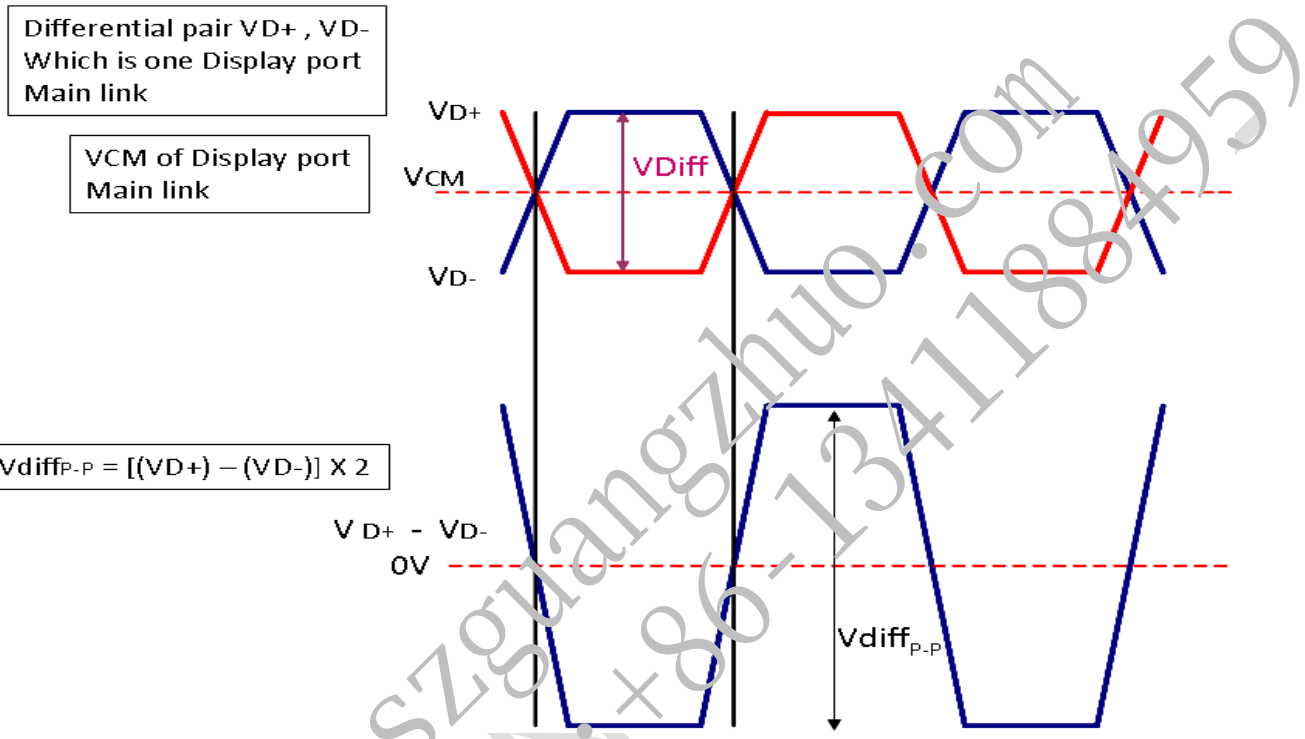
Note 3: Schematic diagram for VDD loop C_{Total} value



5.1.2 Signal Electrical Characteristics

Signal electrical characteristics are as follows;

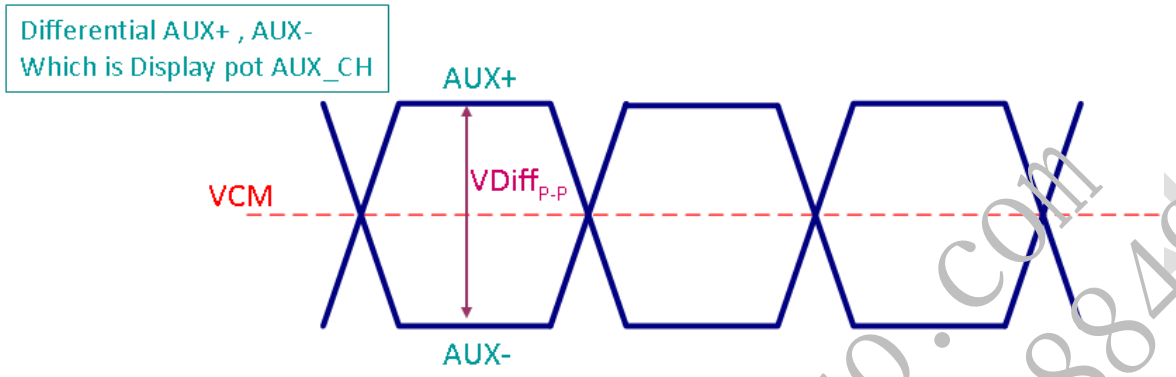
Display Port main link signal:



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	75		1320	mV

Follow as VESA display port standard V1.4

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff P-P	AUX Peak-to-peak Voltage at a receiving Device	270		800	V

Follow as VESA display port standard V1.3

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25	--	3.6	V

Follow as VESA display port standard V1.3

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	4.6	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25℃), Note 2 I_L=20 mA

Note 1: Calculator value for reference $P_{LED} = V_F$ (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED (Note 1)	6	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	3.0	--	3.6	[Volt]	
LED Enable Input Low Level		--	--	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	3.0	--	3.6	[Volt]	
PWM Logic Input Low Level		--	--	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

Note 1 : Recommend system pull up/down resistor no bigger than 10kohm

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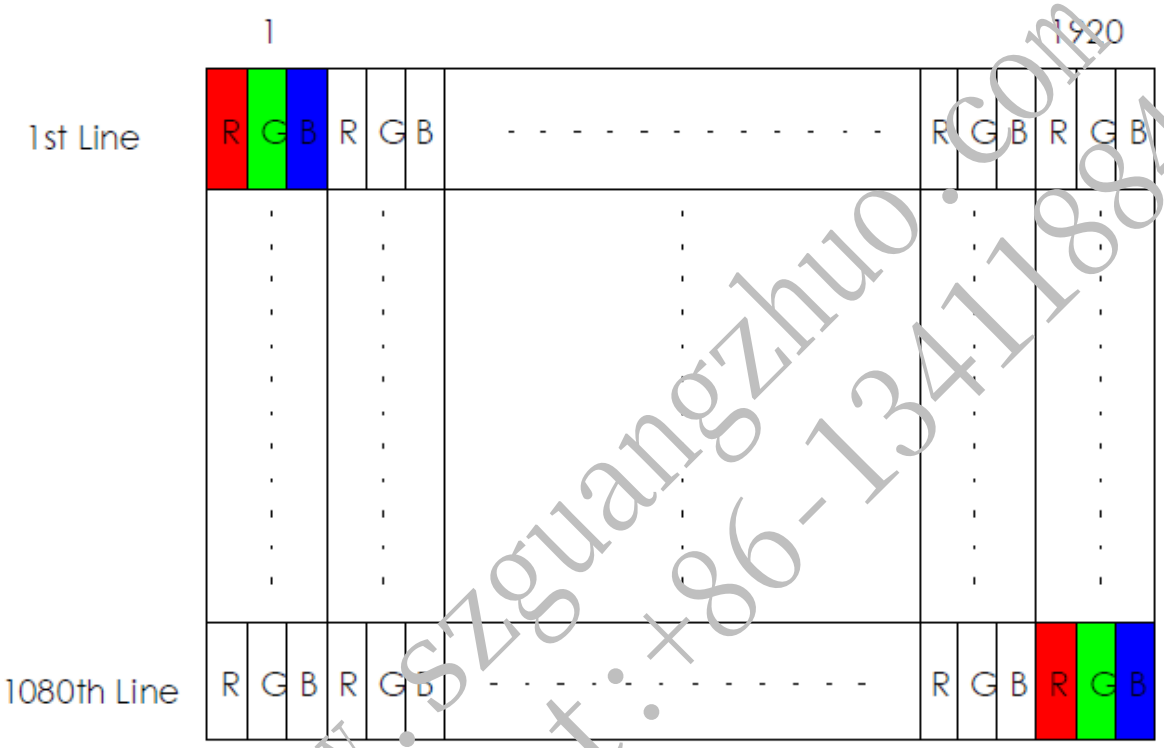
6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

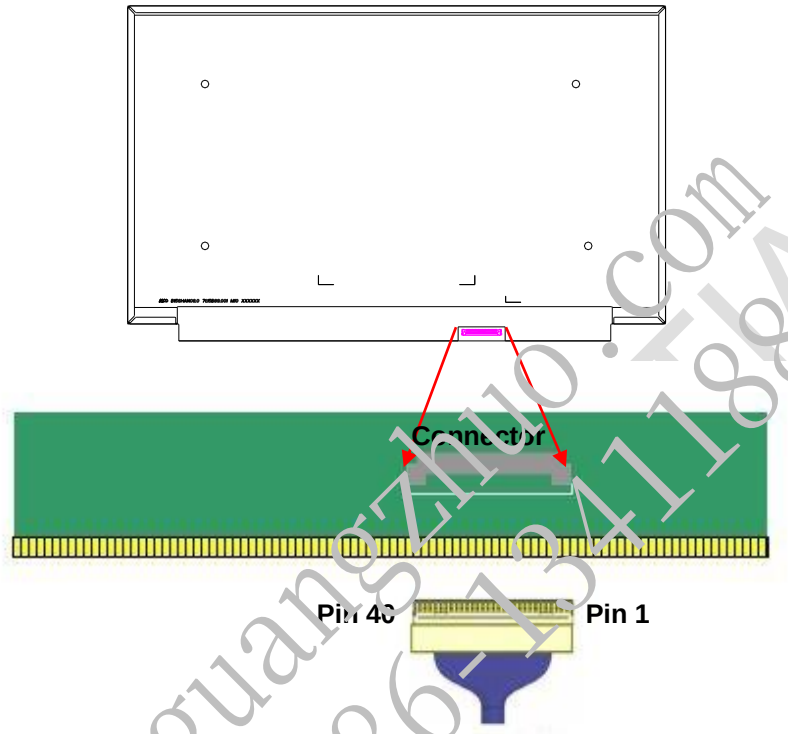
Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	20682-040E-02 or compatible
Mating Housing/Part Number	20679-040T-01 or compatible

6.2.2 Pin Assignment (4 Lane)

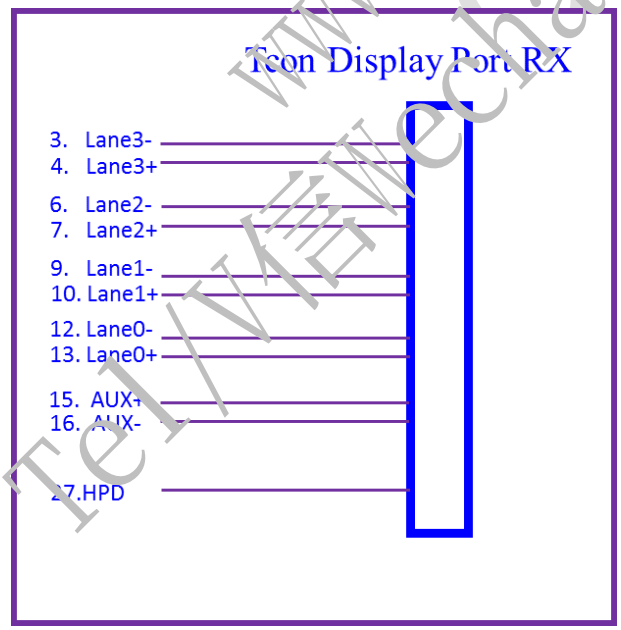
eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN No	Symbol	Function
1	SCL	Nvidia DDS, I2C (SCL)
2	H_GND	High Speed Ground
3	Lane3_N	Comp Signal Lane3
4	Lane3_P	True Signal Link Lane 3
5	H_GND	High Speed Ground
6	Lane2_N	Comp Signal Link Lane 2
7	Lane2_P	True Signal Link Lane 2
8	H_GND	High Speed Ground
9	Lane1_N	Comp Signal Lane 1
10	Lane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12	Lane0_N	Comp Signal Link Lane 0
13	Lane0_P	True Signal Link Lane 0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Ch.
16	AUX_CH_N	Comp Signal Auxiliary Ch.
17	H_GND	High Speed Ground
18	LCD_VCC	LCD logic and driver power

19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	LCD_Self_Test or NC	LCD Panel Self Test Enable (Optional)
23	LCD GND	LCD logic and driver ground
24	LCD GND	LCD logic and driver ground
25	LCD GND	LCD logic and driver ground
26	LCD GND	LCD logic and driver ground
27	HPD	HPD signal pin
28	BL_GND	Backlight_ground
29	BL_GND	Backlight_ground
30	BL_GND	Backlight_ground
31	BL_GND	Backlight_ground
32	BL_Enable	Backlight On / Off
33	BL PWM DIM	System PWM signal Input
34	SDA	Nvidia DDS, I2C (SDA)
35	NC	NC
36	BL_PWR	Backlight power (6V~21V)
37	BL_PWR	Backlight power (6V~21V)
38	BL_PWR	Backlight power (6V~21V)
39	BL_PWR	Backlight power (6V~21V)
40	OD_EN	OD function (Enable @ default/High, Disable@Low)



Note1: Start from right side.
Note2: Input signals shall be low or High-impedance state when VDD is off.
Internal circuit of **eDP inputs** are as following.



6.3 Interface Timing

6.3.1 Timing Characteristics

Basically, interface timings should match the 1920x1080 / 360Hz manufacturing guide line timing.

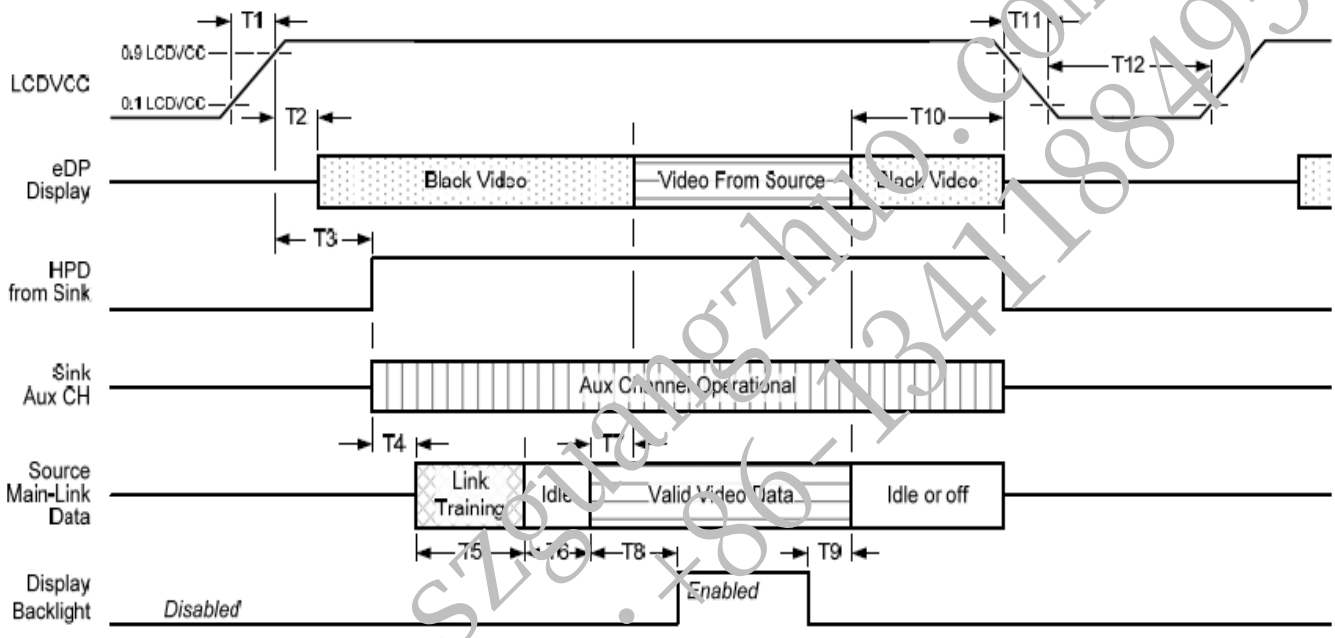
Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	60	360	360	Hz
Clock frequency		1/ T_{Clock}		800		MHz
Vertical Section	Period	T_V		1111		T_{Line}
	Active	T_{VD}		1080		
	Blanking	T_{VB}		31		
Horizontal Section	Period	T_H		2000		T_{Clock}
	Active	T_{HD}		1920		
	Blanking	T_{HB}		80		

Note 1 : The above is as optimized setting

6.4 Power ON/OFF Sequence

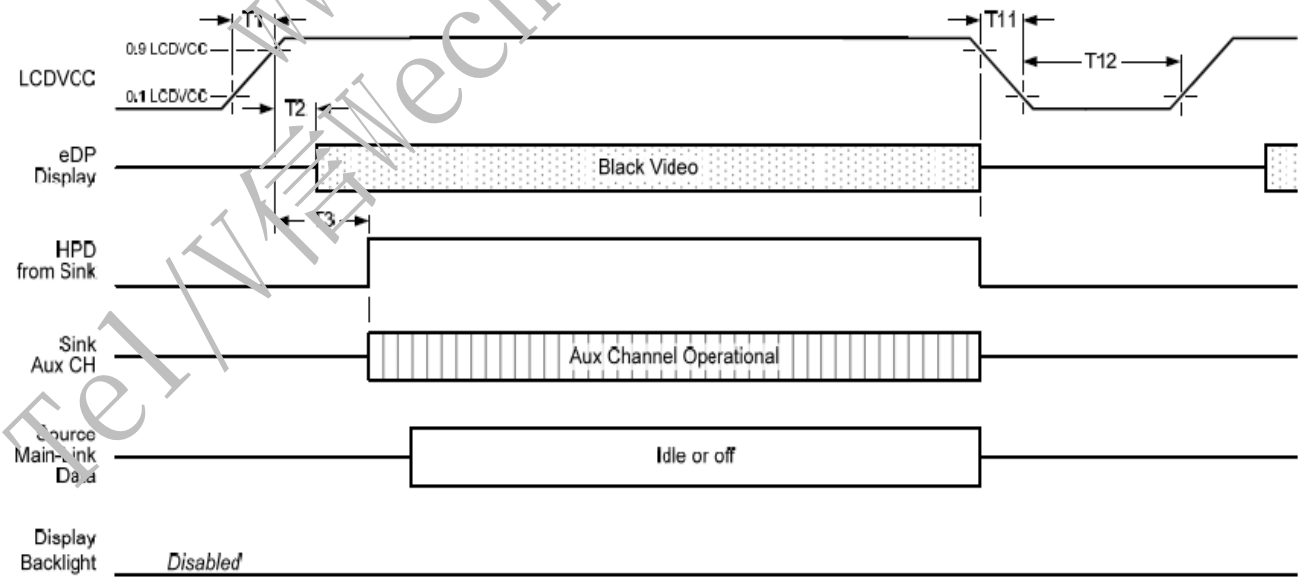
Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port Panel Power Sequence Timing Parameters

Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	50ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

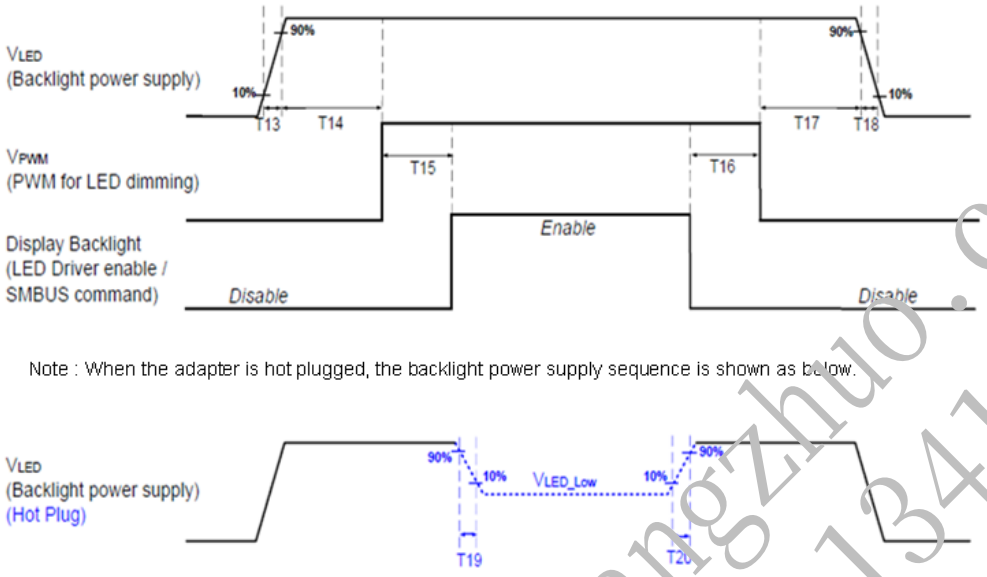
Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Note 4:T8>T7

Display Port panel B/L power sequence timing parameter:



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM}= 1/PWM Frequency

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 35%RH, 300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 300h	
Thermal Shock Test	Ta=-20℃ to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

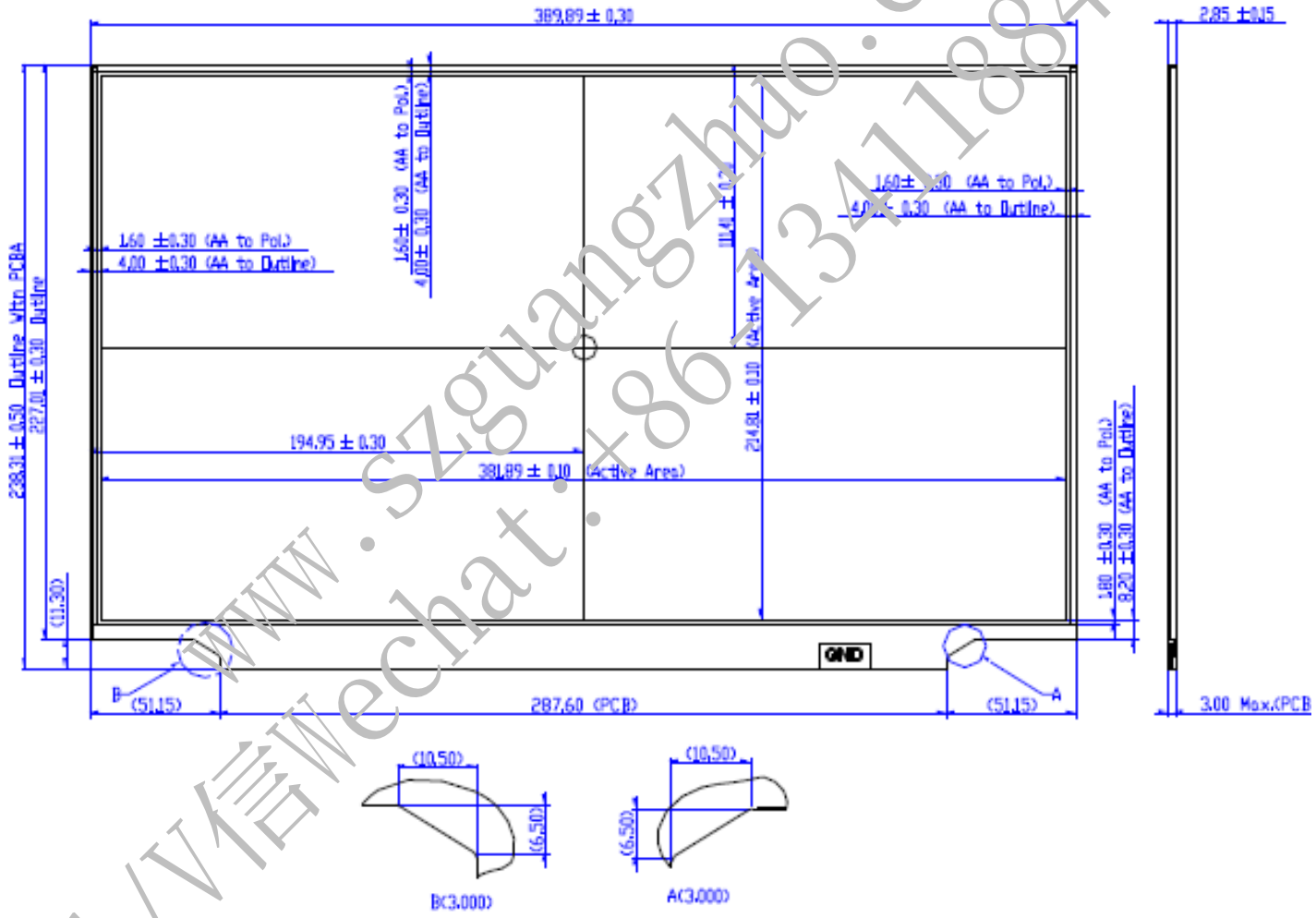
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

. Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

8.1 LCM Outline Dimension



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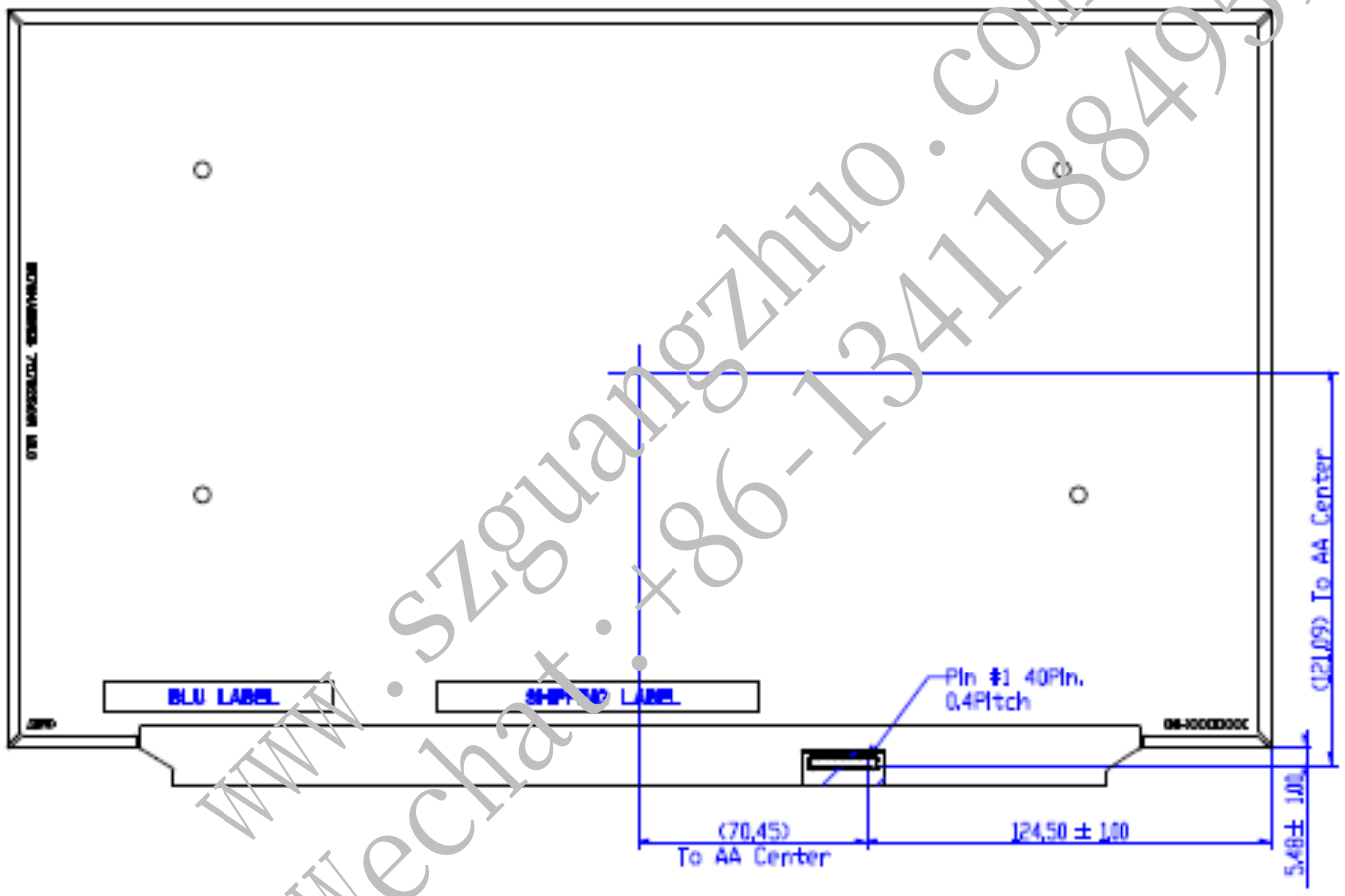
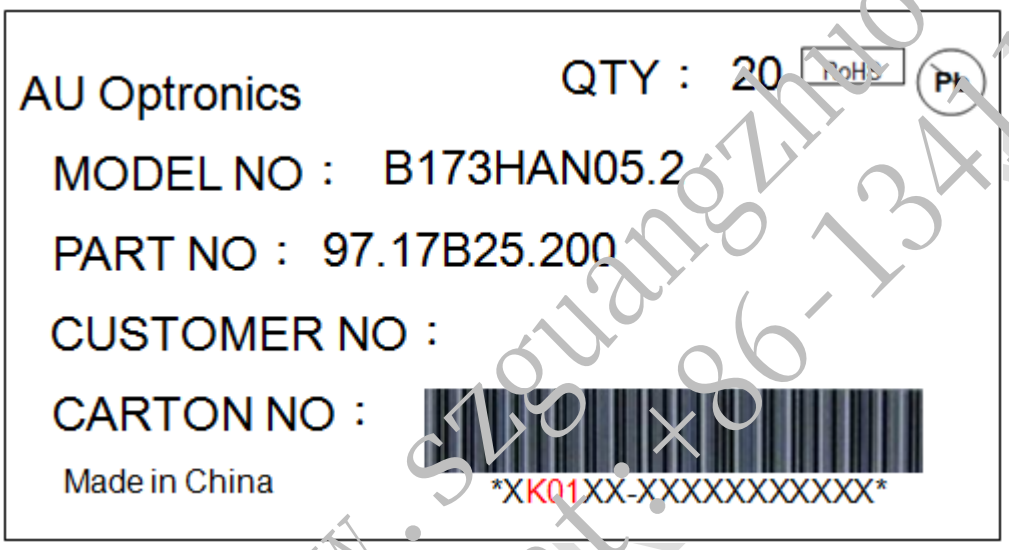


Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

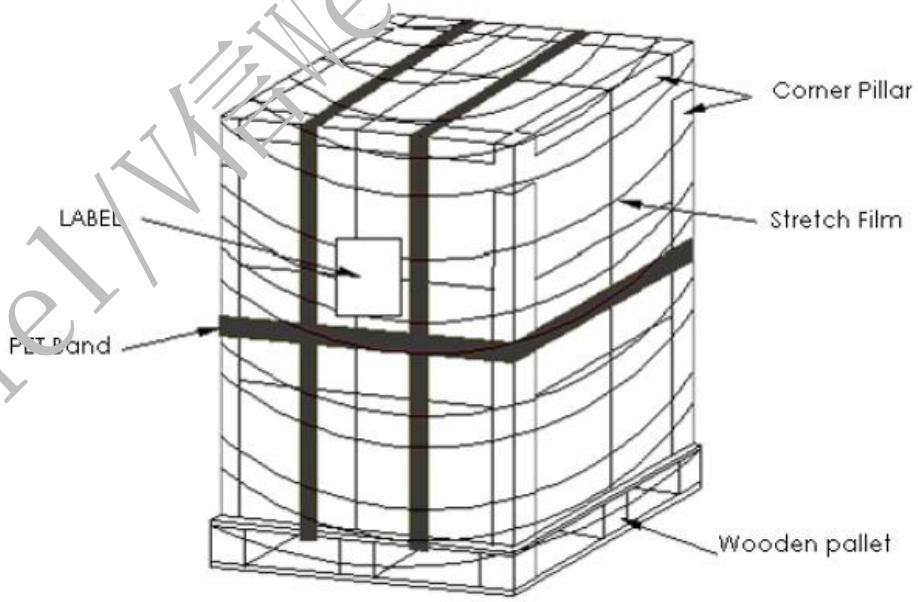
9. Shipping and Package

9.1 Shipping Label Format

9.2 Carton Package



9.3 Shipping Package of Palletizing Sequence



10. Appendix:

10.1 EDID Description

	Byte (hex)	Field Name and Comments	Value (hex)
Header	0	Header	00
	1	Header	FF
	2	Header	FF
	3	Header	FF
	4	Header	FF
	5	Header	FF
	6	Header	FF
	7	Header	00
Vendor / Product EDID Version	8	EISA manufacture code = 3 Character ID	06
	9	EISA manufacture code (Compressed ASCII)	AF
	0A	Panel Supplier Reserved – Product Code	90
	0B	Panel Supplier Reserved – Product Code	BD
	0C	LCD module Serial No - Preferred but Optional (“0” if not used)	00
	0D	LCD module Serial No - Preferred but Optional (“0” if not used)	00
	0E	LCD module Serial No - Preferred but Optional (“0” if not used)	00
	0F	LCD module Serial No - Preferred but Optional (“0” if not used)	00
	10	Week of manufacture	11
	11	Year of manufacture	1F
	12	EDID structure version # = 1	01
	13	EDID revision # = 4	04
Display Parameters	14	Video I/P definition	A5
	15	Max H image size = ?? cm (Rounded to cm)	26
	16	Max V image size = ?? cm (Rounded to cm)	16
	17	Display gamma = (gamma ×100)-100 = Example: (2.2×100) – 100 = 120	78
	18	Feature support	03
Panel Color Coordinates	19	Red/Green Low bit (RxRy/GxGy)	1A
	1A	Blue/White Low bit (BxBy/WxWy)	B5
	1B	Red X Rx = 0.???	A8
	1C	Red Y Ry = 0.???	54
	1D	Green X Rx = 0.???	46
	1E	Green Y Ry = 0.???	9D
	1F	Blue X Rx = 0.???	25
	20	Blue Y Ry = 0.???	0D
	21	White X Rx = 0.???	50
	22	White Y Ry = 0.???	54
she d Tim	23	Established timings 1 (00h if not used)	00

	24	Established timings 2 (00h if not used)	00
	25	Manufacturer's timings (00h if not used)	00
Standard Timing ID	26	Standard timing ID1 (01h if not used)	01
	27	Standard timing ID1 (01h if not used)	01
	28	Standard timing ID2 (01h if not used)	01
	29	Standard timing ID2 (01h if not used)	01
	2A	Standard timing ID3 (01h if not used)	01
	2B	Standard timing ID3 (01h if not used)	01
	2C	Standard timing ID4 (01h if not used)	01
	2D	Standard timing ID4 (01h if not used)	01
	2E	Standard timing ID5 (01h if not used)	01
	2F	Standard timing ID5 (01h if not used)	01
	30	Standard timing ID6 (01h if not used)	01
	31	Standard timing ID6 (01h if not used)	01
	32	Standard timing ID7 (01h if not used)	01
	33	Standard timing ID7 (01h if not used)	01
	34	Standard timing ID8 (01h if not used)	01
	35	Standard timing ID8 (01h if not used)	01
Timing Descripter #1	36	Pixel Clock/10,000 (LSB)	50
	37	Pixel Clock/10,000 (MSB)	D0
	38	Horizontal Active = ???? pixels (lower 8 bits)	80
	39	Horizontal Blanking (Thbp) = 320 pixels (lower 8 bits)	50
	3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	70
	3B	Vertical Active = ??? lines	38
	3C	Vertical Blanking (Tvbp) = ?? lines (DE Blanking typ. for DE only panels)	20
	3D	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	4D
	3E	Horizontal Sync. Offset (Thfp) = ?? pixels	30
	3F	Horizontal Sync. Pulse Width = ??? pixels	20
	40	Vertical Sync. Offset (Tvfp) = ? lines Sync Width = ? lines	A5
	41	Horizontal Vertical Sync Offset/Width upper 2 bits	00
	42	Horizontal Image Size = ??? mm	7E
	43	Vertical image Size = ??? mm	D7
	44	Horizontal Image Size / Vertical image size	10
	45	Horizontal Border = 0 (Zero for Notebook LCD)	00
	46	Vertical Border = 0 (Zero for Notebook LCD)	00

	47	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3 ==> fix=1A	1A
Timing Descripter #2 (=Timing Descripter #1)	48	Pixel Clock/10,000 (LSB)	00
	49	Pixel Clock/10,000 (MSB)	00
	4A	Horizontal Active = xxxx pixels (lower 8 bits)	00
	4B	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)	FD
	4C	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	0E
	4D	Vertical Active = xxxx lines	3C
	4E	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels)	69
	4F	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	91
	50	Horizontal Sync, Offset (Thfp) = xxxx pixels	91
	51	Horizontal Sync, Pulse Width = xxxx pixels	50
	52	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	01
	53	Horizontal Vertical Sync Offset/Width upper 2 bits	0A
	54	Horizontal Image Size = xxx mm	20
	55	Vertical image Size = xxx mm	20
	56	Horizontal Image Size / Vertical image size	20
	57	Horizontal Border = 0 (Zero for Notebook LCD)	20
	58	Vertical Border = 0 (Zero for Notebook LCD)	20
	59	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3 ==> fix=1A	20
Timing Descripter #3 Dell specific information	5A	Flag	00
	5B	Flag	00
	5C	Flag	00
	5D	Data Type Tag: Alphanumeric Data String (ASCII) ==> fix=FE	FE
	5E	Flag	00
	5F	Dell P/N 1st Character	54
	60	Dell P/N 2nd Character	4E
	61	Dell P/N 3rd Character	43
	62	Dell P/N 4th Character	48
	63	Dell P/N 5th Character	48

	64	**EDID Revision** **Bit[6:0] See charts below** **Bit[7] 0: X-rev, 1: A-rev**	80
	65	Manufacturer P/N	42
	66	Manufacturer P/N	31
	67	Manufacturer P/N	37
	68	Manufacturer P/N	33
	69	Manufacturer P/N	43
	6A	Manufacturer P/N	41
	6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	4E
Timing Descripter #4	6C	Flag	00
	6D	Flag	00
	6E	Flag	00
	6F	Data Type Tag: Manufacturer Specified Data 00 ==>fix=00	00
	70	Flag	00
	71	Color Management	02
	72	Panel Structure	41
	73	Frame Rate	0F
	74	Light Controller Interface and Luminance	9E
	75	Outdoor Features	00
	76	Multi-Media Features	01
	77	Multi-Media Features	00
	78	Special Features #1	00
	79	Special Features #2	0F
	7A	Special Features #3	01
	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A
	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20
	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20
Checksum	7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	01
	7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	86

Extend

Address	FUNCTION	Value
HEX		HEX
80		70
81	Display ID Version	13
82	Block Size	79
83		00
84		00
85	Type I timing	03
86	Revision '1'	01
87	Number of Payload Bytes in Block	14
88	Pixel clock	80
89	Pixel clock	38
8A	Pixel clock	01
8B	Preferred timing	84
8C	H-AA	7F
8D	H-AA	07
8E	H-BK	4F
8F	H-BK	00
90	H-offset	2F
91	H-offset	00
92	H-Sync	1F
93	H-Sync	00
94	V-AA	37
95	V-AA	04
96	V-BK	1E
97	V-BK	00
98	V-offset	09
99	V-offset	00
9A	V-Sync	04
9B	V-Sync	00
9C		00
9D		00
9E		00
9F		00
A0		00
A1		00
A2		00
A3		00

A4		00
A5		00
A6		00
A7		00
A8		00
A9		00
AA		00
AB		00
AC		00
AD		00
AE		00
AF		00
B0		00
B1		00
B2		00
B3		00
B4		00
B5		00
B6		00
B7		00
B8		00
B9		00
BA		00
BB		00
BC		00
BD		00
BE		00
BF		00
C0		00
C1		00
C2		00
C3		00
C4		00
C5		00
C6		00
C7		00
C8		00
C9		00
CA		00

CB		00
CC		00
CD		00
CE		00
CF		00
D0		00
D1		00
D2		00
D3		00
D4		00
D5		00
D6		00
D7		00
D8		00
D9		00
DA		00
DB		00
DC		00
DD		00
DE		00
DF		00
E0		00
E1		00
E2		00
E3		00
E4		00
E5		00
E6		00
E7		00
E8		00
E9		00
EA		00
EB		00
EC		00
ED		00
EE		00
EF		00
F0		00
F1		00

F2		00
F3		00
F4		00
F5		00
F6		00
F7		00
F8		00
F9		00
FA		00
FB		00
FC		00
FD		00
FE	Section Checksum (81~FE)	96
FF	EDID Extension Block Checksum (80~FF)	90

10.2 Notes

DPCD Ver.	sDRRS	DCR	DMRRS	PSR	LRR	MRO	VESA DSC	MSO	Free-Sync	HDR	Dimming
1.3	Off	Off	Off	PSR1 off PSR2 off	NA	Off	Off	Off	On	NA	PWM