



# Product Specification

AU OPTRONICS CORPORATION

- ( ) Preliminary Specifications
- ( V ) Final Specifications

<b>Module</b>	<b>17.3”(17.26”) FHD 16:9 Color TFT-LCD with LED Backlight design</b>
<b>Model Name</b>	B173HAN01.8 (H/W:0A)
<b>Note</b> (  )	<b>LED Backlight with driving circuit design</b>

<b>Customer</b>	<b>Date</b>
<b>Checked &amp; Approved by</b>	<b>Date</b>
Note: This Specification is subject to change without notice.	

<b>Approved by</b>	<b>Date</b>
<u>YW Lee</u>	<u>2019/04/02</u>
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### Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2018/09/07	All	First Edition for Customer		
0.2 2018/12/11	29		EDID update	
0.3 2019/04/02	28,32		Carton package and note update	

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### 1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and ensure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.



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### 2. General Description

B173HAN01.8 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 FHD, 1920(H) x 1080(V) screen and 16.2M colors (RGB 6-bits+FRC data driver) with LED backlight driving circuit. All input signals are eDP(Embedded DisplayPort) interface compatible.

B173HAN01.8 is designed for a display unit of notebook style personal computer and industrial machine.

### 2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition.

Items	Unit	Specifications			
Screen Diagonal	[mm]	17.3"(17.26)			
Active Area	[mm]	381.888 x 214.812			
Pixels H x V		1920 x 3 (RGB) x 1080			
Pixel Pitch	[mm]	0.1939 x 0.1939			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black(AHVA)			
White Luminance (ILED=22mA) (Note: ILED is LED current)	[cd/m <sup>2</sup> ]	300 typ. (5 points average) 255 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Luminance Uniformity		1.53 max. (13 points)			
Contrast Ratio		700 typ			
Response Time	[ms]	25 typ			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	6.1 W Max (Max : Include Logic@ mosaic and Blu power)			
Weight	[Grams]	550g max			
Physical Size	[mm]		Min.	Typ.	Max.
		Length	397.6	398.1	398.6
		Width	250	250.5	251
		Thickness	-	-	4
Electrical Interface		2 Lane eDP 1.2			



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Glass Thickness	[mm]	0.5
Surface Treatment		Glare, Hardness 3H
Support Color		6-bit + FRC
Temperature Range	[°C]	0 to +50
Operating	[°C]	-20 to +60
Storage (Non-Operating)		
RoHS Compliance		RoHS Compliance

## 2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

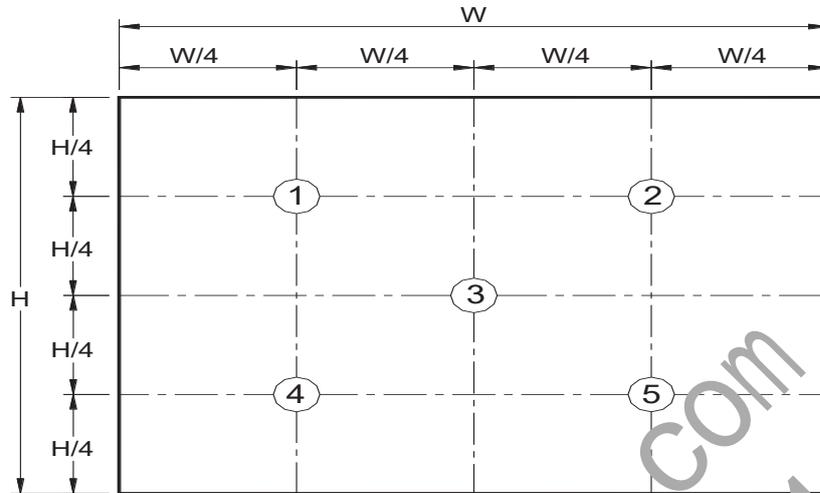
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance ILED=22mA (Base Panel Only)		5 points average	255	300	375	cd/m2	1, 4, 5.
Viewing Angle	θR θL	Horizontal (Right) CR = 10 (Left)	85 85	89 89	- -	degree	4, 9
	ψH ψL	Vertical (Upper) CR = 10 (Lower)	85 85	89 89	- -		
Luminance Uniformity	δ5P	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity	δ13P	13 Points	-	-	1.53		2, 3, 4
Contrast Ratio	CF		-	700	-		4, 6
Cross talk	%				4		4, 7
Response Time	TRT	Rising + Falling	-	25	35		
Color / Chromaticity Coordinates	Red	Rx	0.608	0.638	0.668	CIE 1931	4
		Ry	0.307	0.337	0.367		
	Green	Gx	0.292	0.322	0.352		
		Gy	0.580	0.610	0.640		
	Blue	Bx	0.121	0.151	0.181		
		By	0.018	0.048	0.078		
	White	Wx	0.283	0.313	0.343		
		Wy	0.299	0.329	0.359		
NTSC	%		-	72	-		



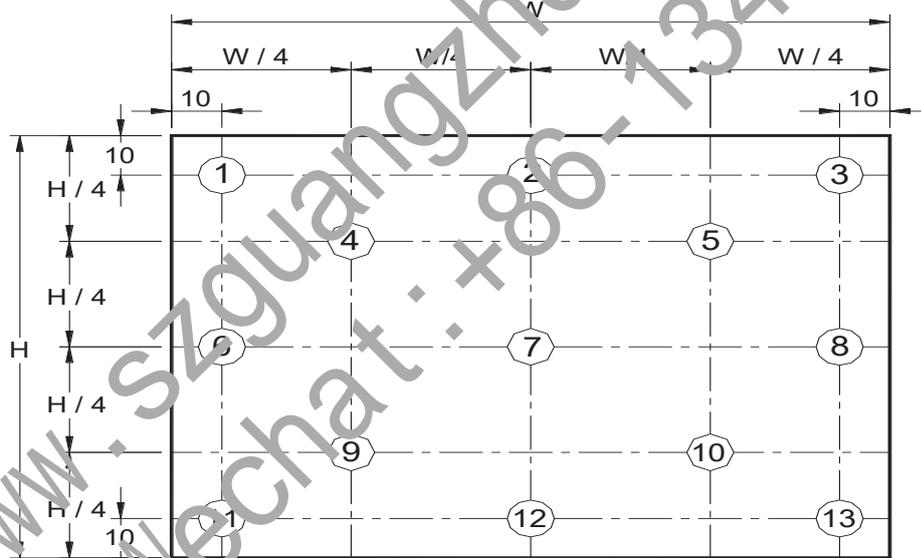
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**Note 1:** 5 points position (Ref: Active area)



**Note 2:** 13 points position (Ref: Active area)



**Note 3:** The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{w5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{w13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

**Note 4:** Measurement method

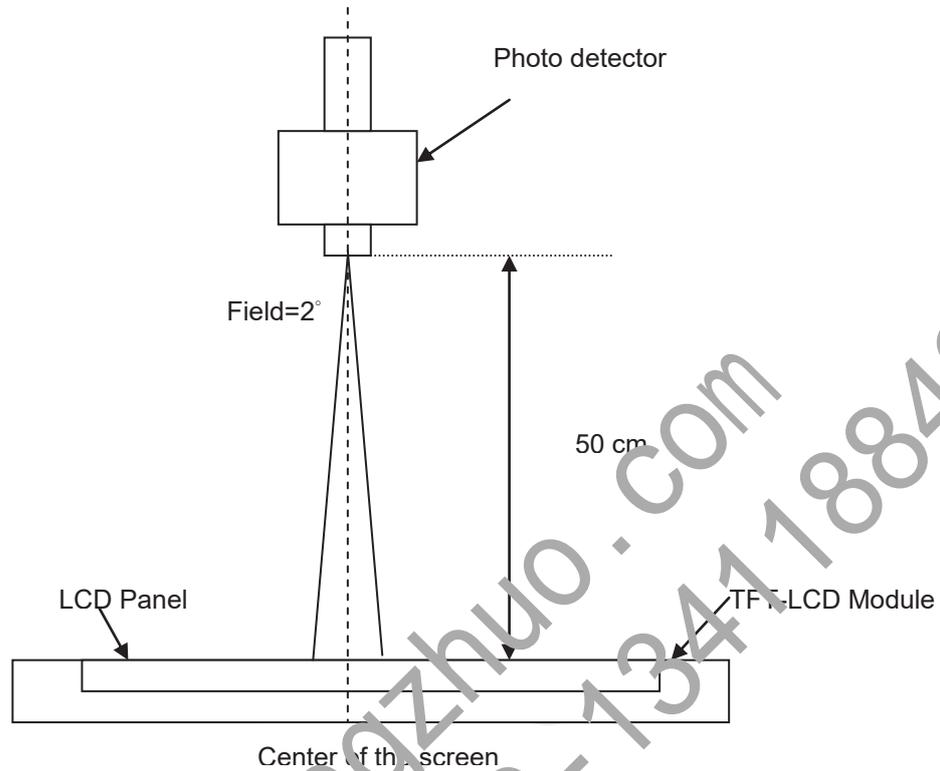
The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting



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Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



**Note 5 :** Definition of Average Luminance of White ( $Y_L$ ):

Measure the luminance of gray level 65 at 5 points ,  $Y_L = [L (1) + L (2) + L (3) + L (4) + L (5)] / 5$

$L (x)$  is corresponding to the luminance of the point X at Figure in Note (1).

**Note 6 :** Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

**Note 7 :** Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

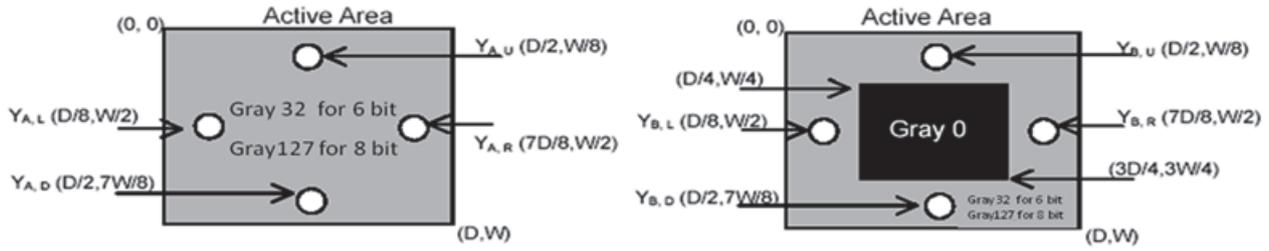
$Y_A$  = Luminance of measured location without gray level 0 pattern (cd/m<sup>2</sup>)

$Y_B$  = Luminance of measured location with gray level 0 pattern (cd/m<sup>2</sup>)



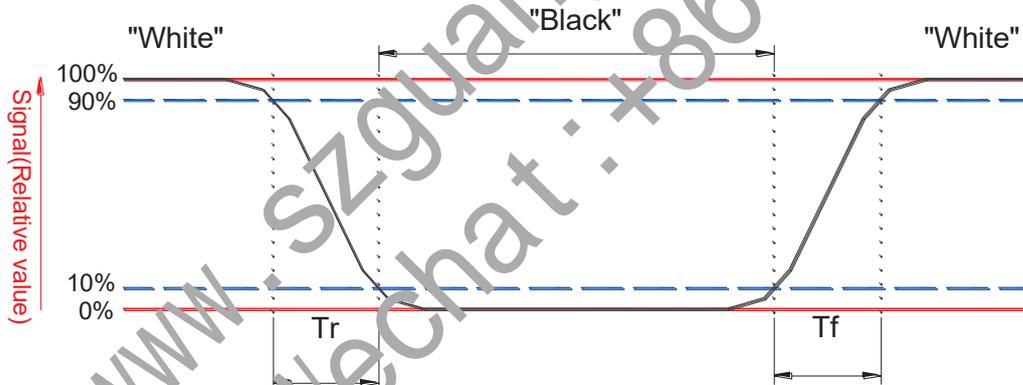
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**Note 8:** Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



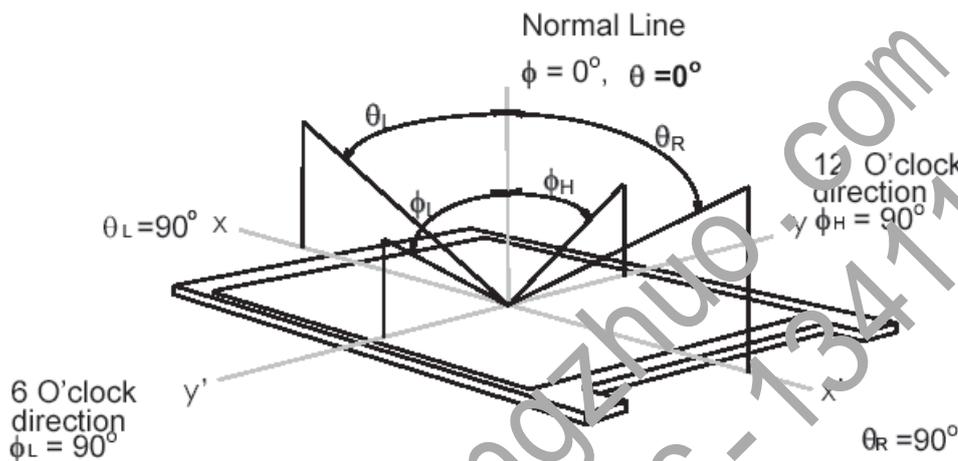


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### Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio  $\geq 10$ , at the screen center, over a  $180^\circ$  horizontal and  $180^\circ$  vertical range (off-normal viewing angles). The  $180^\circ$  viewing angle range is broken down as follows;  $90^\circ$  ( $\theta$ ) horizontal left and right and  $90^\circ$  ( $\Phi$ ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



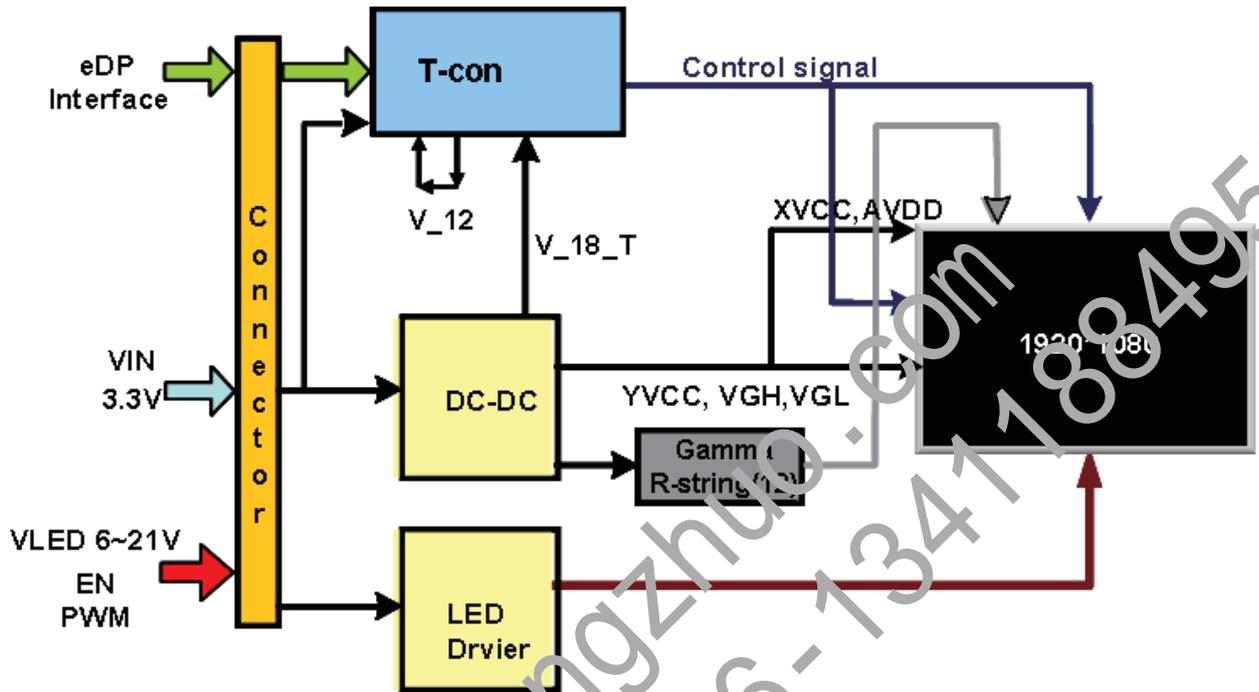


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## 3. Functional Block Diagram

The following diagram shows the functional block of the 17.3 inches wide Color TFT/LCD 30 Pin





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## 4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

### 4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

### 4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

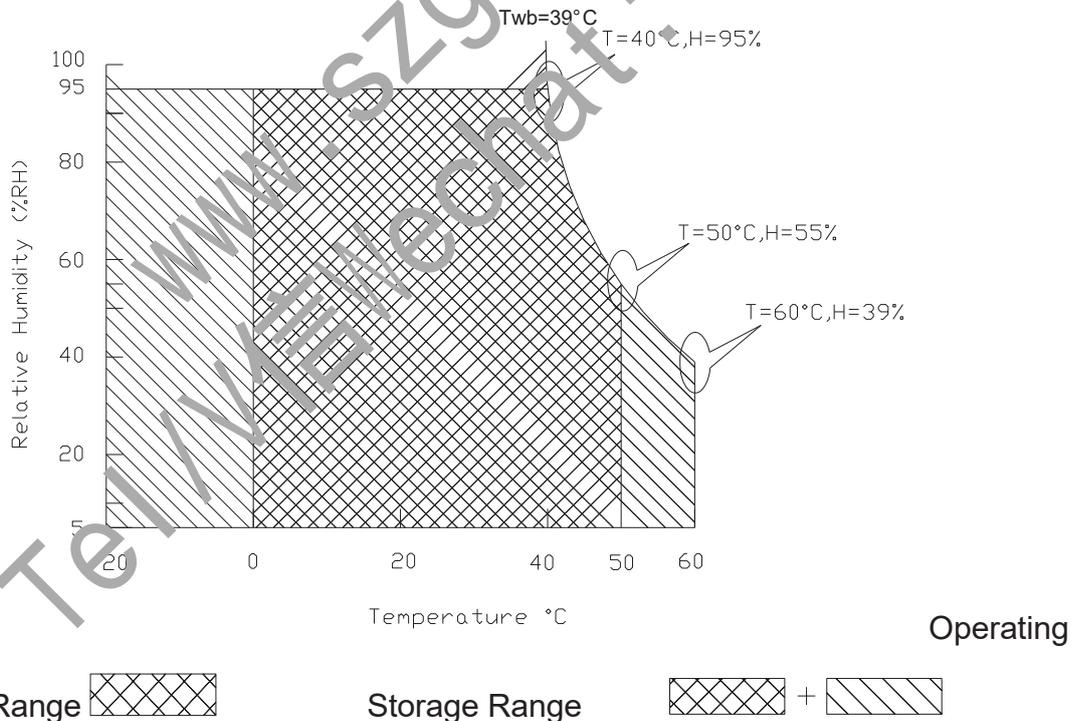
Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).

Note 5: The packing material of system forbid to involve ammonium component

Note 6: The reliability test conditions of system do not exceed the verified conditions of TFT module

Note 7: Be sure the panel test condition do not exceed the component limitation of TFT module(TN Liquid crystal , for example)





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## 5. Electrical Characteristics

### 5.1 TFT LCD Module

#### 5.1.1 Power Specification

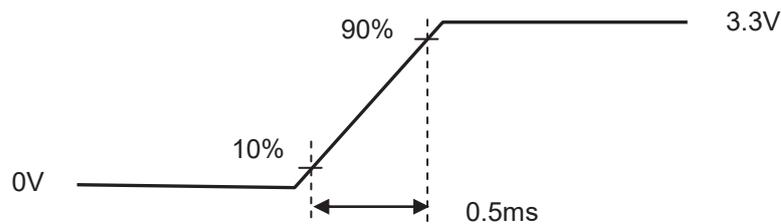
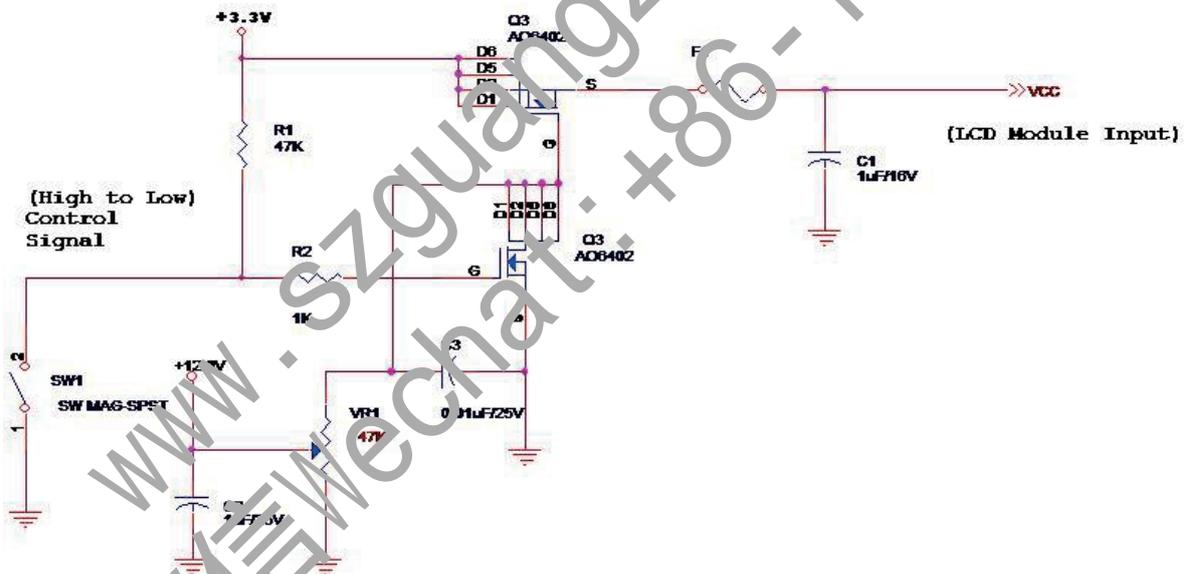
Input power specifications are as follows;

The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1.0	[Watt]	Note 1
IDD	IDD Current(RMS)	-	-	366.7	[mA]	Note 1
IRush	Inrush Current	-	-	1500	[mA]	Note 2
VDDrp	Allowable	-	-	100	[mV]	
Symble	Parameter	Min	Typ	Max	Units	Note

Note 1 : Maximum Measurement Condition : Mosaic pattern (PDD (max) = VDD(min) x IDD(max))

Note 2 : Measure Condition



Vin rising time



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## 5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

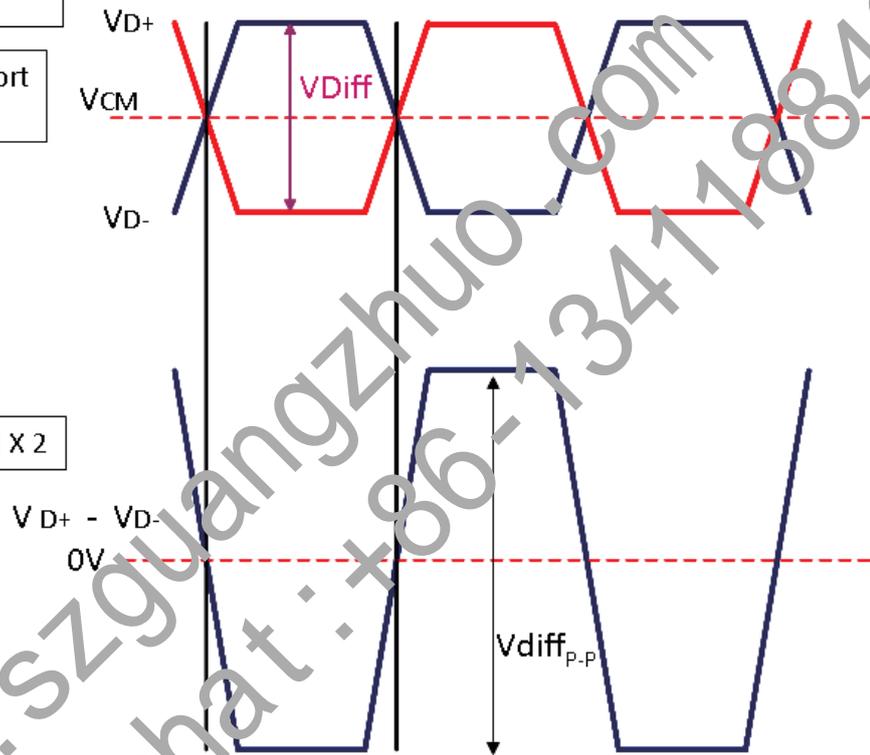
Signal electrical characteristics are as follows;

### Display Port main link signal:

Differential pair VD+ , VD-  
Which is one Display port  
Main link

VCM of Display port  
Main link

$$V_{diff_{P-P}} = [(VD+) - (VD-)] \times 2$$



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
VDiff <sub>P-P</sub>	Peak-to-peak Voltage at a receiving Device	100		1320	mV

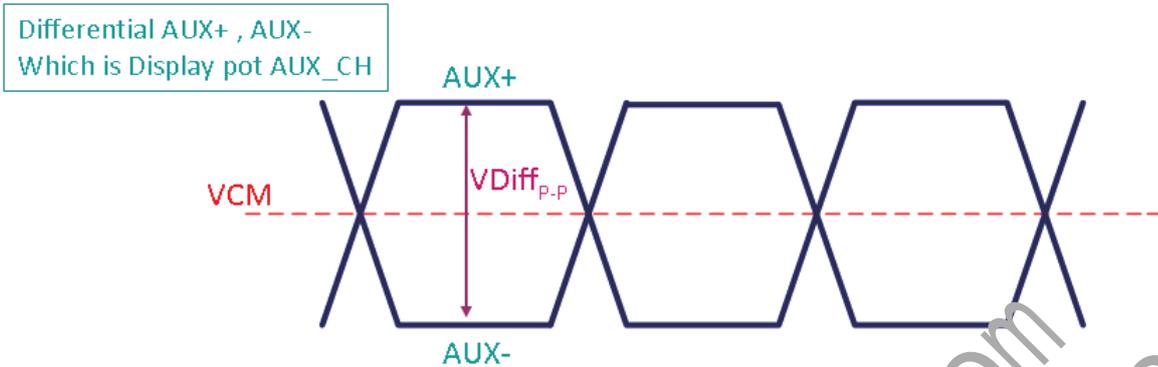
Fallow as VESA display port standard V1.1 a



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## Display Port AUX\_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff <sub>p-p</sub>	AUX Peak-to-peak Voltage at a receiving Device	270		800	mV

Fallow as VESA display port standard V1.1a

## Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25		3.6	V

Fallow as VESA display port standard V1.1a



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### 5.2 Backlight Unit

#### 5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	5.1	[Watt]	(Ta=25 °C), Note 1
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25 °C), Note 2 IF=20 mA

**Note 1:** Calculator value for reference  $P_{LED} = VF$  (Normal Distribution) \*  $IF$  (Normal Distribution) / Efficiency

**Note 2:** The LED life-time define as the estimated time to 50% degradation of initial luminous.

#### 5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	6.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25°C)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

**Note 1 :** Recommend system pull up/down resistor no bigger than 10kohm



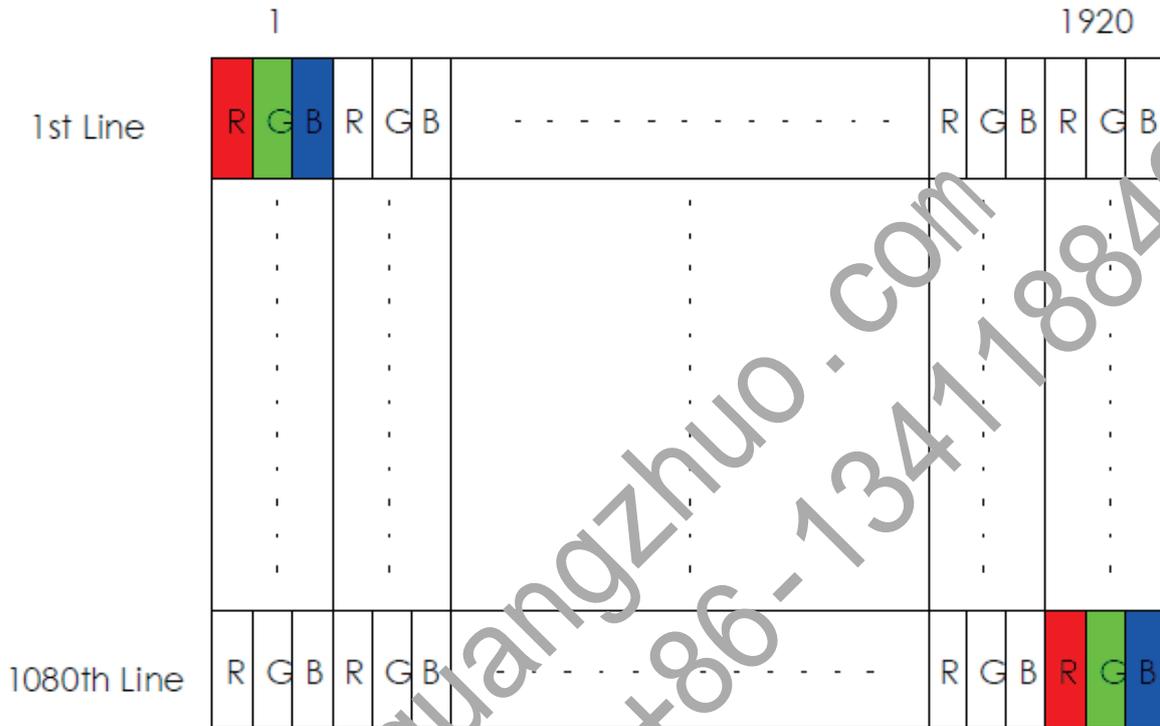
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## 6. Signal Interface Characteristic

### 6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.





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### 6.2 Integration Interface Requirement

#### 6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	<b>SIN SHENG TERMINAL &amp; MACHINE INC.</b>
Type / Part Number	eDP / 20765-030E-11A STM / MSAK24025P30M
Mating Housing/Part Number	IPEX / 20453-030T-01



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### 6.2.2 Pin Assignment ( 2 Lane)

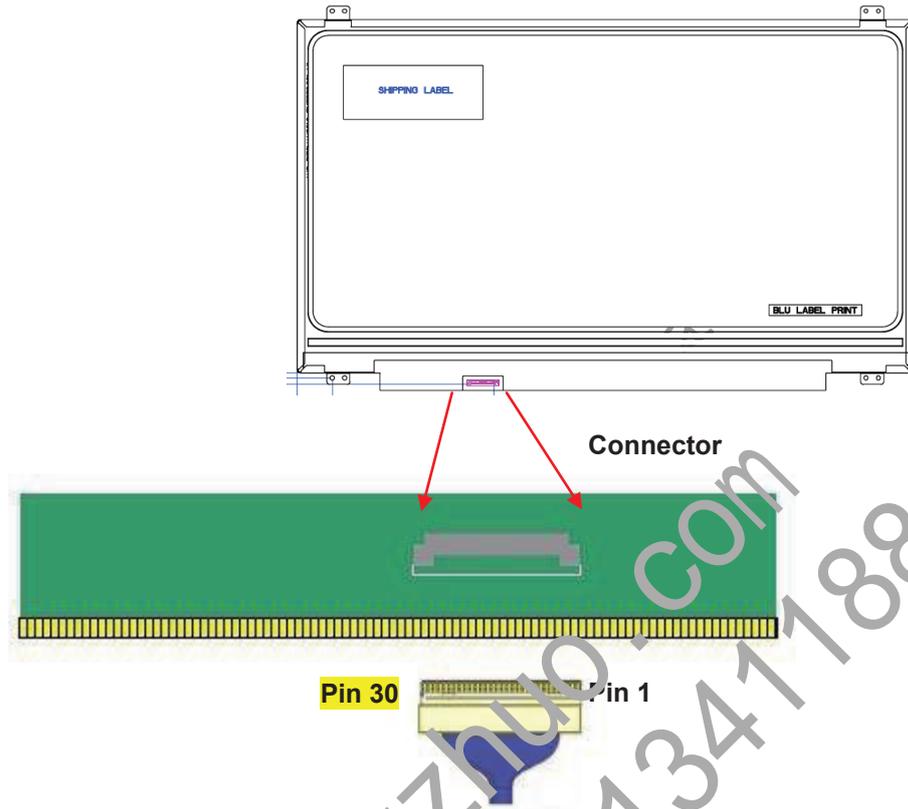
PIN NO	Symbol	Function
1	NC	NC
2	H_GND	High Speed Ground
3	Lane1_N	Complement Signal Link Lane 1
4	Lane1_P	True Signal Link Lane 1
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	LCD_Self_Test	LCD Panel Self Test Enable
15	LCD_GND	LCD logic and driver ground
16	LCD_GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	BL_GND	Backlight_ground
19	BL_GND	Backlight_ground
20	BL_GND	Backlight_ground
21	BL_GND	Backlight_ground
22	BL_Enable	Backlight On / Off
23	BL_PWM_DIM	System PWM signal Input
24	NC	NC
25	NC	NC
26	BL_PWR	Backlight power (6V~21V)
27	BL_PWR	Backlight power (6V~21V)
28	BL_PWR	Backlight power (6V~21V)
29	BL_PWR	Backlight power (6V~21V)
30		NC

**eDP lane** is a differential signal technology for LCD interface and high speed data transfer device.



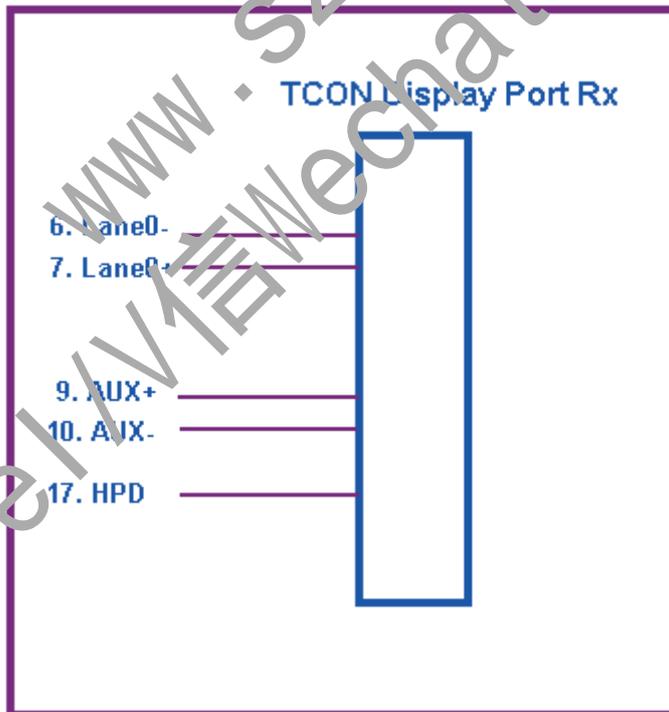
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**Note1:** Start from right side.

**Note2:** Input signals shall be low or High-impedance state when VDD is off.  
Internal circuit of **eDP inputs** are as following.





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## 6.3 Interface Timing

### 6.3.1 Timing Characteristics

For normal display, interface timings should match the 1920\*1080 /60Hz manufacturing guide line timing.

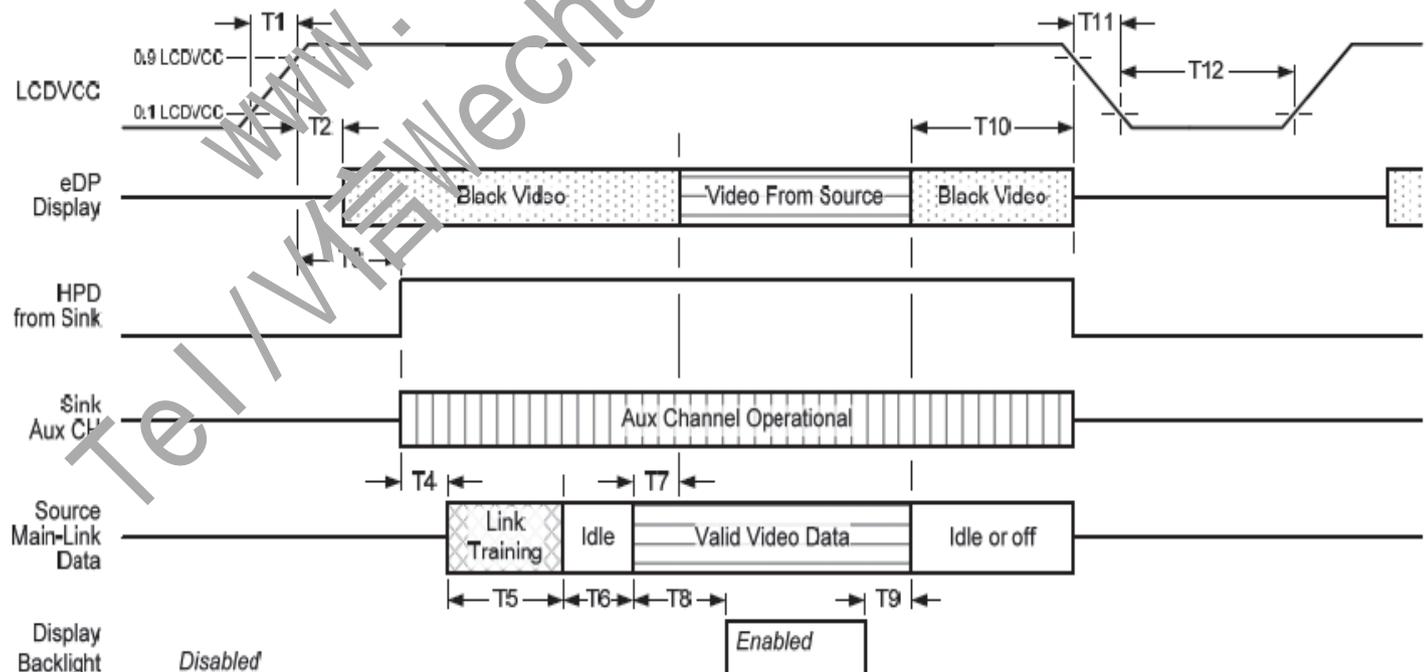
Parameter	Symbol	Min.	Typ.	Max.	Unit	
Frame Rate	-	-	60	-	Hz	
Clock frequency	1/ T <sub>Clock</sub>		143.6		MHz	
Vertical Section	Period	T <sub>V</sub>	1088	1116	1080+A	
	Active	T <sub>VD</sub>	1080			T <sub>Line</sub>
	Blanking	T <sub>VB</sub>	8	36	A	
Horizontal Section	Period	T <sub>H</sub>	2072	2140	1920+B	
	Active	T <sub>HD</sub>	1920			T <sub>Clock</sub>
	Blanking	T <sub>HB</sub>	152	220	B	

Note 1 : The above is as optimized setting

Note 2 : The maximum clock frequency = (1920+B)\*(1080+A)\*60 < 160 MHz

## 6.4 Power ON/OFF Sequence

Display Port panel power sequence:



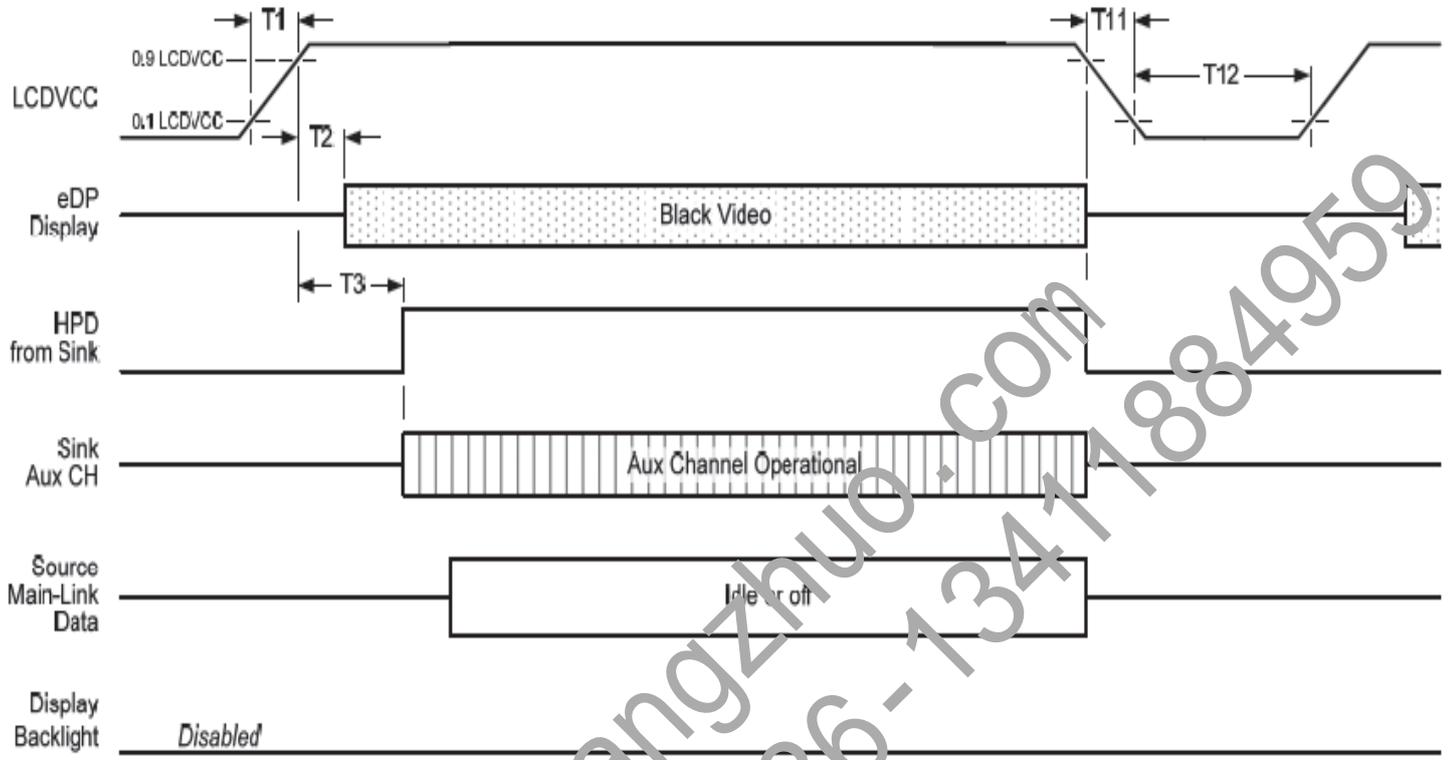


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## Display port interface power up/down sequence, normal system operation

### Display Port AUX\_CH transaction only:



### Display port interface power up/down sequence, AUX\_CH transaction only

### Display Port panel power sequence timing parameter:



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Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allow sink to update video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	50ms		50ms	
T11	power rail fall time, 90% to 10%	source			10ms	
T12	power off time	source	500ms			

**Note1:** The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:

- upon LCDVDD power on (with in T2 max) when the "Novideostream\_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
- when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

**Note 2:** The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

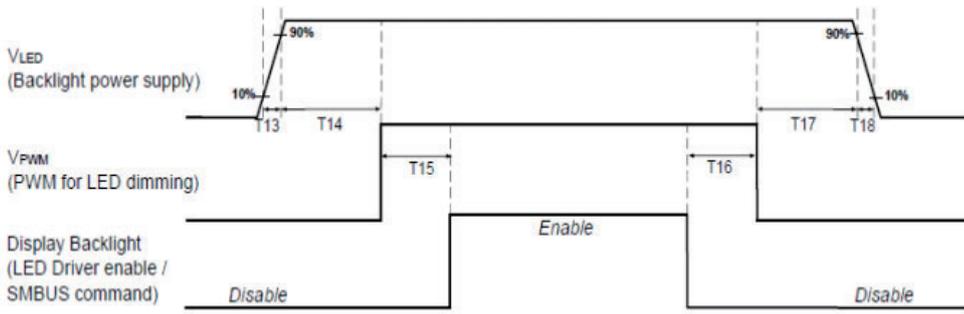
**Note 3:** The sink must support AUX\_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-tr, if the sink is not ready). The sink must be able to respond to an AUX\_CH transaction with the time specified within T3 max.



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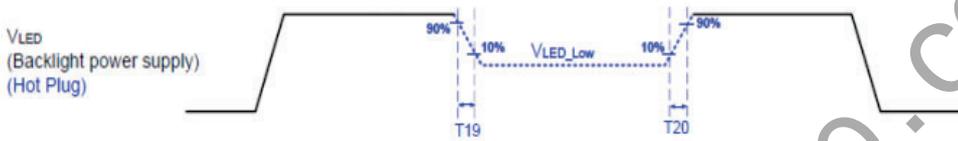
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## Display Port panel B/L power sequence timing parameter:



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	0	-
T16	0	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	-	-

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



Seamless change T19, T20 = 5xT<sub>PWM</sub>\*  
 \*T<sub>PWM</sub> = 1/f<sub>PWM</sub> frequency

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## Product Specification

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### 7. Panel Reliability Test

#### 7.1 Vibration Test

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

#### 7.2 Shock Test

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

#### 7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C, 90%RH, 300h	
High Temperature Operation	Ta= 50°C, Dry, 300h	
Low Temperature Operation	Ta= 0°C, 300h	
High Temperature Storage	Ta= 60°C, 35%RH, 300h	
Low Temperature Storage	Ta= -20°C, 50%RH, 250h	
Thermal Shock Test	Ta=-20°C to 60°C, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

**Note:** According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable.  
No data lost, No hardware failures.

**Remark:** MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

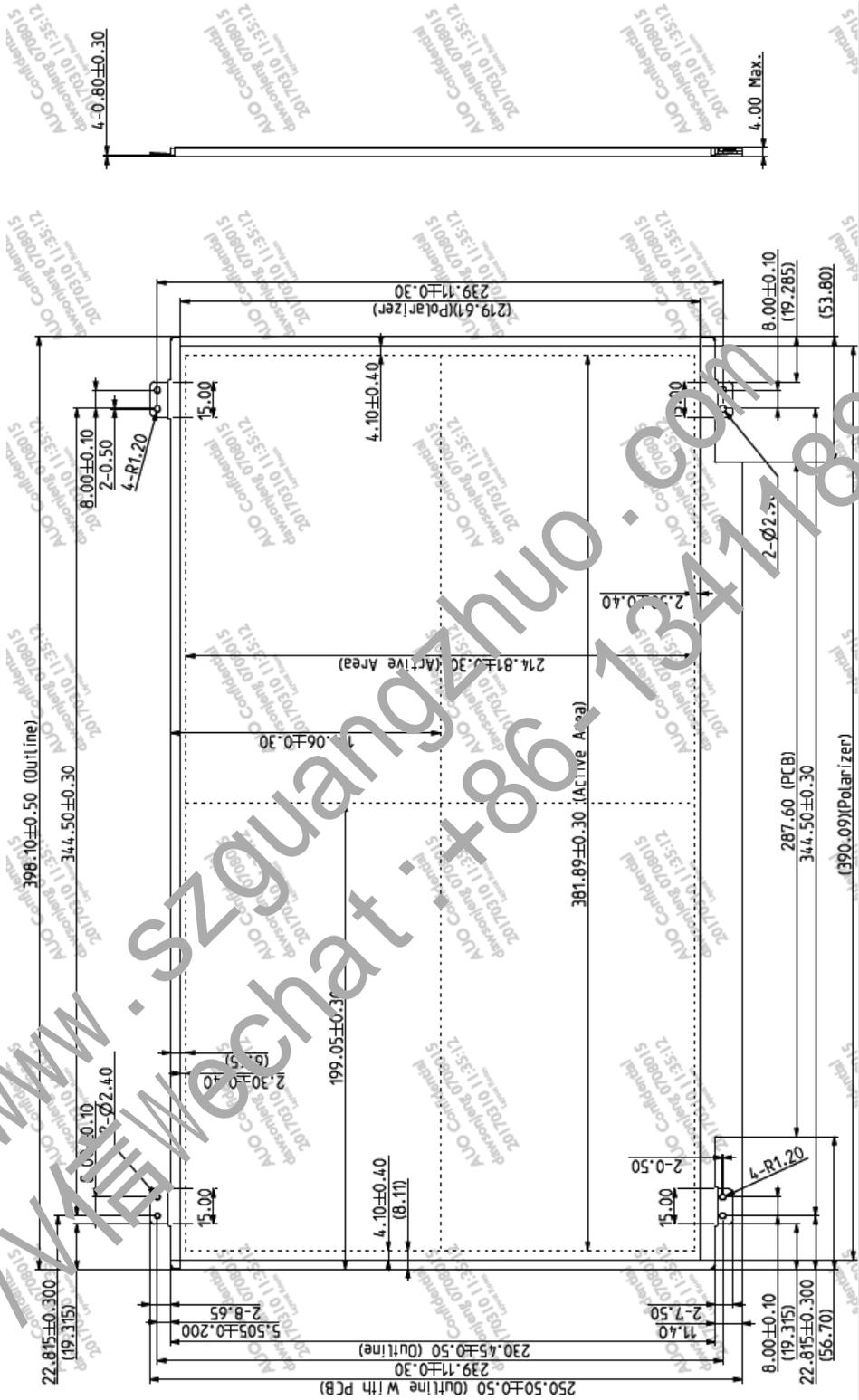


# Product Specification

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## 8. Mechanical Characteristics

### 8.1 LCM Outline Dimension

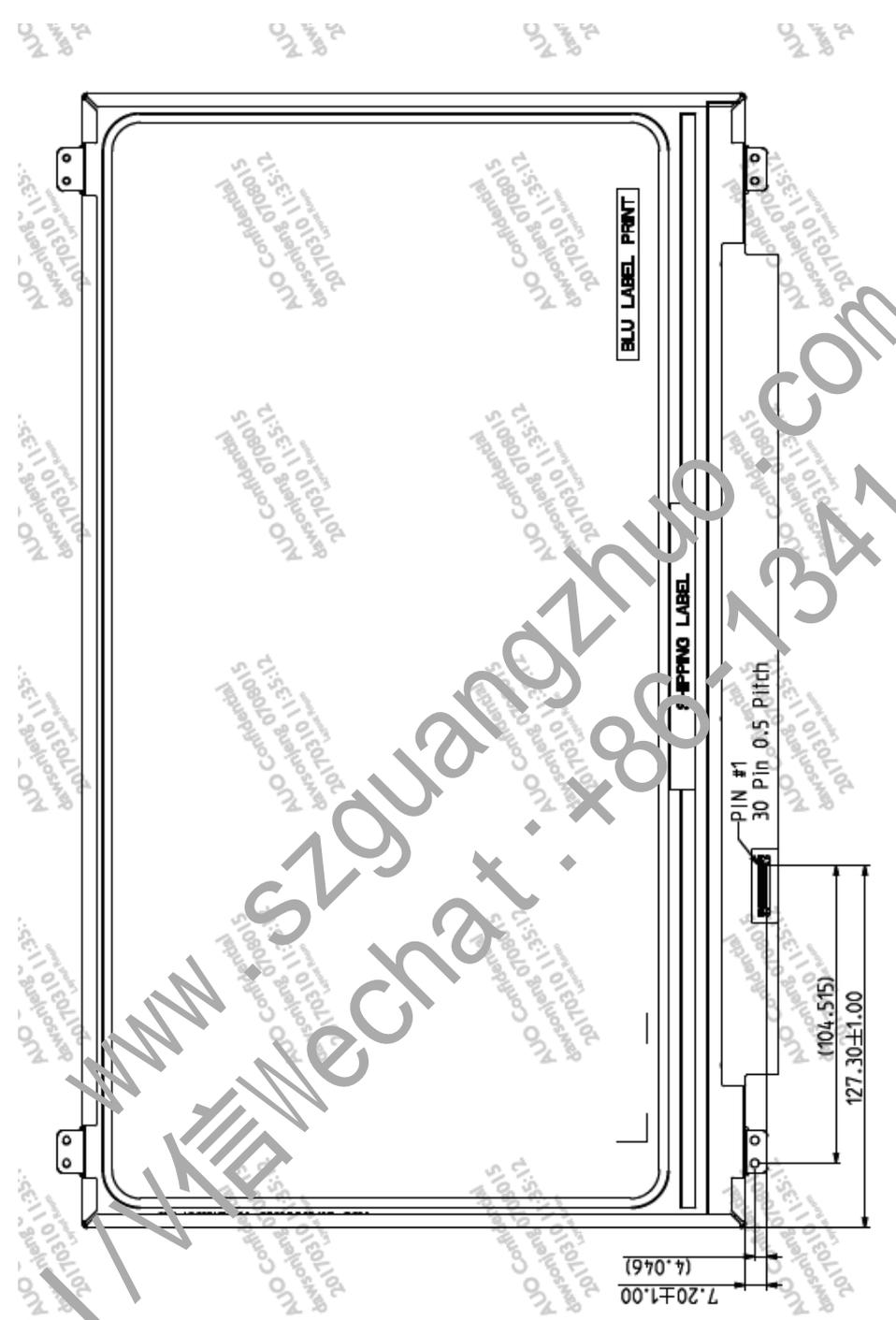


✓ LCD Module's highest portion is the top polarizer and any other LCM material/component is lower than polarizer.



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Note: Prevention IC damage, IC positions not allowed any overlapped in these areas.



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## 9. Shipping and Package

### 9.1 Shipping Label Format

	Manufactured MM/WW Model No: B173HAN01.8 AU Optronics H/W:0A F/W: 1 *XXXXXXXXXXXX-XXXXXX*		c UL US E204356  
		BSSD10T25270A1 RWWYMDXXXX P/NSD10T25270 FRU XXXXXXX MADE IN CHINA(Z40)	

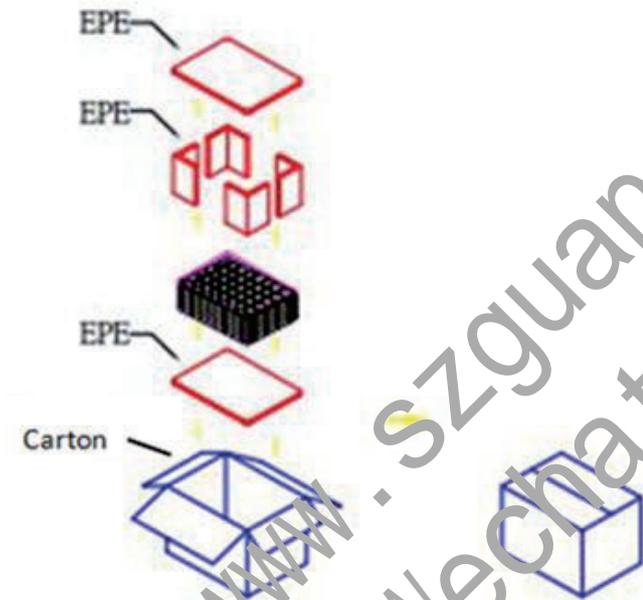
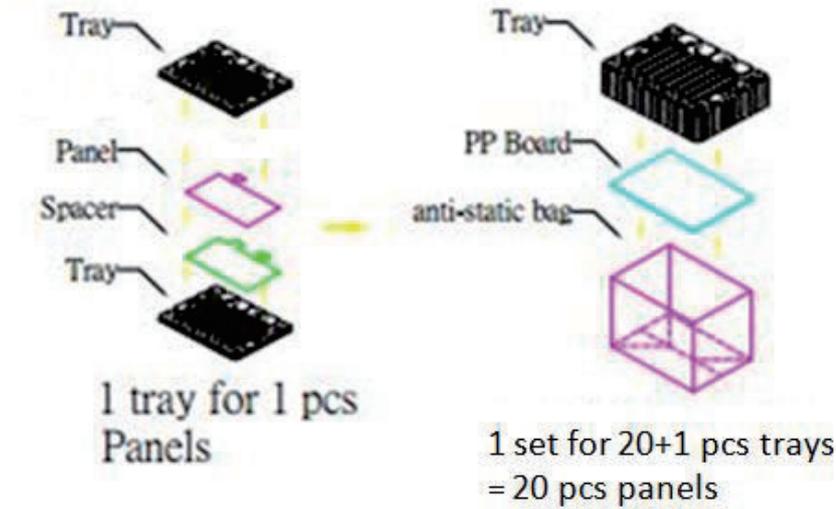
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## Product Specification

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### 9.2 Carton Package



Max capacity : 20 pcs panels per carton

Outside dimension of carton: 516mm\*368mm\*370mm

Pallet size : 1150mm\*1070mm\*132mm

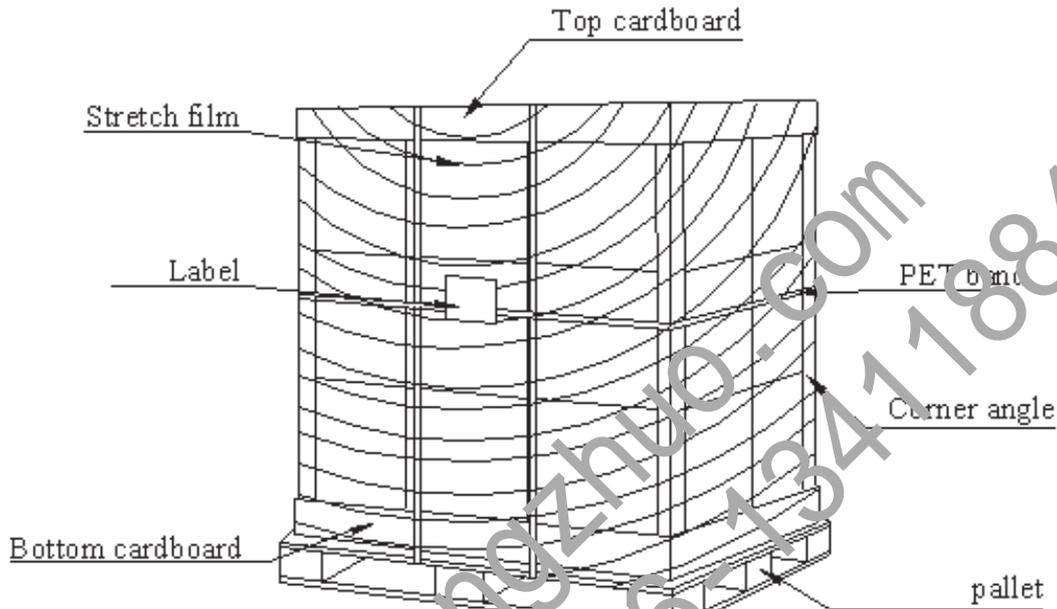
Module by air : (3 \* 2) \* 3 layers, one pallet put 18 boxes, Total 360 pcs .



# Product Specification

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## 9.3 Shipping Package of Palletizing Sequence



## 10. Appendix:

### 10.1 EDID Description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	9D	10011101	157	
0B	hex, LSB first	18	00011000	24	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	00	00000000	0	
11	Year of manufacture	1C	00011100	28	



# Product Specification

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12	EDID Structure Ver.	01	00000001	1
13	EDID revision #	04	00000100	4
14	<b>Video input def.</b> (digital I/P, non-TMDS, CRGB)	A5	10100101	165
15	<b>Max H image size</b> (rounded to cm)	26	00100110	38
16	<b>Max V image size</b> (rounded to cm)	15	00010101	21
17	<b>Display Gamma</b> $(=(\text{gamma} \times 100) - 100)$	78	01111000	120
18	<b>Feature support</b> (no DPMS, Active OFF, RGB, tmg Blk#1)	02	00000010	2
19	Red/green low bits ( <b>Lower 2:2:2:2 bits</b> )	59	01011001	89
1A	Blue/white low bits ( <b>Lower 2:2:2:2 bits</b> )	D5	11010101	213
1B	Red x ( <b>Upper 8 bits</b> )	A3	10100011	163
1C	Red y/ highER 8 bits	56	01010110	86
1D	Green x	52	01010010	82
1E	Green y	9C	10011100	156
1F	Blue x	26	00100110	38
20	Blue y	0C	00001100	12
21	White x	50	01010000	80
22	White y	54	01011000	84
23	Established timing 1	00	00000000	0
24	Established timing 2	00	00000000	0
25	Established timing 3	00	00000000	0
26	Standard timing #1	01	00000001	1
27		01	00000001	1
28	Standard timing #2	01	00000001	1
29		01	00000001	1
2A	Standard timing #3	01	00000001	1
2B		01	00000001	1
2C	Standard timing #4	01	00000001	1
2D		01	00000001	1
2E	Standard timing #5	01	00000001	1
2F		01	00000001	1
30	Standard timing #6	01	00000001	1
31		01	00000001	1
32	Standard timing #7	01	00000001	1
33		01	00000001	1
34	Standard timing #8	01	00000001	1
35		01	00000001	1
36	Pixel Clock/10000 LSB	FA	11111010	250
37	Pixel Clock/10000 USB	37	00110111	55
38	Horz active <b>Lower 8bits</b>	80	10000000	128
39	Horz blanking <b>Lower 8bits</b>	DC	11011100	220
3A	HorzAct:HorzBlk <b>Upper 4:4 bits</b>	70	01110000	112
3B	Vertical Active <b>Lower 8bits</b>	38	00111000	56
3C	Vertical Blanking <b>Lower 8bits</b>	24	00100100	36
3D	Vert Act : Vertical Blanking ( <b>upper 4:4 bit</b> )	40	01000000	64
3E	HorzSync. Offset	10	00010000	16
3F	HorzSync.Width	10	00010000	16



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40	VertSync.Offset : VertSync.Width	3E	00111110	62	
41	Horz&Vert Sync Offset/Width <b>Upper 2bits</b>	00	00000000	0	
42	Horizontal Image Size <b>Lower 8bits</b>	7D	01111101	125	
43	Vertical Image Size <b>Lower 8bits</b>	D6	11010110	214	
44	Horizontal & Vertical Image Size <b>(upper 4:4 bits)</b>	10	00010000	16	
45	Horizontal Border <i>(zero for internal LCD)</i>	00	00000000	0	
46	Vertical Border <i>(zero for internal LCD)</i>	00	00000000	0	
47	Signal <i>(non-intr, norm, no stereo, sep sync, neg pol)</i>	18	00011000	24	
48	Detailed timing/monitor	00	00000000	0	
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		00	00000000	0	
4C		00	00000000	0	
4D		00	00000000	0	
4E		00	00000000	0	
4F		00	00000000	0	
50		00	00000000	0	
51		00	00000000	0	
52		00	00000000	0	
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		1A	00011010	26	
5A	Detailed timing/monitor	00	00000000	0	
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	
6D	descriptor #4	00	00000000	0	



# Product Specification

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6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	42	01000010	66	B
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	37	00110111	55	7
74	Manufacture P/N	33	00110011	51	3
75	Manufacture P/N	48	01001000	72	H
76	Manufacture P/N	41	01000001	65	1
77	Manufacture P/N	4E	01001110	78	N
78	Manufacture P/N	30	00110000	48	0
79	Manufacture P/N	31	00110001	49	1
7A	Manufacture P/N	2E	00101110	46	.
7B	Manufacture P/N	38	00111000	56	8
7C		20	00100000	32	
7D		01	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	EA	11101010	234	

## 10.2 Note

DPCD Ver.	sDRRS	DCR	DMRRS	PSR	MBC	VESA DSC	MSO	Free-Sync	HDR	Dimming
1.1	On	Off	Off	Off	Off	Off	Off	Off	NA	No HDR Global