



Product Specification

AU OPTRONICS CORPORATION

(V) Preliminary Specifications

() Final Specifications

Module	14.0" QHD+(WQXGA)16:10 Color TFT-LCD with LED Backlight design
Model Name	B140QAX01.H
H/W	0A
Note ()	iTP Display

Customer	Date
<u>XXXXXX</u>	<u>MM/DD/YYYY</u>
Checked & Approved by	Date
Note: This Specification is subject to change without notice.	

Approved by	Date
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AU Optronics corporation	



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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2023/03/20	All	First Edition for Customer X20 for new IC LX92515B		



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1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 10) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 11) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC62368-1 or UL62368-1), or be applied exemption.
- 12) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.



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2. General Description

B140QAX01.H is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:10 QHD, 2560(H) x1600(V) screen and 16.7M colors (RGB 8-bits data driver) with LED backlight driving circuit. All input signals are eDP (Embedded DisplayPort) interface compatible.

B140QAX01.H is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[in]	14.0"			
Active Area	[mm]	301.59x188.50			
Pixels H x V		2560x3(RGB) x 2600			
Pixel Pitch	[mm]	0.1178 x 0.1178			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black, LTPS			
White Luminance (ILED=14mA) (Note: ILED is LED current)	[cd/m ²]	400 typ. (5 points average) 340 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		1200 typ			
Response Time	[ms]	30 typ / 35 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	3.75 max. (Include Logic@mosaic 1.15W and Blu power 2.6W)			
Weight	[Grams]	210g (Total solution)			
Total solution [Note: Touch module]	[mm]		Min.	Typ.	Max.
		Length	306.29	306.59	306.89
		Width	198.10	198.40	198.90
		Thicknes	2.0 (Panel Side) 4.0 (PCBA Side)		



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Electrical Interface		2 Lane eDP1.4
Glass Thickness	[mm]	0.2
Surface Treatment		Anti Glare, Hardness 3H
Support Color		16.7M colors (RGB 8-bit)
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance



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2.2 General Touch Specification

Item	Spec	Unit
Type of Touch Sensor	Projective Capacitive	
Panel Size	14.0'	
Outline Dimension	306.59x198.396typ	mm
Total Thickness	2.0 typ	mm
Total Weight	210g max	g
TP View Area	301.594x188.496 typ	mm
TP Active Area	301.594x188.496 typ	mm
Interface	HID-I2C	
Report Rate	Follow win10 –120Hz	Hz
Multi-Touch Point	10 points	
Input method	Finger	
Touch panel sensor IC	LXsemicon LX92515A	
Channel	63x 42	
Surface hardness	3 (Note 1)	H
Surface treatment	Anti-Glare	
TP F/W version	00.04	
Support OS	Window 10	

Note1: Polarizer Test condition: Working speed: 50cycle/min Moves distance: 100mm/sec (Exceptions to the rubber tip of the diameter is 6mm) • Measuring Process: The Load force and the friction material are fixed on 25mm diameter cylinder tooling. Polarizer pasted on bare glass and the start to test. • Inspect on the 500/1000/1500/2000 cycles.



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2.3 Optical Characteristics

The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

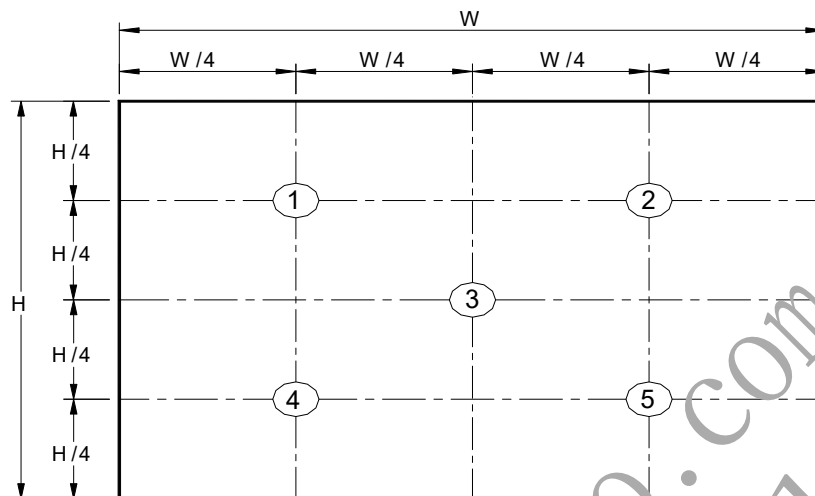
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance ILED=14mA (Base Panel Only)	Y _L	5 points average	340	400	-	cd/m ²	1, 4, 5.
Viewing Angle	θ_R	Horizontal (Right) CR = 10 (Left)	80	85	-	degree	1, 9
	θ_L		80	85	-		
	ϕ_H	Vertical (Upper) CR = 10 (Lower)	80	85	-		
	ϕ_L		80	85	-		
Luminance Uniformity	$\delta 5P$	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity	$\delta 13P$	13 Points	-	-	1.54		2, 3, 4
Contrast Ratio	CR		1000	1200	-		4, 6
Cross talk	%				4		4, 7
Response Time	TRT	Rising + Falling	-	30	35		
Color / Chromaticity Coordinates	Red	R _x	0.628	0.658	0.688	-	4
		R _y	0.300	0.330	0.360		
	Green	G _x	0.250	0.280	0.310		
		G _y	0.580	0.610	0.640		
	Blue	B _x	0.114	0.144	0.174		
		B _y	0.028	0.058	0.088		
	White	W _x	0.283	0.313	0.343		
		W _y	0.299	0.329	0.359		
	Color gamut sRGB	%	95	100	-		
Low Blue Light	K	CCT	5500	-	7000		
	%	TUV	TUV method 2				10
Gamma Value	-		1.7	2.2	2.7		



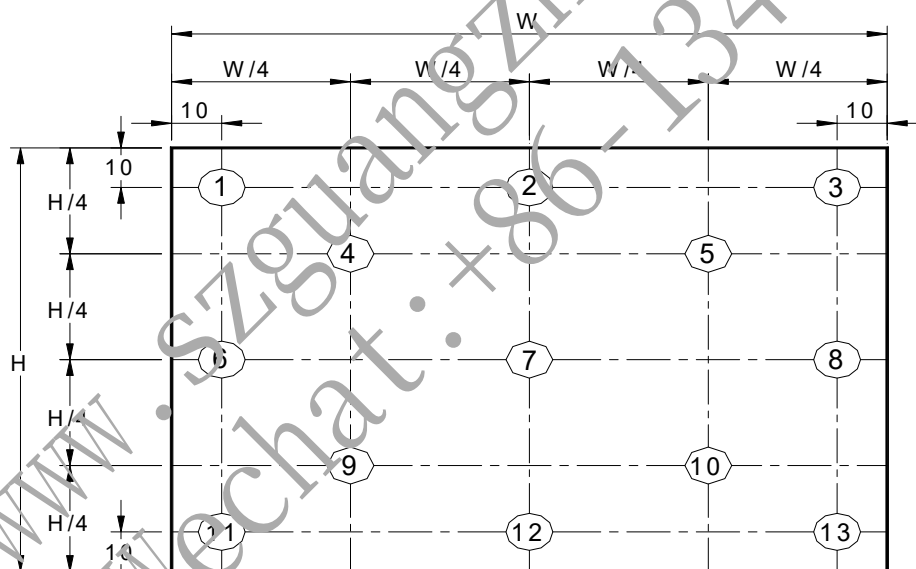
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Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{w5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{w13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

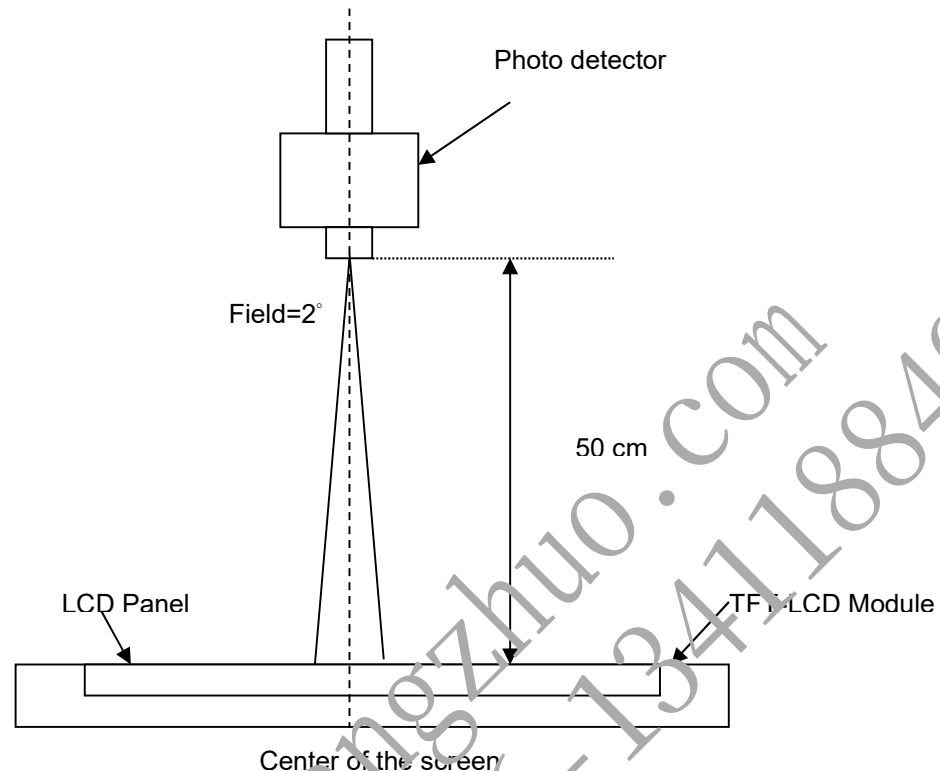
The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting



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Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points , $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

Note 7 : Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

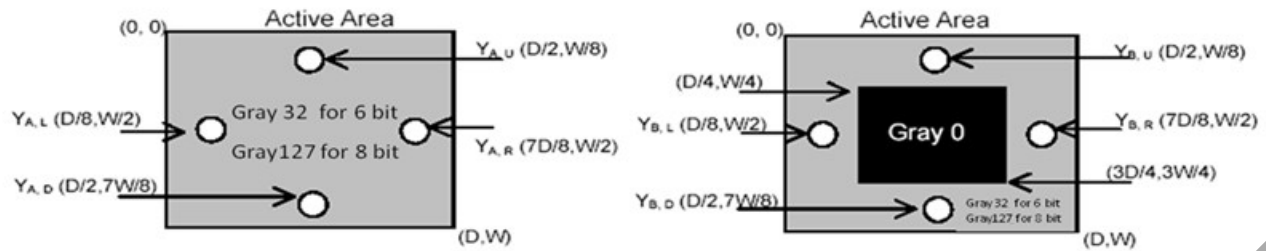
Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



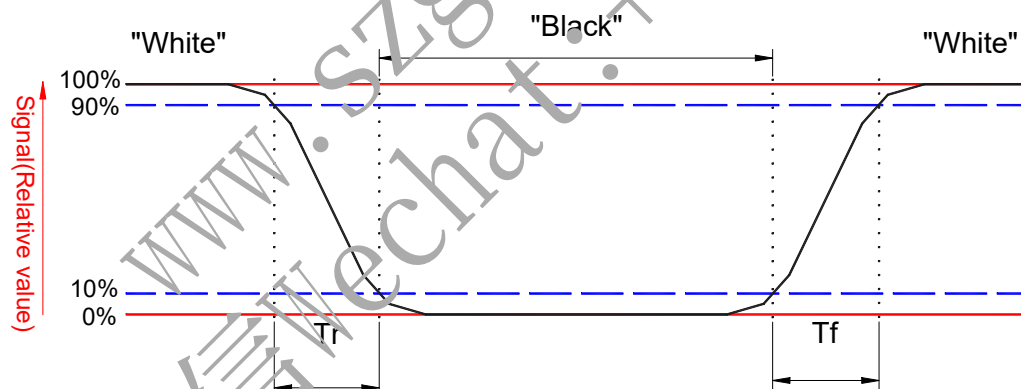
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Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



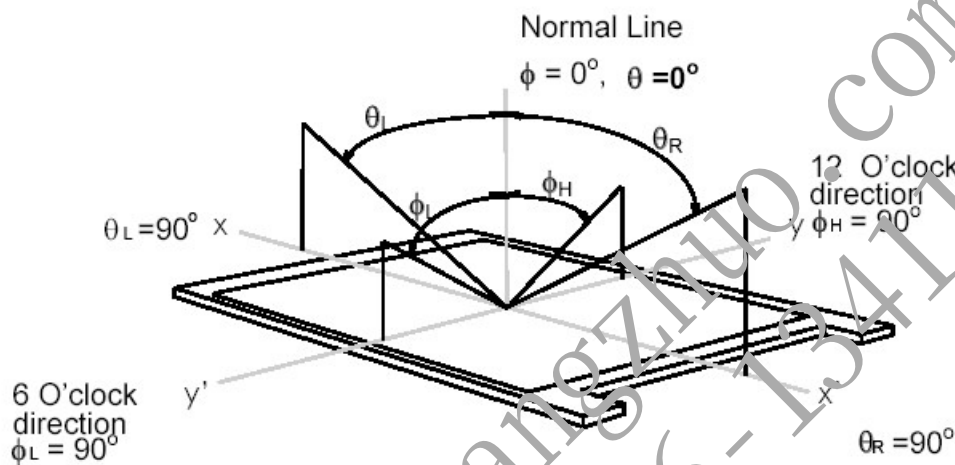


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Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (ϕ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



Note 10. TUV defined by TÜV Rheinland Eyesafe Low Blue Light Certification.

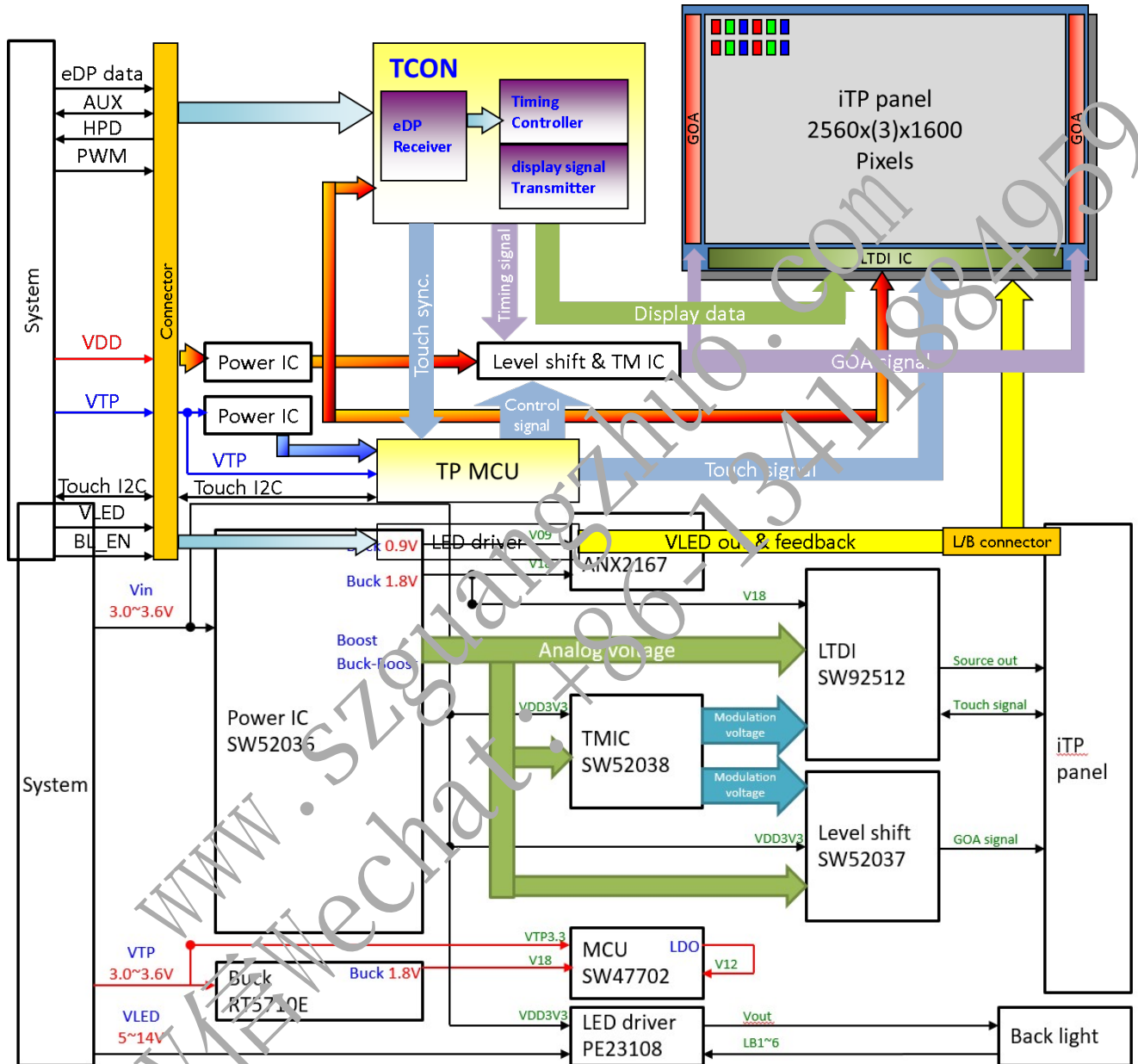


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3. Functional Block Diagram

The following diagram shows the functional block of the 14.0 inches wide Color TFT/LCD 40 Pin





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4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Touch Sensor Module

Item	Symbol	Min	Max	Unit	Conditions
Touch Sensor Module Power Voltage	VTSP	-0.3	+4.0	[Volt]	
Touch Sensor Module Reset Signal	RST	-0.3	+4.0	[Volt]	
Touch Sensor Module enable Signal	TP_EN	-0.3	+4.0	[Volt]	

4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operating Humidity	HOP	5	90	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	90	[%RH]	Note 4

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).

Note 5: The packing material of system forbid to involve ammonium component

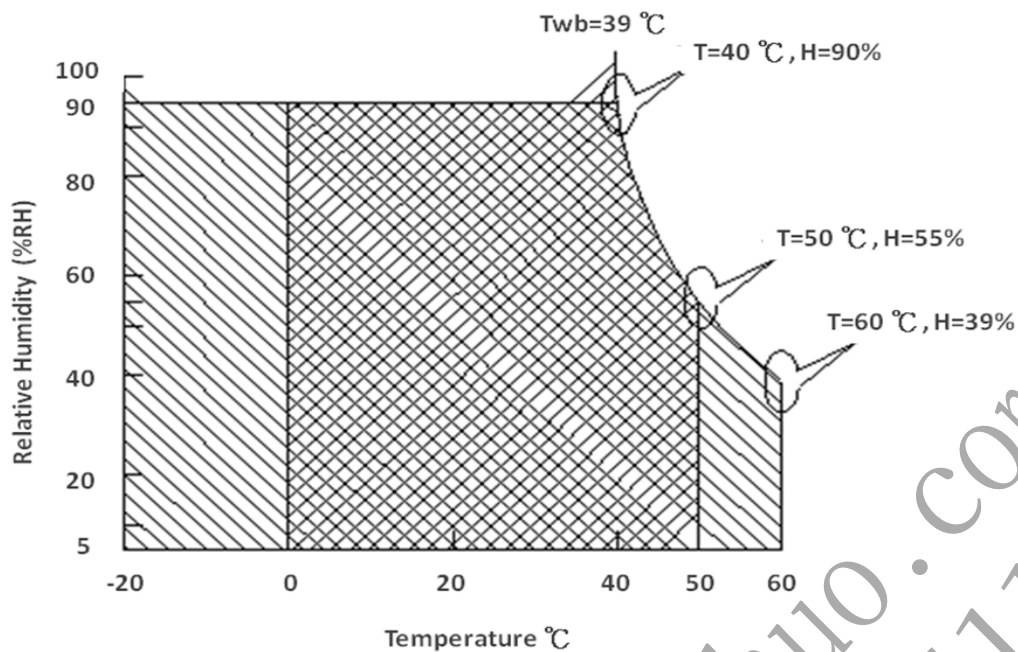
Note 6: The reliability test conditions of system do not exceed the verified conditions of TFT module

Note 7: Be sure the panel test condition do not exceed the component limitation of TFT module(TN Liquid crystal , for example)



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Operating Range



Storage Range





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5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power @ mosaic pattern	-	-	1.15	[Watt]	Note 1
IDD	IDD Current(RMS) @ mosaic pattern	-	-	385	[mA]	Note 1
PDD	VDD Power @ R/G/B pattern	-	-	1.2	[Watt]	Note 1
IDD	IDD Current(RMS) @ R/G/B pattern	-	-	400	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
Ipeak	Peak Current	-	-	1500	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	
CDD	VDD Capacitance	-	-	90.7	[uF]	Note3

Note 1 : PDD(Max)@ mosaic pattern Maximum Power

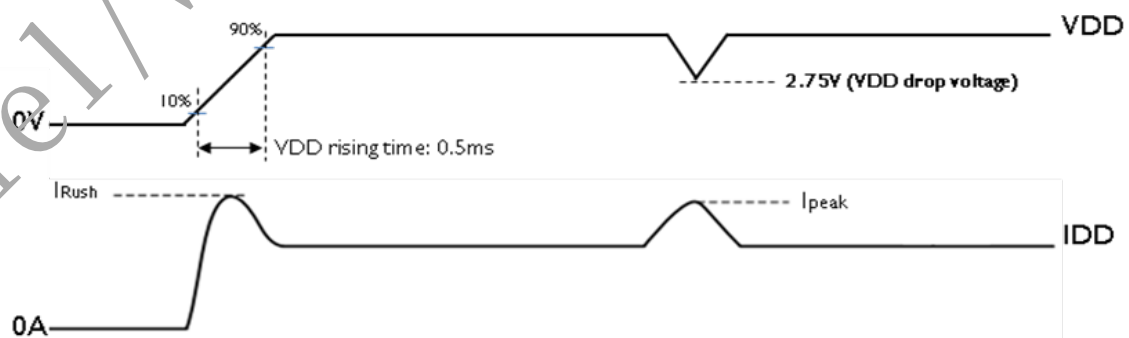
PDD(Max)@ R/G/B pattern Maximum Power

$IDD(Max) = PDD(Max) / VDD(Min)$

Note 2 :

a. IRush: VDD measured rising timing @ 0.5ms

b. IPeak: VDD drop Voltage $\geq 2.75V$ at this Ipeak current

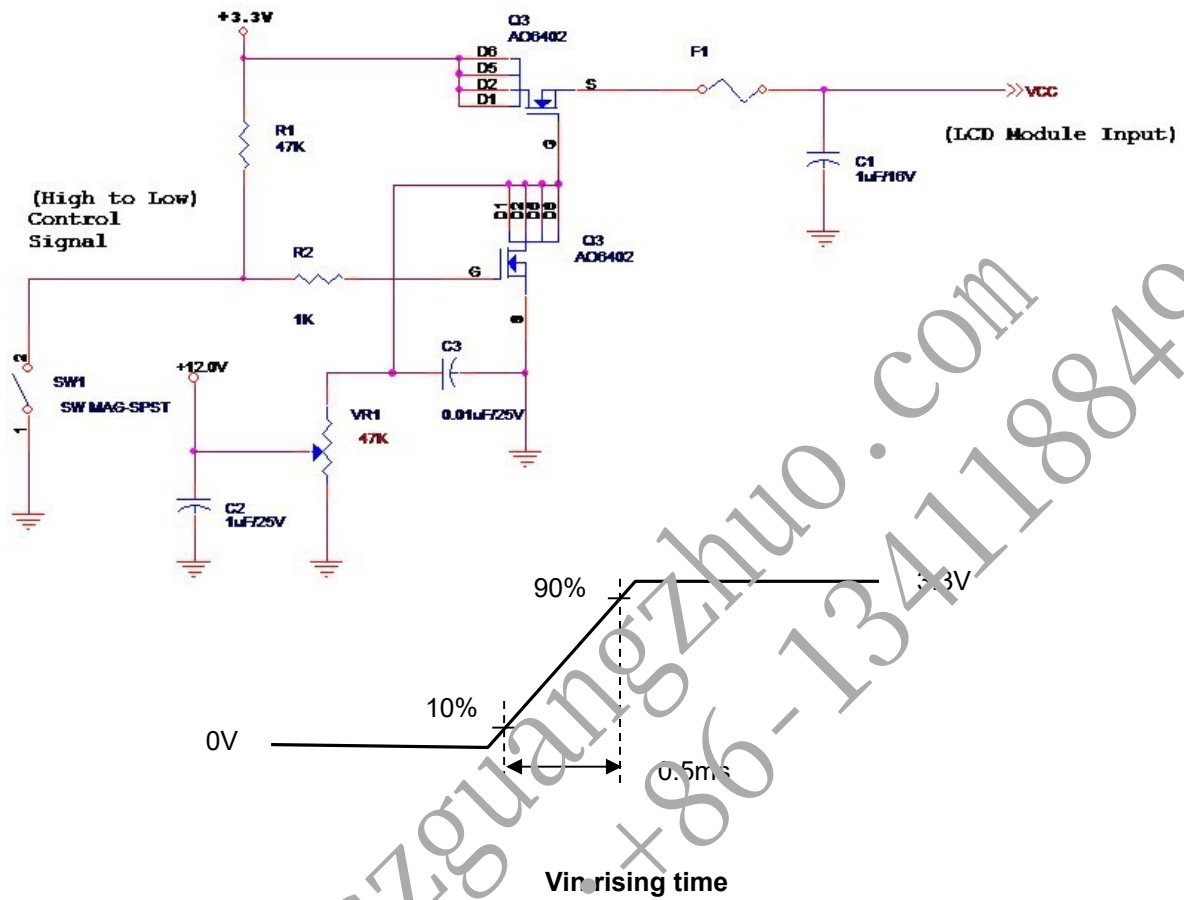




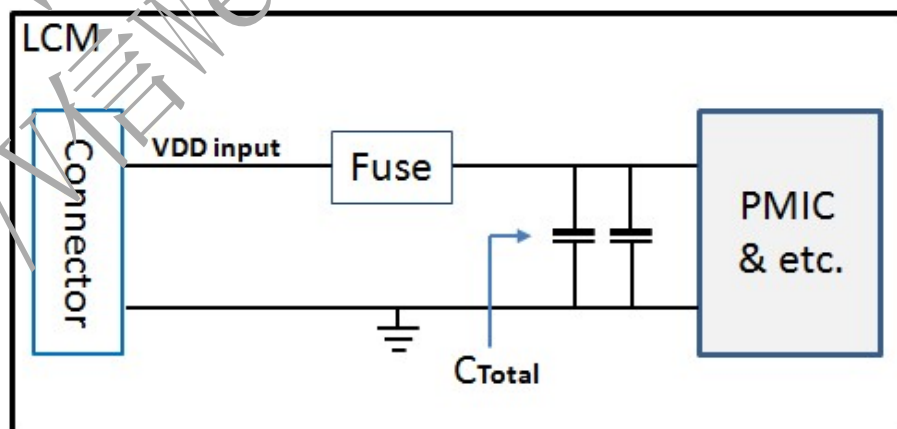
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c. IRush Measure Condition:



Note 3: Schematic diagram for VDD loop C_{Total} value



5.1.2 Signal Electrical Characteristics



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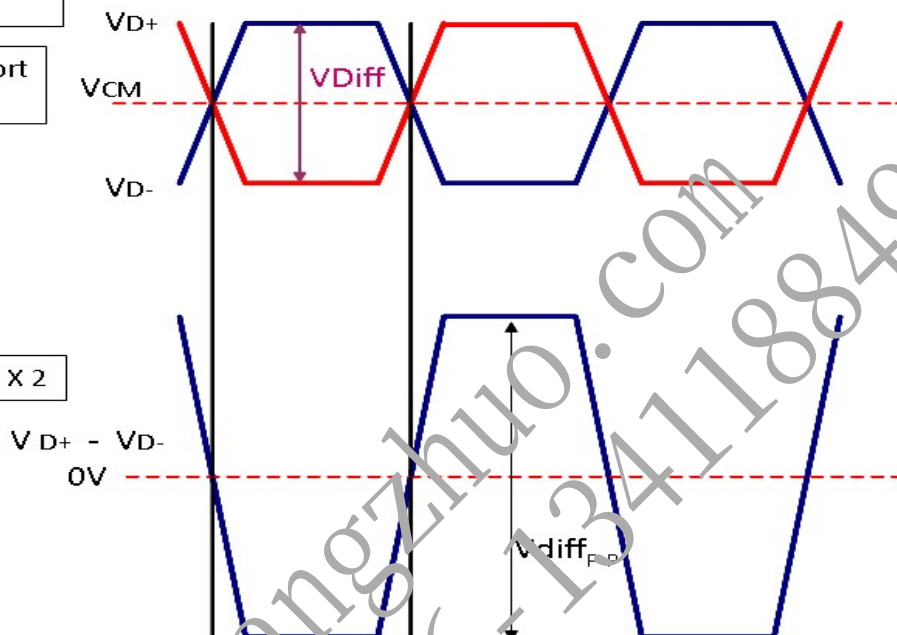
Signal electrical characteristics are as follows;

Display Port main link signal:

Differential pair VD+, VD-
Which is one Display port
Main link

VCM of Display port
Main link

$$V_{diffP-P} = [(VD+) - (VD-)] \times 2$$



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
VDiff _{P-P}	Peak-to-peak Voltage at a receiving Device	75		1320	mV

Follow as VESA display port standard V1.4

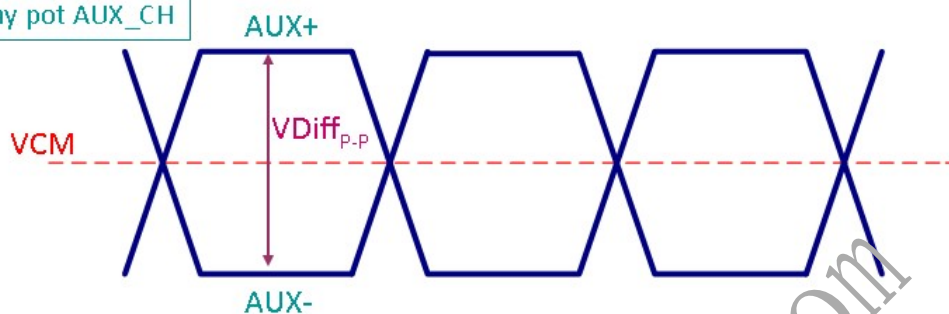


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Display Port AUX_CH signal:

Differential AUX+ , AUX-
Which is Display port AUX_CH



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff _{P-P}	AUX Peak-to-peak Voltage at a receiving Device	270		800	mV

Follow as VESA display port standard V1.3

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25		3.6	V

Follow as VESA display port standard V1.3



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5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	2.6	[Watt]	(Ta=25°C), Note 1
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25°C), Note 2 If=17mA
Inrush Current	VLED	-	-	-	mA	VLED : 12V/White pattern , Note3

Note 1: Calculator value for reference $P_{LED} = V_F$ (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

Note 3: VDD measured rising timing @ 0.5ms / VLED input 12V / test pattern : White pattern / 1000nit

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	5.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25°C) Note 1 Note 3
LED Enable Input High Level	VLED_EN	2.5	-	5	[Volt]	
LED Enable Input Low Level		-	-	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	3.0	-	3.45	[Volt]	
PWM Logic Input Low Level		-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	1 * Note 2	--	100	%	

Note 1: Recommender system pull up/down resistor no bigger than 10kohm

Note 2: If the PWM duty ratio(min) is set between 5% to 1% , the PWM input frequency should be set below 1KHz . The brightness-duty characteristic might not be able to keep in it's linearity if the dimming control is operated in 1% to 5% range.

Note 3: BL Control Mode is DC diming mode.

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**5.3 Touch Sensor Module****5.3.1 Power Specification**

Items	Symbol		Specifications			Unit	Notes
			Min.	Typ.	Max.		
Touch sensor module Power Supply	VTSP		3.0	3.3	3.6	V	
Touch sensor module Power Consumption	PTP	Active	-	-	120	mW	
		Idle	-	-	55	mW	
		Sleep	-	-	45	mW	
Touch Sensor Module Power ripple	VTSPrp		-	-	50	mV	
Input Voltage	RST, TP_EN	VIH	2		3.3	V	
		VL	0		0.8	V	

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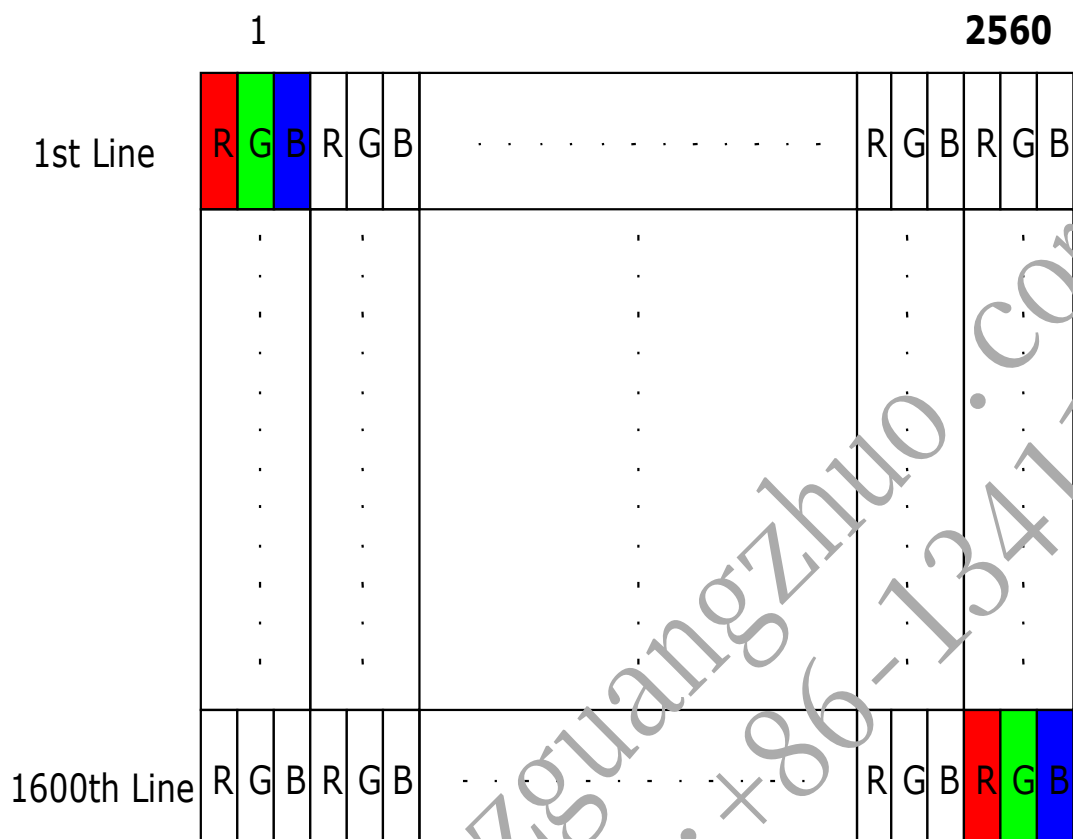
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6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



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6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or Compatible
Type / Part Number	IPEX 20682-040E-02 or compatible
Mating Housing/Part Number	IPEX 20679-040T-01 or compatible

6.2.2 Pin Assignment

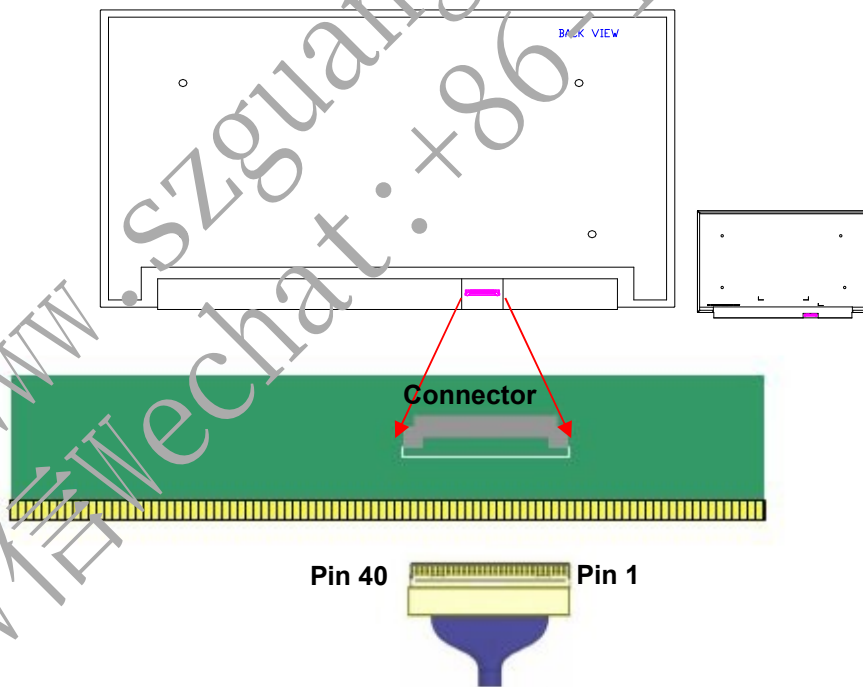
Pin	Symbol	Description
1	NC	Reserve DBC hardware
2	DP_GND	High Speed Ground
3	Lane 1_N	Complement Signal Link Lane 1
4	Lane 1_P	True Signal Link Lane 1
5	DP_GND	High Speed Ground
6	Lane 0_N	Complement Signal Link Lane 0
7	Lane 0_P	True Signal Link Lane 0
8	DP_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Channel
10	AUX_CH_N	Complement Signal Auxiliary Channel
11	DP_GND	High Speed Ground
12	LCD_VCC (3.0~3.6V)	LCD logic and driver power
13	LCD_VCC (3.0~3.6V)	LCD logic and driver power
14	LCD_Self_Test	LCD Panel Self Test Enable (Optional)
15	LCD_GND	LCD logic and driver ground
16	LCD_GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	BL_GND	LED Backlight ground
19	BL_GND	LED Backlight ground
20	BL_GND	LED Backlight ground
21	NC	Reserved for LCD manufacture's use
22	BL_EN	LED Backlight control on/off control
23	PWM_IN	System PWM signal input for dimming
24	NC	Reserved for LCD manufacture's use
25	NC	Reserved for LCD manufacture's use
26	NC	Reserved for LCD manufacture's use
27	V_LED(5~21V)	LED Backlight power (5~21V)
28	V_LED(5~21V)	LED Backlight power (5~21V)
29	V_LED(5~21V)	LED Backlight power (5~21V)

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30	NC	Reserved for LCD manufacture's use
31	NC(TP_D-)	Reserved for Touch panel USB D-
32	NC(TP_D+)	Reserved for Touch panel USB D+
33	LCD_GND	LCD logic and driver ground
34	VTSP(3.0~3.6V)	Touch Power line 3.3V
35	VTSP(3.0~3.6V)	Touch Power line 3.3V
36	Touch_EN	Touch_EN (Report Switch) (pull-up 3.3V at PCBA follow VTSP)
37	TP I2C_SCK	Touch panel I2C-SCK (pull-up 3.3V at PCBA follow VTSP)
38	TP I2C_SDA	Touch panel I2C-SDA (pull-up 3.3V at PCBA follow VTSP)
39	TP I2C_INT	Touch panel I2C-INT (pull-up 3.3V at PCBA follow VTSP)
40	TP_RST	Touch panel IC reset, Low active (pull-up 3.3V at PCBA follow VTSP)

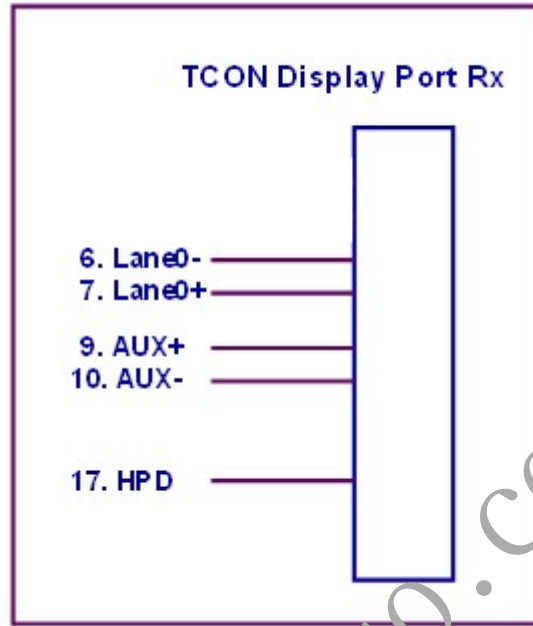


Note1: Start from right side.

Note2: Input signals shall be low or High-impedance state when VDD is off.
Internal circuit of **eDP inputs** are as following.

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6.3 Interface Timing

6.3.1 Timing Characteristics

For normal display, interface timings should match the 2560x1600 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		1/ T _{Clock}	259.56	268.64	272.9	MHz
Vertical Section	Period	T _V	1630	1646	1600+A	T _{Line}
	Active	T _{VD}	1600			
	Blanking	T _{VB}	30	46	A	
Horizontal Section	Period	T _H	2654	2720	2560+B	T _{Clock}
	Active	T _{HD}	2560			
	Blanking	T _{HB}	94	160	B	

Note 1 : The above is as optimized setting

Note 2 : The maximum clock frequency = (1366+B)*(768+A)*60<80MHz

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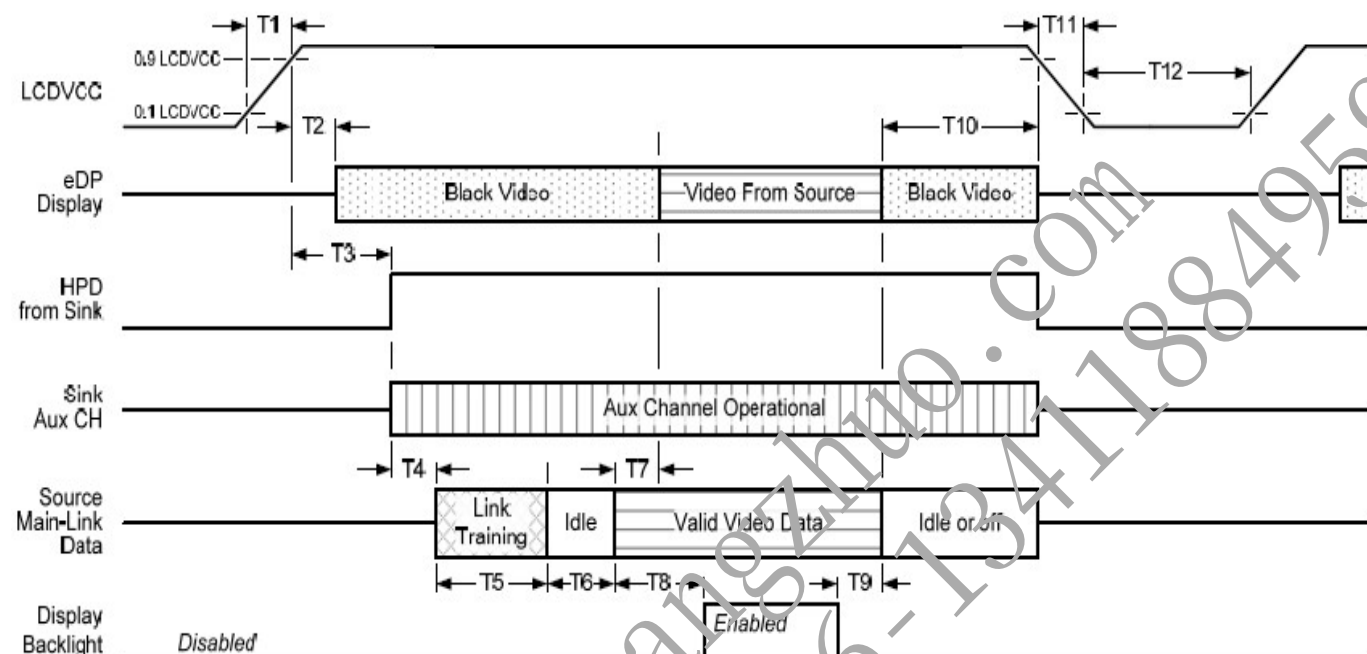
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6.4 Power ON/OFF Sequence

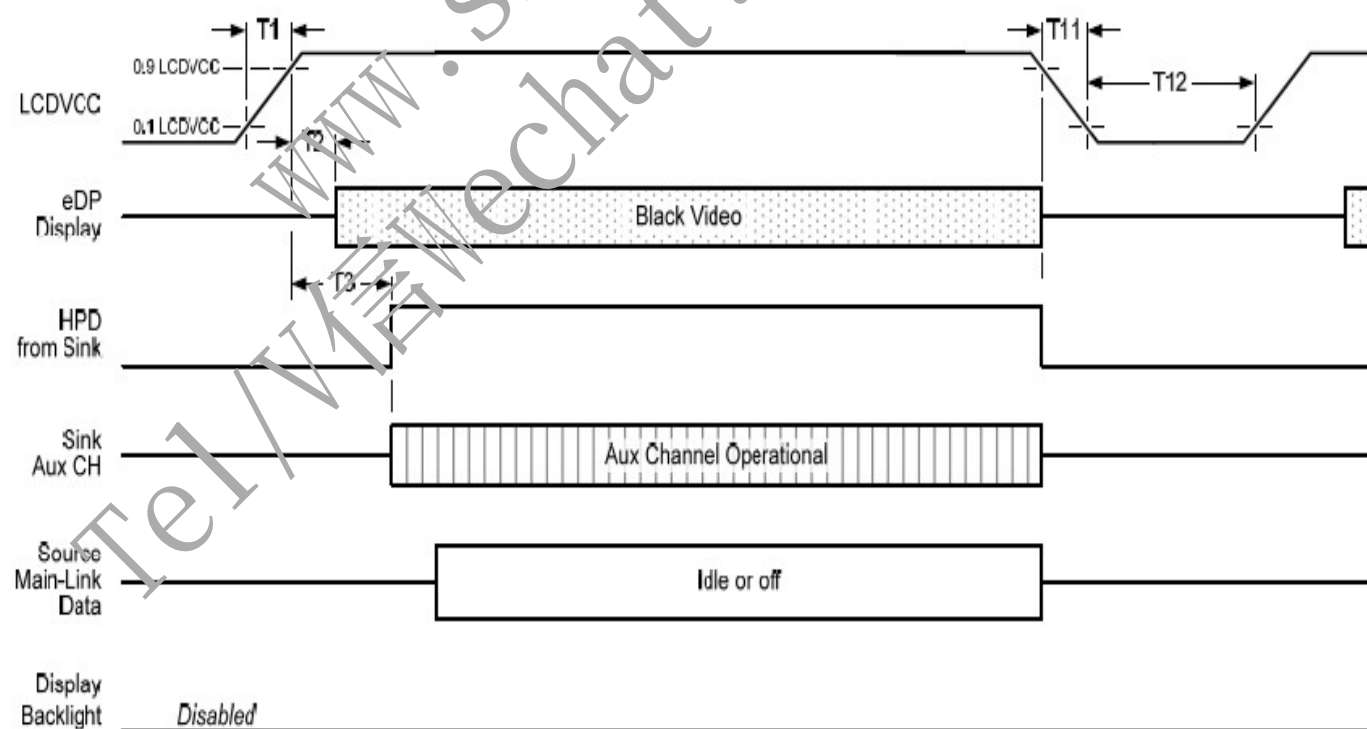
Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

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Display Port panel power sequence timing parameter:

Timing Parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	Power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	Delay from LCDVDD to black video generation	sink	0ms		eDP 1.2 =>200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		eDP 1.4 =>80ms	sink AUX_CH must be operational upon HPD high
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize
T5	link training duration	source				dependent on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 90% to 10%	source			10ms	
T12	power off time	source	500ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:

-upon LCDVDD power on (within T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).

-When no main link data or invalid video data is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

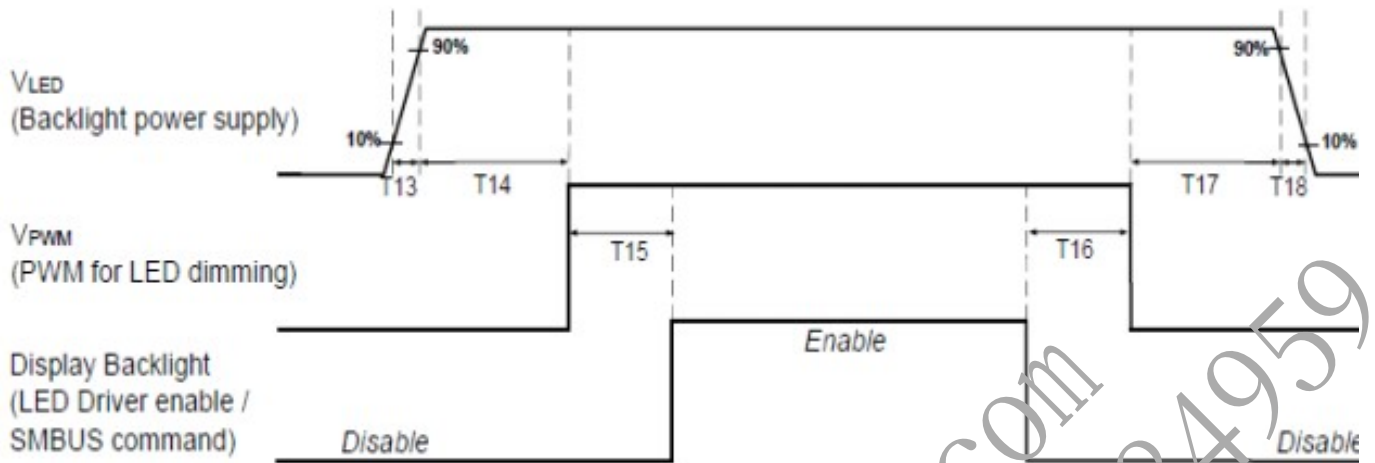
Note 4: T8>T7

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Display Port panel B/L power sequence timing parameter:



Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.

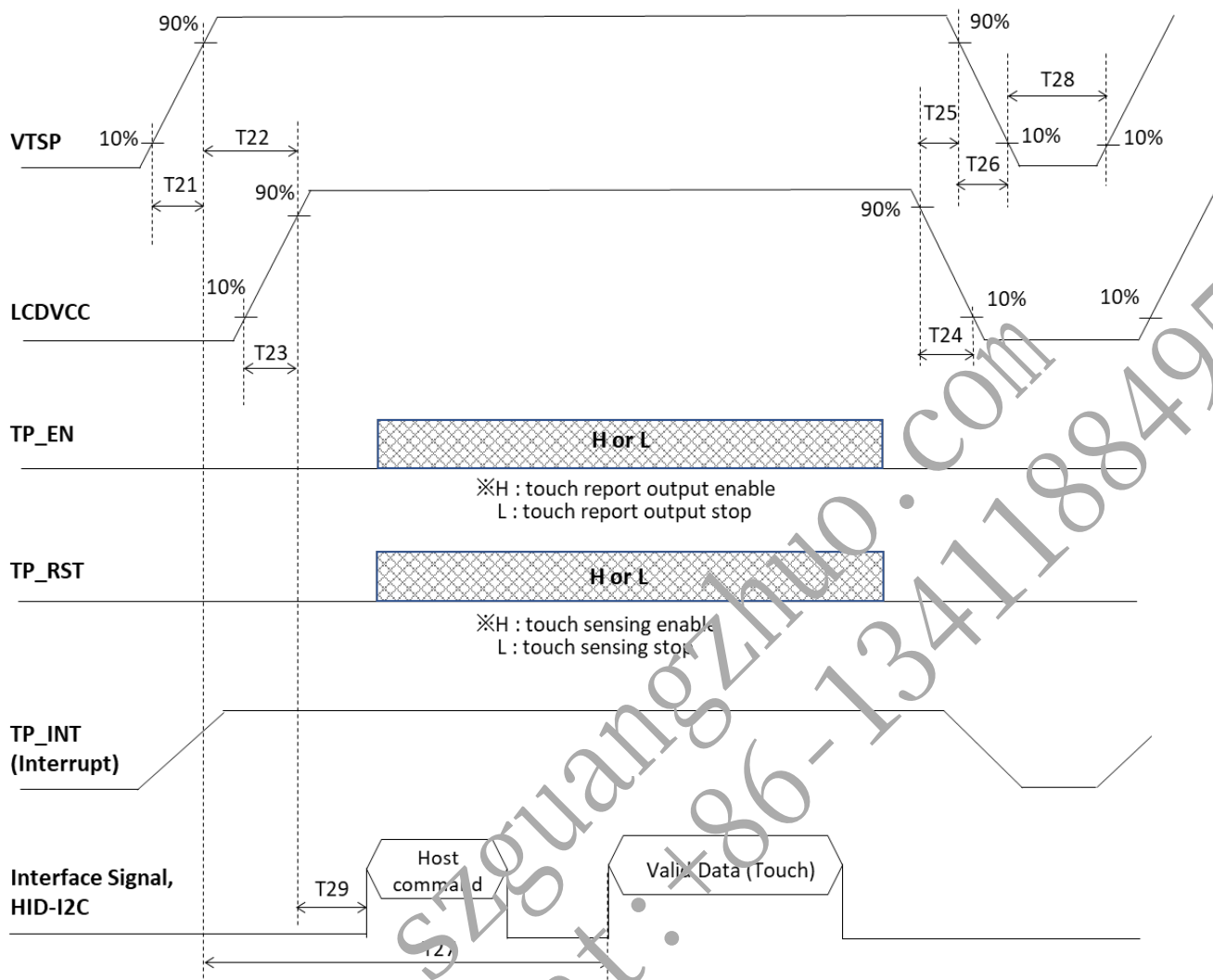
Touch Panel Power on Sequence

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HID-I2C



parameter	Min.	Max.	Units
T21	0.5	10	ms
T22	0	10	ms
T23	0.5	10	ms
T24	--	10	ms
T25	0	--	ms
T26	0.5	10	ms
T27	600	--	ms
T28	500	--	ms
T29	250	--	ms

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation

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- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

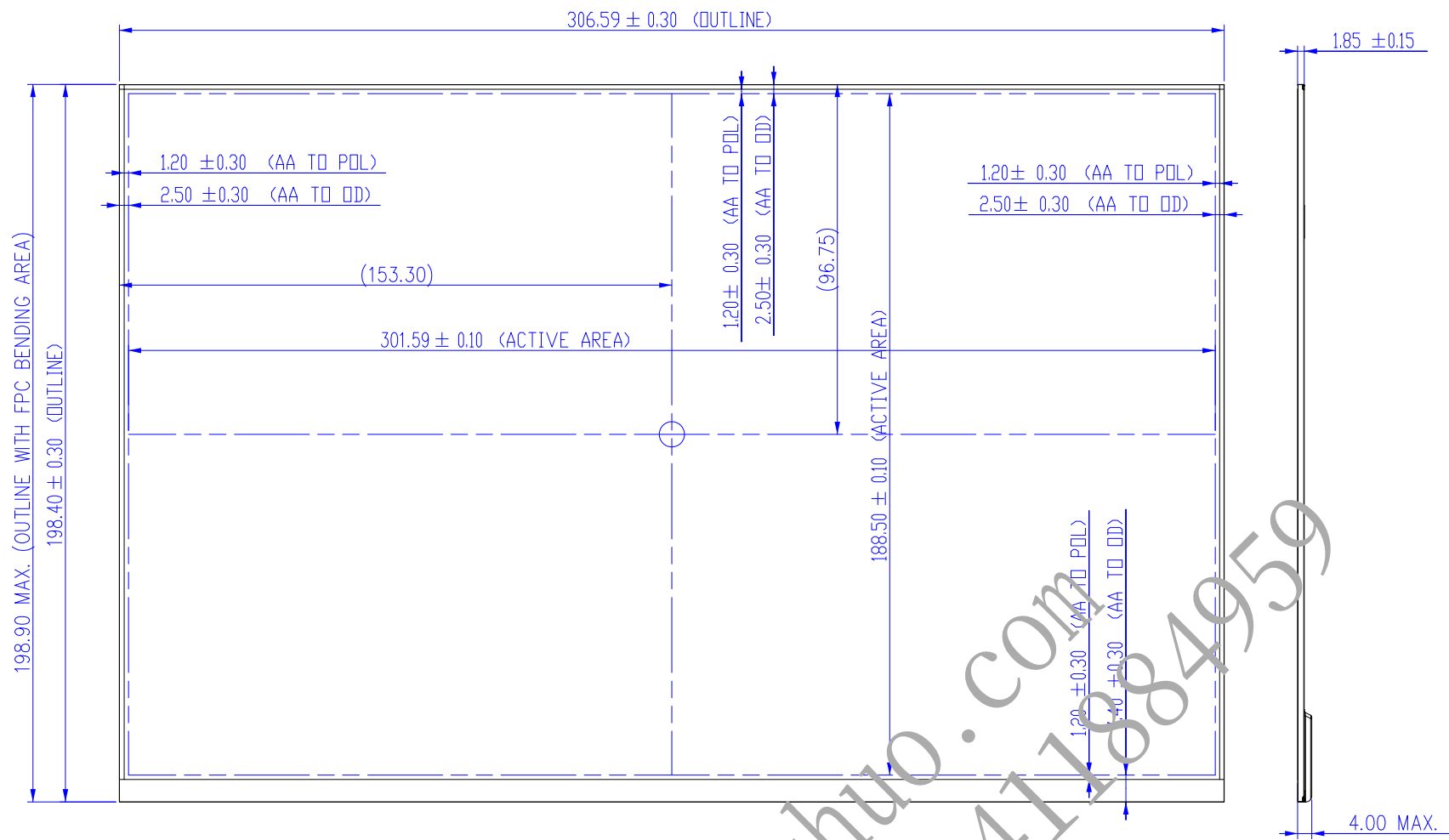
Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C , 90%RH, 240h	
High Temperature Operation	Ta= 50°C , Dry, 240h	
Low Temperature Operation	Ta=0°C , 240h	
High Temperature Storage	Ta= 60°C , 240h	
Low Temperature Storage	Ta= -20°C , 240h	
Thermal Shock Test	Ta= -20°C (30min) ~60°C (30min), 20cycles condition.	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2, ESD class B: Some performance degradation allowed. No data lost self-recoverable, no hardware failures.

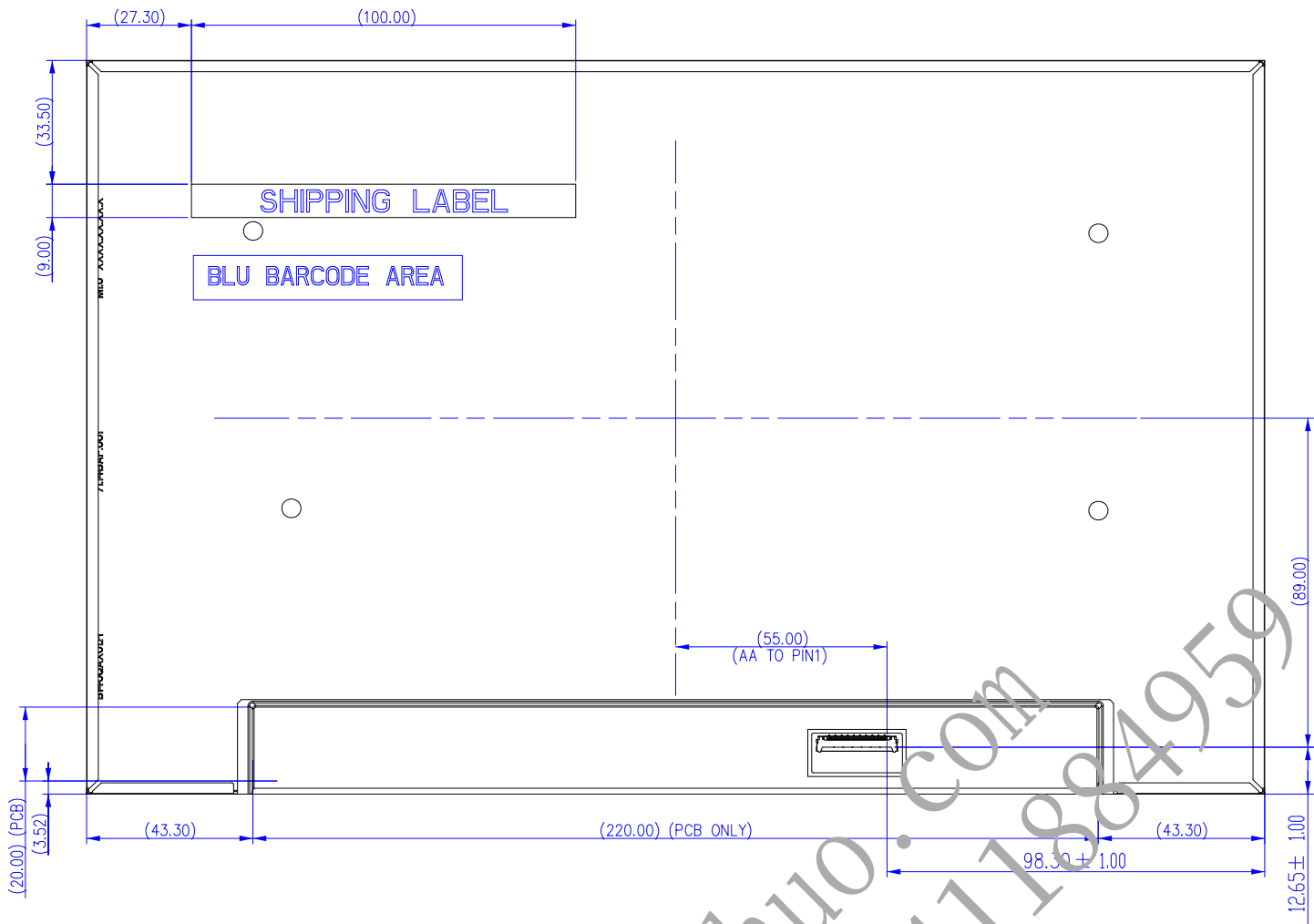
Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

8.1 Total Solution Outline Dimension



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Note: Prevention IC damage, IC positions not allowed any overlap over these areas.



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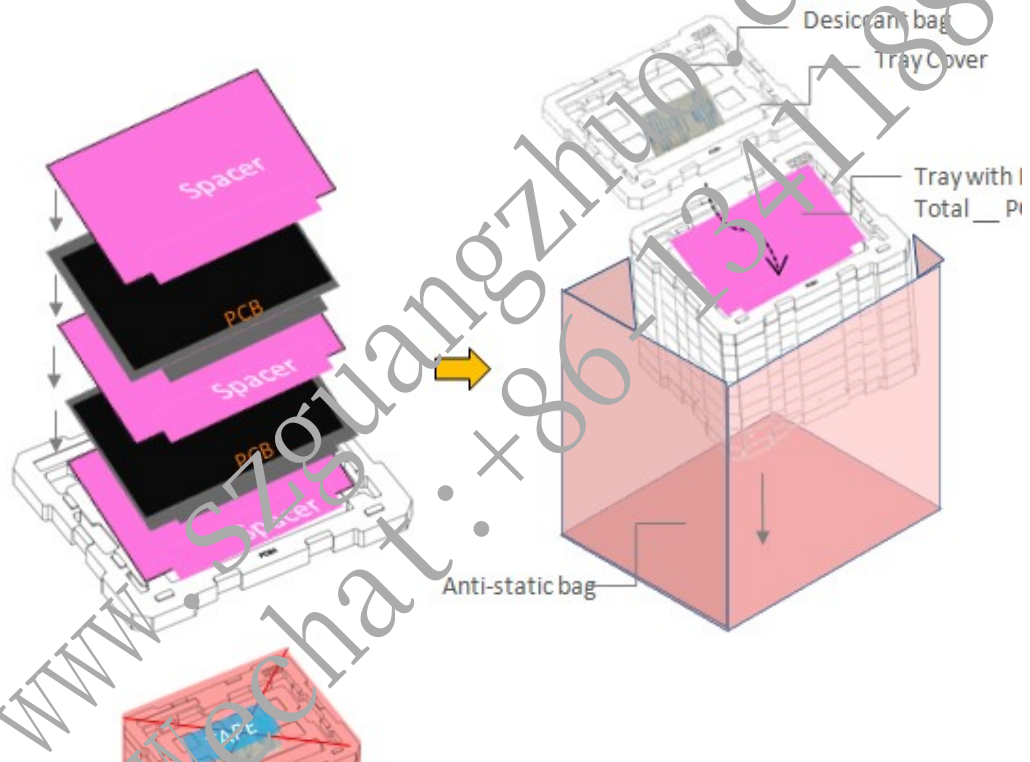
9. Shipping and Package

9.1 Shipping Label Format

 *XXXXXXXXXX-XXXXX* H/W: 0A F/W: 1 MADE IN CHINA(K01)	Manufactured YY/WW Model No: B140QAX01.H AUO Corporation	 CN-069R1W-AUK00- XXX-XXX-X20 Made In China DP/N 069R1W	c AL US E204354 15 Pb RoHS
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9.2 Carton Package

24 Modules / Carton

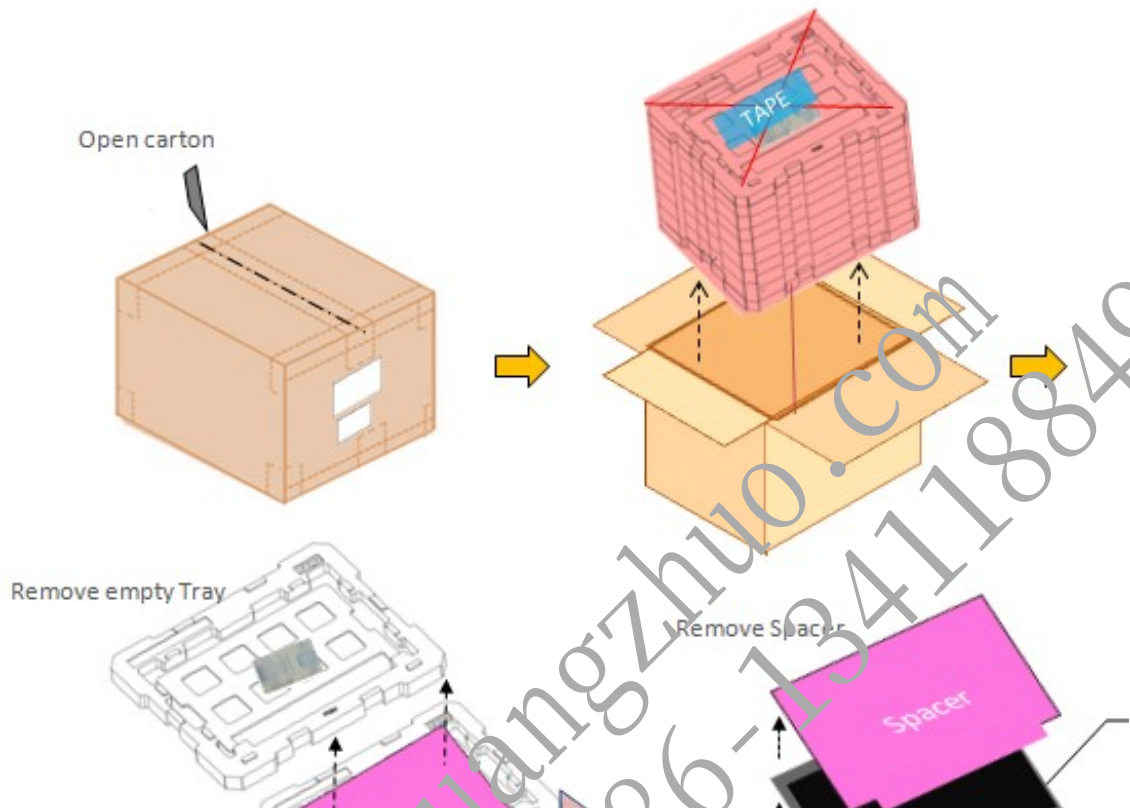




UN-Packing Method

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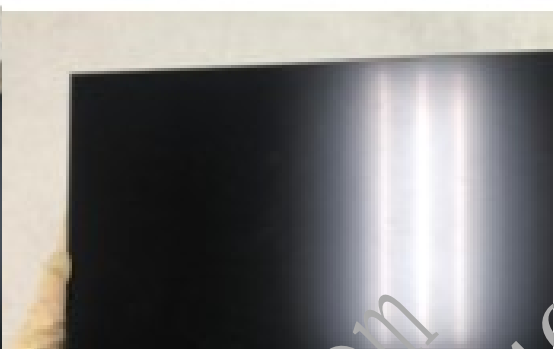
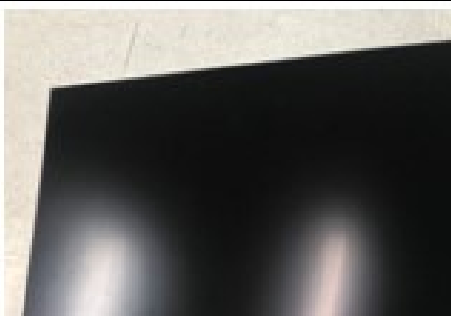
Precaution for handling Tray

The bottom pp board must be lifted with both hands when holding the tray	Caution : Do not lift trays by one hand
Always place tray on flat surface. Hold center of short side of tray with both	Caution : Do not lift tray by one hand

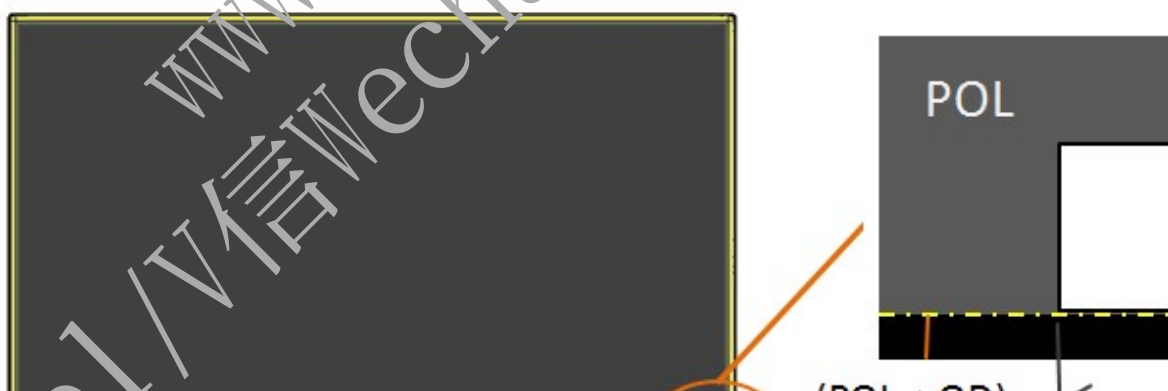


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hands when handling one or more trays.	
	
Handle panel at left and right edge with both hands carefully.	
	
Caution : Don't lift with one hand	Caution : Don't handle at PCBA side

Pull Bar Position:

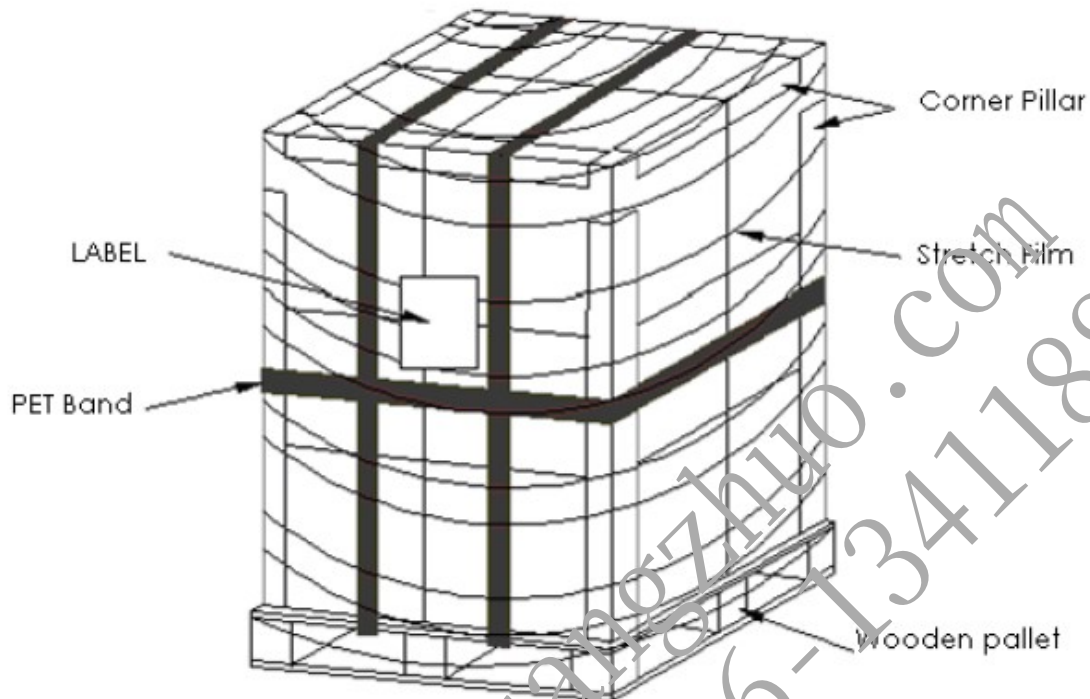




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9.3 Shipping Package of Palletizing Sequence





Product Specification

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10. Appendix:

10.1 EDID Description

Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)	Value (DEC)
0	Header	00	00000000	0
1	Header	FF	11111111	255
2	Header	FF	11111111	255
3	Header	FF	11111111	255
4	Header	FF	11111111	255
5	Header	FF	11111111	255
6	Header	FF	11111111	255
7	Header	00	00000000	0
8	EISA manufacture code = 3 Character ID	06	00000110	6
9	EISA manufacture code (Compressed ASCII)	AF	10101111	175
0A	Panel Supplier Reserved – Product Code	A4	10100100	164
0B	Panel Supplier Reserved – Product Code	0B	00001011	11
0C	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000	0
0D	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000	0
0E	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000	0
0F	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000	0
10	Week of manufacture	00	00000000	0
11	Year of manufacture	20	00100000	32
12	EDID structure version # = 1	01	00000001	1
13	EDID revision # = 4	04	00000100	4
14	Video I/P definition	A5	10100101	165
15	Max H image size = ?? cm(Rounded to cm)	1E	00011110	30
16	Max V image size = ?? cm(Rounded to cm)	13	00010011	19
17	Display gamma = (gamma × 100) - 100 = Example: (2.2 × 100) - 100 = 120	78	01111000	120
18	Feature support	03	00000011	3
19	Red/Green Low bit (RxR /GxGy)	AD	10101101	173
1A	Blue/White Low bit (BxBv/WxWy)	F5	11110101	245
1B	Red X Rx = 0.???	A8	10101000	168
1C	Red Y Ry = 0.???	54	01010100	84
1D	Green X Rx = 0.???	47	01000111	71
1E	Green Y Ry = 0.???	9C	10011100	156
1F	Blue X Rx = 0.???	24	00100100	36
20	Blue Y Ry = 0.???	0E	00001110	14
21	White X Rx = 0.???	50	01010000	80
22	White Y Ry = 0.???	54	01010100	84
23	Established timings 1 (00h if not used)	00	00000000	0
24	Established timings 2 (00h if not used)	00	00000000	0
25	Manufacturer's timings (00h if not used)	00	00000000	0
26	Standard timing ID1 (01h if not used)	01	00000001	1
27	Standard timing ID1 (01h if not used)	01	00000001	1
28	Standard timing ID2 (01h if not used)	01	00000001	1
29	Standard timing ID2 (01h if not used)	01	00000001	1
2A	Standard timing ID3 (01h if not used)	01	00000001	1
2B	Standard timing ID3 (01h if not used)	01	00000001	1
2C	Standard timing ID4 (01h if not used)	01	00000001	1



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2D	Standard timing ID4 (01h if not used)	01	00000001	1
2E	Standard timing ID5 (01h if not used)	01	00000001	1
2F	Standard timing ID5 (01h if not used)	01	00000001	1
30	Standard timing ID6 (01h if not used)	01	00000001	1
31	Standard timing ID6 (01h if not used)	01	00000001	1
32	Standard timing ID7 (01h if not used)	01	00000001	1
33	Standard timing ID7 (01h if not used)	01	00000001	1
34	Standard timing ID8 (01h if not used)	01	00000001	1
35	Standard timing ID8 (01h if not used)	01	00000001	1
36	Pixel Clock/10,000 (LSB)	F0	11110000	240
37	Pixel Clock/10,000 (MSB)	68	01101000	104
38	Horizontal Active = ??? pixels (lower 8 bits)	00	00000000	0
39	Horizontal Blanking (Thbp) = 320 pixels (lower 8 bits)	A0	10100000	160
3A	Horizontal Active/Horizontal blanking (Thbp) (upper 4 bits)	A0	10100000	160
3B	Vertical Active = ??? lines	40	01000000	64
3C	Vertical Blanking (Tvbp) = ?? lines (DE Blanking typ. for DE only panels)	2E	00101110	46
3D	Vertical Active : Vertical Blanking (Tvbp) (upper 4:4 bits)	60	01100000	96
3E	Horizontal Sync, Offset (Thfp) = ?? pixels	30	00110000	48
3F	Horizontal Sync, Pulse Width = ??? pixels	20	00100000	32
40	Vertical Sync, Offset (Tvfp) = ? lines Sync Width = ? lines	35	00110101	53
41	Horizontal Vertical Sync Offset Width upper 2 bits	00	00000000	0
42	Horizontal Image Size = ??? mm	2D	00101101	45
43	Vertical image Size = ??? mm	BC	10111100	188
44	Horizontal Image Size / Vertical image size	10	00010000	16
45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0
46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0
47	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no stereo, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3==> fix=1A	1A	00011010	26
48	Pixel Clock/10,000 (LSB)	F3	11110011	243
49	Pixel Clock/10,000 (MSB)	53	01010011	83
4A	Horizontal Active = xxxx pixels (lower 8 bits)	00	00000000	0
4B	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)	A0	10100000	160
4C	Horizontal Active/Horizontal blanking (Thbp) (upper 4:4 bits)	A0	10100000	160
4D	Vertical Active = xxxx lines	40	01000000	64
4E	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels)	2E	00101110	46
4F	Vertical Active : Vertical Blanking (Tvbp)	60	01100000	96



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	(upper 4:4 bits)			
50	Horizontal Sync, Offset (Thfp) = xxxx pixels	30	00110000	48
51	Horizontal Sync, Pulse Width = xxxx pixels	20	00100000	32
52	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	35	00110101	53
53	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0
54	Horizontal Image Size =xxx mm	2D	00101101	45
55	Vertical image Size = xxx mm	BC	10111100	188
56	Horizontal Image Size / Vertical image size	10	00010000	16
57	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0
58	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0
	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no stereo, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3			
59	Bit[0] : See VESA EDID Spec 1.3==> fix=1A	1A	00011010	26
5A	Flag	00	00000000	0
5B	Flag	00	00000000	0
5C	Flag	00	00000000	0
5D	Data Type Tag: Alphanumeric Data String (ASCII) ==> fix=FE	FE	11111110	254
5E	Flag	00	00000000	0
5F	Dell P/N 1 st Character	36	00110110	54
60	Dell P/N 2 nd Character	39	00111001	57
61	Dell P/N 3 rd Character	52	01010010	82
62	Dell P/N 4 th Character	31	00110001	49
63	Dell P/N 5 th Character	57	01010111	87
64	EDID Revision Bit[6:0] See charts below Bit[7] 0: X-rev, 1: A-rev	14	00010100	20
65	Manufacturer P/N	42	01000010	66
66	Manufacturer P/N	31	00110001	49
67	Manufacturer P/N	34	00110100	52
68	Manufacturer P/N	30	00110000	48
69	Manufacturer P/N	51	01010001	81
6A	Manufacturer P/N	41	01000001	65
6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	58	01011000	88
6C	Flag	00	00000000	0
6D	Flag	00	00000000	0
6E	Flag	00	00000000	0
6F	Data Type Tag: Manufacturer Specified Data 00 ==>fix=00	00	00000000	0
70	Flag	00	00000000	0
71	Color Management	02	00000010	2
72	Panel Structure	41	01000001	65
73	Frame Rate	21	00100001	33
74	Light Controller Interface and Luminance	A8	10101000	168
75	Outdoor Features	00	00000000	0
76	Multi-Media Features	01	00000001	1
77	Multi-Media Features	00	00000000	0



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78	Special Features #1	00	00000000	0
79	Special Features #2	1A	00011010	26
7A	Special Features #3	41	01000001	65
7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010	10
7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00	00000000	0
7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	0D	00001101	13

10.2 Notes

DPCD Ver.	sDRRS	DCR
1.4	On	N/A

MSO	G-Sync
N/A	N/A

ASSR	Auto ASSR (Tcon support)
On	On

Dell

- Any other PCB component is lower than top polarizer.
- The vernier caliper is used to measure the X,Y outline dimension, the micrometer is used to measure the Z, the flatness is measured by the thick gauge.
- Attached cell tape is naturally floating, and need to be compressed while measuring, this applies to z outline dimension measurement & POL surface is the highest check.
- The Height Gauge is used to measure the Bracket.