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NV140WUM-N4H V8.0

Customer: Lenovo

Product Specification

Rev.0

BOE Optoelectronics Technology Co., Ltd

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A4(210 X 297)

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1.0 GENERAL DESCRIPTION

1.1 Introduction

NV140WUM-N4H V8.0 is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 14.0 inch diagonally measured active area with WUXGA resolutions (1920 horizontal by 1200 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.2M(6bit+2FRC) colors and color gamut NTSC 45%. The TFT LCD panel used for this module is a low reflection and higher color type. Therefore, this module is suitable for Notebook PC. The LED driver for back-light driving is built in this model. All input signals are eDP1.2 interface compatible.

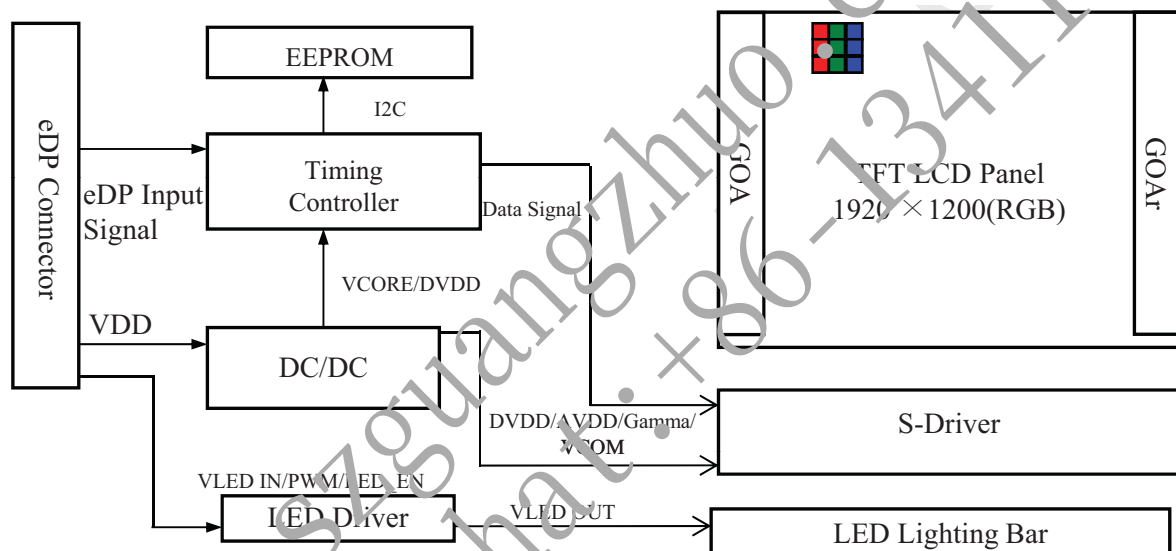


Figure 1, Drive Architecture

1.2 Features

- 2 lane eDP interface with 2.7Gbps link rates
- Thin and light weight
- 16.2(6bit+2FRC) color depth, color gamut NTSC 45%.
- Single LED lighting bar (Bottom side/Horizontal Direction)
- Data enable signal mode
- Green product (RoHS & Halogen free product)
- On board LED driving circuit
- Low driving voltage and low power consumption
- On board EDID chip
- Adjust backlight brightness with DC mode

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1.0 GENERAL DESCRIPTION						
1.2 Features						
DPCD Ver.	sDRRS	DCR	DMRRS	PSR	LRR	MBO
1.1	off	off	off	off	off	off
VESA DSC	MSO	AMD Free-sync	HDR	Dimming	OD	BIST
off	off	on	off	PWM in DC out	off	on
FRC	DDS	G-sync				
on	off	off				
www.szguangzhuo.com Tel/V信Wechat: +86-13411884953						
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1.3 Application ● Notebook PC (Wide type) 1.4 General Specification The followings are general specifications at the model NV140WUM-N4H V8.0. (listed in Table 1) <Table 1. General Specifications> <table><tr><th>Parameter</th><th>Specification</th><th>Unit</th><th>Remarks</th></tr><tr><td>Active area</td><td>301.5936(H) × 188.496mm (V)</td><td>mm</td><td></td></tr><tr><td>Number of pixels</td><td>1920 (H) × 1200 (V)</td><td>pixels</td><td></td></tr><tr><td>Pixel pitch</td><td>157.08(H) × 157.08 (V)</td><td>um</td><td></td></tr><tr><td>Pixel arrangement</td><td>RGB Vertical stripe</td><td></td><td></td></tr><tr><td>Display colors</td><td>16.2M(6bit+2FRC)</td><td></td><td></td></tr><tr><td>Color gamut</td><td>NTSC 45% Typ & 42% min</td><td></td><td>CIE1976uv</td></tr><tr><td>Display mode</td><td>Normally black</td><td></td><td></td></tr><tr><td>Dimensional outline</td><td>306.59 ± 0.3(H)*197.5 ± 0.3(V)(W/O PCB)*3.0(Max) 306.59 ± 0.3(H)*205 ± 0.5(V)(W/PCB)*3.0(Max)</td><td>mm</td><td></td></tr><tr><td>Weight</td><td>300(max)</td><td>g</td><td></td></tr><tr><td>Surface treatment</td><td>Anti-Glare</td><td></td><td></td></tr><tr><td>Surface hardness</td><td>3H</td><td></td><td></td></tr><tr><td>Back-light</td><td>Bottom edge side, 1-LED lighting bar type</td><td></td><td>Note 1</td></tr><tr><td rowspan="3">Power consumption</td><td>P_D : 0.6(Max.)</td><td>W</td><td>@Mosaic</td></tr><tr><td>P_{BL} : 3.1(Max.)</td><td>W</td><td>@VLED=12V</td></tr><tr><td>P_{Total} : 3.7(Max.)</td><td>W</td><td>@Mosaic</td></tr></table> Notes : 1. LED Lighting Bar (66*LED Array)				Parameter	Specification	Unit	Remarks	Active area	301.5936(H) × 188.496mm (V)	mm		Number of pixels	1920 (H) × 1200 (V)	pixels		Pixel pitch	157.08(H) × 157.08 (V)	um		Pixel arrangement	RGB Vertical stripe			Display colors	16.2M(6bit+2FRC)			Color gamut	NTSC 45% Typ & 42% min		CIE1976uv	Display mode	Normally black			Dimensional outline	306.59 ± 0.3(H)*197.5 ± 0.3(V)(W/O PCB)*3.0(Max) 306.59 ± 0.3(H)*205 ± 0.5(V)(W/PCB)*3.0(Max)	mm		Weight	300(max)	g		Surface treatment	Anti-Glare			Surface hardness	3H			Back-light	Bottom edge side, 1-LED lighting bar type		Note 1	Power consumption	P _D : 0.6(Max.)	W	@Mosaic	P _{BL} : 3.1(Max.)	W	@VLED=12V	P _{Total} : 3.7(Max.)	W	@Mosaic
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2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Absolute Maximum Ratings>

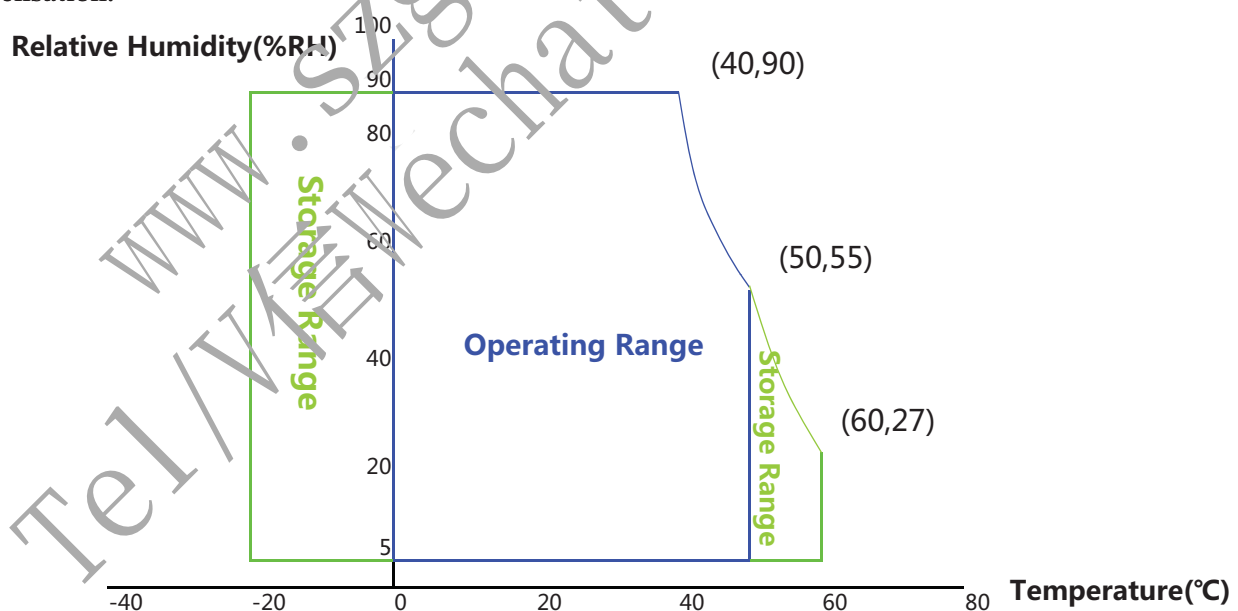
Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-0.3	4.0	V	Note 1
eDP input Voltage	V_{eDP}	0	2.0	V	
Logic Supply Voltage	V_{IN}	$V_{SS}-0.3$	$V_{DD}+0.3$	V	
Operating Temperature	T_{OP}	0	+50	°C	Note 2
Storage Temperature	T_{ST}	-20	+60	°C	

Notes :

1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.

2. Temperature and relative humidity range are shown in the figure below.

90 % RH Max. ($40\text{ }^{\circ}\text{C} \geq T_a$) Maximum wet - bulb temperature at $39\text{ }^{\circ}\text{C}$ or less. ($T_a > 40\text{ }^{\circ}\text{C}$) No condensation.



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3.0 ELECTRICAL SPECIFICATIONS								
3.1 Electrical Specifications								
< Table 3. Electrical Specifications >				Ta=25+/-2℃				
Parameter			Min.	Typ.	Max.	Unit	Remarks	
Power Supply Voltage		V _{DD}	3.0	3.3	3.6	V	Note 1	
Permissible Input Ripple Voltage		V _{RF}	-10% VDD	-	+10% VDD	V	@ V _{DD} =3.5V, note4	
BIST Control Level		High Level	2	-	3.3	V	@V _{DDIO} =1.8 or 2.5V(根据实际填写具体数值)	
		Low Level	0	-	0.375	V		
Power Supply Inrush Current		Inrush	-	-	2	A	Note3	
Power Supply Current	Mosaic	I _{DD}	-	-	182	mA	Note 1	
	RGB		-	-	364	mA		
Power Consumption	Mosaic	P _M	-	-	0.6	W		Note 2
	RGB	P _{RGB}	-	-	1.2	W		
	BLU	P _{BL}	-	-	3.1	W		
	Total	P _{Total}	-	-	3.7	W	@Mosaic	
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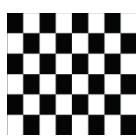
3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

Notes :

1. The supply voltage is measured and specified at the interface connector of LCM.
The current draw and power consumption specified is for 3.3V at 25 °C.

- a) Mosaic pattern 8*8
- b) R/G/B patterns



(a)



(b)

Figure 3. Power Measure Patterns

2. Calculated value for reference ($V_{LED} \times I_{LED}$) , The power consumption with LED Driver are under the $V_{LED} = 12.0V$, 25°C, PWM Duty 100% .

3. Measure condition (Figure 4)

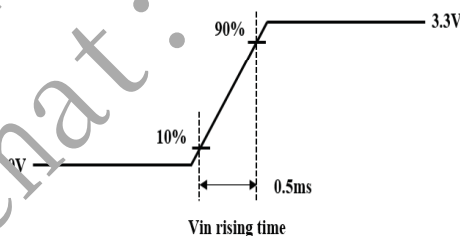


Figure 4. Inrush Measure Condition

4. Input voltage range: 3.0~3.6V. Test condition: Oscilloscope bandwidth 20MHz, AC coupling

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3.2 Backlight Unit

< Table 4. LED Driving Guideline Specifications >

Ta=25+/-2°C

Parameter		Min.	Typ.	Max.	Unit	Remarks
LED Forward Voltage	V_F	-	-	2.9	V	
LED Forward Current	I_F	-	13	-	mA	
LED Power Input Voltage	VLED	5	12	21	V	
LED Power Input Current	I_{LED}	-	-	258.3	mA	Note 1
LED Power Consumption	P_{LED}	-	-	2.1	W	
Power Supply Voltage for LED Driver Inrush	Iled inrush	-	-	2	A	Note 3
LED Life-Time	N/A	15,000	-	-	Hour	IF = 13mA Note 2
EN Control Level	Backlight On	V_{BL_EN}	2.5	5.0	V	
	Backlight Off	V_{BL_EN}	0	0.5	V	
PWM Control Level	High Level	V_{BL_PWM}	2.5	5.0	V	
	Low Level	V_{BL_PWM}	0	0.5	V	
PWM Control Frequency	F_{PWM}	200	-	2,000	Hz	
Duty Ratio		1	-	100	%	

Notes :

1. Power supply voltage 12V for LED driver.

Calculator value for reference $IF \times VF \times 66 / \text{driver efficiency} = P_{LED}$

2. The LED life-time define as the estimated time to 50% degradation of initial luminous.

3. Measure condition (Figure 5)

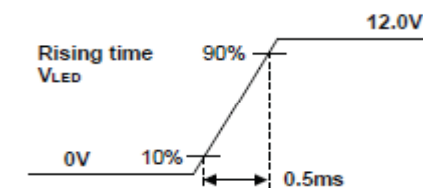


Figure 5. Inrush Measure Condition

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3.3 LED Structure

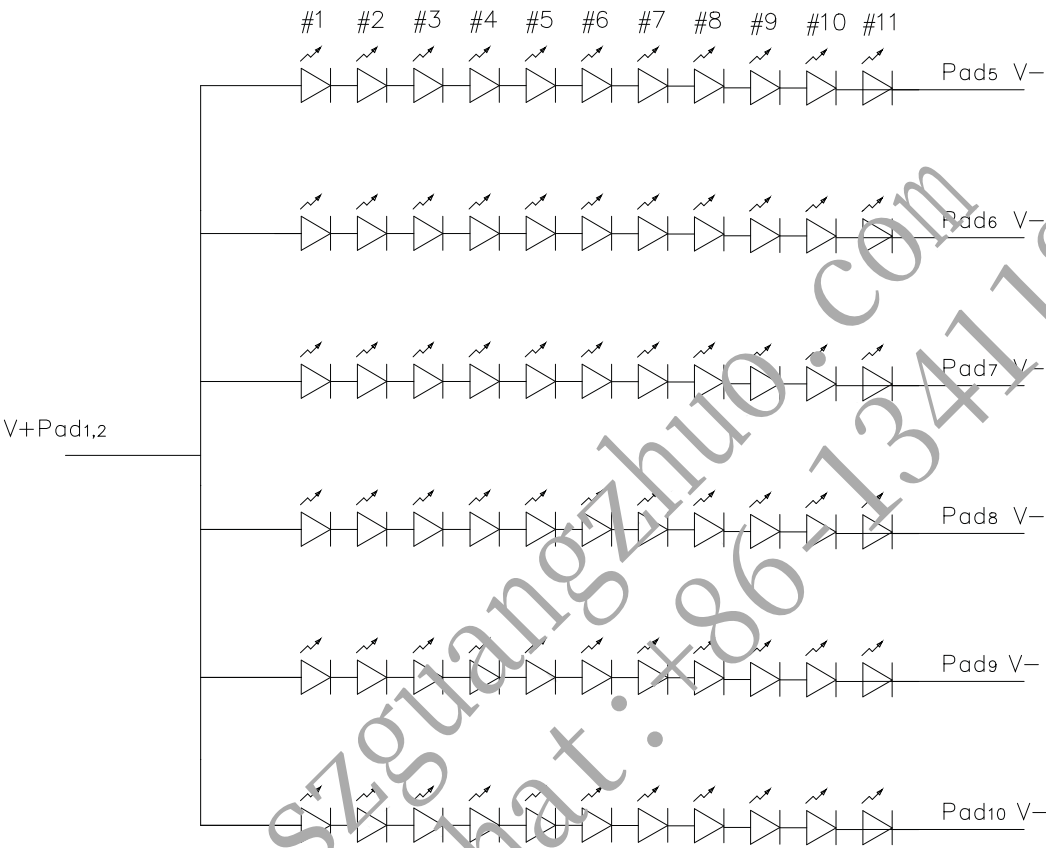


Figure 6. LED Structure

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4.0 OPTICAL SPECIFICATION

4.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = $25 \pm 2^\circ\text{C}$) with the equipment of luminance meter system (PR730&PR810) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0° . We refer to $\theta\Phi=0$ ($=\theta_3$) as the 3 o'clock direction (the "right"), $\theta\Phi=90$ ($=\theta_{12}$) as the 12 o'clock direction ("upward"), $\theta\Phi=180$ ($=\theta_9$) as the 9 o'clock direction ("left") and $\theta\Phi=270$ ($=\theta_6$) as the 6 o'clock direction ("bottom"). While scanning θ and/or Φ , the center of the measuring spot on the display surface shall stay fixed. The backlight should be operating for 30 minutes prior to measurement. VDD shall be $3.3 \pm 0.3\text{V}$ at 25°C .

4.2 Optical Specifications

<Table 5. Optical Specifications>

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ_3	$CR > 10$	80	89	-	Deg.	Note 1
		Θ_9		80	89	-	Deg.	
	Vertical	Θ_{12}		80	89	-	Deg.	
		Θ_6		80	89	-	Deg.	
Luminance Contrast Ratio		CR	$\Theta = 0^\circ$	800	1000	-		Note 2
Luminance of White	5 Points&Center	Y_w	$\Theta = 0^\circ$ $H, ED = 13\text{mA}$	255	300	345	cd/m ²	Note 3
White Luminance Uniformity	5 Points	ΔY_5		80	-	-	%	Note 4
	13 Points	ΔY_{13}		66.7	-	-	%	
White Chromaticity		W_x	$\Theta = 0^\circ$	0.283	0.313	0.343		Note 5
		W_y		0.299	0.329	0.359		
Reproduction of Color	Red	P_x	$\Theta = 0^\circ$	Typ.-0.03	0.588	Typ.+0.03		
		R_x			0.365			
	G_x	0.346						
	Green	G_y			0.582			
		B_x			0.161			
	Blue	B_y			0.115			
Color Gamut			42	45	-	%	CIE1976uv	
CCT				6000	-	7500		
Response Time (Rising + Falling)		T_{RT}	$T_a = 25^\circ\text{C}$ $\Theta = 0^\circ$	-	20	25	ms	Note 6
Cross Talk		CT	$\Theta = 0^\circ$	-	-	2.0	%	Note 7
Gamma		-	-	2.0	2.2	2.4	-	

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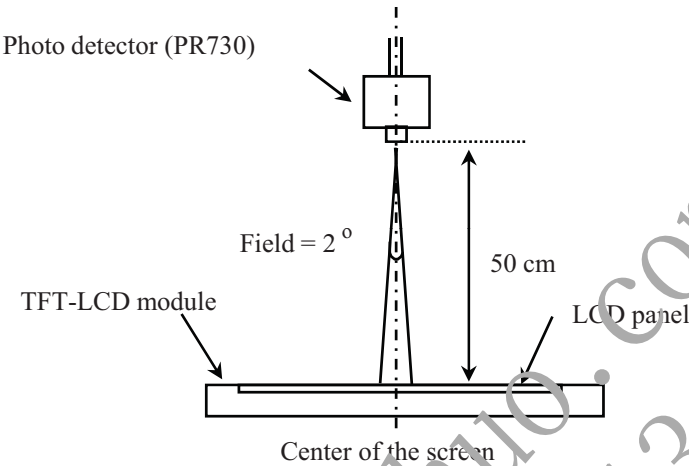
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Notes : - Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 7). - Contrast measurements shall be made at viewing angle of $\Theta = 0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see Figure 7) Luminance Contrast Ratio (CR) is defined mathematically. $CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$ - Center Luminance of white is defined as luminance values of 5 point average across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 8 for a total of the measurements per display. - The White luminance uniformity on LCD surface is then expressed as : $\Delta Y = \text{Minimum Luminance of 5(or 13) points} / \text{Maximum Luminance of 5(or 13) points.}$(see Figure 8 and Figure 9). - The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel. - The electro-optical response time measurements shall be made as Figure 10 by switching the “data” input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_r, and 90% to 10% is T_r. - Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark. (See Figure 11).			
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4.3 Optical Measurements



Optical characteristics measurement setup

Figure 7. Measurement Set Up

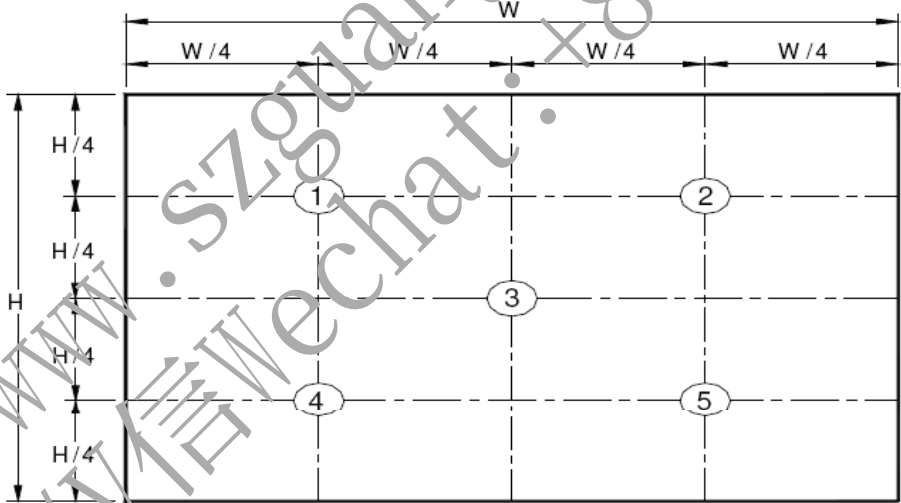


Figure 8. White Luminance and Uniformity Measurement Locations (5 points)

Center Luminance of white is defined as luminance values of center 5 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 7 for a total of the measurements per display.

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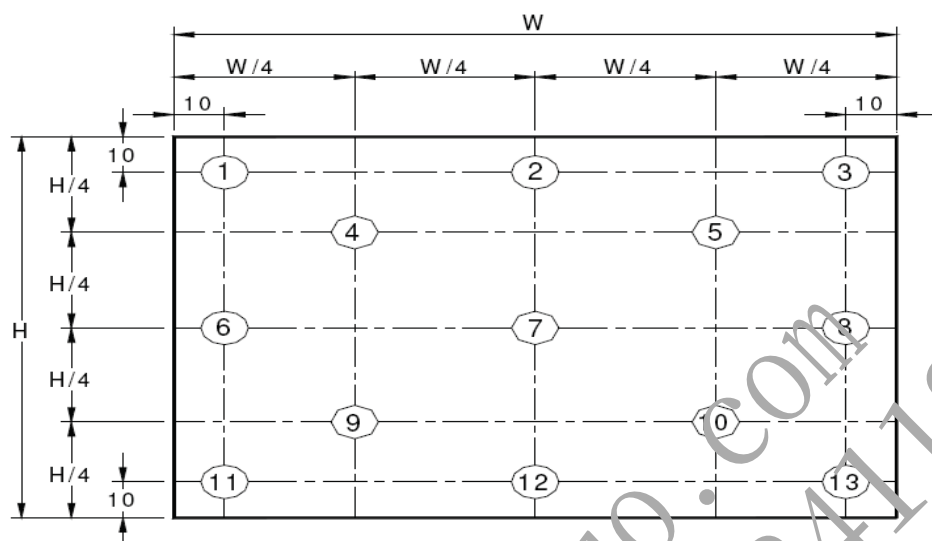


Figure 9. Uniformity Measurement Locations (13 points)

The White luminance uniformity on LCD surface is then expressed as : $\Delta Y5$ = Minimum Luminance of five points / Maximum Luminance of five points (see Figure 8) , $\Delta Y13$ = Minimum Luminance of 13 points / Maximum Luminance of 13 points (see Figure 9).

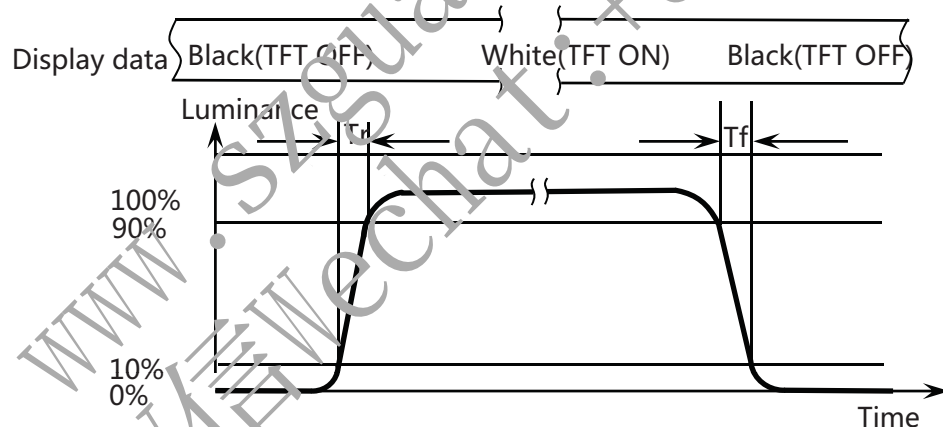


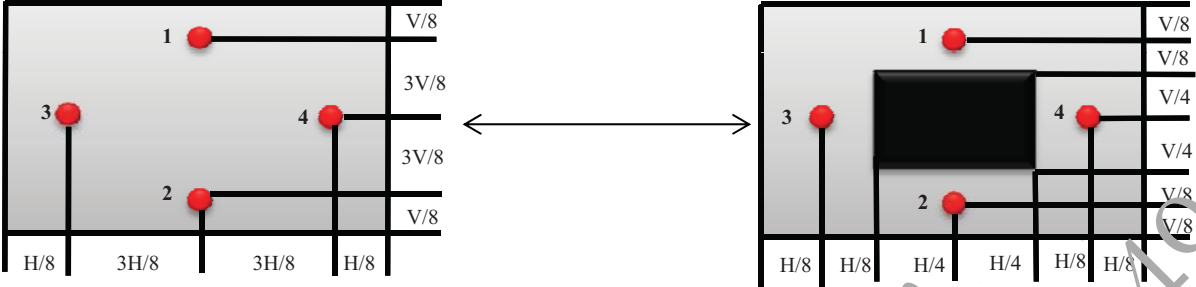
Figure 10. Response Time Testing

The electro-optical response time measurements shall be made as shown in Figure 10 by switching the “data” input signal ON and OFF. T_r : The luminance to change from 10% to 90% , T_f : The luminance to change from 90% to 10% .

The test system : LMS PR810

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Cross Talk (%) = $\left| \frac{Y_B - Y_A}{Y_A} \right| \times 100$

Figure 11. Cross Talk Modulation Test Description

Where:

- Y_A = Initial luminance of measured area (cd/m²)
- Y_B = Subsequent luminance of measured area (cd/m²)

The location 1/2/3/4 measured will be exactly the same in both patterns. The test background gray is from L64 to L192.Take the largest data as the result.

Cross Talk of one area of the LCD surface by another shall be measured by comparing the luminance (Y_A) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (Y_B) of that same area when any adjacent area is driven dark.(Refer to Figure 11)

The test system: PR730

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5.0 INTERFACE CONNECTION

5.1 Electrical Interface Connection

The electronics interface connector is C&T W05030-30P-H.

The connector interface pin assignments are listed in Table 6.

<Table 6. Pin Assignments for the Interface Connector>

Terminal	Symbol	Functions
Pin No.	Symbol	Description
1	NC	No Connection
2	H_GND	Ground
3	LANE1_N	eDP RX Channel 1 Negative
4	LANE1_P	eDP RX Channel 1 Positive
5	H_GND	Ground
6	LANE0_N	eDP RX Channel 0 Negative
7	LANE0_P	eDP RX Channel 0 Positive
8	H_GND	Ground
9	AUX_CH_P	eDP AUX CH Positive
10	AUX_CH_N	eDP AUX CH Negative
11	H_GND	Ground
12	LCD_VCC	Power Supply, 3.3V (typ.)
13	LCD_VCC	Power Supply, 3.3V (typ.)
14	BIST	Panel Self Test Enable
15	H_GND	Ground
16	H_GND	Ground
17	HPD	Hot Plug Detect Output
18	BL_GND	LED Ground
19	BL_GND	LED Ground
20	BL_GND	LED Ground
21	BL_GND	LED Ground
22	BL_ENABLE	LED Enable Pin(+3.3V Input)
23	BL_PWM	System PWM Signal Input
24	NC	No Connection
25	NC	No Connection
26	BL_POWER	LED Power Supply 5V-21V
27	BL_POWER	LED Power Supply 5V-21V
28	BL_POWER	LED Power Supply 5V-21V
29	BL_POWER	LED Power Supply 5V-21V
30	NC	No Connection

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5.2 eDP Interface

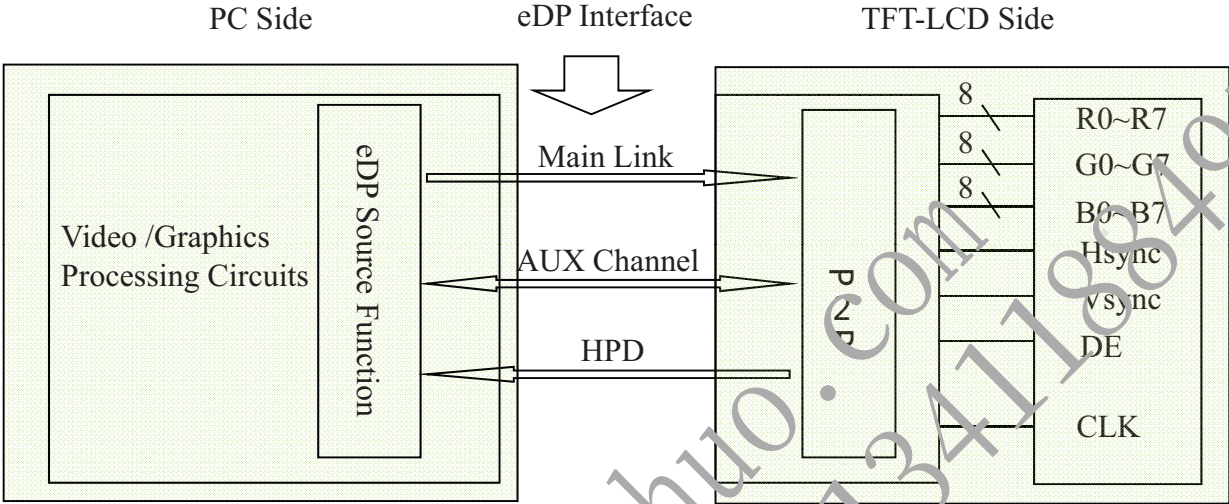


Figure 12. eDP Interface Architecture

Note:
Transmitter : Parade DP501 or equivalent.
Transmitter is not contained in module.

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5.3 Data Input Format

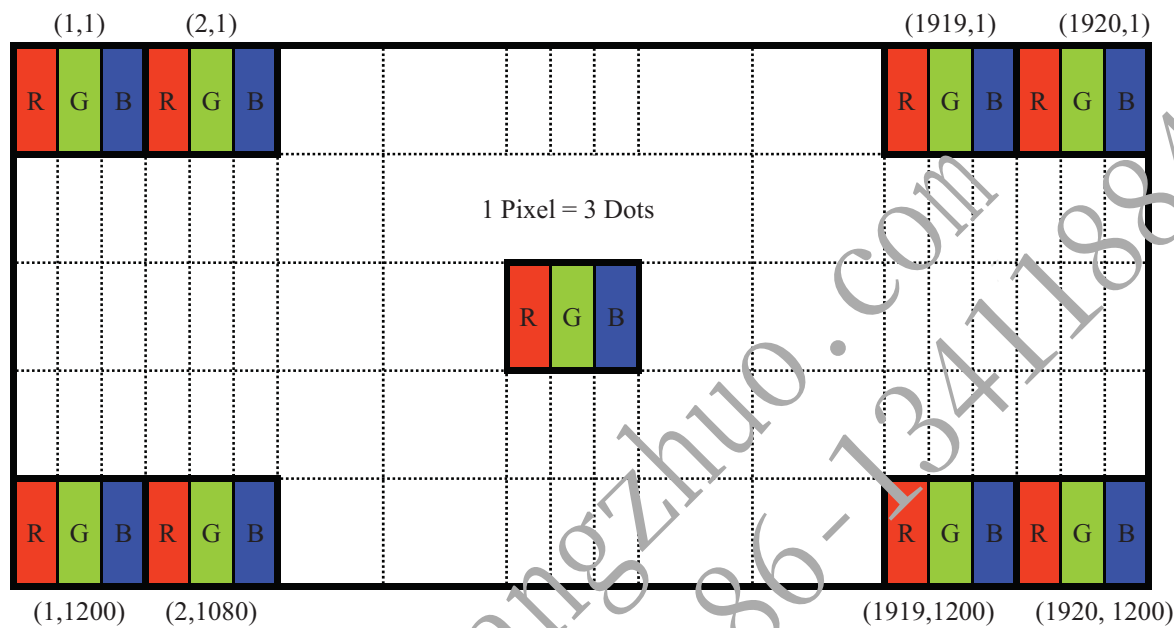


Figure 13. Display Position of Input Data (V-H)

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5.4 Back-light & LCM Interface Connection

BLU Interface Connector: STM MSAK24037P10D .

<Table 7. Pin Assignments for the BLU Connector>

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vout	LED anode connection	6	LED	LED cathode connection
2	Vout	LED anode connection	7	LED	LED cathode connection
3	NC	No Connection	8	LED	LED cathode connection
4	GND	GND	9	LED	LED cathode connection
5	LED	LED cathode connection	10	LED	LED cathode connection

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6.0 SIGNAL TIMING SPECIFICATION

6.1 The NV140WUM-N4H V8.0 Is Operated By The DE Only

< Table 8. Signal Timing Specification >

Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	160.76	161.78	162.8	MHz
Frame Period		Tv	1255	1260	1265	lines
			-	60	-	Hz
			-	16.67	-	ms
Vertical Display Period		Tvd	-	1200	-	lines
One line Scanning Period		Th	2135	2140	2145	clocks
Horizontal Display Period		Thd	-	1920	-	clocks

Note : The above is as optimized setting.

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6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 9.

<Table 9. eDP Main-Link RX TP4 Package Pin Parameters>

Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock (Link clock down-spreading)	SSC	-	-	0.5	%	
Differential peak-to-peak input voltage at package pins	VRX-DIFFp-p	120	-	1200	mV	
Rx input DC common mode voltage	VRX_DC_CM	0	-	2	V	
Differential termination resistance	RRX-DIFF	80	-	100	Ω	
Single-ended termination resistance	RRX-SE	40	-	60	Ω	
Rx short circuit current limit	IRX_SHORT		-	20	mA	
Intra-pair skew at Rx package pins (HBR) RX intra-pair skew tolerance at HBR	LRX_SKEW INTRA_PAIR	-	-	60	ps	
AC Coupling Capacitor	CSCURCE_ML	75		200	nF	Source side

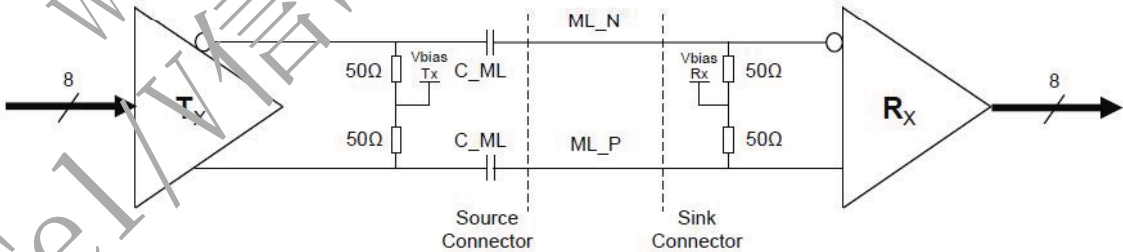


Figure 14. Main link differential pair

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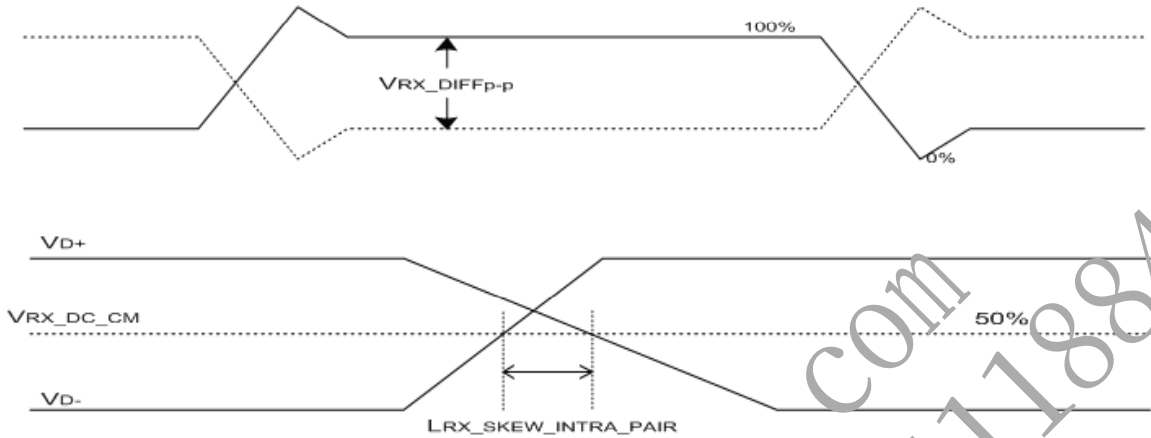


Figure 15. VRX-DIFFp-p & LRX_SKEW_INTRA_PAIR

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<Table 10. HPD Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
HPD voltage	V _{HPD}	2.25	-	3.6	V	
Hot Plug Detection Threshold	-	2.0	-	-	V	Source side Detecting
Hot Unplug Detection Threshold	-	-	-	0.8V	V	
HPD_IRQ Pulse Width	HPD_IRQ	0.5	-	1	ms	
HPD_TimeOut	-	2.0	-	-	ms	

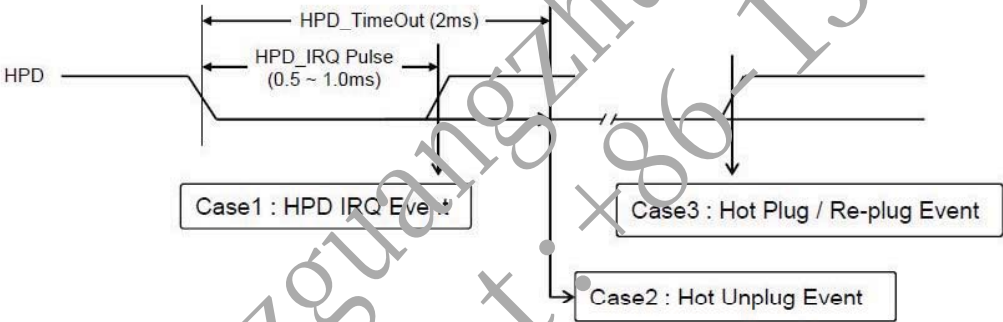


Figure 16. HPD Events

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<Table 11. AUX Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
AUX unit interval	UIAUX	0.4	0.5	0.6	Us	
AUX peak-to-peak input differential voltage	VAUX-RX-DIFFp-p	0.29	-	1.38	V	
AUX CH termination DC resistance	RAUX-TERM	80	100	120	Ohm	
AUX DC common mode voltage	VAUX-DC-CM	0	-	2	V	
AUX turn around common mode voltage	VAUX-TURN-CM	-	-	0.3	V	
AUX short circuit current limit	IAUX-SHORT	-	-	90	mA	
AUX AC Coupling Capacitor	CSOURCE-AUX	75	-	200	nf	Source side

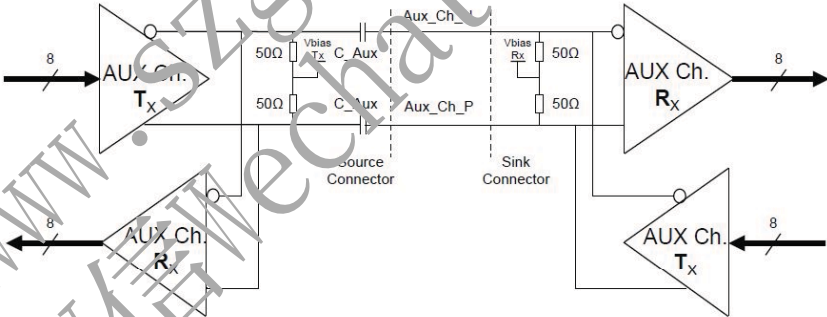


Figure 17. AUX differential pair

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7.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

<Table 12. Input Signal & Basic Display Colors & Gray Scale of Colors >

	Colors & Gray scale	Data signal																							
		R0 R1 R2 R3 R4 R5 R6 R7	G0 G1 G2 G3 G4 G5 G6 G7	B0 B1 B2 B3 B4 B5 B6 B7																					
Basic colors	Black	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																					
	Blue	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1																					
	Green	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0																					
	Light Blue	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1																					
	Red	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																					
	Purple	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1																					
	Yellow	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0																					
	White	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1																					
Gray scale of Red	Black	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																					
	△	1 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																					
	Darker	0 1 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																					
	△		↑																						
	▽		↓																						
	Brighter	1 0 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																					
	▽	0 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																					
	Red	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																					
Gray scale of Green	Black	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																					
	△	0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																					
	Darker	0 0 0 0 0 0 0 0	0 1 0 0 0 0 0 0	0 0 0 0 0 0 0 0																					
	△		↑																						
	▽		↓																						
	Brighter	0 0 0 0 0 0 0 0	1 0 1 1 1 1 1 1	0 0 0 0 0 0 0 0																					
	▽	0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0																					
	Green	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0																					
Gray scale of Blue	Black	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																					
	△	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0																					
	Darker	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 1 0 0 0 0 0 0																					
	△		↑																						
	▽		↓																						
	Brighter	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 0 1 1 1 1 1 1																					
	▽	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1																					
	Blue	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1																					
Gray scale of White& Black	Black	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																					
	△	1 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0																					
	Darker	0 1 0 0 0 0 0 0	0 1 0 0 0 0 0 0	0 1 0 0 0 0 0 0																					
	△		↑																						
	▽		↓																						
	Brighter	1 0 1 1 1 1 1 1	1 0 1 1 1 1 1 1	1 0 1 1 1 1 1 1																					
	▽	0 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1																					
	White	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1																					

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8.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below.

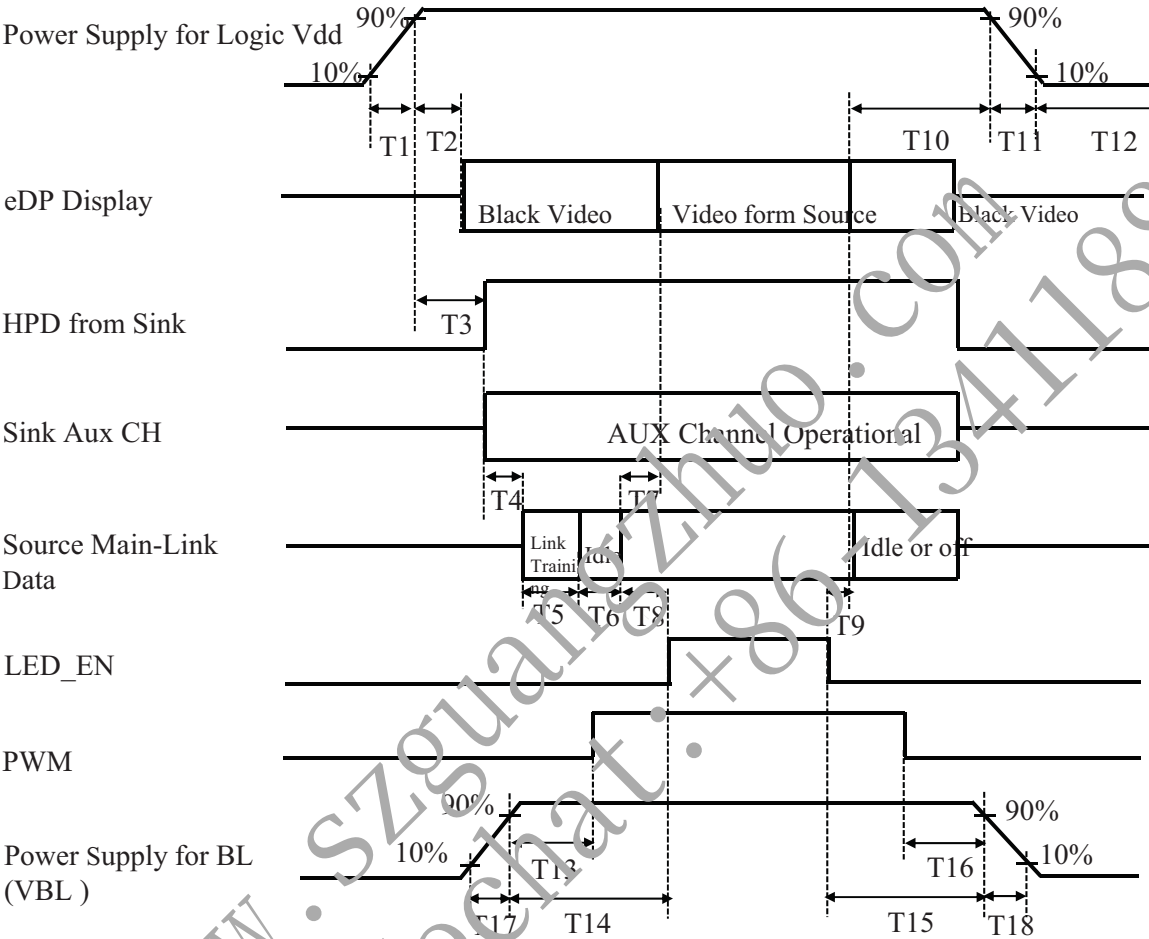


Figure 18. Power Sequence

- $0.5\text{ms} \leq T1 \leq 10\text{ms}$
- $0\text{ms} < T2 \leq 200\text{ms}$
- $0\text{ms} < T3 \leq 200\text{ms}$
- $T4+T5+T6+T8 \geq 80\text{ms}$
- $0\text{ms} < T7 \leq 50\text{ms}$
- $50\text{ms} < T8$
- $0\text{ms} < T9$
- $100\text{ms} < T10 < 500\text{ms}$
- $0.5\text{ms} \leq T11 \leq 10\text{ms}$
- $500\text{ms} \leq T12$
- $0\text{ms} < T13$
- $0\text{ms} < T14$
- $0\text{ms} < T15$
- $0\text{ms} < T16$
- $0.5\text{ms} \leq T17$
- $0.5\text{ms} \leq T18$

Notes:

1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal are valid.

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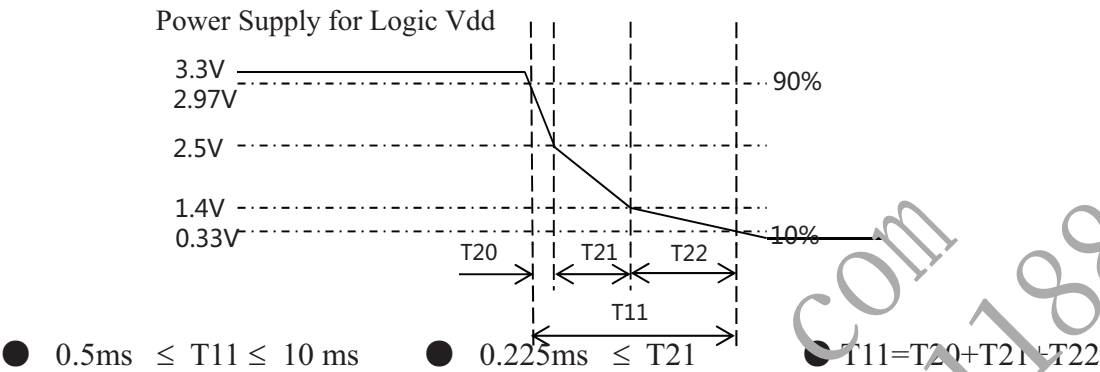


Figure 19. T11 timing requirements

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9.0 Connector Description

Physical interface is described as for the connector on LCM.
These connectors are capable of accommodating the following signals and will be following components

9.1 TFT LCD Module

< Table 13. Signal Connector >

Connector Name /Description	For Signal Connector
Manufacturer	C&T
Type/ Part Number	W05030-20F-H
Mating Housing/ Part Number	I-PEX 20454-030T

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10.0 MECHANICAL CHARACTERISTICS

10.1 Dimensional Requirements

Figure 23 shows mechanical outlines for the model NV140WUM-N4H V8.0.
Other parameters are shown in Table 14.

<Table 14. Dimensional Parameters>

Parameter	Specification	Unit
Active Area	301.5936(H) × 188.496mm (V)	mm
Number of pixels	1920 (H) × 1200 (V)	pixels
Pixel pitch	157.08(H) × 157.08 (V)	um
Pixel arrangement	RGB Vertical stripe	
Display colors	16.2M (6bit+2FRC)	
Display mode	Normally black	
Dimensional outline	306.59 ± 0.3(H) * 197.5 ± 0.3 (V) (W/O PCB) * 3.0(Max) 306.59 ± 0.3(H) * 205 ± 0.5 (V) (W/PCB) * 3.0(Max)	mm
Weight	300 (max)	g

10.2 Mounting

See Figure 24.

10.3 Anti-Glare and Polarizer Hardness.

The surface of the LCD has an Anti-Glare coating treatment with 3H hardness to Minimize reflection and to reduce scratching.

10.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 300lux.

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11.0 RELIABILITY TEST

The reliability test items and its conditions are shown in below.

<Table 15. Reliability Test>

No	Test Items	Conditions
1	High temperature storage test	Ta = 60°C , 60%RH, 240 hrs
2	Low temperature storage test	Ta = -20°C , 240 hrs
3	High temperature & high humidity operation test	Ta = 50°C , 80%RH, 240 hrs
4	High temperature operation test	Ta = 50°C , 60%RH, 240 hrs
5	Low temperature operation test	Ta = 0°C , 240 hrs
6	Thermal shock	Ta = -20 °C ↔ 60 °C (0.5 hr), 60% ± 3%RH, 100 cycle
7	Vibration test (non-operating)	Ta = 25°C , 60%RH, 1.5G, 10~500Hz, Sine X,Y,Z / Sweep rate : 1 hour
8	Shock test (non-operating)	Ta = 25 °C , 60%RH, 220G, Half Sine Wave 2msec ± X, ± Y ± Z Once for each direction
9	Electro-static discharge test (operating)	Air : 150 pF, 330Ω, ± 15 KV Contact : 150 pF, 330Ω, ± 8 KV Ta = 25 °C , 60%RH,

Notes :

1. The fixture must be hard enough , so that the module would not be twisted or bent.
2. Self- recovery and restart recovery is allowed. No hardware failures.

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12.0 HANDLING & CAUTIONS

- (1) Cautions when taking out the module
 - Pick the pouch only, when taking out module from a shipping package.
- (2) Cautions for handling the module
 - As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
 - As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
 - As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
 - Do not pull the interface connector in or out while the LCD module is operating.
 - Put the module display side down on a flat horizontal plane.
 - Handle connectors and cables with care.
- (3) Cautions for the operation
 - When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
 - Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.
- (4) Cautions for the atmosphere
 - Dew drop atmosphere should be avoided.
 - Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.
- (5) Cautions for the module characteristics
 - Do not apply fixed pattern data signal to the LCD module at product aging.
 - Applying fixed pattern for a long time may cause image sticking.
- (6) Other cautions
 - Do not disassemble and/or re-assemble LCD module.
 - Do not re-adjust variable resistor or switch etc.
 - When returning the module for repair or etc. Please pack the module not to be broken. We recommend to use the original shipping packages.

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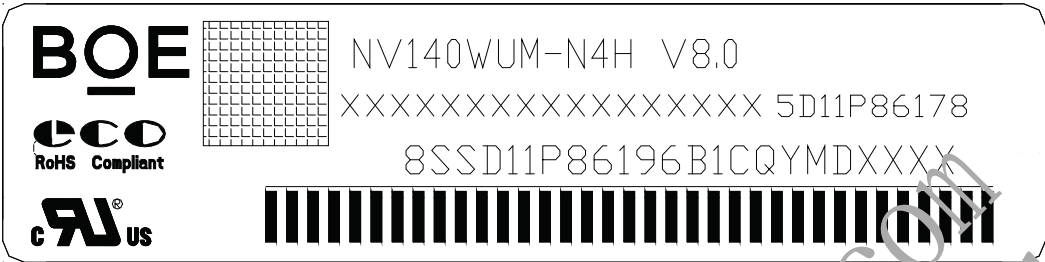
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13.0 LABEL

(1) Product Label



标签尺寸: 48mm × 12mm, 厚度0.075mm

- 1. FG-CODE: NV140WUM-N4H V8.0
- 2. FRU码 : 5D11P86178; PN码 : SD11P86196
- 3. MDL ID(厂内信息)
- 4. PPID 8S码 : SD11P86196
- 5. MDL ID 条纹码(厂内信息)
- 6. PPID对应二维码(客户端信息)

<Table 16. Module ID Naming Rule>

MDL ID 编码规则

序号号	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
代码	X	X	X	3	X	X	X	3	S	P	0	X	X	X	X	X	X
描述	GBN代 码		等级	B3	年	月	日	FG Code后四位				序列号					

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(2) High voltage caution label

	HIGH VOLTAGE CAUTION	COLD CATHODE FLUORESCENT LAMP IN LCD PANEL CONTAINS A SMALL AMOUNT OF MERCURY. PLEASE FOLLOW LOCAL OR- DINANCES OR REGULATIONS FOR DISPOSAL.
	RISK OF ELECTRIC SHOCK. DISCONNECT THE ELECTRIC POWER BEFORE SERVICING	

Figure 21. High Voltage Caution Label

(3) Box label



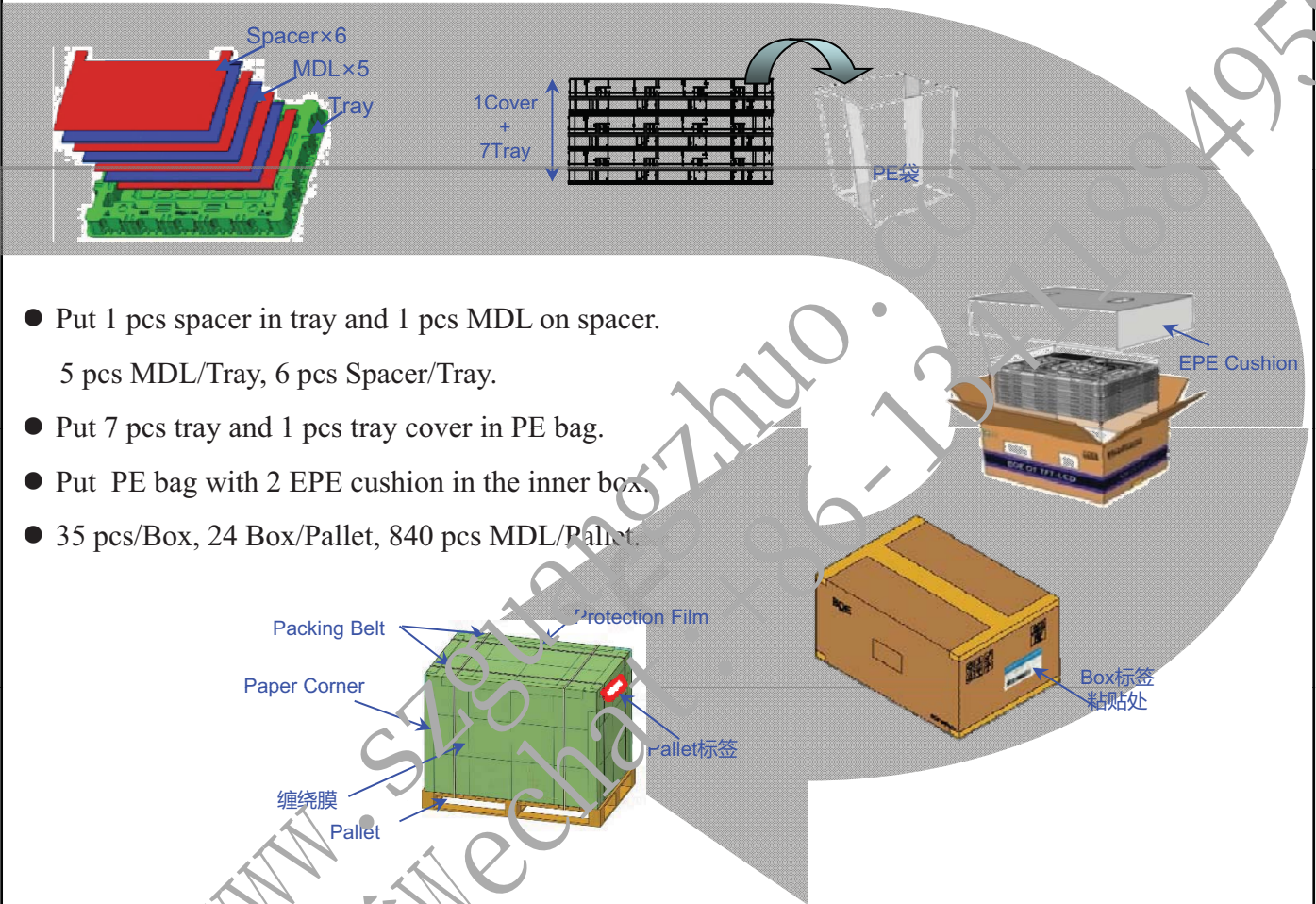
Figure 22. Box Label

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14.0 PACKING INFORMATION

14.1 Packing Order



- Put 1 pcs spacer in tray and 1 pcs MDL on spacer.
5 pcs MDL/Tray, 6 pcs Spacer/Tray.
- Put 7 pcs tray and 1 pcs tray cover in PE bag.
- Put PE bag with 2 EPE cushion in the inner box.
- 35 pcs/Box, 24 Box/Pallet, 840 pcs MDL/Pallet.

Figure 23. Packing Order

14.2 Note

- Box dimension: 440mm*328mm*300mm
- Package quantity in one box: 35 pcs
- Total weight: 8.1 kg/Box

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15.0 MECHANICAL OUTLINE DIMENSION

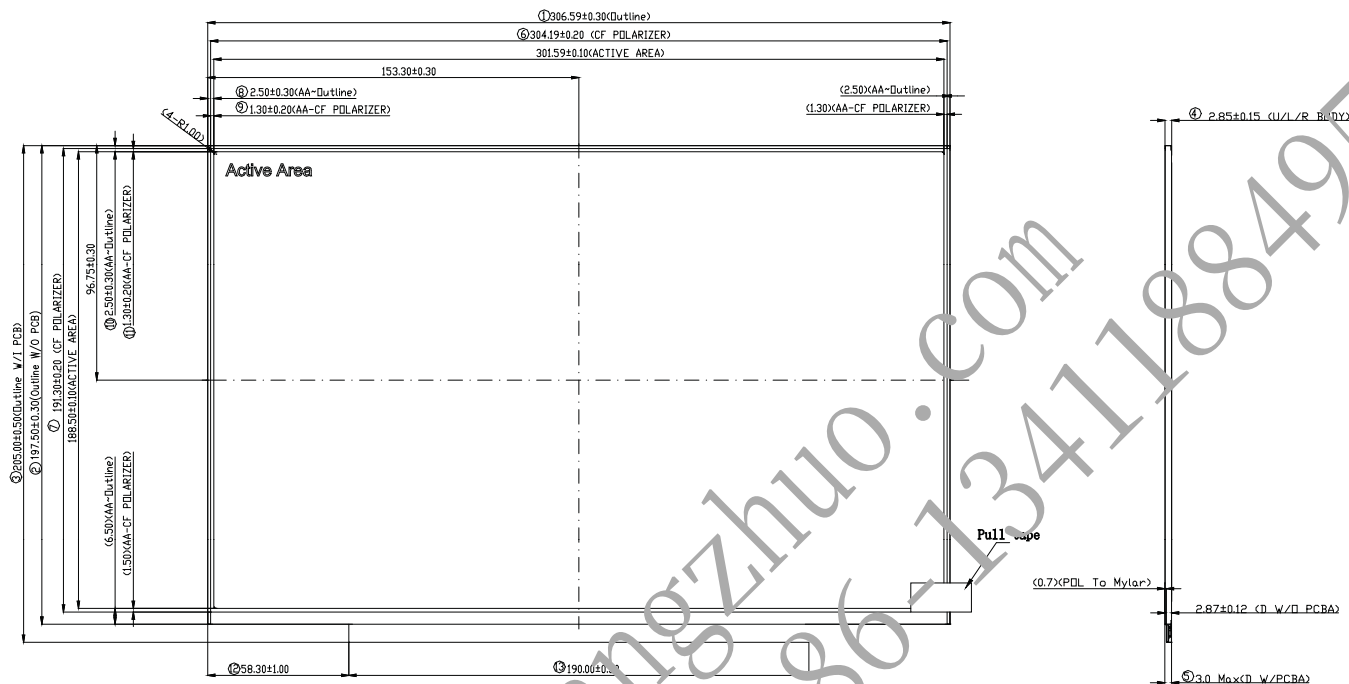


Figure 24. TTT-LCD Module Outline Dimension (Front View)

Notes:

1. Warpage and deformation Spec.: 0.5mm Max.
2. The eDP connector is measured at PIN 1 and mating line.
3. Unspecified tolerance refer to ± 0.3 mm.
4. Top polarizer is the highest portion.
5. Critical dimension: ① ~ ④5 CPK: ① ~ ④5
6. Do not have light leakage on four corners of module.
7. Measurement method refer to Appendix A
8. System matching refer to Appendix B
9. “()”marks the reference dimensions.
10. Cell tape and polarizer step tolerance is 0.075 ± 0.026 mm for L/R/U portion.

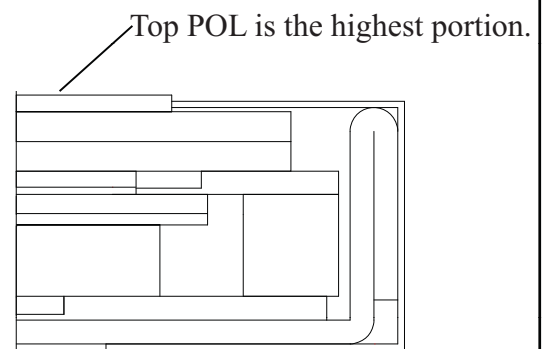


Figure 25. Highest Point Position

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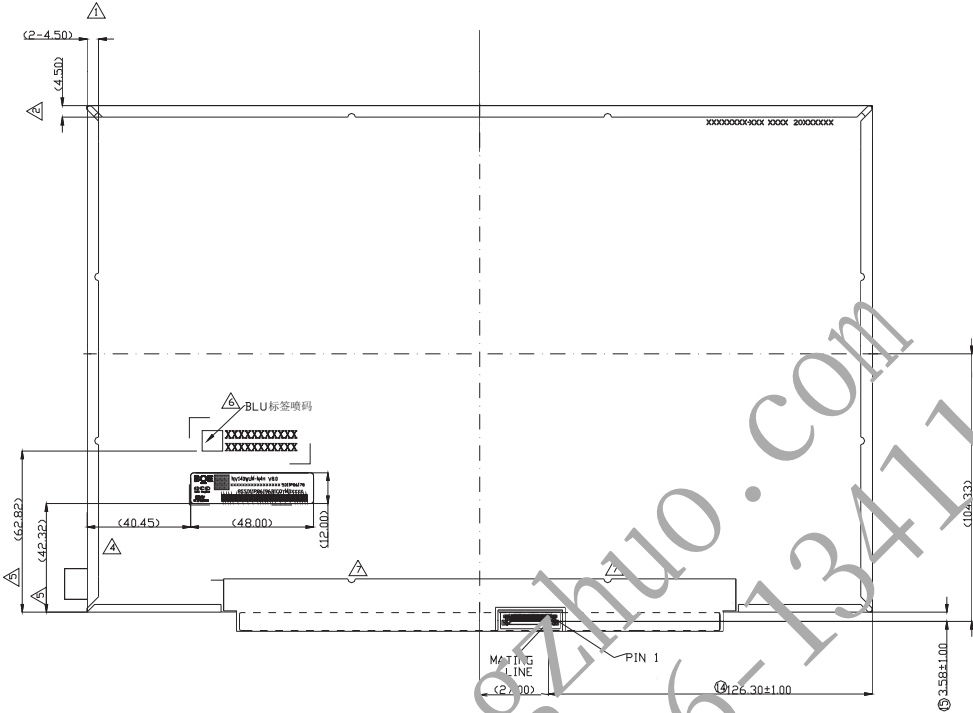


Figure 26. TFT-LCD Module Outline Dimensions (Rear view)

- Notes:
- 1. Warpage and deformation Spec.: 0.5mm Max.
 - 2. The eDP connector is measured at PIN 1 and mating line.
 - 3. Unspecified tolerance refer to $\pm 0.3\text{ mm}$.
 - 4. Top polarizer is the highest portion.
 - 5. Critical dimension: ① ~ ⑤ CPK: ① ~ ⑤
 - 6. Do not have light leakage on four corners of module.
 - 7. Measurement method refer to Appendix A
 - 8. System matching refer to Appendix B
 - 9. “()”marks the reference dimensions.
 - 10. Cell tape and polarizer step tolerance is $0.075\pm 0.026\text{mm}$ for L/R/U portion.

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16.0 EDID Table

Address (HEX)	Function	Hex	Dec	crc	Input values.	Notes
00	Header	00	0		0	EDID Header
01		FF	255		255	
02		FF	255		255	
03		FF	255		255	
04		FF	255		255	
05		FF	255		255	
06		FF	255		255	
07		00	0		0	
08	ID Manufacturer Name	09	9		BOE	ID = BOE
09		E5	229			
0A	ID Product Code	E3	227		3299	ID 3299
0B		0C	12			
0C	32-bit serial No.	00	0		0	
0D		00	0		0	
0E		00	0		0	
0F		00	0		0	
10	Week of manufacture	0C	12		1	
11	Year of Manufacture	22	34		2024	Manufactured in 2024
12	EDID Structure Ver.	01	1		1	EDID Ver 1.0
13	EDID revision #	04	4		4	EDID Rev. 0.4
14	Video input definition	A5	165		-	Refer to right table
15	Max H image size	1E	30		30	30.15936 cm (Approx)
16	Max V image size	13	19		19	18.8496 cm (Approx)
17	Display Gamma	78	120		2.2	Gamma curve = 2.2
18	Feature support	03	3		-	Refer to right table
19	Red/Green low bits	A0	168		-	Red / Green Low Bits
1A	Blue/White low bits	65	101		-	Blue / White Low Bits
1B	Red x high bits	96	150	602	0.588	Red (x) = 10010110 (0.588)
1C	Red y high bits	5D	93	374	0.365	Red (y) = 01011101 (0.365)
1D	Green x high bits	58	88	354	0.346	Green (x) = 01011000 (0.346)
1E	Green y high bits	95	149	596	0.582	Green (y) = 10010101 (0.582)
1F	Blue x high bits	29	41	165	0.161	Blue (x) = 00101001 (0.161)
20	Blue y high bits	1D	29	118	0.115	Blue (y) = 00011101 (0.115)
21	White x high bits	50	80	321	0.313	White (x) = 01010000 (0.313)
22	White y high bits	54	84	337	0.329	White (y) = 01010100 (0.329)
23	Established timing 1	00	0		-	Refer to right table
24	Established timing 2	00	0		-	
25	Established timing 3	00	0		-	

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26	Standard timing #1	01	1			Not Used	
27		01	1				
28	Standard timing #2	01	1			Not Used	
29		01	1				
2A	Standard timing #3	01	1			Not Used	
2B		01	1				
2C	Standard timing #4	01	1			Not Used	
2D		01	1				
2E	Standard timing #5	01	1			Not Used	
2F		01	1				
30	Standard timing #6	01	1			Not Used	
31		01	1				
32	Standard timing #7	01	1			Not Used	
33		01	1				
34	Standard timing #8	01	1			Not Used	
35		01	1				
36	Detailed timing/monitor descriptor #1	33	51		161.8	161.784MHz Main clock	
37		3F	63				
38		80	128		1920	Hor Active = 1920	
39		DC	220		220	Hor Blanking = 220	
3A		70	112		-	4 bits of Hor. Active + 4 bits of Hor. Blanking	
3B		B0	120		1200	Ver Active = 1200	
3C		30	60		60	Ver Blanking = 60	
3D		40	64		-	4 bits of Ver. Active + 4 bits of Ver. Blanking	
3E		30	48		48	Hor Sync Offset = 48	
3F		20	32		32	H Sync Pulse Width = 32	
40		30	64		3	V sync Offset = 3 line	
41		00	0		6	V Sync Pulse width : 6 line	
42		2E	46		302	Horizontal Image Size = 301.5936 mm (Low 8 bits)	
43		3C	188		188	Vertical Image Size = 188.496 mm (Low 8 bits)	
44		10	16		-	4 bits of Hor Image Size + 4 bits of Ver Image Size	
45		00	0		0	Hor Border (pixels)	
46	00	0		0	Vertical Border (Lines)		
47	1A	26		-	Refer to right table		

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48	Detailed timing/monitor descriptor #2	00	0		-	Indicates descriptor is a display Descriptor	
49		00	0		-		
4A		00	0		-	Reserved	
4B		FD	253		-	Tag Number for Display Range Limits Descriptor	
4C		00	0		0	Vertical/Horizontal Rate Offset are zero	
4D		28	40		40	Minimum Vertical Rate:40 Hz	
4E		3C	60		60	Maximum Vertical Rate:60 Hz	
4F		4C	76		75.6	Minimum Horizontal Rate:75.6 kHz	
50		4C	76		75.6	Maximum Horizontal Rate:75.6 kHz	
51		10	16		161.78	Maximum Pixel Clock:161.784 MHz	
52		01	1		-	Range Limits Only	
53		0A	10		-	Display Range Limits & CVT Support Definition	
54		20	32		-		
55		20	32		-		
56		20	32		-		
57		20	32		-		
58		20	32		-		
59		20	32		-		
5A		Detailed timing/monitor descriptor #3	00	0			Indicates descriptor #3 is a display Descriptor
5B	00		0				
5C	00		0			Reserved	
5D	FE		254			Tag : ASCII String	
5E	00		0			Reserved	
5F	42		60		B	Manufacture name : BOECQ	
60	4F		79		O		
61	45		69		E		
62	20		32				
63	43		67		C		
64	51		80		Q		
65	0A		10				
66	20		32				
67	20		32				
68	20	32					
69	20	32					
6A	20	32					
6B	20	32					

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6C	Detailed timing/monitor descriptor #4	00	0			Indicates descriptor #4 is a display Descriptor	
6D		00	0				
6E		00	0			Reserved	
6F		FC	252			Tag : ASCII String	
70		00	0			Reserved	
71		4E	78		N		
72		56	86		V		
73		31	49		1		
74		34	52		4		
75		30	48		0		
76		57	87		W		
77		55	85		U	Model name : NV140WUM-N4H	
78		4D	77		M		
79		2D	45		-		
7A		4E	78		N		
7B		34	52		4		
7C	48	72		H			
7D	0A	10					
7E	Extension flag	01	1		1	0 : 1↑EDID; 1 : N↑EDID	
7F	Checksum	64	100	100	-		
80	DID Extension Header	70	112		112	Display ID EDID Extension Block tag	
81		20	32		32	Display ID Version/Revision = 7.0	
82		79	121		121	Section Size (byte) = 121 bytes	
83		02	2		2	Display Product Primary Use Case	
84		00	0		0	Extension count	
85	DID Block #1 Header	81	129		129	DID2.0 Data block tag[81h] = CTA DisplayID	
86		00	0		0	Block revision = Revision 0	
87		15	21		21	Number of Payload Bytes in block= 19 Bytes	
88	DID DATA Block #1 AMD VSDB	74	116		116	CTA Block1 Tag Code and Block1 Length = Vendor Specific Data Block(03h), Size(byte) = 18 bytes	
89		1A	26		26	AMD IEEE OUI value (0x00001A)	
8A		00	0		26	(Hex. LSB first)	
8B		00	0		26	(Hex. LSB first)	
8C		03	3		3	AMD VSDB Version 3	
8D		01	1		1	Indicate AMD FreeSync™ function capability.	
8E		2B	40		40	Min Refresh Rate	
8F		3C	60		60	Max Refresh Rate	
90		00	0		0	FreeSync MCCS VCP Code	
91		00	0		0	Indicate AMD FreeSync™ Premium PRO capability.	
92		53	81		300	Max Luminance 1 (for HDR) = 300nit	
93		51	81		0.3	Max Luminance 2 (for HDR) = 0.3nit	
94		53	83		300	Max Luminance 2 (for HDR) = 300nit	
95		51	81		0.3	Max Luminance 2 (for HDR) = 0.3nit	
96		3C	60		60	Bits 7:0 -FreeSync Maximum Refresh Rate (MSB)	
97		00	0			Bits 9:8 - MSB FreeSync Maximum refresh rate [Hz]	
98		00	0		0	Maximum Fast Transport Input Pixel Rate [kHz] - bits 7:0	
99		00	0			Maximum Fast Transport Input Pixel Rate [kHz] - bits 15:8	
9A	00	0		Maximum Fast Transport Input Pixel Rate [kHz] - bits 23:16			
9B	80	128		0	Additional Sink information offset DP/eDP Port: offset from DPCD 0x403		
9C	00	0		0	eDP Display Features Handshake DPCD offset, eDP Port: offset from DPCD 0x380		
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9D		00	0		0	Reseved	
9E		00	0		0	Reseved	
9F		00	0		0	Reseved	
A0		00	0		0	Reseved	
A1		00	0		0	Reseved	
A2		00	0		0	Reseved	
A3		00	0		0	Reseved	
A4		00	0		0	Reseved	
A5		00	0		0	Reseved	
A6		00	0		0	Reseved	
A7		00	0		0	Reseved	
A8		00	0		0	Reseved	
A9		00	0		0	Reseved	
AA		00	0		0	Reseved	
AB		00	0		0	Reseved	
AC		00	0		0	Reseved	
AD		00	0		0	Reseved	
AE		00	0		0	Reseved	
AF		00	0		0	Reseved	
B0		00	0		0	Reseved	
B1		00	0		0	Reseved	
B2		00	0		0	Reseved	
B3		00	0		0	Reseved	
B4		00	0		0	Reseved	
B5		00	0		0	Reseved	
B6		00	0		0	Reseved	
B7		00	0		0	Reseved	
B8		00	0		0	Reseved	
B9		00	0		0	Reseved	
BA		00	0		0	Reseved	
BB		00	0		0	Reseved	
BC		00	0		0	Reseved	
BD		00	0		0	Reseved	
BE		00	0		0	Reseved	
BF		00	0		0	Reseved	
C0		00	0		0	Reseved	
C1		00	0		0	Reseved	
C2		00	0		0	Reseved	
C3		00	0		0	Reseved	
C4		00	0		0	Reseved	
C5		00	0		0	Reseved	
C6		00	0		0	Reseved	
C7		00	0		0	Reseved	
C8		00	0		0	Reseved	
C9		00	0		0	Reseved	
CA		00	0		0	Reseved	
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CB		00	0		0	Reseved	
CC		00	0		0	Reseved	
CD		00	0		0	Reseved	
CE		00	0		0	Reseved	
CF		00	0		0	Reseved	
D0		00	0		0	Reseved	
D1		00	0		0	Reseved	
D2		00	0		0	Reseved	
D3		00	0		0	Reseved	
D4		00	0		0	Reseved	
D5		00	0		0	Reseved	
D6		00	0		0	Reseved	
D7		00	0		0	Reseved	
D8		00	0		0	Reseved	
D9		00	0		0	Reseved	
DA		00	0		0	Reseved	
DB		00	0		0	Reseved	
DC		00	0		0	Reseved	
DD		00	0		0	Reseved	
DE		00	0		0	Reseved	
DF		00	0		0	Reseved	
E0		00	0		0	Reseved	
E1		00	0		0	Reseved	
E2		00	0		0	Reseved	
E3		00	0		0	Reseved	
E4		00	0		0	Reseved	
E5		00	0		0	Reseved	
E6		00	0		0	Reseved	
E7		00	0		0	Reseved	
E8		00	0		0	Reseved	
E9		00	0		0	Reseved	
EA		00	0		0	Reseved	
EB		00	0		0	Reseved	
EC		00	0		0	Reseved	
ED		00	0		0	Reseved	
EE		00	0		0	Reseved	
EF		00	0		0	Reseved	
F0		00	0		0	Reseved	
F1		00	0		0	Reseved	
F2		00	0		0	Reseved	
F3		00	0		0	Reseved	
F4		00	0		0	Reseved	
F5		00	0		0	Reseved	
F6		00	0		0	Reseved	
F7		00	0		0	Reseved	
F8		00	0		0	Reseved	
F9		00	0		0	Reseved	
FA		00	0		0	Reseved	
FB		00	0		0	Reseved	
FC		00	0		0	Reseved	
FD		00	0		0	Reseved	
FE		D5	213			DisplayID section checksum (81h~FDh)	
FF		90	144			Extended block checksum (80h~FEh)	
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17.0 GENERAL PRECAUTIONS

17.1 HANDLING

- (1) When the module is assembled, It should be attached to the system firmly using every mounting holes.
Be careful not to twist or bend the modules.
- (2) Refrain from strong mechanical shock or any force to the module. Otherwise, it may cause improper operation or damage to the module.
- (3) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than 1 HB pencil lead.
- (4) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.
- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use Ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth .In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static , it may cause damage to the module.
- (9) Use fingerstalls with soft gloves to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Do not pull or fold the LED FPC.
- (12) Do not touch any component which is located on the back side.
- (13) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (14) Pins of connector shall not be touched directly with bare hands.

17.2 STORAGE

- (1) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃ and relative humidity of less than 70%.
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.

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17.3 OPERATION (1) Do not connect, disconnect the module in the “ Power On” condition. (2) Power supply should always be turned on/off by following item 8.0 “ Power on/off sequence “. (3) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference. (4) The standard limited warranty is only applicable when the module is used for general notebook applications. If used for purposes other than as specified, BOE is not to be held reliable for the defective operations. It is strongly recommended to contact BOE to find out fitness for a particular purpose. 17.4 OTHERS (1) Avoid condensation of water. It may result in improper operation or disconnection of electrode. (2) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation, Variation in part contents and environmental temperature, so on) Otherwise the module may be damaged. (3) If the module displays the same pattern continuously for a long period of time, it can be the situation when The “ image sticks” to the screen. (4) This module has its circuitry PCB’s on the rear or bottom side and should be handled carefully to avoid being stressed.			
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Appendix A

The Measurement Methods for the Dimensions of Module

1. Caliper:

- Thickness of Outline (Without/With PCB For Flat Project)
(Without PCB For Bend Project)
- Length of Outline (Without Tape Wrinkle or Bulged)
- Width of Outline (Without PCB) (Without Tape Wrinkle or Bulged)
- Width of Outline (With PCB)

2. Micrometer:

Thickness with PCB For Bend Project (Without FPC/COF Air Gap Effect)

3. Coordinate Measuring Machine:

- CF Polarizer Size
- Active Area (Or AA_BM) Size
- Active Area to Outline (Without Tape Wrinkle or Bulged)
- Active Area to CF Polarizer
- The Distance of Bracket Holes
- P-Cover to Outline (Without Tape Wrinkle or Bulged)
- Length of P-Cover
- Connector Pin 1 to Outline (Without Tape Wrinkle or Bulged)

4. Height Gauge: The Different Height of Root and Top on the Bracket
(Need to Calculate From Bracket Angle Spec.)

5. Feeler Gauge: The Warpage Spec. of Module

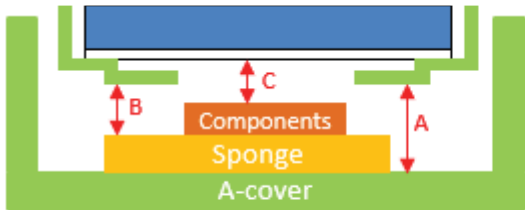
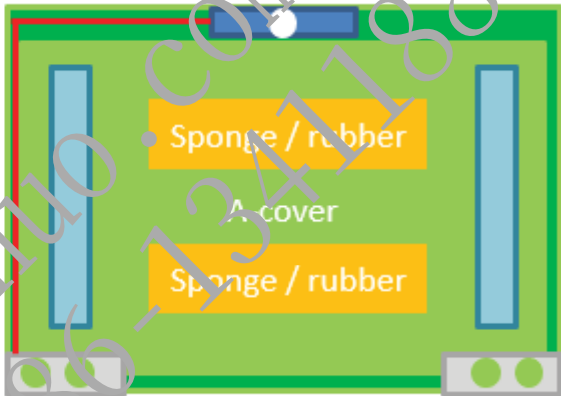
Notes:

Except the Critical Dimensions as Above, Other Dimensions are Measured by Coordinate Measuring Machine If Necessary.

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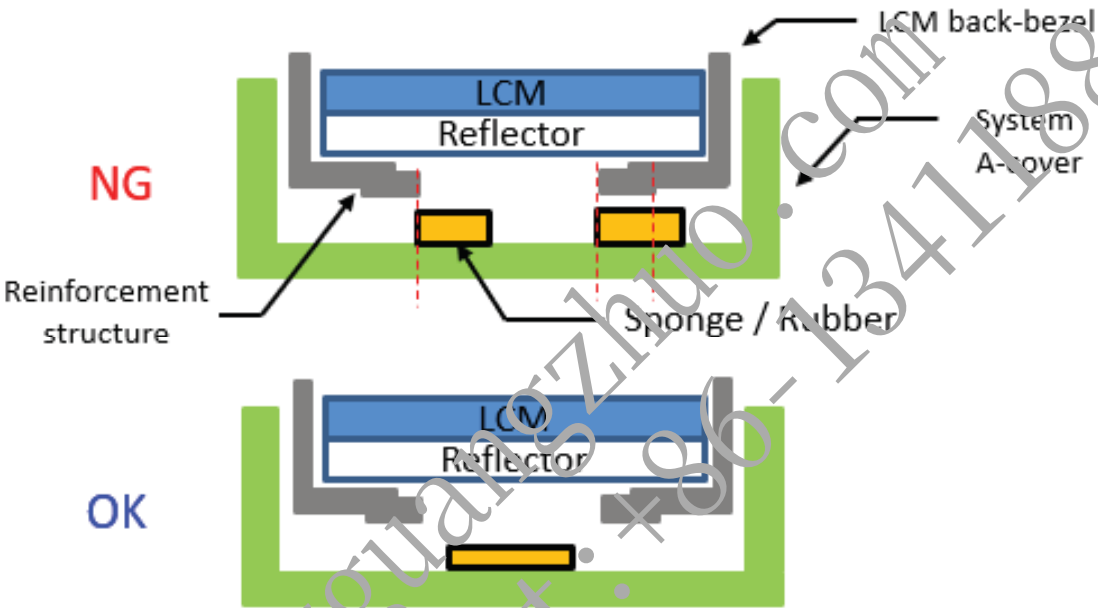
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Appendix B: System design Recommendation															
LCM to A-Cover / sponges Z-gap															
<table><tr><th></th><th>Plastic Cover</th><th>Metal Cover</th></tr><tr><td>A</td><td>≥ 1.0mm</td><td>≥ 0.8mm</td></tr><tr><td>B</td><td colspan="2">≥ 0mm</td></tr><tr><td>C</td><td colspan="2">> 0.5mm</td></tr></table> 					Plastic Cover	Metal Cover	A	≥ 1.0mm	≥ 0.8mm	B	≥ 0mm		C	> 0.5mm	
	Plastic Cover	Metal Cover													
A	≥ 1.0mm	≥ 0.8mm													
B	≥ 0mm														
C	> 0.5mm														
Purpose	The reflector area is very sensitive, BOE would suggest that design enough z-gap to decrease the risk of water ripple, white spots and other abnormal display														
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Appendix B: System design Recommendation

LCM to A-Cover / sponges z-gap



Purpose	If attach sponges or rubbers which correspond to white reflector area, it may cause white spot, pooling or other relative issues. BOE would suggest that attach wide range sponges / rubbers which can cover the LCM back-bezel opening
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Appendix B: System design Recommendation

LCM to side wall / protrusions

Diagram illustrating the LCM (Liquid Crystal Module) layout and required gap around the LCM for side wall / protrusions. The diagram shows the LCM (blue) surrounded by a gap (green). Dimensions X1, X2, Y1, Y2, Px1, Px2, and Py are indicated. A-cover is shown at the top left.

	Normal border (screws)	Narrow border (fix by tapes)
X1 / X2	Min: 0.45mm	Min: 0.35mm
Y1 / Y2	Min: 0.45mm	Min: 0.35mm
Px1 / Px2	Min: 0.55mm	
Py		

Purpose	BOE would suggest that design enough gap around LCM to prevent shock test failure, or interference, cell crack, abnormal display...etc. in the reliability test
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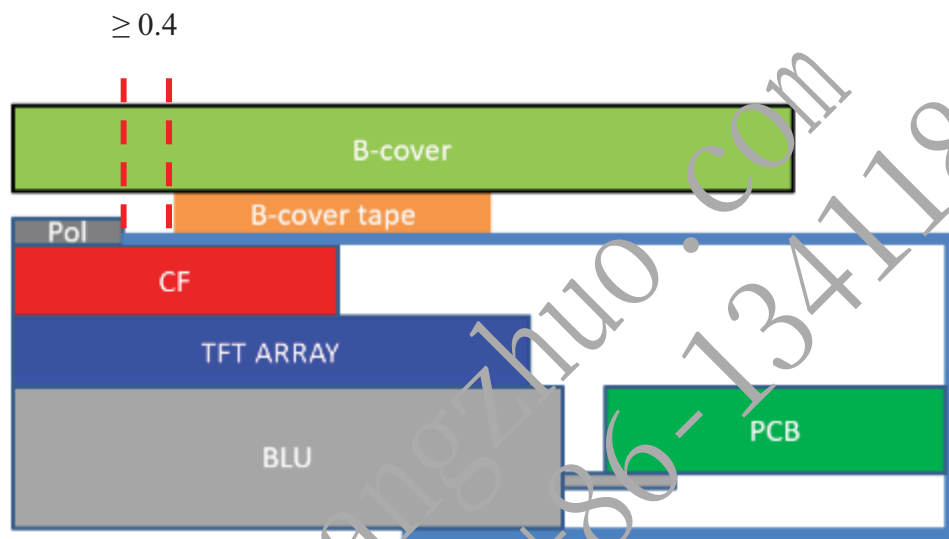
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	Customer Spec	Rev. 0	2024.10.25						
Appendix B: System design Recommendation									
LCM to B-cover z-gap									
Pol LCM A-cover Z-gap <table><tr><th>Bezel Tape</th><th>Z-Gap</th></tr><tr><td>Without</td><td>0.15 ~ 0.25mm</td></tr><tr><td>With</td><td>0.15 ~ 0.20mm</td></tr></table>				Bezel Tape	Z-Gap	Without	0.15 ~ 0.25mm	With	0.15 ~ 0.20mm
Bezel Tape	Z-Gap								
Without	0.15 ~ 0.25mm								
With	0.15 ~ 0.20mm								
Purpose	Too less z-gap between system B-cover and LCM top pol has high risk that may cause cell crack, pooling, light leakage and other issues								
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Appendix B: System design Recommendation

B-cover tape to top pol edge



If attach b-cover and LCM with tapes,
Please let tapes to be located out of top pol edges 0.4mm away on 4 sides

Purpose	To avoid the B-cover tape override top pol then cause pooling or light leakage issue
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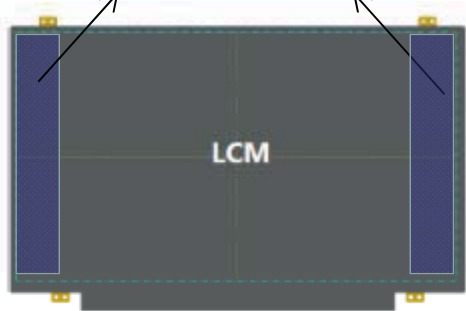
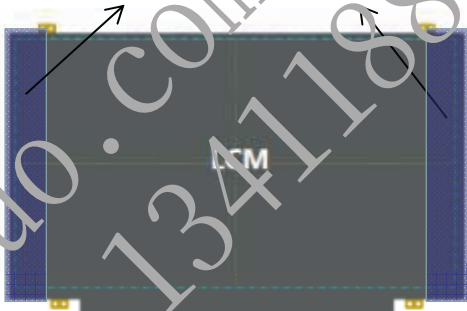
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A4(210 X 297)

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Appendix B: System design Recommendation			
Antenna Cable & Webcam wire			
Antenna cable WebCam wire OK NG NG OK Reflector Back bezel rubber A-cover If sponge within the reflector area is necessary, we suggest that the gap between reflector and sponge is more than 0.5mm			
Purpose	1. BOE would suggest that do not set Antenna or WebCam cable / wire go behind LCM to avoid backpack test, hinge test ,twist test or pogo test with abnormal display 2. If the cable / wire is necessary to go behind LCM, please make a groove with rounds or chamfers to protect the cable / wire, or attach with higher sponges / rubbers adjacent to the cable / wire route 3. Suggest that attach the cable / wire with tapes to A-cover 4. Do not attach anything with LCM reflector area. If attach cable / wire with LCM reflector area, it may cause pooling, white spot, light leakage and other related issues		
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Appendix B: System design Recommendation			
LCM paste area LCM rear view White Reflector Attachable area			
Purpose	If use the stretch remove tapes to fix LCM with A-cover, please set the stretch remove tapes correspond to the LCM back-bezel and do not let the tapes override the back-bezel's level step of opening		
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Appendix B: System design Recommendation			
LCM pressable area			
Position of pressure head (Inside AA W/O border)  NG Position of pressure head (With Border)  OK			
Purpose	1. If LCM is fixed on A-cover by using the press jig during assembling. 2. To avoid panel broken the design of pressure head of press jig can not only pin on cell panel. The pressure head needs to pin on the LCM frame, which the LCM frame can share the pressure of the pressing head.		
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Appendix B: System design Recommendation			
Wire setting			
LCM A-cover OK cable LCM A-cover Not Recommend cable			
Purpose	Wires should be placed between protrusions/side wall and A-cover. If place the wires between LCM and Protrusions/side wall, it may interfere with LCM when assembling, or even cause LCM broken in reliability test.		
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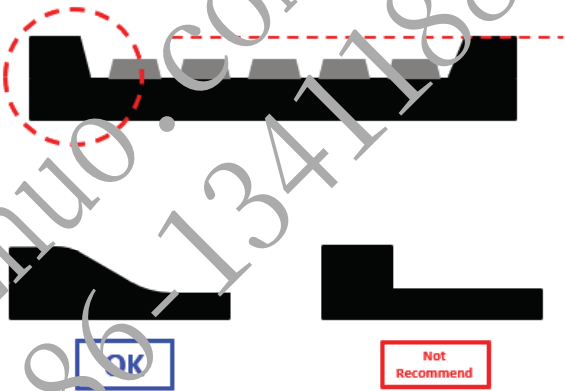
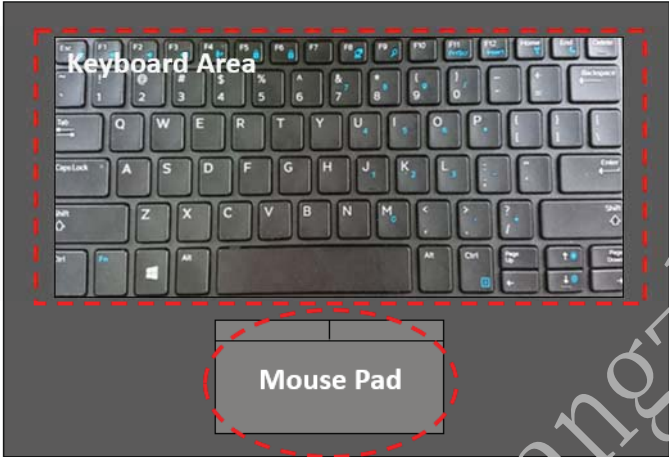
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Appendix B: System design Recommendation			
A-cover strength			
LCM Rib/ Bracket A-cover OK LCM A-cover Not Recommend			
Purpose	1. BOE would recommend that structural Rib/Bracket height is higher than LCM, in order to avoiding pressures to LCM. 2. The L-shape Bracket is recommended.		
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Appendix B: System design Recommendation			
System A-cover Inner Surface 			
Purpose	There should not exist any burr, segment gap or protrusions beside Logo, which may cause White Spot or Glass Broken by stress concentration.		
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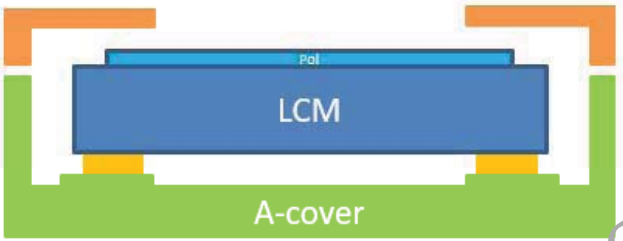
Appendix B: System design Recommendation

Keyboard area & Mouse pad

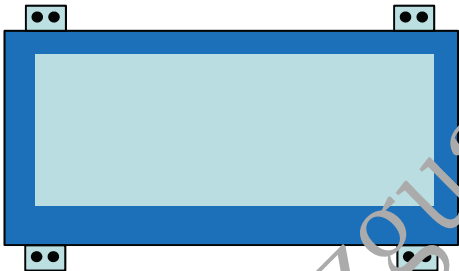
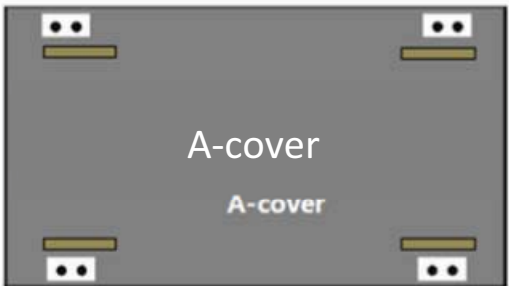


Purpose	The transition surface between keyboard and mouse pad should be smooth and without vertical steps\ too large level steps
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Appendix B: System design Recommendation			
System cover reliability			
 OK  Not Recommend			
Purpose	1. No interference between system and LCM in assembly process except compressible grounding gaskets 2. The permanent deformation which caused by Reliability test is not allowed to contact LCM		
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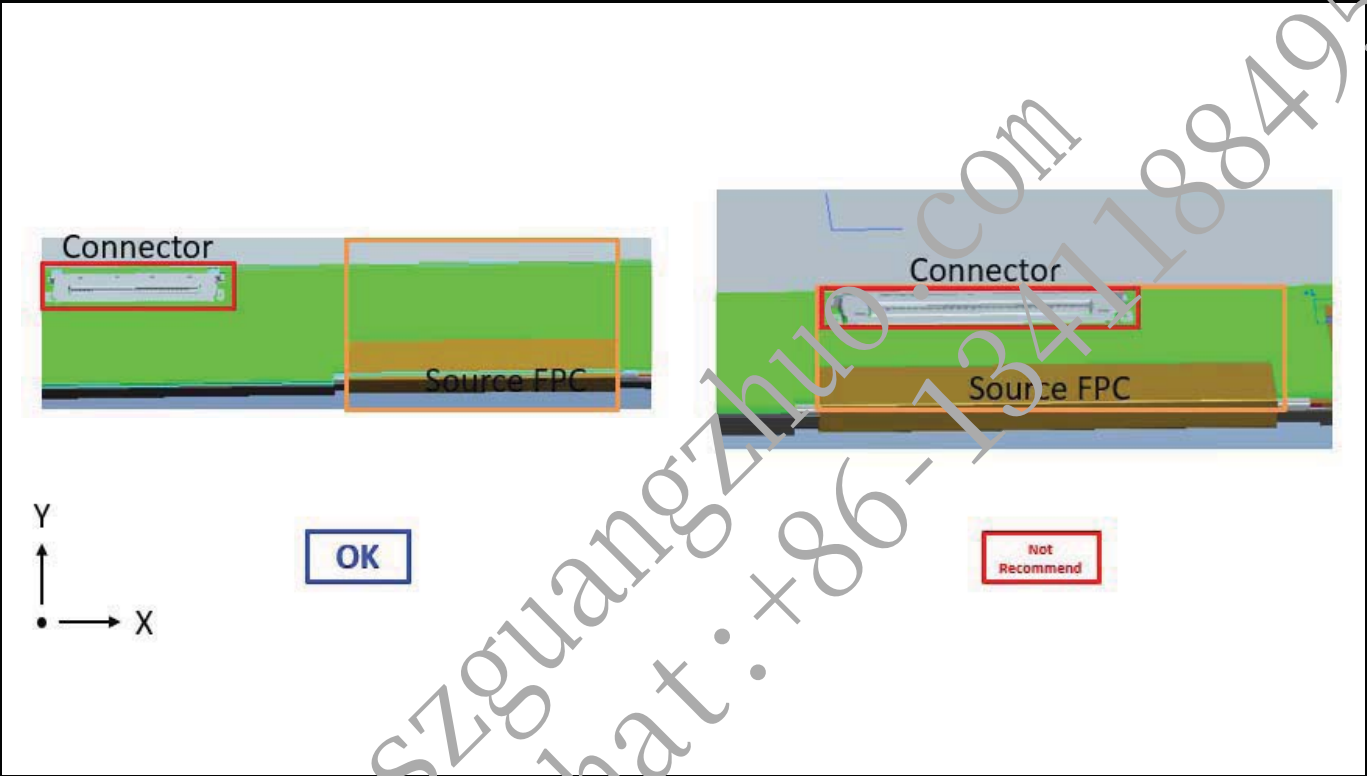
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Appendix B: System design Recommendation			
A/B-cover near LCD PCBA			
LCM No any magnet			
Purpose	There should not been any magnet object close to LCM PCBA, it may cause physical or electricity noise issue		
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Appendix B: System design Recommendation			
A-cover add sponges on Boss side wall			
			
Purpose	BOE would suggest to attach Sponges to the side-wall of the Boss column of A-cover to reduce the risk of panel broken in assembling process.		
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Appendix B: System design Recommendation

LCM to A-Cover / sponges z-gap



Purpose	Bent type product: The System Connector should not overlap with LCM FPC in X-direction, it may cause FPC lead broken during system connector plug and un-plug process (Panel FPC Bonding location is related to Mask and can not be changed easily)
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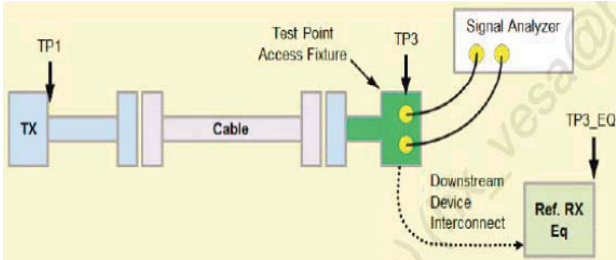
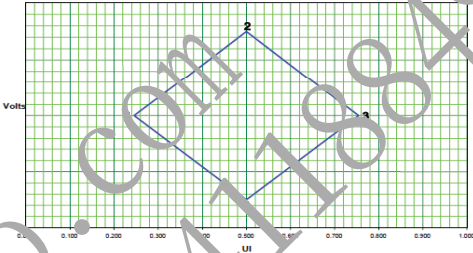
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Appendix C : System design Recommendation			
HPD Signal recognition			
Logic Vdd 90% 10% HPD from Sink 2.0V HPD Glitch Sink Aux Aux command Normal Signal (Ignore HPD Glitch) Logic Vdd 90% 10% HPD from Sink 2.0V HPD Glitch Sink Aux Aux command Abnormal Signal			
Purpose	When HPD glitch voltage less than 2.0(V), system signal can't output AUX command data.		
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Appendix C : System design Recommendation			
HPD Signal Definition IRQ (Interrupt Request)			
Logic Vdd HPD from Sink Sink Aux Source Main-Link 90% 10% Link Training Normal Video Link Training Normal Video Aux command Aux command IRQ (0.5ms to 1ms)			
Purpose	When HPD signal low than 0.5ms to 1ms, the source device should check sink status field from the DPCD and take link training again.		
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Appendix C : System design Recommendation

Main link eye diagram of TP3																																
 																																
Measured TP3 on LCM connector. <table><thead><tr><th></th><th>UI</th><th>Voltage</th></tr></thead><tbody><tr><td>1</td><td>0.246</td><td>0</td></tr><tr><td>2</td><td>0.5</td><td>0.075</td></tr><tr><td>3</td><td>0.755</td><td>0</td></tr><tr><td>4</td><td>0.5</td><td>-0.075</td></tr></tbody></table> Eye for TP3 at HBR Downstream Device Mask at TP3 <table><thead><tr><th></th><th>UI</th><th>Voltage</th></tr></thead><tbody><tr><td>1</td><td>0.375</td><td>0</td></tr><tr><td>2</td><td>0.5</td><td>0.023</td></tr><tr><td>3</td><td>0.625</td><td>0</td></tr><tr><td>4</td><td>0.5</td><td>-0.023</td></tr></tbody></table> Eye for TP3 at RBR				UI	Voltage	1	0.246	0	2	0.5	0.075	3	0.755	0	4	0.5	-0.075		UI	Voltage	1	0.375	0	2	0.5	0.023	3	0.625	0	4	0.5	-0.023
	UI	Voltage																														
1	0.246	0																														
2	0.5	0.075																														
3	0.755	0																														
4	0.5	-0.075																														
	UI	Voltage																														
1	0.375	0																														
2	0.5	0.023																														
3	0.625	0																														
4	0.5	-0.023																														
Purpose	1. 2. Main Link EYE Diagram should meet TP3 point of VESA. The measure method is through access fixture.																															
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Appendix C : System design Recommendation

Impedance Profile through a DP Connector

Differential Impedance Profile Measurement Data Example

Segment	Differential Impedance Value	Maximum Tolerance
Fixture	100Ω/VESA	±10%
Connector	100Ω/VESA	±10%
Wire management	100Ω/VESA	±10%
Cable	100Ω/VESA	±5%

Impedance Profile Values for Cable Assembly

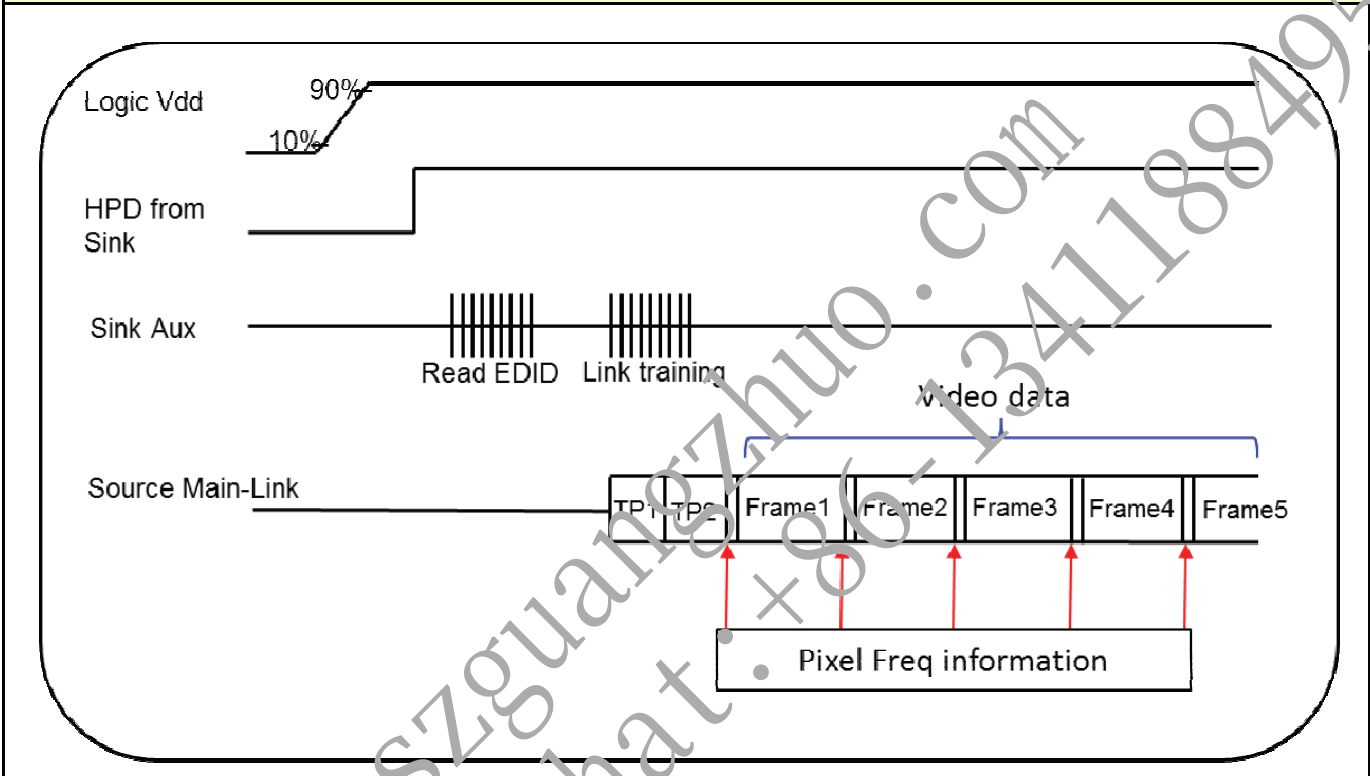
Purpose	Cable Impedance Profile 100ohm for Cable Assembly
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Appendix C : System design Recommendation

Main Link Pixel Freq information value of MSA data



Purpose	1. It need to fix pixel freq information value of MSA data output to prevent the initial abnormal pixel freq information value from incoming after power on. 2. BOE can read LPCD to check this value. Ex: BIOS is 1.62G , but into windows is 2.7G.
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Appendix C : System design Recommendation

System Input PWM Rising/Falling time														
VIH(90%) VIL(10%) INPUT PWM VIH(90%) VIL(10%) PWM (internal logic 0 or 1) Backlight flicker PWM Period Example: <table><tr><th>Freq</th><th>Cycle Time</th><th>PWM Rising Time</th><th>PWM Falling Time</th></tr><tr><td>200Hz</td><td>5ms</td><td>≤1us</td><td>≤1us</td></tr><tr><td>1KHz</td><td>1ms</td><td>≤200ns</td><td>≤200ns</td></tr></table>			Freq	Cycle Time	PWM Rising Time	PWM Falling Time	200Hz	5ms	≤1us	≤1us	1KHz	1ms	≤200ns	≤200ns
Freq	Cycle Time	PWM Rising Time	PWM Falling Time											
200Hz	5ms	≤1us	≤1us											
1KHz	1ms	≤200ns	≤200ns											
Purpose	1. LED driver need to calculate the duty cycle of input PWM signal. 2. To avoid backlight flicker visible on LCD, system input PWM suggest : PWM rising ≤ 200ppm*cycle time ; PWM falling ≤ 200ppm*cycle time.													
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