

NV140FHM-N4K V8.0**Final Product Specification****Rev. 0****BOE Optoelectronics Technology Co., Ltd**

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www.szguangzhuo.com 广卓液晶屏 echodeng61@hotmail.com jimeij@jimeihk.com +86-13411884959

TFT-LCD

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1 OF 34

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REVIEWED

Designer	Manager
Mei Wenlin(Array)	Wang Xiaolin
Lei Dan(Cell)	Hu Jingyong
Liu Chao(CF)	Li Min
Zhang Yuanping(EE)	Gao Xianyong
Geng Yuxu(MO)	Gao Liang
Huang Longbo(OE)	Huang Yuan
Wen Jianghong(M)	Wang Zhihui

APPROVED

Yan Jiang(PM)

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1.0 GENERAL DESCRIPTION

1.1 Introduction

NV140FHM-N4K V8.0 is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 14.0 inch diagonally measured active area with Full-HD resolutions (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 262k(6bit) colors and color gamut 45%. The TFT-LCD panel used for this module is a low reflection and higher color type. Therefore, this module is suitable for Notebook PC. The LED driver for back-light driving is built in this model.

All input signals are eDP1.2 interface compatible.

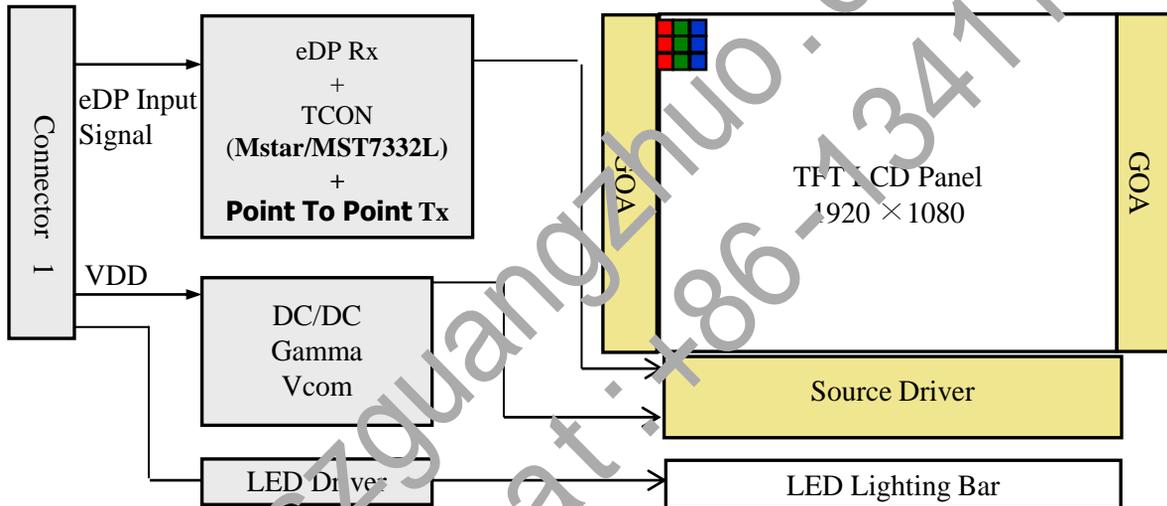


Figure 1 Drive Architecture

1.2 Features

- 2 lane eDP interface with 2.7Gbps link rates
- Thin and light weight
- 262k(6bit) color depth, color gamut 45%
- Single LED lighting bar (Bottom side/Horizontal Direction)
- Data enable signal mode
- Side mounting frame
- Green product (RoHS & Halogen free product)
- On board LED driving circuit
- Low driving voltage and low power consumption
- On board EDID chip

1.3 Application

- Notebook PC (Wide type)

1.4 General Specification

The followings are general specifications at the model NV140FHM-N4K V8.0. (listed in Table 1)

<Table 1. General Specifications>

Parameter	Specification	Unit	Remarks
Active area	309.312(H) × 173.988(V)	mm	
Number of pixels	1920 (H) × 1080 (V)	pixels	
Pixel pitch	161.1(H) × 161.1(V)	um	
Pixel arrangement	RGB Vertical stripe		
Display colors	262k(6bit)		
Color gamut	45%		
Display mode	Normally Black		
Dimensional outline	316.11(H)*186.37(V) (W/O PCB)*3.0(Max) 316.11(H)*197.98(V) (W/ PCB)*3.0(Max)	mm	
Weight	285(max)	g	
Surface treatment	Anti-Glare		
Surface hardness	3H		
Back-light	Bottom edge side, 1-LED lighting bar type		Note 1
Power consumption	P _D : 0.9	W	@Mosaic
	P _{BL} : 2.7	W	
	P _{Total} : 3.6	W	@Mosaic

Notes : 1. LED Lighting Bar (32*LED Array)

2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Absolute Maximum Ratings >

Ta=25 \pm 2 $^{\circ}$ C

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V _{DD}	-0.3	4.0	V	
eDP input Voltage	V _{eDP}	0	2.0	V	Note 1
Logic Supply Voltage	V _{IN}	V _{SS} -0.3	V _{DD} +0.3	V	
Operating Temperature	T _{OP}	0	+50	$^{\circ}$ C	Note 2
Storage Temperature	T _{ST}	-20	+60	$^{\circ}$ C	

Notes :

1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.
2. Temperature and relative humidity range are shown in the figure below.
90 % RH Max. (40 $^{\circ}$ C \geq Ta) Maximum wet - bulb temperature at 39 $^{\circ}$ C or less. (Ta > 40 $^{\circ}$ C) No condensation.

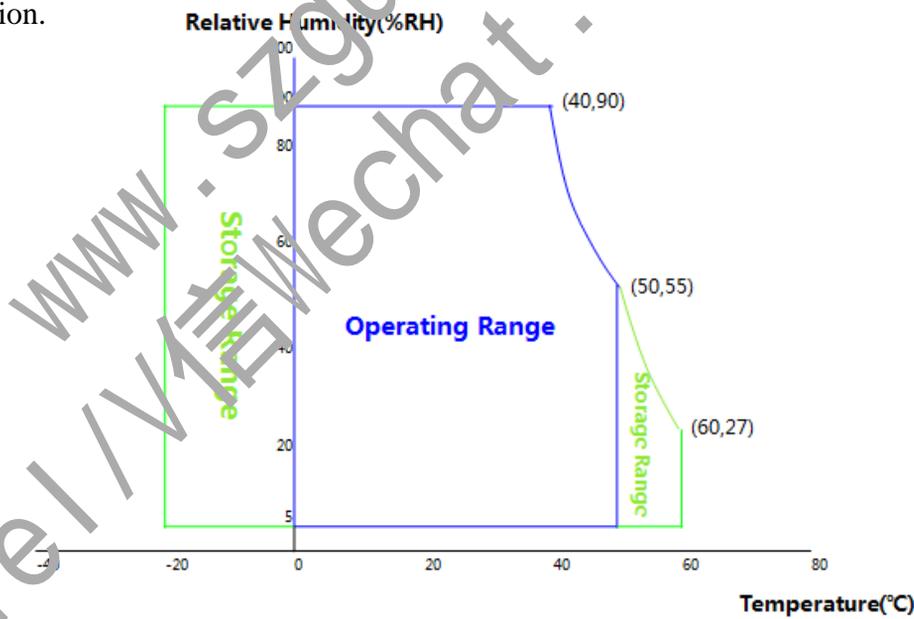


Figure 2. Temperature and Relative Humidity Range

3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

< Table 3. Electrical Specifications >

Ta=25+/-2°C

Parameter		Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V _{DD}	3.0	3.3	3.6	V	Note 1
Permissible Input Ripple Voltage	V _{RF}	-	-	100	mV	@ V _{DD} = 3.3V
BIST Control Level	High Level	2	-	3.5	V	-
	Low Level	0	-	0.8	V	-
Power Supply Current	I _{DD}	-	172	424	mA	Note 1
Power Supply Inrush Current	I _{inrush}	-	-	2.0	A	Note3
Power Consumption	P _D	-	0.9	1.4	W	Note 1
	P _{BLE}	-	-	2.7	W	Note 2
	P _{total}	-	3.6	4.1	W	Note 1

Notes :

- The supply voltage is measured and specified at the interface connector of LCM.
The current draw and power consumption specified is for 3.3V at 25 °C.

- Typ : Mosaic pattern 8*8
- Max : R/G/B patterns



Figure 3. Power Measure Patterns

- Calculated value for reference (V_{LED} × I_{LED})
- Measure condition (Figure 4)

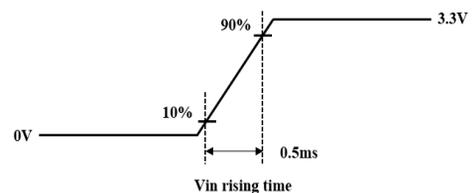


Figure 4. Inrush Measure Condition

3.2 Backlight Unit

< Table 4. LED Driving Guideline Specifications >

Ta=25+/-2°C

Parameter		Min.	Typ.	Max.	Unit	Remarks	
LED Forward Voltage		V _F	-	-	2.9	V	-
LED Forward Current		I _F	-	23.6	-	mA	-
LED Power Consumption		P _{LED}	-	-	2.7	W	Note 1
LED Life-Time		N/A	15,000	-	-	Hour	I _F = 23.6mA
Power Supply Voltage for LED Driver		V _{LED}	5	12	21	V	-
Power Supply Voltage for LED Driver Inrush		I _{led inrush}	-	-	2.0	A	Note 3
EN Control Level	Backlight On		2.0	-	5.0	V	-
	Backlight Off		0	-	0.8	V	-
PWM Control Level	High Level		2.0	-	5.0	V	-
	Low Level		0	-	0.8	V	-
PWM Control Frequency		F _{PWM}	200	-	10,000	Hz	-
Duty Ratio			5	-	100	%	-

Notes :

- Power supply voltage 2V for LED driver.
Calculator value for reference $I_F \times V_F \times 32 / \text{driver efficiency} = P_{LED}$
- The LED life-time define as the estimated time to 50% degradation of initial luminous.
- Measure condition (Figure 5)

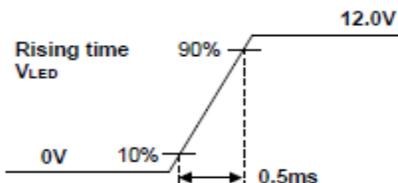


Figure 5. Inrush Measure Condition

3.3 LED Structure

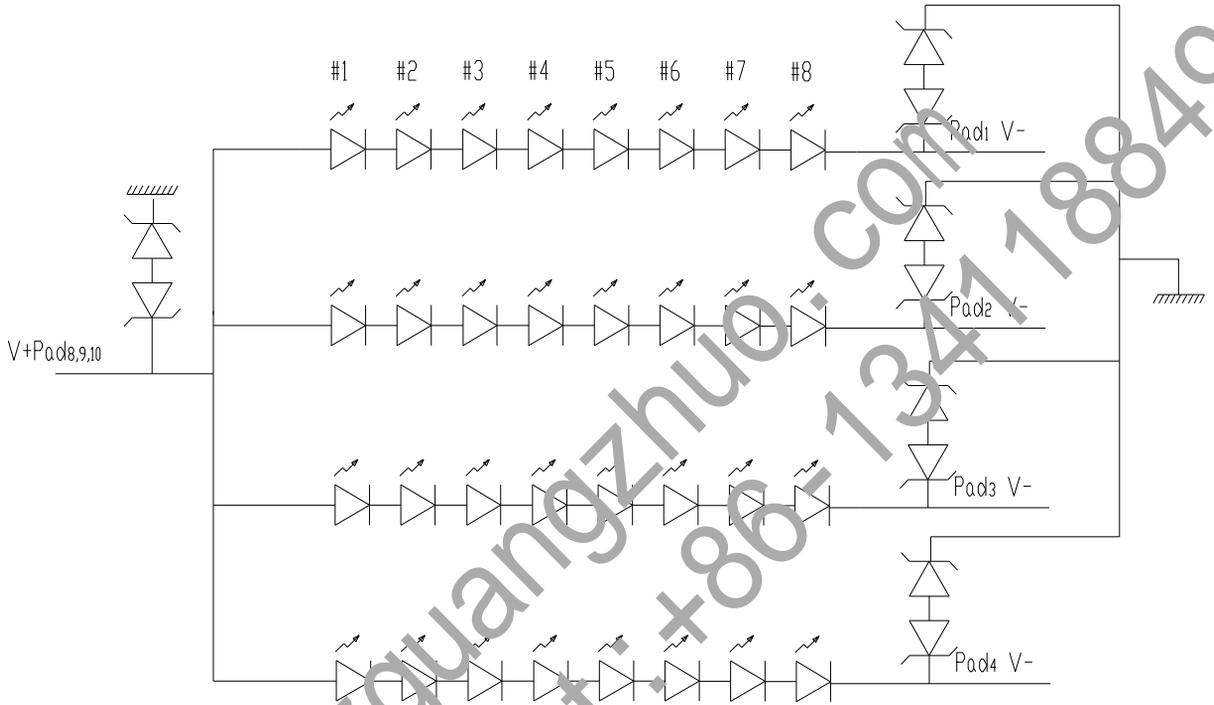


Figure 6. LED Structure

4.0 OPTICAL SPECIFICATION

4.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = $25 \pm 2^\circ\text{C}$) with the equipment of luminance meter system (PR730&PR810) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and ϕ equal to 0° . We refer to $\theta=0$ ($=\theta_3$) as the 3 o'clock direction (the "right"), $\theta=90$ ($=\theta_{12}$) as the 12 o'clock direction ("upward"), $\theta=180$ ($=\theta_9$) as the 9 o'clock direction ("left") and $\theta=270$ ($=\theta_6$) as the 6 o'clock direction ("bottom"). While scanning θ and/or ϕ , the center of the measuring spot on the display surface shall stay fixed. The backlight should be operating for 30 minutes prior to measurement. VDD shall be $3.3 \pm 0.3\text{V}$ at 25°C . Optimum viewing angle direction is 6 o'clock.

4.2 Optical Specifications

<Table 5. Optical Specifications>

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	θ_3	$\theta = 0^\circ$ CR = 10	80	85	-	Deg.	Note 1
		θ_9		80	85	-	Deg.	
	Vertical	θ_{12}		80	85	-	Deg.	
		θ_6		80	85	-	Deg.	
Luminance Contrast Ratio		CR	$\theta = 0^\circ$	600	800	-		Note 2
Luminance of White	5 Points	L_m	$\theta = 0^\circ$ $I_{LED} = 27.6\text{mA}$	212.5	250	-	cd/m^2	Note 3
White Luminance Uniformity	5 Point	ΔY_5		80	-	-	%	Note 4
	13 Points	ΔY_{13}		62.5	-	-	%	
White Chromaticity		W_x	$\theta = 0^\circ$	0.283	0.313	0.343	-	Note 5
		W_y		0.299	0.329	0.359	-	
Reproduction of Color	Red	R_x	$\theta = 0^\circ$	-0.03	0.590	+0.03	-	-
		R_y			0.350		-	-
	Green	G_x			0.330		-	-
		G_y			0.555		-	-
	Blue	B_x			0.153		-	-
		B_y			0.119		-	-
Color Gamut		-	-	-	45	-	%	-
Response Time (Rising + Falling)		T_{RT}	$T_a = 25^\circ\text{C}$ $\theta = 0^\circ$	-	30	35	ms	Note 6
Cross Talk		CT	$\theta = 0^\circ$	-	-	2	%	Note 7

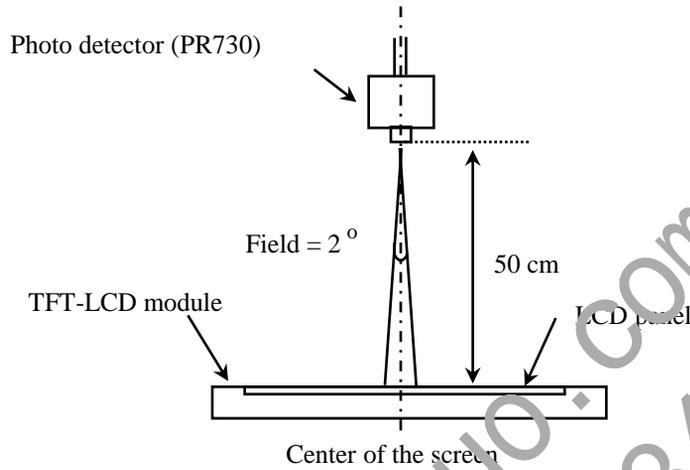
Notes :

- Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 7).
- Contrast measurements shall be made at viewing angle of $\Theta = 0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see Figure 7) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

- Center Luminance of white is defined as luminance values of 5 point average across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 8 for a total of the measurements per display.
- The White luminance uniformity on LCD surface is then expressed as : $\Delta Y = \text{Minimum Luminance of 5(or 13) points} / \text{Maximum Luminance of 5(or 13) points.}$ (see Figure 8 and Figure 9).
- The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
- The electro-optical response time measurements shall be made as Figure 10 by switching the "data" input signal CN and OFF. The times needed for the luminance to change from 10% to 90% is T_r , and 90% to 10% is T_f .
- Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 10 ± 1 mm diameter area, with all display pixels set to gray 127(of 0 to 255), to the luminance (YB) of that same area when any adjacent area is driven dark.The luminance ratio shall not exceed 1:1.05 (See Figure 11).

4.3 Optical Measurements



Optical characteristics measurement setup

Figure 7. Measurement Set Up

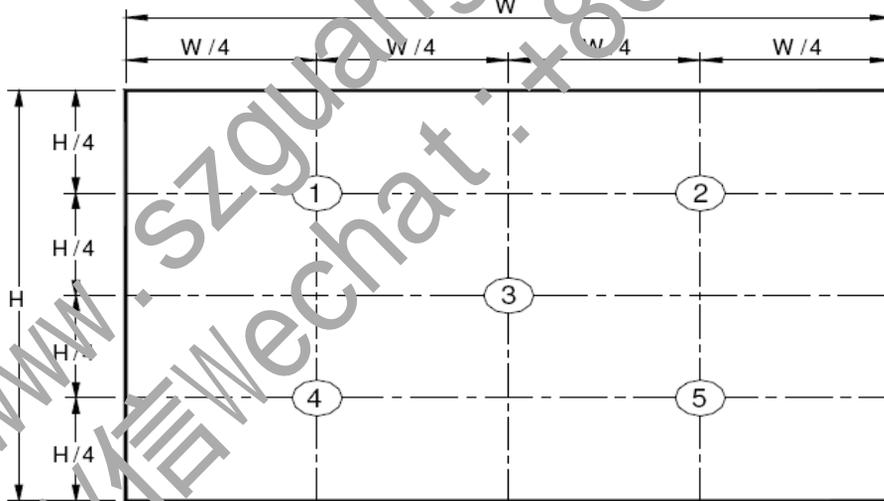


Figure 8. White Luminance and Uniformity Measurement Locations (5 points)

Center Luminance of white is defined as luminance values of center 5 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 7 for a total of the measurements per display.

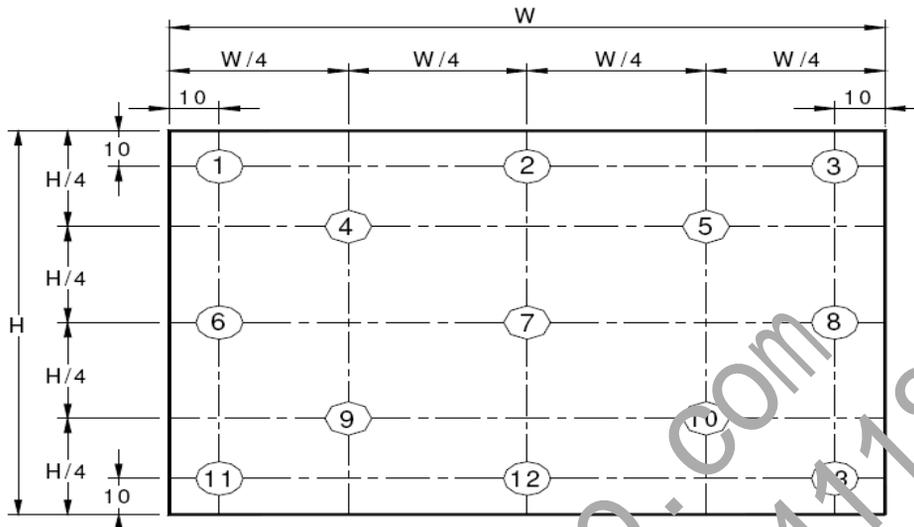


Figure 9. Uniformity Measurement Locations (13 points)

The White luminance uniformity on LCD surface is then expressed as : $\Delta Y5$ = Minimum Luminance of five points / Maximum Luminance of five points (see Figure 8), $\Delta Y13$ = Minimum Luminance of 13 points / Maximum Luminance of 13 points (see Figure 9).

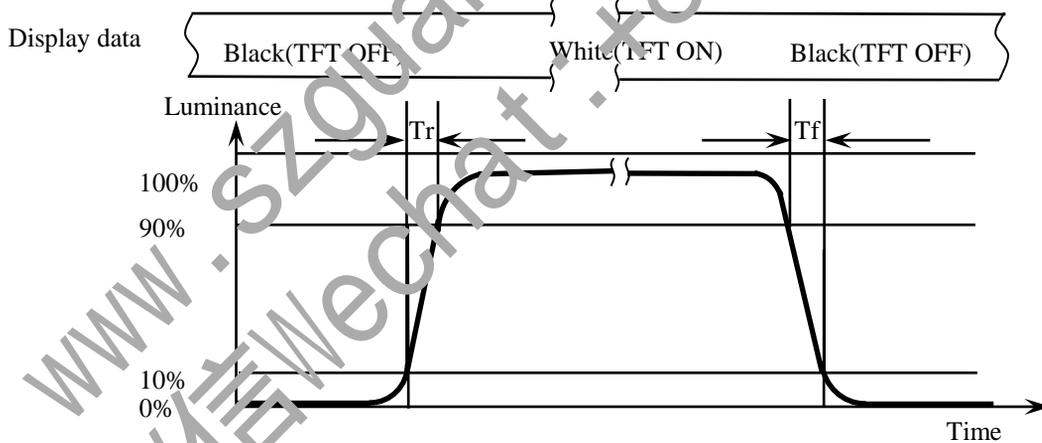
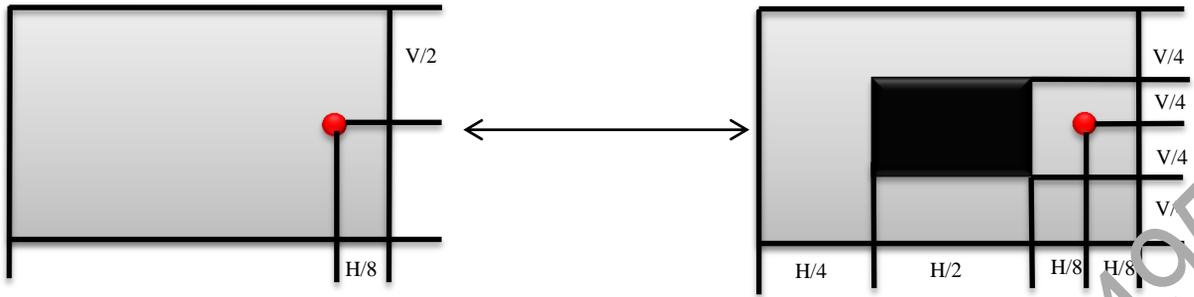


Figure 10. Response Time Testing

The electro optical response time measurements shall be made as shown in Figure 10 by switching the “data” input signal ON and OFF. Tr: The luminance to change from 10% to 90% ,Tf: The luminance to change from 90% to 10% .

The test system : PR810



$$\text{Cross Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_B} \right| \times 100$$

Figure 11. Cross Talk Modulation Test Description

Where:

Y_A = Initial luminance of measured area (cd/m^2)

Y_B = Subsequent luminance of measured area (cd/m^2)

The location measured will be exactly the same in both patterns. The test background gray is L127.

Cross Talk of one area of the LCD surface by another shall be measured by comparing the luminance (Y_A) of a $10 \pm 1\text{mm}$ diameter area, with all display pixels set to a gray level 127, to the luminance (Y_B) of that same area when any adjacent area is driven dark. (Refer to Figure 11)

The test system: PR730

5.0 INTERFACE CONNECTION

5.1 Electrical Interface Connection

The electronics interface connector is **STM MSAK24025P30**.

The connector interface pin assignments are listed in Table 6.

<Table 6. Pin Assignments for the Interface Connector>

Terminal	Symbol	Functions
Pin No.	Symbol	Description
1	NC	No connection
2	H-GND	Ground
3	LAN1_N	Complement Signal Link_Lane1
4	LAN1_P	True Signal Link_Lane1
5	H-GND	Ground
6	LAN0_N	Complement Signal Link_Lane0
7	LAN0_P	True Signal Link_Lane0
8	H-GND	High Speed Ground
9	AUXP	True Signal Link_Auxiliary Channel
10	AUXN	Complement Signal Link_Auxiliary Channel
11	H-GND	Ground
12	LCD_VCC	Power Supply, 3.3V (typ.)
13	LCD_VCC	Power Supply, 3.3V (typ.)
14	BIST	No connection
15	H-GND	Ground
16	H-GND	Ground
17	HPD	HPD(Hot Plug Detect) Signal Pin
18	BL_GND	High Speed Ground
19	BL_GND	High Speed Ground
20	BL_GND	High Speed Ground
21	BL_GND	High Speed Ground
22	BL_EN	Backlight on/off Control pin
23	BL_PWM	Back light PWM Dimming
24	NC	No connection
25	NC	No connection
26	BL_PWR	Backlight power
27	BL_PWR	Backlight power
28	BL_PWR	Backlight power
29	BL_PWR	Backlight power
30	NC	No connection

5.2 eDP Interface

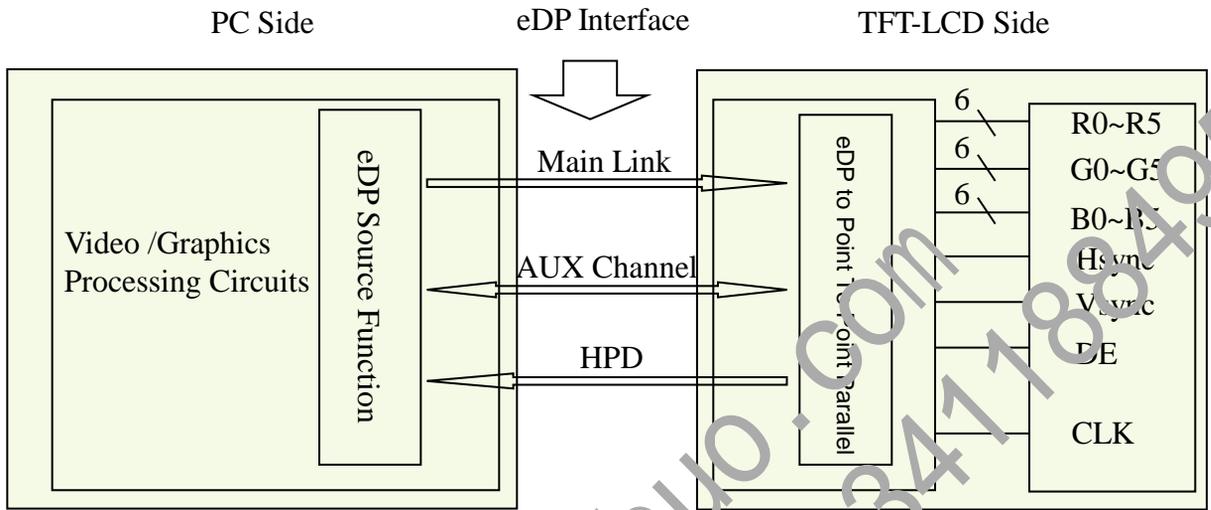


Figure 12. eDP Interface Architecture

Note:

Transmitter : Parade DP501 or equivalent
Transmitter is not contained in module.

5.3 Data Input Format

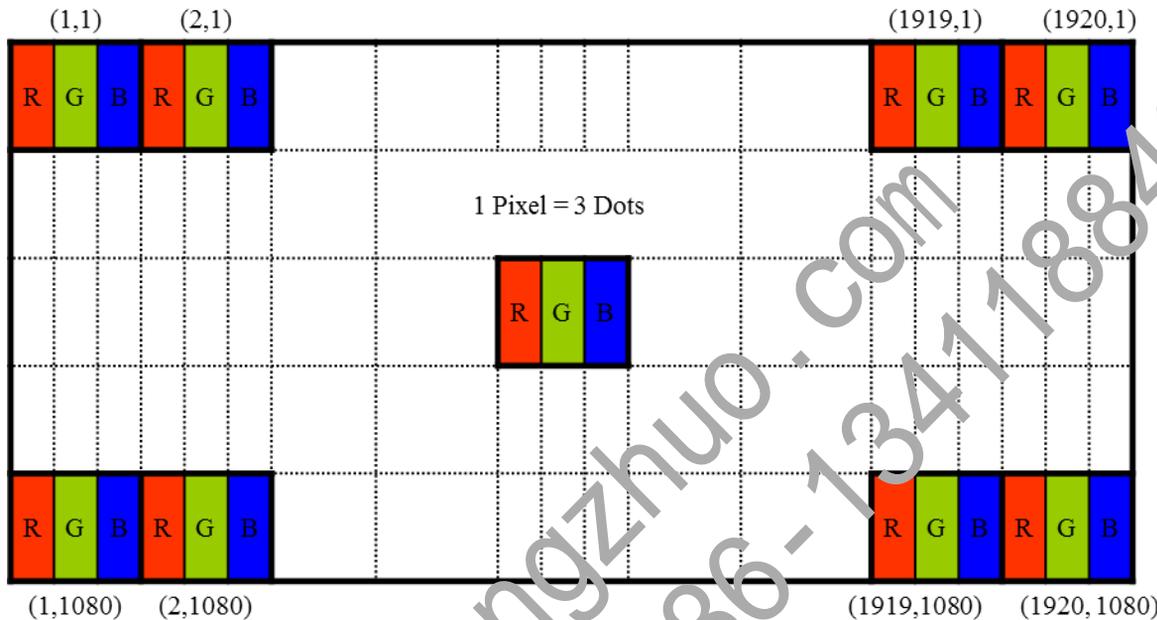


Figure 13. Display Position of Input Data (V-H)

5.4 Back-light & LCM Interface Connection

BLU Interface Connector: STM MSK24022P10

<Table 7. Pin Assignments for the BLU Connector>

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	LED	LED cathode connection	6	GND	GND
2	LED	LED cathode connection	7	NC	No Connection
3	LED	LED cathode connection	8	Vout	LED anode connection
4	LED	LED cathode connection	9	Vout	LED anode connection
5	NC	No Connection	10	Vout	LED anode connection

6.0 SIGNAL TIMING SPECIFICATION

6.1 The NV140FHM-N4K V8.0 Is Operated By The DE Only

< Table 8. Signal Timing Specification >

Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	141.56	142.73	143.91	MHz
Frame Period		Tv	1115	1120	1125	lines
			-	60	-	Hz
			-	16.67	-	ms
Vertical Display Period		Tvd	-	1080	-	lines
One line Scanning Period		Th	2116	2124	2132	clocks
Horizontal Display Period		Tnc	-	1920	-	clocks

Note : The above is as optimized setting.

6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 9.

<Table 9. eDP Main-Link RX TP4 Package Pin Parameters>

Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock (Link clock down-spreading)	ssc	0	-	0.5	%	
Differential peak-to-peak input voltage at package pins	VRX-DIFFp-p	100	-	1320	mV	
Rx input DC common mode voltage	VRX_DC_CM	0	-	2	V	
Differential termination resistance	RRX-DIFF	80	-	120	Ω	
Single-ended termination resistance	RRX-SE	40	-	60	Ω	
Rx short circuit current limit	IRX_SHORT	-	-	50	mA	
Intra-pair skew at Rx package pins (HBR) RX intra-pair skew tolerance at HBR	LRX_SKEW_INTRA_PAIR	-	-	60	ps	

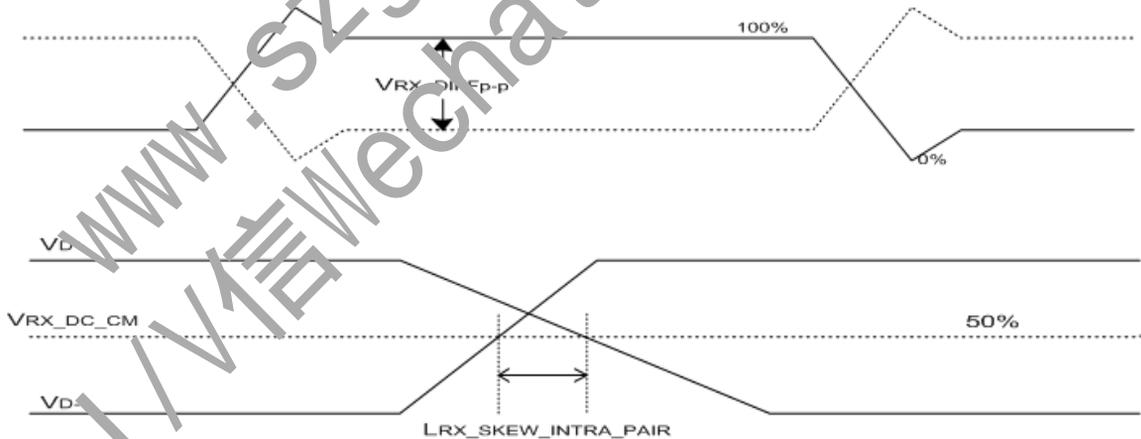


Figure 14. VRX-DIFFp-p & LRX_SKEW_INTRA_PAIR

7.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

<Table 10. Input Signal & Basic Display Colors & Gray Scale of Colors >

	Colors & Gray scale	Data signal																	
		R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	B5
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Light Blue	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Purple	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	△	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Darker	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	△																		
	▽																		
	Brighter	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	
Gray scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	△	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	
	Darker	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	
	△																		
	▽																		
	Brighter	1	0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	
Gray scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	△	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	
	△																		
	▽																		
	Brighter	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	
Gray scale of White & Black	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	△	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	
	Darker	0	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	
	△																		
	▽																		
	Brighter	1	0	1	1	1	1	1	0	1	1	1	1	0	1	1	1	1	
White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		

8.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below.

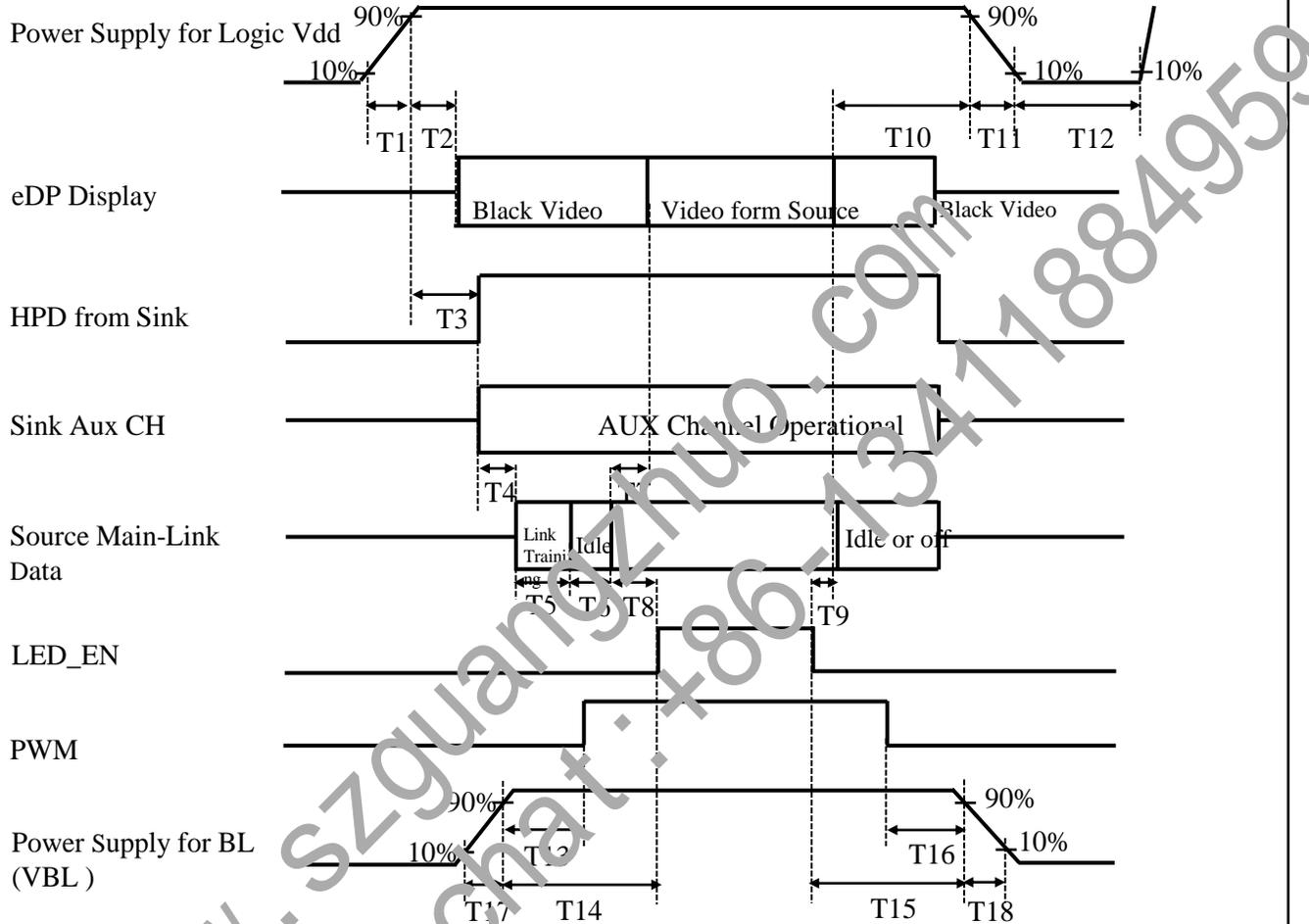


Figure 15. Power Sequence

- $0.5\text{ms} \leq T1 \leq 10\text{ms}$
- $0\text{ms} < T2 \leq 200\text{ms}$
- $0\text{ms} < T3 \leq 20\text{ms}$
- $T3+T4+T5+T6+T8 > 200\text{ms}$
- $0\text{ms} < T7 \leq 50\text{ms}$
- $50\text{ms} < T8$
- $0\text{ms} < T9$
- $0\text{ms} < T10 < 500\text{ms}$
- $0.5\text{ms} \leq T11 \leq 10\text{ms}$
- $500\text{ms} \leq T12$
- $0\text{ms} < T13$
- $0\text{ms} < T14$
- $0\text{ms} < T15$
- $0\text{ms} < T16$
- $0.5\text{ms} \leq T17$
- $0.5\text{ms} \leq T18$

Note:

- When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
- Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal are valid.

9.0 Connector Description

Physical interface is described as for the connector on LCM.

These connectors are capable of accommodating the following signals and will be following components.

9.1 TFT LCD Module

< Table 11. Signal Connector >

Connector Name /Description	For Signal Connector
Manufacturer	STM
Type/ Part Number	MSAK24025P30.
Mating Housing/ Part Number	I-PEX 20-54-030T

10.0 MECHANICAL CHARACTERISTICS

10.1 Dimensional Requirements

Figure 23 shows mechanical outlines for the model NV140FHM-N4K V8.0.
Other parameters are shown in Table 12.

<Table 12. Dimensional Parameters>

Parameter	Specification	Unit
Active Area	309.312 (H) × 173.988 (V)	mm
Number of pixels	1920 (H) X 1080 (V) (1 pixel = R + G + B dot)	pixels
Pixel pitch	161.1 (H) X 161.1 (V)	um
Pixel arrangement	RGB Vertical stripe	
Display colors	262K(6bit)	
Display mode	Normally Black	
Dimensional outline	316.11(H)*186.37(V) (W/PCB)*3.0(Max) 316.11(H)*197.98 (V) (W/PCB)*3.0(Max)	mm
Weight	285 (max)	g

10.2 Mounting

See Figure 20.

10.3 Anti-Glare and Polarizer Hardness

The surface of the LCD has an Anti-Glare coating to minimize reflection and a coating to reduce scratching.

10.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance ≥ 50cm from the screen with an overhead light level of 350lux.

11.0 RELIABILITY TEST

The reliability test items and its conditions are shown in below.

<Table 13. Reliability Test>

No	Test Items	Conditions
1	High temperature storage test	Ta = 60°C , 60%RH, 240 hrs
2	Low temperature storage test	Ta = -20°C , 240 hrs
3	High temperature & high humidity operation test	Ta = 50°C , 80%RH, 240 hrs
4	High temperature operation test	Ta = 50°C , 60%RH, 240 hrs
5	Low temperature operation test	Ta = 0°C , 240 hrs
6	Thermal shock	Ta = -20 °C ↔ 60 °C (0.5 h), 60% ± 3%RH, 100 cycle
7	Vibration test (non-operating)	Ta = 25 °C , 60%RH ± 5% 10~500Hz, Sine X, Y, Z / Sweep rate : 1 hour
8	Shock test (non-operating)	Ta = 25 °C , 60%RH, 220G, Half Sine Wave 2 msec ± X ± Y ± Z Once for each direction
9	Electro-static discharge test (operating)	Air : 150 pF, 330Ω, ± 15 KV Contact : 150 pF, 330Ω, ± 8 KV Ta = 25 °C , 60%RH,

12.0 HANDLING & CAUTIONS

- (1) Cautions when taking out the module
 - Pick the pouch only, when taking out module from a shipping package.
- (2) Cautions for handling the module
 - As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protector sheet off from the LCD panel surface as slowly as possible.
 - As the LCD panel and back light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
 - As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
 - Do not pull the interface connector in or out while the LCD module is operating.
 - Put the module display side down on a flat horizontal plane.
 - Handle connectors and cables with care.
- (3) Cautions for the operation
 - When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
 - Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

(4) Cautions for the atmosphere

- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics

- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions

- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc. Please pack the module not to be broken. We recommend to use the original shipping packages.

13.0 LABEL

(1) Product Label



Figure 16. Product Label

Module ID Naming Rule.

<Table 14. Module ID Naming Rule>

Code	Digit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Code		S	L	S	5	1	2	3	5	9	4	2	0	0	0	1	D	B
Description		Model Code /GBN		Grade	Line	Year		Month	Model Extension Code (Last 4 Digits Of FGCOD)				Serial No 00001-ZZZZZZ					

(2) High voltage caution label

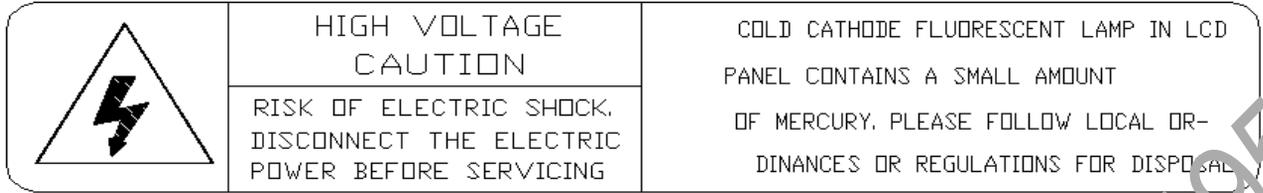


Figure 17. High Voltage Caution Label

(3) Box Label



Figure 18. Box Label

Serial number marked part needs to print, show as follows:

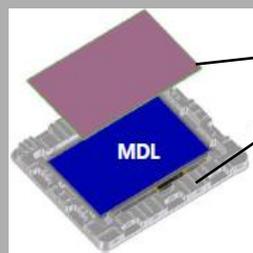
1. FG-CODE (Before 12 bit)
2. Product quantity
3. Box ID
4. Date
5. The client section material number (The client)
6. FG-Code After four
7. The supplier code
8. Total Size: 100×50mm

<Table 15. Box Label Naming Rule >

Digit code	1	2	3	4	5	6	7	8	9	10	11	12	13
Code													
Description	Product Name	Product grade	B8	year	Month	revision	Box serial Number						

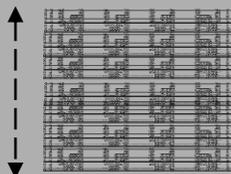
14.0 PACKING INFORMATION

14.1 Packing Order



EPE
Spacer
Tray

7层



PE Bag



- Put 1 pcs spacer in tray and 1 pcs MDL on spacer.
5pcs MDL/Tray,6pcs Spacer/Tray.
- Put 7 pcs tray and 1 pcs tray cover in PE bag.
- Put PE bag with 6 EPE cover in the inner box.
- 35pcs/Box,18Box/Pallet,630pcs MDL/Pallet.



EPE Cover

Inner Box

Figure 19. Packing Order

14.2 Note

- Box dimension: 480mm*350mm*285mm
- Package quantity in one box: 35pcs
- Total weight: 12.4kg/Box

15.0 MECHANICAL OUTLINE DIMENSION



Figure 20. TFT-LCD Module Outline Dimension (Front View)

Note:

1. Top Polarizer is the highest part.
2. Curve Spec: $0 \leq d \leq 0.5$ mm.
3. No light leakage from all 4 corners of LCM.
4. Size Unit: mm.
5. General Tolerance: ± 0.3 mm.
6. The MDL dimension measurement tool is a Vernier Caliper;

Top POL is the highest part.

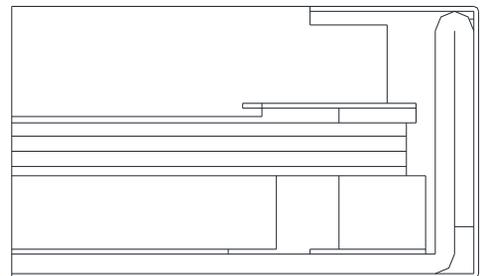


Figure 21. Highest Point Position

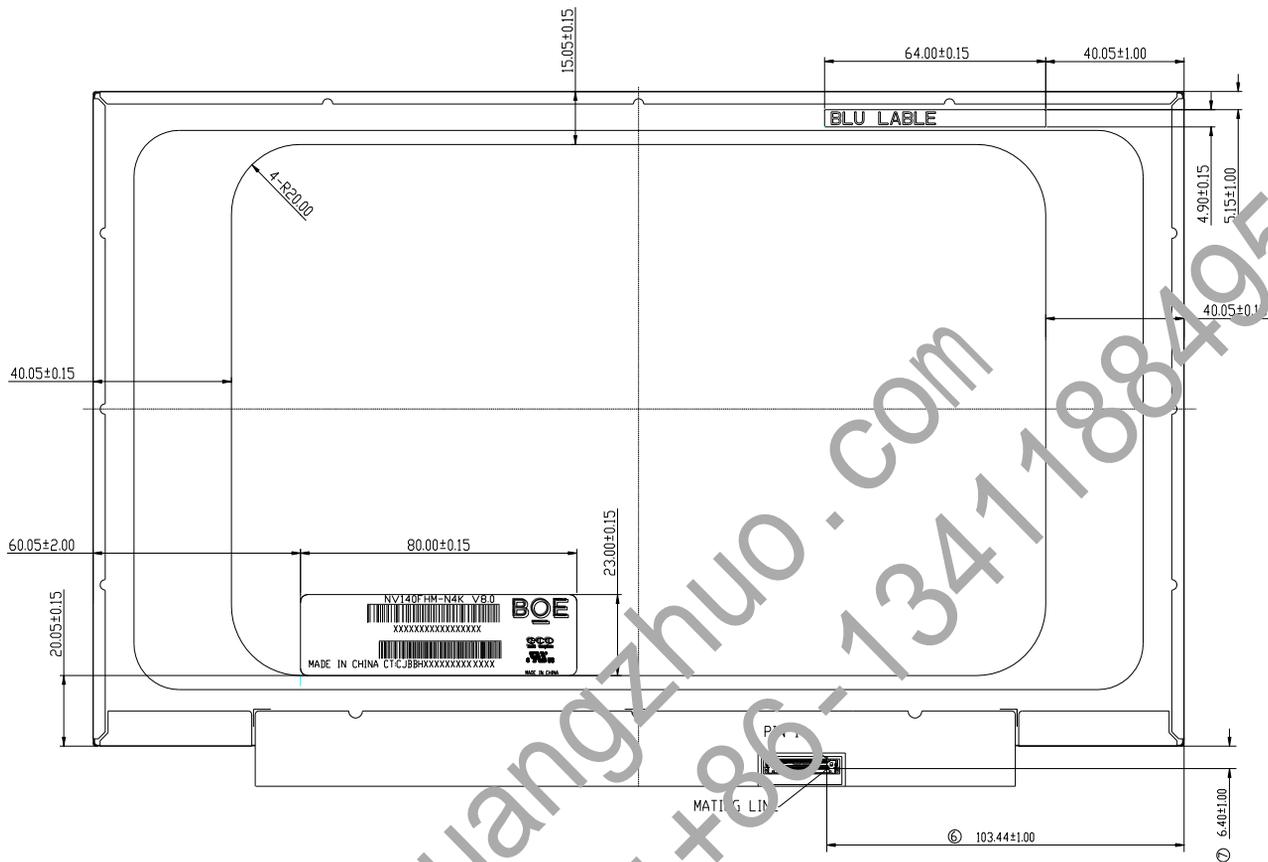


Figure 22. TFT-LCD Module Outline Dimensions (Rear view)

Note:

1. Top Polarizer is the highest part.
2. Curve Spec: $0 \leq d \leq 0.5$ mm.
3. No light leakage from all 4 corners of LCM.
4. Size Unit: mm.
5. General Tolerance: ± 0.3 mm.
6. The MDL dimension measurement tool is a Vernier Caliper;

16.0 EDID Table

Address (HEX)	Function	Hex	Dec	crc	Input values.	Notes
00	Header	00	0		0	EDID Header
01		FF	255		255	
02		FF	255		255	
03		FF	255		255	
04		FF	255		255	
05		FF	255		255	
06		FF	255		255	
07		00	0		0	
08	ID Manufacturer Name	09	9		BOE	ID = BOE
09		E5	229			
0A	ID Product Code	68	104		2152	ID = 2152
0B		08	8			
0C	32-bit serial No.	00	0		0	
0D		00	0		0	
0E		00	0		0	
0F		00	0		0	
10	Week of manufacture	03	3		3	
11	Year of Manufacture	1D	29		2019	Manufactured in 2019
12	EDID Structure Ver.	01	1			EDID Ver 1.0
13	EDID revision #	04	4		4	EDID Rev. 0.4
14	Video input definition	95	149		-	Refer to right table
15	Max H image size	1F	31		31	30.9312 cm (Approx)
16	Max V image size	11	17		17	17.3988 cm (Approx)
17	Display Gamma	78	120		2.2	Gamma curve = 2.2
18	Feature support	03	3		-	Refer to right table
19	Red/Green low bits	28	40		-	Red / Green Low Bits
1A	Blue/White low bits	65	101		-	Blue / White Low Bits
1B	Red x high bits	9	151	604	0.590	Red (x) = 10010111 (0.59)
1C	Red y high bits	39	89	358	0.350	Red (y) = 01011001 (0.35)
1D	Green x high bits	5	84	338	0.330	Green (x) = 01010100 (0.33)
1E	Green y high bits	8E	142	568	0.555	Green (y) = 10001110 (0.555)
1F	Blue x high bits	27	39	157	0.153	Blue (x) = 00100111 (0.153)
20	Blue y high bits	1E	30	122	0.119	
21	White x high bits	50	80	321	0.313	White (x) = 01010000 (0.313)
22	White y high bits	54	84	337	0.329	White (y) = 01010100 (0.329)
23	Established timing 1	00	0		-	Refer to right table
24	Established timing 2	00	0		-	
25	Established timing 3	00	0		-	

26	Standard timing #1	01	1			Not Used
27		01	1			
28	Standard timing #2	01	1			Not Used
29		01	1			
2A	Standard timing #3	01	1			Not Used
2B		01	1			
2C	Standard timing #4	01	1			Not Used
2D		01	1			
2E	Standard timing #5	01	1			Not Used
2F		01	1			
30	Standard timing #6	01	1			Not Used
31		01	1			
32	Standard timing #7	01	1			Not Used
33		01	1			
34	Standard timing #8	01	1			Not Used
35		01	1			
36	Detailed timing (monitor descriptor #1)	C2	194		142.7	142.7328MHz Main clock
37		37	55			
38		80	128		1920	Hor Active = 1920
39		CC	204		204	Hor Blanking = 204
3A		70	112		-	4 bits of Hor. Active + 4 bits of Hor. Blanking
3B		38	56		1080	Ver Active = 1080
3C		28	40		40	Ver Blanking = 40
3D		40	64		-	4 bits of Ver. Active + 4 bits of Ver. Blanking
3E		30	48		48	Hor Sync Offset = 48
3F		20	32		32	H Sync Pulse Width = 32
40		56	54		3	V sync Offset = 3 line
41		00	0		6	V Sync Pulse width : 6 line
42		35	53		309	Horizontal Image Size = 309.312 mm (Low 8 bits)
43		AE	174		174	Vertical Image Size = 173.988 mm (Low 8 bits)
44		10	16		-	4 bits of Hor Image Size + 4 bits of Ver Image Size
45		00	0		0	Hor Border (pixels)
46		00	0		0	Vertical Border (Lines)
47	1A	26		-	Refer to right table	

48	Detailed timing/monitor descriptor #2	2C	44		95.2	95.1552MHz Main clock	
49		25	37				
4A		80	128		1920	Hor Active = 1920	
4B		CC	204		204	Hor Blanking = 204	
4C		70	112		-	4 bits of Hor. Active + 4 bits of Hor. Blanking	
4D		38	56		1080	Ver Active = 1080	
4E		28	40		40	Ver Blanking = 40	
4F		40	64		-	4 bits of Ver. Active + 4 bits of Ver. Blanking	
50		30	48		48	Hor Sync Offset = 48	
51		20	32		32	Hor Sync Pulse Width = 32	
52		36	54		3	V sync Offset = 3 line	
53		00	0		6	V Sync pulse width : 6 line	
54		35	53		309	Horizontal Image Size = 309.312 mm (Low 8 bits)	
55		AE	174		173	Vertical Image Size = 173.988 mm (Low 8 bits)	
56		10	16		-	4 bits of Hor Image Size + 4 bits of Ver Image Size	
57		00	0		0	Hor Border (pixels)	
58		00	0		0	Vertical Border (Lines)	
59		1A	26		-	Refer to right above table	
5A		Detailed timing/monitor descriptor #3	00	0			
5B			00	0			
5C	00		0				
5D	00		0				
5E	00		0				
5F	00		0				
60	00		0				
61	00		0				
62	00		0			Nvidia nvDPS (Refer the tab of nvDPS)	
63	00		0			Lowest refresh rate that does not cause any visual/optical side effect	
64	00	0					
65	00	0					
66	00	0					
67	00	0					
68	00	0					
69	00	0					
6A	00	0					
6B	00	0					

6C	Detailed timing/monitor descriptor #4	00	0		Detailed Timing Description #4
6D		00	0		Flag
6E		00	0		Reserved
6F		02	2		For Brightness Table and Power consumption
70		00	0		Flag
71		0D	13	-	PWM % [7:0] @ Step 0
72		40	64	-	PWM % [7:0] @ Step 5
73		FF	255	-	PWM % [7:0] @ Step 10
74		0A	10	-	Nits [7:0] @ Step 0
75		3C	60	-	Nits [7:0] @ Step 5
76		7D	125	-	Nits [7:0] @ Step 10
77		16	22	-	Panel Electronics Power @ 3x32 Chess Pattern = 900mW
78		11	17	-	Backlight Power @60 nits = 686.117647058824mW
79		21	33	-	Backlight Power @Step 10 = 2700mW
7A		7D	125	-	Nits @ 50% PWM Duty = 250nit
7B		00	0		Format : Terminate with ASCII code 0Ah and pad field with ASCII code 20h
7C	00	0			
7D	00	0			
7E	Extension flag	00	0	1	
7F	Checksum	ED	23	237	-