NV140FHM-N40

HW:V3.1

Product Specification

Rev. P1

HEFEI BOE Optoelectronics Technology Co., Ltd

REVISION HISTORY

(√)Preliminary Specification

( )Final Specification

Revision No.	Page	Description of Changes	Date	Prepared
P0	64	Initial Release	2023.7.7	Zhou Kun
P1	39	Update EDID	2023.11.15	Zhou Kun

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Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

NV140FHM-N40 V3.1 is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 14.0 inch diagonally measured active area with Full-HD resolutions (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.7M (8 bit) colors and color gamut NTSC 45% typ.,40%min.. The TFT-LCD panel used for this module is a low reflection and higher color type. Therefore, this module is suitable for Notebook PC. The LED driver for back-light driving is built in this model.

All input signals are eDP1.2 interface compatible.

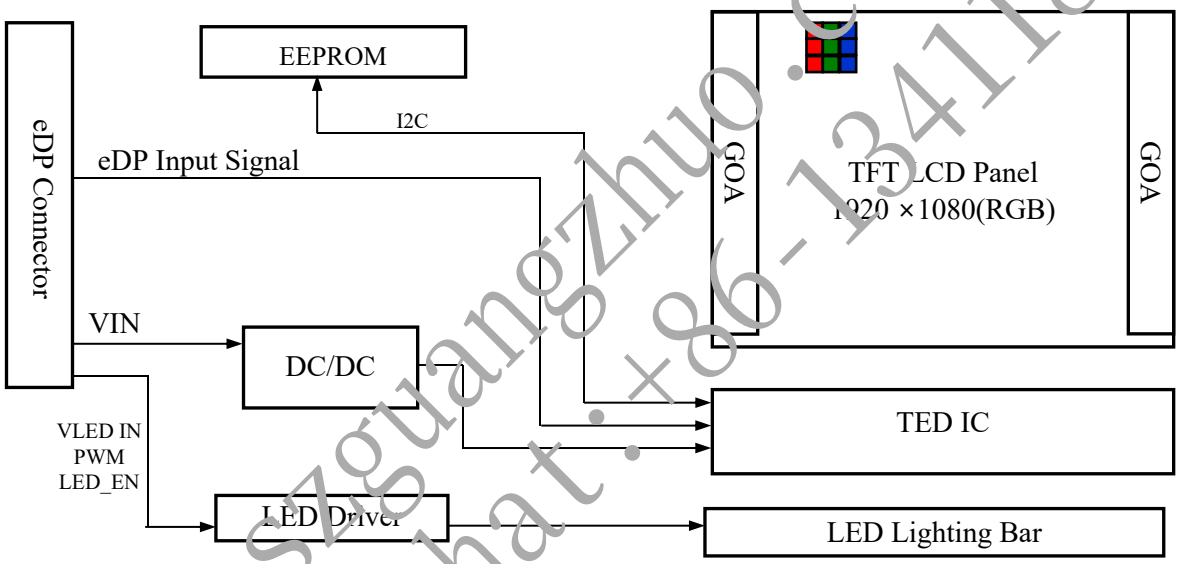


Figure 1. Drive Architecture

1.2 Features

- 2 lane eDP interface with 2.7Gbps link rates
- 16.7M (8bit) color depth, color gamut NTSC 45% typ.,40%min.
- Single LED lighting bar (Bottom side/Horizontal Direction)
- Data enable signal mode
- Side mounting frame
- Green product (RoHS & Halogen free product)
- On board LED driving circuit
- Low driving voltage and low power consumption
- On board EDID chip
- DPCD Version 1.2

1.2.1 Feature Status(no need certification)

No.	Function	Y/N	Remark
1	CABC	N	
2	PSR (remark PSR1 or PSR2 or PSR SU or PSRSU-RC)	N	
3	SDRRS	N	
4	DMRRS	Y	
5	BIST	N	
6	OD (pull high or pull low to enable)	N	
7	DSC	N	
8	FEC	N	
9	LRR (remark LRR1.0 or LRR2.0 or LRR2.5)	N	
10	HDR (remark 400/600/1000)	N	
11	Color Calibration*	N	
12	LBL	N	

1.2.2 Feature Status(need certification)

No.	Function	Y/N	Certification status	Remark
1	Free sync (remark free sync/free sync premium/free sync premium Pro)[1]	Y	Sample Preparing	Free sync
2	G-sync[1]	N		
3	NVSR[1]	N		
4	DDS[1]	N		

[1] need certification under panel alone

1.3 Application

● Notebook PC (Wide type)

1.4 General Specification

The followings are general specifications at the model NV140FHM-N40 V3.1 . (listed in Table 1)

<Table 1. General Specifications>

Parameter	Specification	Unit	Remarks
Active area	309.312(H) x 173.988(V)	mm	
Number of pixels	1920 (H) ×1080 (V)	pixels	
Pixel pitch	161.1(H) ×161.1(V)	um	
Pixel arrangement	RGB Vertical stripe		
Display colors	16.7M(8bit)		
Color gamut	45% typ.,40%min.		NTSC
Display mode	Normally black		
Dimensional outline	315.012±0.3(H)x184.838±0.3(V) *3.0 Max.(Body) 315.012±0.3(H)x184.838±0.3(V) *5.0 Max.(PCBA)	mm	
Weight	290(max)	g	
Surface treatment	Anti-Glare		
Surface hardness	3H		
Back-light	Bottom edge side, 1-LED lighting bar type		Note 1
Power consumption	P_D : 0.39(Max)	W	@Mosaic
	P_{BL} :2.0(Max)	W	W/LED driver
	P_{Total} : 2.39(Max)	W	@Mosaic

Notes : 1. LED Lighting Bar (54*LED Array)

2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Absolute Maximum Ratings>

Ta=25+/-2°C

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-0.3	4.0	V	Note 1
eDP input Voltage	V_{eDP}	-0.3	1.4	V	
Logic Supply Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V	
Operating Temperature	T_{OP}	0	+50	°C	Note 2
Storage Temperature	T_{ST}	-20	+60	°C	

Notes :
1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.
2. Temperature and relative humidity range are shown in the figure below.
95 % RH Max. (40 °C ≥ Ta) Maximum wet - bulb temperature at 39 °C or less. (Ta > 40 °C) No condensation.

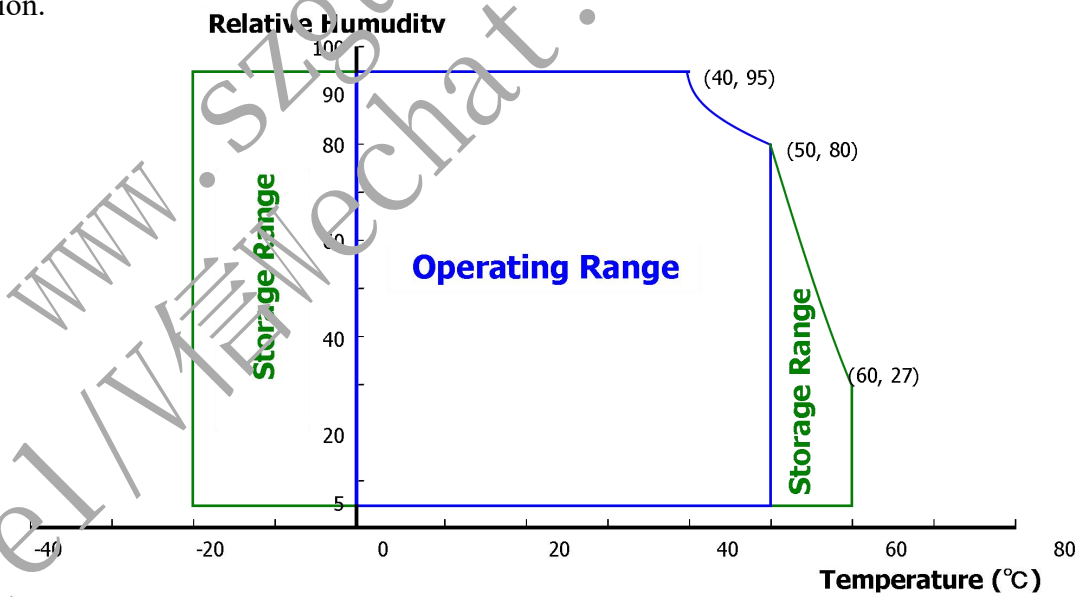


Figure 2. Temperature and Relative Humidity Range

3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

< Table 3. Electrical Specifications > Ta=25+/-2°C

Parameter			Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage		V_{DD}	3.0	3.3	3.6	V	Note 1
Permissible Input Ripple Voltage		V_{RF}	-10% VDD	-	+10% VDD	V	@ V_{DD} = 3.3 V
Power Supply Inrush Current		Inrush	-	-	2	A	Note3
Power Supply Current	Mosaic	I_{DD}	-	109	118	mA	Note 1
	RGB		-	-	121	mA	
Power Consumption	Mosaic	P_M	-	0.36	0.39	W	
	RGB	P_{RGB}	-	-	0.40	W	
	BLU	P_{BL}	-	-	2.0	W	Note 2
	Total	P_{Total}	-	-	2.39	W	@Mosaic

3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

Notes :

1. The supply voltage is measured and specified at the interface connector of LCM.
   The current draw and power consumption specified is for 3.3V at 25 ℃.
   a) Mosaic pattern 8*8
   b) R/G/B patterns

(a) (b)

Figure 3. Power Measure Patterns

2. Calculated value for reference ($V_{LED} \times I_{LED}$) , The power consumption with LED Driver are under the VLED = 12.0V , 25℃, PWM Duty 100%.
3. Measure condition (Figure 4)

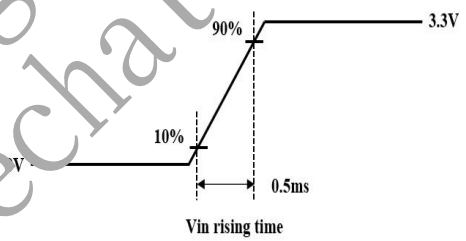


Figure 4. Inrush Measure Condition

4. Input voltage range:3.0~3.6V.Test condition: Oscilloscope bandwidth 20MHz, AC coupling

3.2 Backlight Unit

< Table 4. LED Driving Guideline Specifications > Ta=25+/-2°C

Parameter			Min.	Typ.	Max.	Unit	Remarks
LED Forward Voltage		V_F	-	-	2.9	V	
LED Forward Current		I_F	-	9.6	-	mA	
LED Power Input Voltage		VLED	5	12	21	V	
LED Power Input Current		I_{LED}	-	-	166.67	mA	Note 1
LED Power Consumption		P_{LED}	-	-	2.0	W	
Power Supply Voltage for LED Driver Inrush		Iled inrush	-	-	1.5	A	Note 3
LED Life-Time		N/A	15,000	-	-	Hour	I_F = 9.6mA Note 2
EN Control Level	Backlight On	V_{BL_EN}	1.2	-	5.0	V	
	Backlight Off		-	-	0.6	V	
PWM Control Level	High Level	V_{BL_PWM}	1.2	-	5.0	V	
	Low Level		-	-	0.6	V	
PWM Control Frequency		F_{PWM}	200	-	2,000	Hz	
Duty Ratio			5	-	100	%	

Notes :
1. Power supply voltage12V for LED driver.
   Calculator value for reference IF × VF ×54 /driver efficiency = PLED
2. The LED life-time define as the estimated time to 50% degradation of initial luminous.
3. Measure condition (Figure 5)

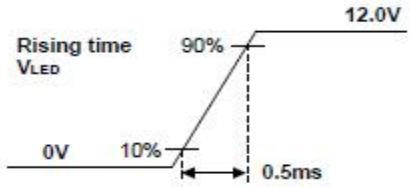


Figure 5. Inrush Measure Condition

3.3 LED Structure

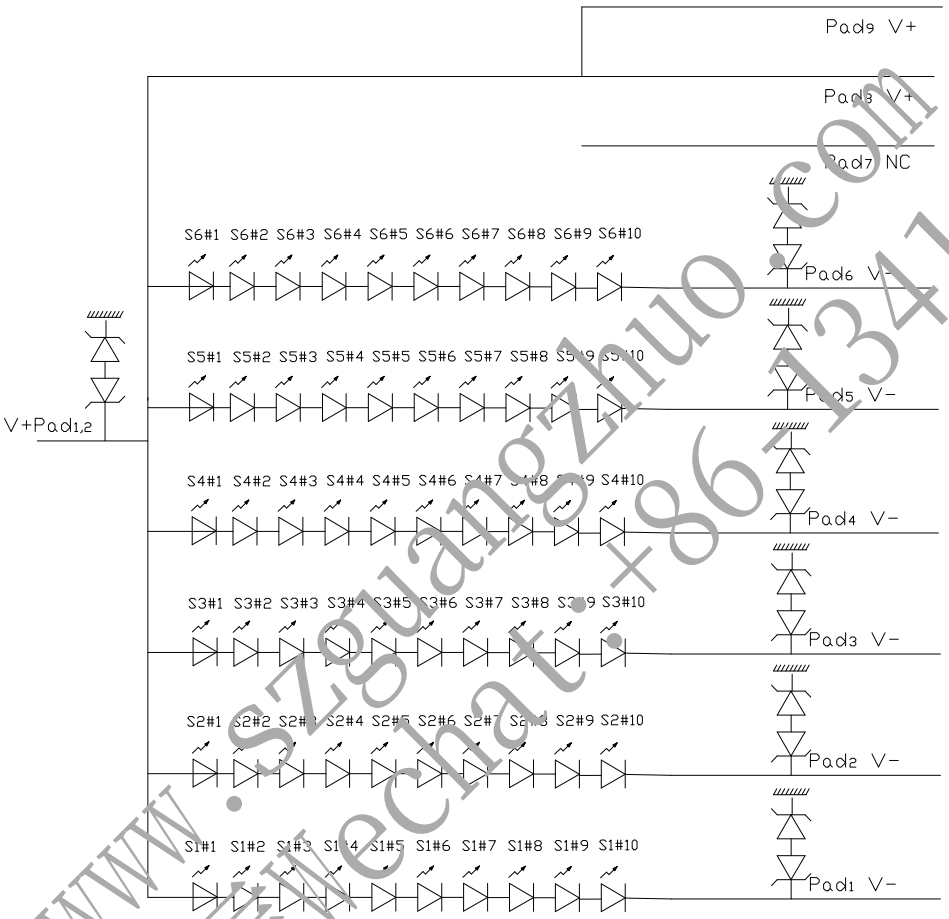


Figure 6. LED Structure

4.0 OPTICAL SPECIFICATION

4.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2°C) with the equipment of luminance meter system (SR3&ENC Q-FPMS-37A) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to θØ=0 (=θ3) as the 3 o'clock direction (the "right"), θØ=90 (= θ12) as the 12 o'clock direction ("upward"), θØ=180 (= θ9) as the 9 o'clock direction ("left") and θØ=270(= θ6) as the 6 o'clock direction ("bottom"). While scanning θand/or Ø, the center of the measuring spot on the display surface shall stay fixed. The backlight should be operating for 30 minutes prior to measurement. VDD shall be 3.3+/- 0.3V at 25°C. Optimum viewing angle direction is 6 'clock.

4.2 Optical Specifications

<Table 5. Optical Specifications>

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ_3	CR > 10	80	89	-	Deg.	Note 1
		Θ_9		80	89	-	Deg.	
	Vertical	Θ_{12}		80	89	-	Deg.	
		Θ_6		80	89	-	Deg.	
Luminance Contrast Ratio		CR	Θ = 0°	1000	1200	-		Note 2
Luminance of White	5 Points	Y_L	Θ = 0° I_{LED} = 9.6mA	255	300	-	cd/m²	Note 3
White Luminance Uniformity	5 Points	ΔY5		-	-	-	%	Note 4
	13 Points	ΔY13		62.5	71.4	-	%	
White Chromaticity		W_x	Θ = 0°	0.283	0.313	0.343		Note 5
		W_y		0.299	0.329	0.359		
Reproduction of Color	Red	R_x	Θ = 0°	Typ.-0.03	0.59	Typ.+0.03		
		R_y			0.35			
	Green	G_x			0.34			
		G_y			0.56			
	Blue	B_x			0.16			
		B_y			0.14			
Color Gamut				40	45	-	%	NTSC
Response Time (Rising + Falling)		T_{RT}	Ta= 25°C Θ = 0°	-	25	35	ms	Note 6
Cross Talk		CT	Θ = 0°	-	-	2.0	%	Note 7
Gamma		-	-	2.0	2..2	2.4		

Notes :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 7).

2. Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see Figure 7) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Center Luminance of white is defined as luminance values of 5 point average across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 8 for a total of the measurements per display.

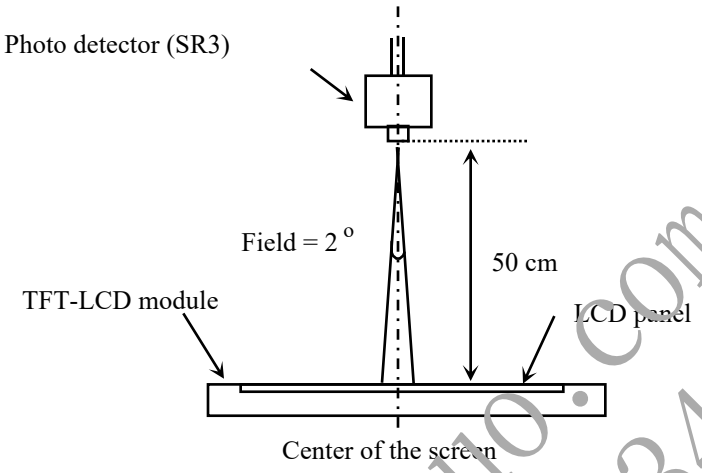
4. The White luminance uniformity on LCD surface is then expressed as : ΔY =Minimum Luminance of 5(or 13) points / Maximum Luminance of 5(or 13) points.(see Figure 8 and Figure 9).

5. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

6. The electro-optical response time measurements shall be made as Figure 10 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_f, and 90% to 10% is T_r.

7. Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 10±1mm diameter area, with all display pixels set to gray 127(of 0 to 255), to the luminance (YB) of that same area when any adjacent area is driven dark.The luminance ratio shall not exceed 1:1.05 (See Figure 11).

4.3 Optical Measurements



Optical characteristics measurement setup

Figure 7. Measurement Set Up

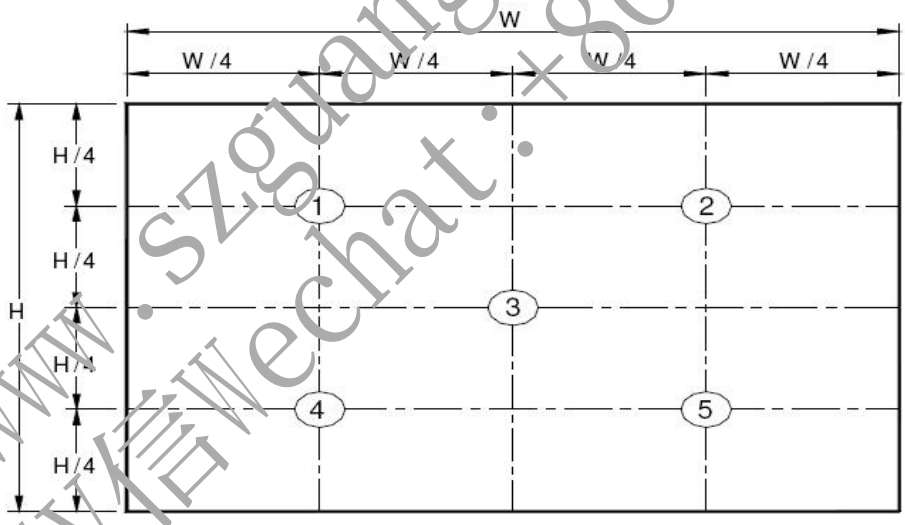


Figure 8. White Luminance and Uniformity Measurement Locations (5 points)

Center Luminance of white is defined as luminance values of center 5 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 7 for a total of the measurements per display.

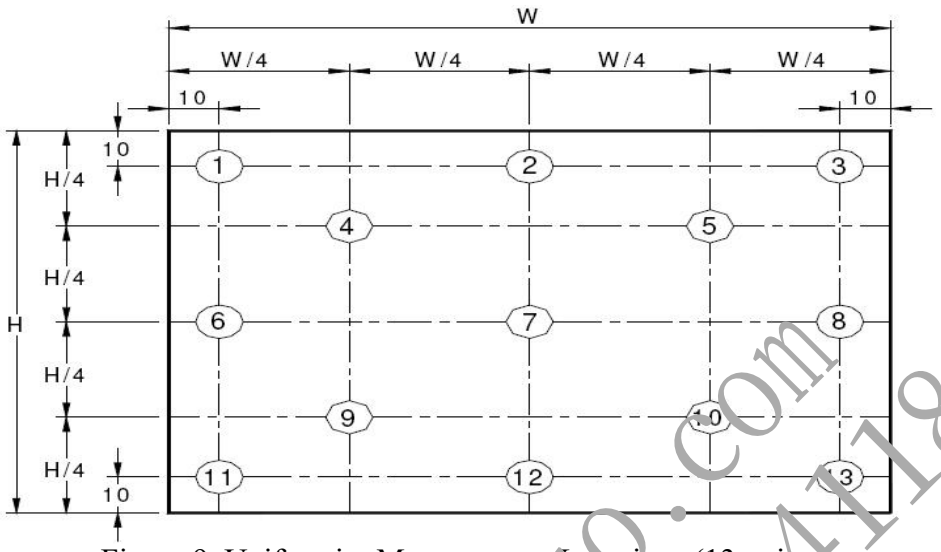


Figure 9. Uniformity Measurement Locations (13 points)

The White luminance uniformity on LCD surface is then expressed as : ΔY5 = Minimum Luminance of five points / Maximum Luminance of five points (see Figure 8) , ΔY13 = Minimum Luminance of 13 points /Maximum Luminance of 13 points (see Figure 9).

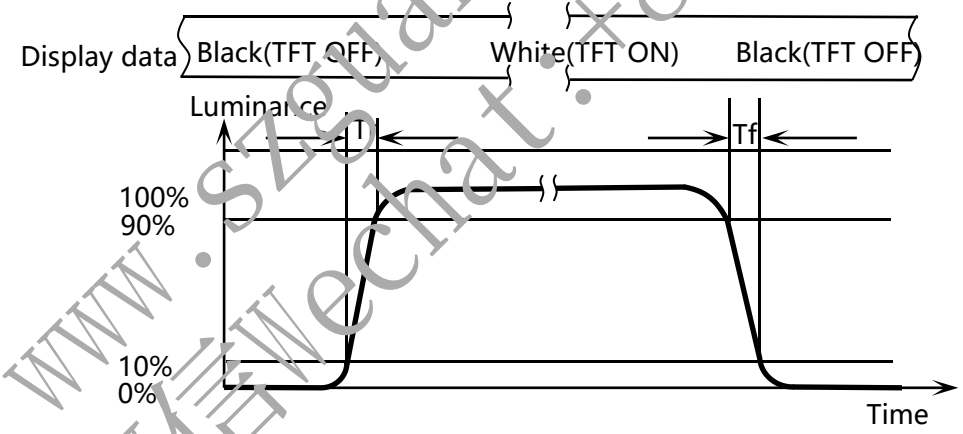
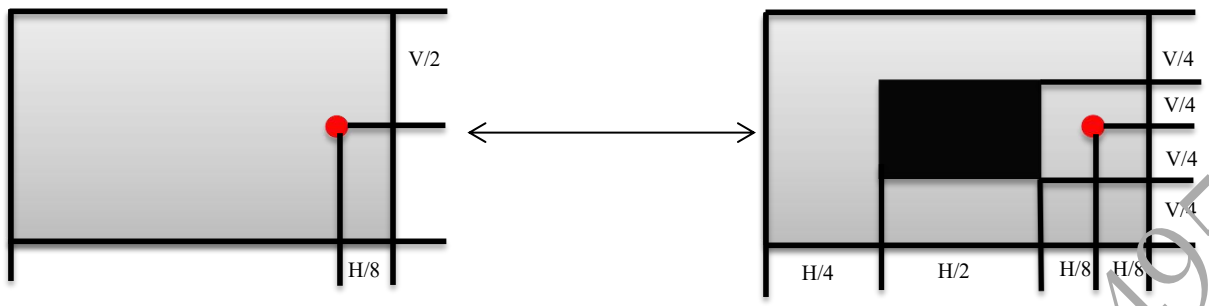


Figure 10. Response Time Testing

The electro optical response time measurements shall be made as shown in Figure 10 by switching the "data" input signal ON and OFF. Tr: The luminance to change from 10% to 90% ,Tf: The luminance to change from 90% to 10% .

The test system : LMS ENC Q-FPMS-37A



$$\text{Cross Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_B} \right| \times 100$$

Figure 11. Cross Talk Modulation Test Description

Where:

Y_A = Initial luminance of measured area (cd/m^2)

Y_B = Subsequent luminance of measured area (cd/m^2)

The location measured will be exactly the same in both patterns. The test background gray is L127.

Cross Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 10±1mm diameter area, with all display pixels set to a gray level 127, to the luminance (YB) of that same area when any adjacent area is driven dark.(Refer to Figure 11)

The test system: SR3

5.0 INTERFACE CONNECTION

5.1 Electrical Interface Connection

The electronics interface connector is STM MSAK24025P30.

The connector interface pin assignments are listed in Table 6.

<Table 6. Pin Assignments for the Interface Connector>

Terminal	Symbol	Functions
Pin No.	Symbol	Description
1	CABC_EN	Disable
2	H_GND	Ground
3	LANE1_N	eDP RX Channel 1 Negative
4	LANE1_P	eDP RX Channel 1 Positive
5	H_GND	Ground
6	LANE0_N	eDP RX Channel 0 Negative
7	LANE0_P	eDP RX Channel 0 Positive
8	H_GND	Ground
9	AUX_CH_P	eDP AUX CH Positive
10	AUX_CH_N	eDP AUX CH Negative
11	H_GND	Ground
12	LCD_VCC	Power Supply, 3.3V (typ.)
13	LCD_VCC	Power Supply, 3.3V (typ.)
14	BIST	Disable
15	H_GND	Ground
16	H_GND	Ground
17	HPD	Hot Plug Detect Output
18	BL_GND	LED Ground
19	BL_GND	LED Ground
20	BL_GND	LED Ground
21	BL_GND	LED Ground
22	BL_ENABLE	LED Enable Pin(+3.3V Input)
23	BL_PWM	System PWM Signal Input
24	NC	No Connection
25	NC	No Connection
26	BL_POWER	LED Power Supply 5V-21V
27	BL_POWER	LED Power Supply 5V-21V
28	BL_POWER	LED Power Supply 5V-21V
29	BL_POWER	LED Power Supply 5V-21V
30	NC	No Connection

5.2 eDP Interface

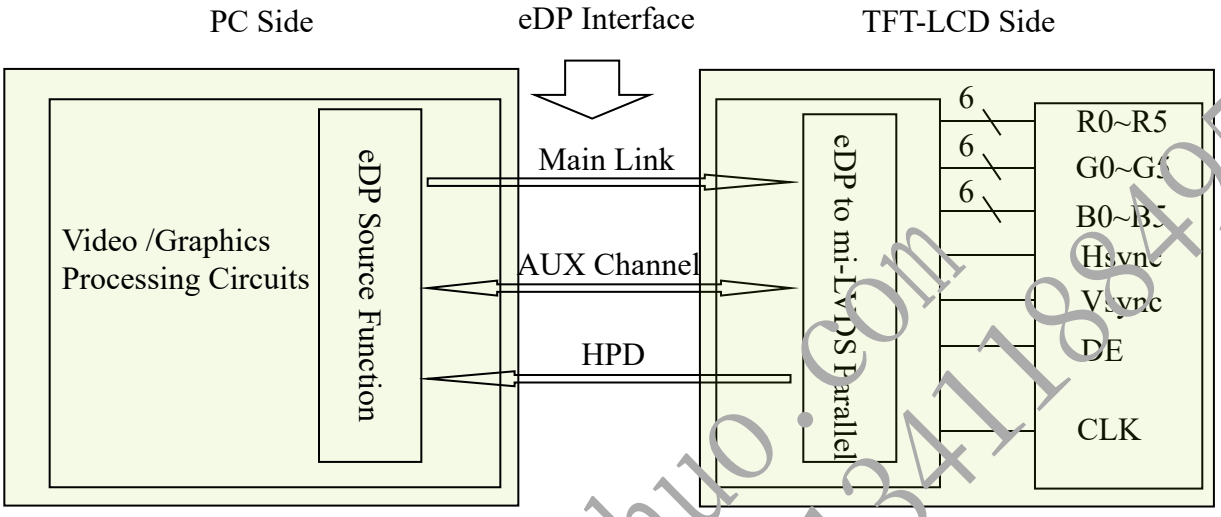


Figure 12. eDP Interface Architecture

Note:
Transmitter : Cerebrex CRX2000AC or equivalent.

5.3 Data Input Format

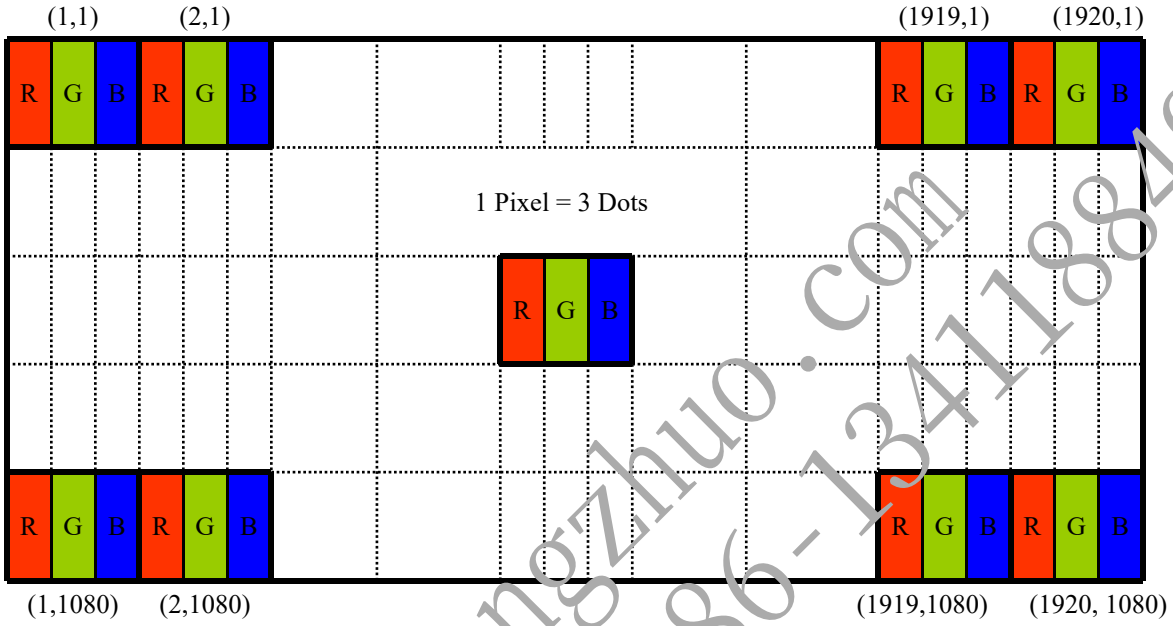


Figure 13. Display Position of Input Data (V-H)

5.4 Back-light & LCM Interface Connection

BLU Interface Connector: STM MSK24036P9HC .

<Table 7. Pin Assignments for the BLU Connector>

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vout	LED anode connection	6	LED	LED cathode connection
2	Vout	LED anode connection	7	LED	LED cathode connection
3	NC	No Connection	8	LED	LED cathode connection
4	LED	LED cathode connection	9	LED	LED cathode connection
5	LED	LED cathode connection	-	-	-

6.0 SIGNAL TIMING SPECIFICATION

6.1 The NV140FHM-N40 V3.1 Is Operated By The DE Only

< Table 8. Signal Timing Specification >

Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	95.2	142.8	142.8	MHz
Frame Period		Tv	1120	1120	1120	lines
			40	60	60	Hz
			16.67	16.67	25	ms
Vertical Display Period		Tvd	1080	1080	1080	lines
One line Scanning Period		Th	2124	2124	2124	clocks
Horizontal Display Period		Thd	1920	1920	1920	clocks

Note : The above is as optimized setting.

6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 9.

<Table 9. eDP Main-Link RX TP4 Package Pin Parameters>

Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock (Link clock down-spreading)	ssc	-	-	0.5	%	
Differential peak-to-peak input voltage at package pins	$V_{RX-DIFFp-p}$	200	-	800	mV	
Rx input DC common mode voltage	$V_{RX\_DC\_CM}$	0.8	-	1	V	
Differential termination resistance	$R_{RX-DIFF}$	-	100	-	Ω	
Single-ended termination resistance	R_{RX-SE}	40	-	60	Ω	
Rx short circuit current limit	I_{RX_SHORT}	-	-	50	mA	
Intra-pair skew at Rx package pins (HBR) RX intra-pair skew tolerance at HBR	$L_{RX\_SKEW\_INTRA\_PAIR}$	-	370	-	ps	
AC Coupling Capacitor	C_{SOURCE_ML}	75		200	nF	Source side

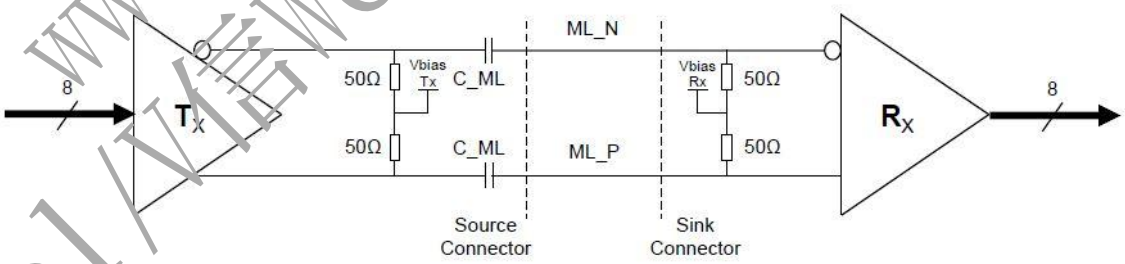


Figure 14. Main link differential pair

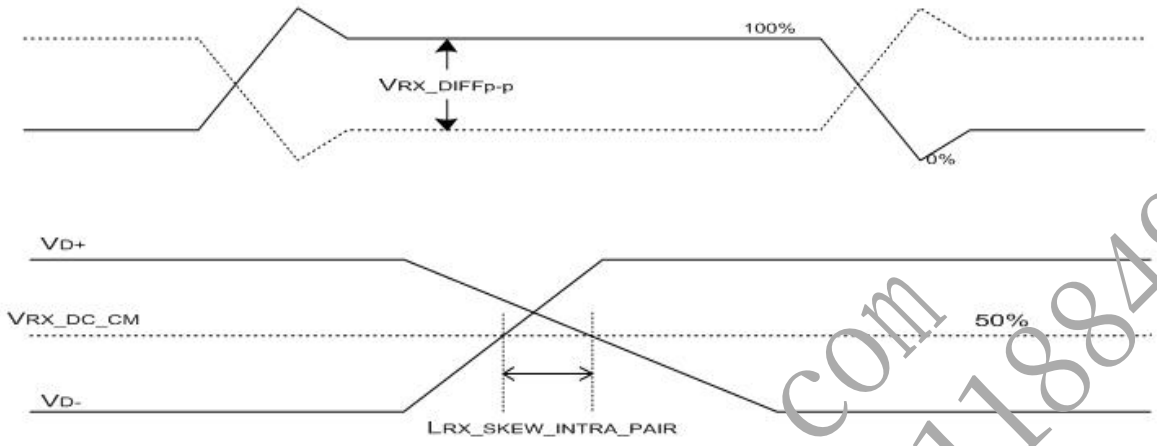


Figure 15. VRX-DIFFp-p と LRX_SKEW_INTRA_PAIR

<Table 10. HPD Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
HPD voltage	V_{HPD}	2.25	-	3.6	V	
Hot Plug Detection Threshold	-	2.0	-	-	V	Source side Detecting
Hot Unplug Detection Threshold	-	-	-	0.8V	V	
HPD_IRQ Pulse Width	HPD_IRQ	0.5	-	1	ms	
HPD_TimeOut	-	2.0	-	-	ms	

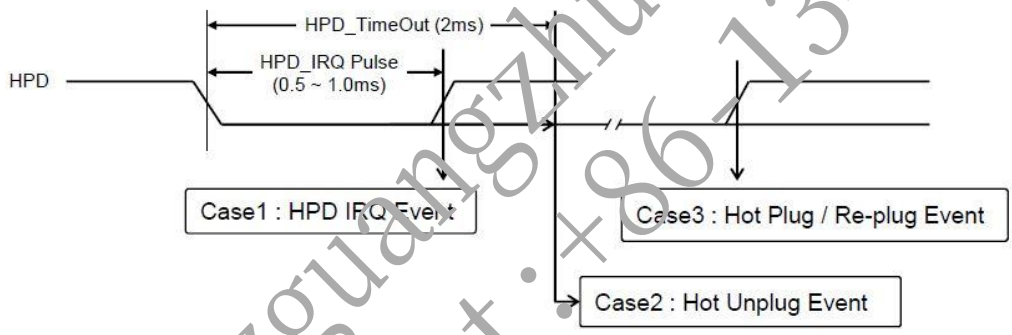


Figure 16. HPD Events

<Table 11. AUX Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
AUX unit interval	UIAUX	0.4	0.5	0.6	Us	
AUX peak-to-peak input differential voltage	VAUX-RX-DIFFp-p	0.29	-	1.38	V	
AUX CH termination DC resistance	RAUX-TERM	80	100	120	Ohm	
AUX DC common mode voltage	VAUX-DC-CM	0	-	2	V	
AUX turn around common mode voltage	VAUX-TURN-CM	-	-	0.3	V	
AUX short circuit current limit	IAUX-SHORT	-	-	90	mA	
AUX AC Coupling Capacitor	CSOURCE-AUX	75	-	200	nf	Source side

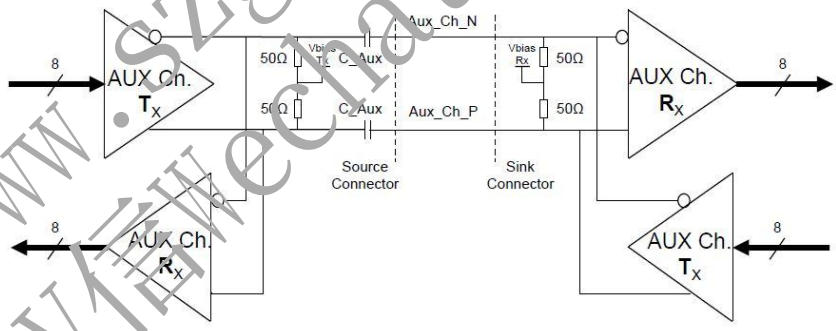


Figure 17. AUX differential pair

7.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

<Table 12. Input Signal & Basic Display Colors & Gray Scale of Colors >

	Colors & Gray scale	Data signal																							
		R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Light Blue	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Purple	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△				↑								↑								↑				
	▽				↓								↓								↓				
	Brighter	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▽	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△				↑								↑								↑				
	▽				↓								↓								↓				
	Brighter	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	▽	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	△				↑								↑								↑				
	▽				↓								↓								↓				
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Gray scale of White & Black	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	△				↑								↑								↑				
	▽				↓								↓								↓				
	Brighter	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1
	▽	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

8.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown i n below.

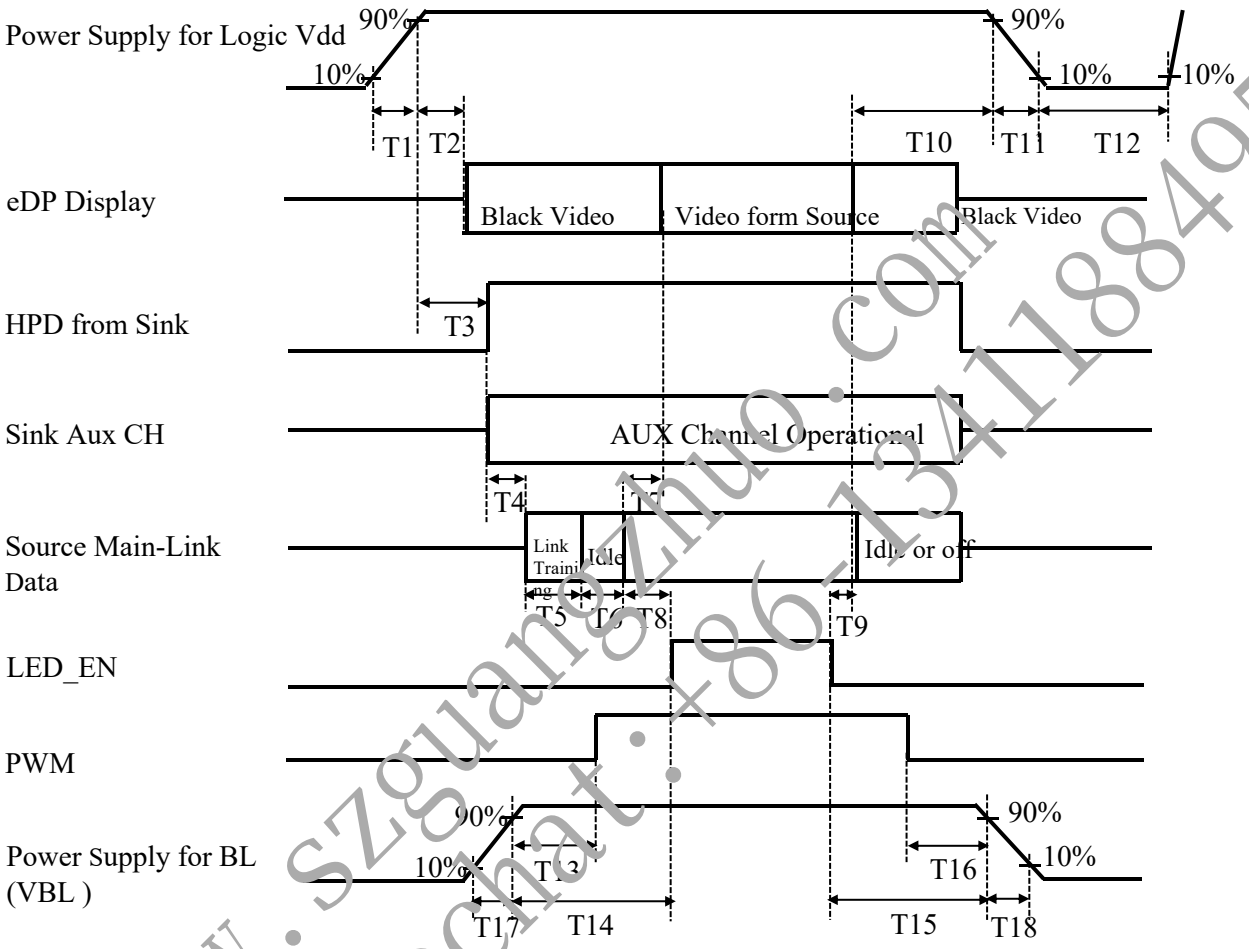


Figure 18. Power Sequence

- 0.5ms ≤ T1 ≤ 10 ms
- 0ms < T2 ≤ 200 ms
- 0ms < T3 ≤ 200 ms
- T4+T5+T6+T8>80ms
- 0ms < T7 ≤ 50ms
- 50ms < T8
- 0ms < T9
- 100ms < T10 < 500 ms
- 0.5ms ≤ T11 ≤ 10 ms
- 500ms ≤ T12
- 0ms < T13
- 0ms < T14
- 0ms < T15
- 0ms < T16
- 0.5ms ≤ T17
- 0.5ms ≤ T18

Notes:

1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal are valid.

9.0 Connector Description

Physical interface is described as for the connector on LCM.
These connectors are capable of accommodating the following signals and will be following components.

9.1 TFT LCD Module

< Table 13. Signal Connector >

Connector Name /Description	For Signal Connector
Manufacturer	STM
Type/ Part Number	MSAK24025R30
Mating Housing/ Part Number	I-PEX 20454-030T

10.0 MECHANICAL CHARACTERISTICS

10.1 Dimensional Requirements

Figure 23shows mechanical outlines for the model NV140FHM-N40 V3.1 .
Other parameters are shown in Table 14.

<Table 14. Dimensional Parameters>

Parameter	Specification	Unit
Active Area	309.312(H) x 173.988(V)	mm
Number of pixels	1920 (H) X 1080 (V) (1 pixel = R + G + B dots)	pixels
Pixel pitch	161.1(H) ×161.1(V)	um
Pixel arrangement	RGB Vertical stripe	
Display colors	16.7M(8bit)	
Display mode	Normally Black	
Dimensional outline	315.012±0.3(H)x184.838±0.3(V) *3.0 Max.(Body) 315.012±0.3(H)x184.838±0.3(V) *5.0 Max.(PCBA)	mm
Weight	290(max)	g

10.2 Mounting

See Figure 23.

10.3 Anti-Glare and Polarizer Hardness.

The surface of the LCD has an Anti-Glare coating to minimize reflection and the surface hardness is 3H.

10.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen fro m a distance 50cm from the screen with an overhead light level of 350lux.

11.0 RELIABILITY TEST

The reliability test items and its conditions are shown in below.

<Table 15. Reliability Test>

No	Test Items	Conditions	Remark
1	High temperature storage test	Ta = 60°C, 300 hrs	
2	Low temperature storage test	Ta = -20°C , 300 hrs	
3	High temperature & high humidity operation test	Ta = 40°C , 90%RH, 300 hrs	
4	High temperature operation test	Ta = 50°C , 300 hrs	
5	Low temperature operation test	Ta = 0°C , 300 hrs	
6	Thermal shock	Ta = -20 °C ↔ 60 °C (0.5 hr), 60%±3%RH, 100 cycle	
7	Vibration test (non-operating)	Ta = 25°C , 60%RH, 1.5G, 10~500Hz, Sine X,Y,Z / Sweep rate : 30mins	Note 1
8	Shock test (non-operating)	Ta = 25°C , 60%RH, 220G, Half Sine Wave 2 msec ±X,±Y,±Z Once for each direction	Note 1
9	Electro-static discharge test (operating)	Air : 150 pF, 330Ω, ±15 KV Contact : 150 pF, 330Ω, ±8 KV Ta = 25°C , 60%RH,	Note 2

Notes :

1. The fixture must be hard enough so that the module would not be twisted or bent.
2. Self- recovery and restart recovery is allowed. No hardware failures.

12.0 HANDLING & CAUTIONS

(1) Cautions when taking out the module
- Pick the pouch only, when taking out module from a shipping package.

(2) Cautions for handling the module
- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation
- When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

(4) Cautions for the atmosphere
- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics
- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions
- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc. Please pack the module not to be broken. We recommend to use the original shipping packages.

13.0 LABEL

(1) Product Label

Figure 19. Product Label

Label Size: 48mm × 12mm
1. FG-CODE: NV140FHM-N40
2. Version Number: V3.1
3. Customer CT 2D label（客户端使用）
4. CT number，A.CODE: TDPD
5. HP PN: N69396-L91
6. MDL ID
7. MDL ID Bar code（厂内使用）
8. MADE IN CHINA (产地)

<Table 16. Module ID Naming Rule>

MDL ID 编码规则

序列号	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
代码	X	X	X	3	X	X	X	X	X	X	X	X	X	X	X	X	X
描述	CBN代码		等级	B3	年		月	FG Code后四位				序列号					

(2) High voltage caution label

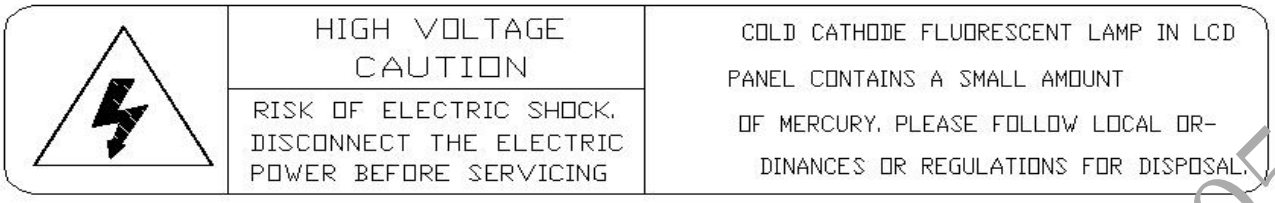


Figure 20. High Voltage Caution Label

(3) Box label

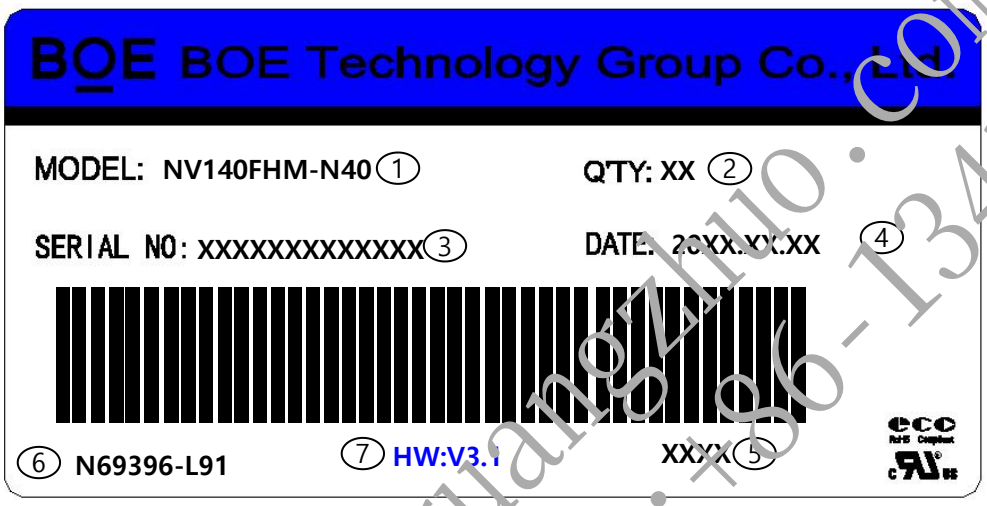


Figure 21.Box Label

Label Size: 110mm*55mm

1. FG-CODE
2. Box 产品数量
3. Box ID
4. Box Packing 日期
5. FG-CODE 后四位
6. 客户料号 N69396-L91
7. HW:V3.1

<Table 17. Box Label Naming Rule >

Digit / Code	1	2	3	4	5	6	7	8	9	10	11	12	13
Code	B	9	A	F	1	7	8	N	0	0	3	2	7
Description	Product Name		Product Grade	B3	Year		Month	Revision	BOX Serial Number				

14.0 PACKING INFORMATION

14.1 Packing Order

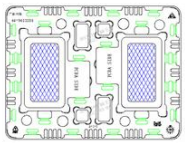
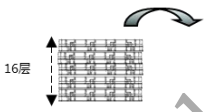
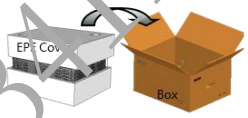
在Tray每穴中各放入1pcs LCM （CF面朝上），再在产品上各放置1pcs EPE Spacer 容量：2pcs EPE Spacer / Tray 2pcs LCM/Tray	堆叠放置15pcs Tray（不旋转堆叠），顶部再放置1pcs空Tray，将16pcs Tray平放入PE Bag	在Inner Box底部放置1ea EPE Cover，将堆叠好的16pcs Tray平放入Box，再放置1ea EPE Cover 容量：30pcs LCM/Box
 Step 1	 Step 2	 Step 3
对Box进行封箱，并粘贴Box标签	每个Pallet上放4层Box，田字形码放， 1层4箱 Pallet外进行缠绕包装 容量：16pcs Box/Pallet 480pcs LCM/Pallet	两车装载方式：一横一竖双层码放 一车装载量_12m：19200pcs（40托）
 Step 4	 Step 5	

Figure 22 Packing Order

14.2 Note

- Box dimension: 607mm*507mm*240mm
- Package quantity in one box: 30pcs

15.0 MECHANICAL OUTLINE DIMENSION

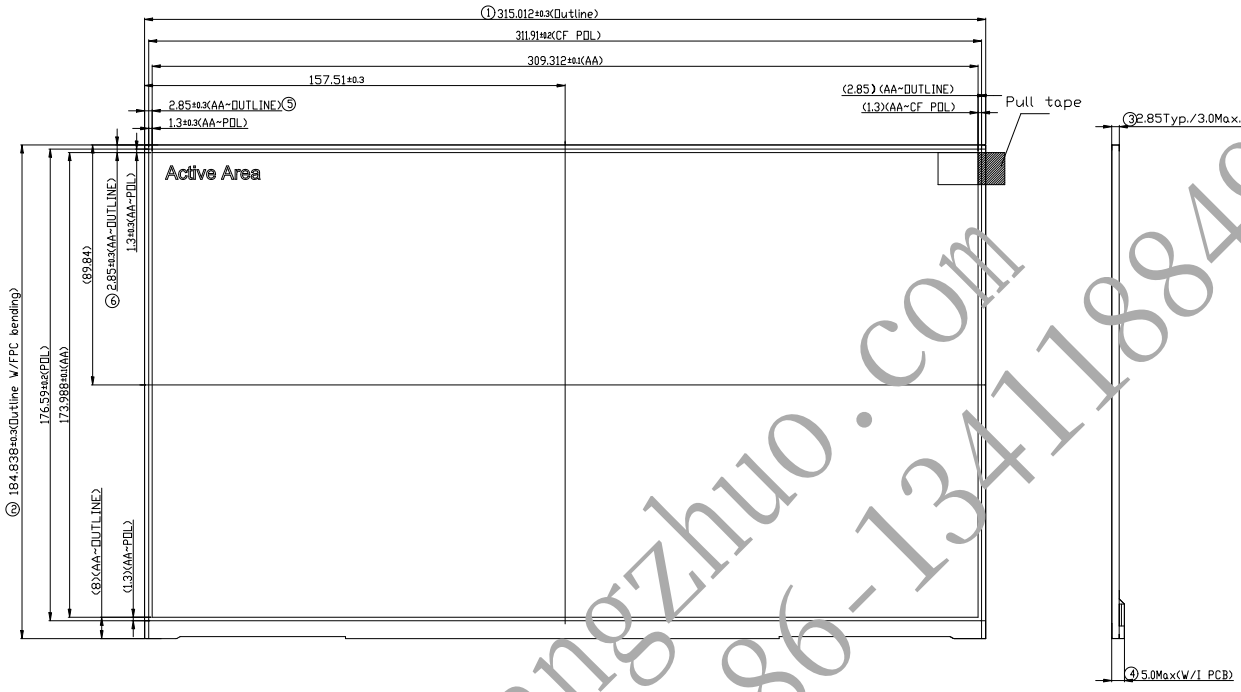


Figure 23. TFT-LCD Module Outline Dimension (Front View)

Notes:

1. The eDP connector is measured at PIN 1 and mating line.
2. Top polarizer is the highest portion.
3. Critical dimension:
4. Measurement method refer to Appendix A
5. System matching refer to Appendix B
6. "()"marks the reference dimensions.

Top POL is the highest portion.

Figure 24. Highest Point Position

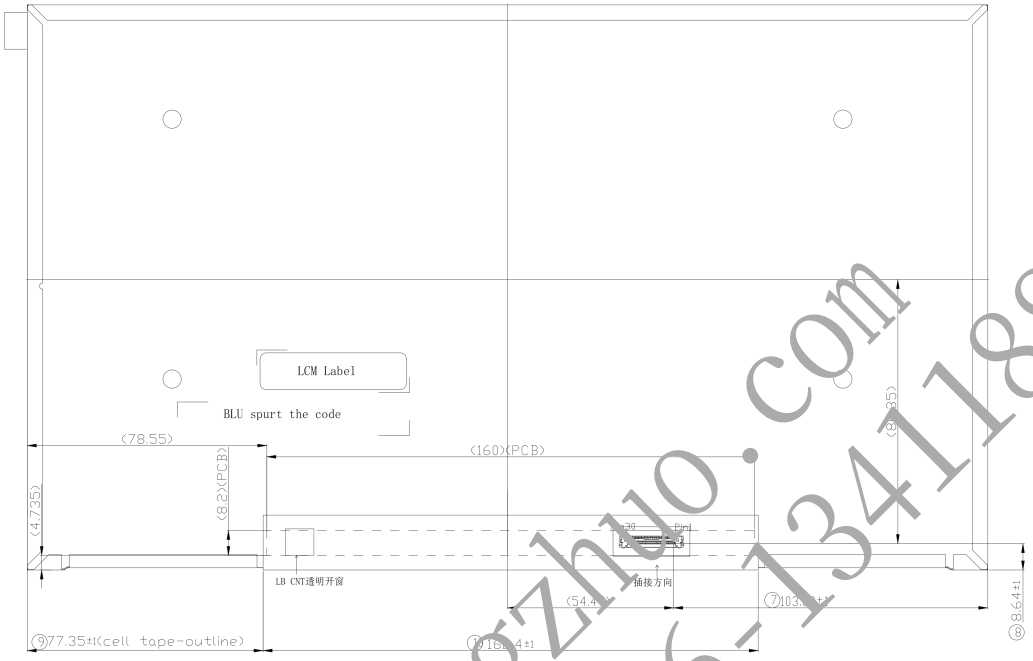


Figure 25. TFT-LCD Module Outline Dimensions (Rear view)

Notes:
1. The eDP connector is measured at PIN 1 and mating line.
2. Top polarizer is the highest portion.
3. Critical dimension:
4. Measurement method refer to Appendix A
5. System matching refer to Appendix B
6. “()”marks the reference dimensions.

16.0 EDID Table

Address (HEX)	Function	Hex	Dec	crc	Input values.	Notes
00	Header	00	0		0	EDID Header
01		FF	255		255	
02		FF	255		255	
03		FF	255		255	
04		FF	255		255	
05		FF	255		255	
06		FF	255		255	
07		00	0		0	
08	ID Manufacturer Name	09	9		BOE	ID = BOE
09		E5	229			
0A	ID Product Code	6F	111		3183	ID = 3183
0B		0C	12			
0C	32-bit serial No.	00	0		0	
0D		00	0		0	
0E		00	0		0	
0F		00	0		0	
10	Week of manufacture	19	25		25	
11	Year of Manufacture	21	33		2023	Manufactured in 2023
12	EDID Structure Ver.	01	1		1	EDID Ver 1.0
13	EDID revision #	04	4		4	EDID Rev. 0.4
14	Video input definition	A5	165		-	Refer to right table
15	Max H image size	1F	31		31	30.9 cm (Approx)
16	Max V image size	11	17		17	17.4 cm (Approx)
17	Display Gamma	78	120		2.2	Gamma curve = 2.2
18	Feature support	03	3		-	Refer to right table
19	Red/Green low bits	21	33		-	Red / Green Low Bits
1A	Blue/White low bits	35	53		-	Blue / White Low Bits
1B	Red x high bits	97	151	604	0.590	Red (x) = 10010111 (0.59)
1C	Red y high bits	59	89	358	0.350	Red (y) = 01011001 (0.35)
1D	Green x high bits	57	87	348	0.340	Green (x) = 01010111 (0.34)
1E	Green y high bits	8F	143	573	0.560	Green (y) = 10001111 (0.56)
1F	Blue x high bits	29	41	164	0.160	Blue (x) = 00101001 (0.16)
20	BLue y high bits	23	35	143	0.140	Blue (y) = 00100011 (0.14)
21	White x high bits	50	80	321	0.313	White (x) = 01010000 (0.313)
22	White y high bits	54	84	337	0.329	White (y) = 01010100 (0.329)
23	Established timing 1	00	0		-	Refer to right table
24	Established timing 2	00	0		-	
25	Established timing 3	00	0		-	
26	Standard timing #1	01	1			Not Used
27		01	1			
28	Standard timing #2	01	1			Not Used
29		01	1			
2A	Standard timing #3	01	1			Not Used
2B		01	1			
2C	Standard timing #4	01	1			Not Used
2D		01	1			
2E	Standard timing #5	01	1			Not Used
2F		01	1			
30	Standard timing #6	01	1			Not Used
31		01	1			
32	Standard timing #7	01	1			Not Used
33		01	1			
34	Standard timing #8	01	1			Not Used
35		01	1			
36	Detailed timing/monitor descriptor #1	C2	194		142.7	142.7328MHz Main clock
37		37	55			
38		80	128		1920	Hor Active = 1920
39		CC	204		204	Hor Blanking = 204
3A		70	112		-	4 bits of Hor. Active + 4 bits of Hor. Blanking
3B		38	56		1080	Ver Active = 1080
3C		28	40		40	Ver Blanking = 40
3D		40	64		-	4 bits of Ver. Active + 4 bits of Ver. Blanking
3E		6C	108		108	Hor Sync Offset = 108
3F		30	48		48	H Sync Pulse Width = 48
40		AA	170		10	V sync Offset = 10 line
41		00	0		10	V Sync Pulse width : 10 line
42		35	53		309.00	Horizontal Image Size = 309 mm (Low 8 bits)
43		AE	174		174.00	Vertical Image Size = 174 mm (Low 8 bits)
44		10	16		-	4 bits of Hor Image Size + 4 bits of Ver Image Size
45		00	0		0	Hor Border (pixels)
46		00	0		0	Vertical Border (Lines)
47		1A	26		-	Refer to right table

48	Detailed timing/monitor descriptor #2	2C	44		95.2	95.1552MHz Main clock
49		25	37			
4A		80	128		1920	Hor Active = 1920
4B		CC	204		204	Hor Blanking = 204
4C		70	112		-	4 bits of Hor. Active + 4 bits of Hor. Blanking
4D		38	56		1080	Ver Active = 1080
4E		28	40		40	Ver Blanking = 40
4F		40	64		-	4 bits of Ver. Active + 4 bits of Ver. Blanking
50		6C	108		108	Hor Sync Offset = 108
51		30	48		48	H Sync Pulse Width = 48
52		AA	170		10	V sync Offset = 10 line
53		00	0		10	V Sync Pulse width : 10 line
54		35	53		309.00	Horizontal Image Size = 309 mm (Low 8 bits)
55		AE	174		174.00	Vertical Image Size = 174 mm (Low 8 bits)
56		10	16		-	4 bits of Hor Image Size + 4 bits of Ver Image Size
57		00	0		0	Hor Border (pixels)
58		00	0		0	Vertical Border (Lines)
59		1A	26		-	Refer to right above table
5A	Detailed timing/monitor descriptor #3	00	0			Reserved
5B		00	0			
5C		00	0			
5D		00	0			
5E		00	0			
5F		00	0			
60		00	0			
61		00	0			
62		00	0			
63		00	0			
64		00	0			
65		00	0			
66		00	0			
67		00	0			
68		00	0			
69		00	0			
6A		00	0			
6B		00	0			
6C	Detailed timing/monitor descriptor #4	00	0			Detailed Timing Description #4
6D		00	0			Flag
6E		00	0			Reserved
6F		02	2			For brightness Table and Power consumption header
70		00	0			Flag
71		0D	13		-	PWM % [7:0] @ Step 0
72		36	54		-	PWM % [7:0] @ Step 5
73		FF	255			PWM % [7:0] @ step 10
74		0A	10		-	Nits [7:0] @ Step 0
75		3C	60		-	Nits [7:0] @ Step 5
76		96	150		-	Nits [7:0] @ Step 10
77		09	9		-	Panel Electronics Power @32x32 Chess Pattern = 390mW
78		0A	10		-	Backlight Power @60 nits = 423.529411764706mW
79		19	25		-	Backlight Power @Step 10 = 2000mW
7A		96	150		-	Nits @ 100% PWM Duty = 300nit
7B		00	0		-	
7C		00	0		-	
7D		00	0		-	
7E	Extension flag	01	1		1	
7F	Checksum	57	87	87	-	
80	DID Extension Header	70	112		112	DisplayID EDID Extension Block tag
81		20	32		32	DisplayID Version/Revsion = 2.0
82		79	121		121	Section Size (byte) = 121 bytes
83		02	2		2	Display Product Primary Use Case
84		00	0		0	Extension count
85	DID Block #1 Header	25	37		37	DID2.0 Data block tag[25h] = Dynamic Video Timing Range Limits
86		01	1		1	Block revision = Revision 1
87		09	9		9	Number of Payload Bytes in block= 9 Bytes
88	DID DATA Block #1	8C	140		142.7	Minimum Pixel Clock (Low bit, Range = 0.001Mhz (000000h) ~ 16,777.216Mhz (FFFFFFh))
89		2D	45			Minium Pixel Clock (Middle bit)
8A		02	2			Minium Pixel Clock (High bit)
8B		8C	140		142.7	Maximum Pixel Clock (Low bit, Range = 0.001Mhz (000000h) ~ 16,777.216Mhz (FFFFFFh))
8C		2D	45			Maximum Pixel Clock (Middle bit)
8D		02	2			Maximum Pixel Clock (High bit)
8E		28	40		40	Min. Vertical Rate : 60 Hz (Range : 0Hz (00h) ~ 255Hz (FFh)
8F		3C	60		60	Max. Vertical Rate : 120 Hz (Range : 0Hz (000h) ~ 255Hz (FFh))
90		80	128		128	Seamless Dynamic Video Timing Support : Seamless Dynamic Video Timing change shall be supported with a fixed horizontal pixel rate and dynamic vertical blanking.

91	DID Block #2 Header	**81**	129		129	DID2.0 Data block tag[81h] = CTA DisplayID
92		**00**	0		0	Block revision = Revision 0
93		**10**	16		16	Number of Payload Bytes in block= 16 Bytes
94	DID DATA Block #2 AMD VSDB	**6F**	111		111	CTA Block1 Tag Code and Block1 Length = Vendor Specific Data Block(03h), Size(byte) = 15 bytes
95		**1A**	26		26	AMD IEEE OUI value (0x00001A)
96		**00**	0			Hex. LSB first)
97		**00**	0			Hex. LSB first)
98		**03**	3		3	AMD VSDB Version 3
99		**01**	1		1	Bit 0 = 1 FreeSync supported by panel
9A		**28**	40		40	Min Refresh Rate
9B		**3C**	60		60	Max Refresh Rate
9C		**00**	0		0	Freesync MCCS VCP Code
9D		**00**	0		0	Support WCG and HDR features : Gamma 2.2 EOTF Not Supported ， PQ EOTF Not Supported
9E		**53**	83		300	Max Luminance 1 (for HDR) = 300nit
9F		**4A**	74		0.25	Max Luminance 2 (for HDR) = 0.25nit
A0		**53**	83		300	Max Luminance 2 (for HDR) = 300nit
A1		**4A**	74		0.25	Max Luminance 2 (for HDR) = 0.25nit
A2		**3C**	60		60	Bits 7:0 -Freesync Maximum Refresh Rate (MSB)
A3		**00**	0			Bits 9:8 - MSB FreeSync Maximum refresh rate [Hz]
A4		**00**	0		0	Maximum Fast Transport Input Pixel Rate [kHz] - bits 7:0
A5		**00**	0		0	Maximum Fast Transport Input Pixel Rate [kHz] - bits 15:8
A6		**00**	0		0	Maximum Fast Transport Input Pixel Rate [kHz] - bits 23:16
A7	DID Block #3 Header	**00**	0		0	Reseved
A8		**00**	0		0	Reseved
A9		**00**	0		0	Reseved
AA	DID DATA Detailed Timing Data Block #3	**00**	0		0	Reseved
AB		**00**	0		0	Reseved
AC		**00**	0		0	Reseved
AD		**00**	0		0	Reseved
AE		**00**	0		0	Reseved
AF		**00**	0		0	Reseved
B0		**00**	0		0	Reseved
B1		**00**	0		0	Reseved
B2		**00**	0		0	Reseved
B3		**00**	0		0	Reseved
B4		**00**	0		0	Reseved
B5		**00**	0		0	Reseved
B6		**00**	0		0	Reseved
B7		**00**	0		0	Reseved
B8		**00**	0		0	Reseved
B9		**00**	0		0	Reseved
BA		**00**	0		0	Reseved
BB		**00**	0		0	Reseved
BC		**00**	0		0	Reseved
BD		**00**	0		0	Reseved
BE		**00**	0		0	Reseved
BF		**00**	0		0	Reseved
C0		**00**	0		0	Reseved
C1		**00**	0		0	Reseved
C2		**00**	0		0	Reseved
C3		**00**	0		0	Reseved
C4		**00**	0		0	Reseved
C5		**00**	0		0	Reseved
C6		**00**	0		0	Reseved
C7		**00**	0		0	Reseved
C8		**00**	0		0	Reseved
C9		**00**	0		0	Reseved
CA		**00**	0		0	Reseved
CB		**00**	0		0	Reseved
CC		**00**	0		0	Reseved
CD		**00**	0		0	Reseved
CE		**00**	0		0	Reseved
CF		**00**	0		0	Reseved
D0		**00**	0		0	Reseved
D1		**00**	0		0	Reseved
D2		**00**	0		0	Reseved
D3		**00**	0		0	Reseved
D4		**00**	0		0	Reseved
D5		**00**	0		0	Reseved
D6		**00**	0		0	Reseved
D7		**00**	0		0	Reseved
D8		**00**	0		0	Reseved
D9		**00**	0		0	Reseved
DA		**00**	0		0	Reseved
DB		**00**	0		0	Reseved
DC		**00**	0		0	Reseved
DD		**00**	0		0	Reseved

DE		**00**	0		0	Reseved
DF		**00**	0		0	Reseved
E0		**00**	0		0	Reseved
E1		**00**	0		0	Reseved
E2		**00**	0		0	Reseved
E3		**00**	0		0	Reseved
E4		**00**	0		0	Reseved
E5		**00**	0		0	Reseved
E6		**00**	0		0	Reseved
E7		**00**	0		0	Reseved
E8		**00**	0		0	Reseved
E9		**00**	0		0	Reseved
EA		**00**	0		0	Reseved
EB		**00**	0		0	Reseved
EC		**00**	0		0	Reseved
ED		**00**	0		0	Reseved
EE		**00**	0		0	Reseved
EF		**00**	0		0	Reseved
F0		**00**	0		0	Reseved
F1		**00**	0		0	Reseved
F2		**00**	0		0	Reseved
F3		**00**	0		0	Reseved
F4		**00**	0		0	Reseved
F5		**00**	0		0	Reseved
F6		**00**	0		0	Reseved
F7		**00**	0		0	Reseved
F8		**00**	0		0	Reseved
F9		**00**	0		0	Reseved
FA		**00**	0		0	Reseved
FB		**00**	0		0	Reseved
FC		**00**	0		0	Reseved
FD		**00**	0		0	Reseved
FE		**E4**	228			DisplayID section checksum (81h~FDh)
FF		**90**	144			Extended block checksum (00h~FEh)

17.0 GENERAL PRECAUTIONS

17.1 HANDLING

(1) When the module is assembled, It should be attached to the system firmly using every mounting holes. Be careful not to twist or bend the modules.

(2) Refrain from strong mechanical shock or any force to the module. Otherwise, it may cause improper operation or damage to the module.

(3) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use Ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth .In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static , it may cause damage to the module.

(9) Use fingerstalls with soft gloves to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Do not pull or fold the LED FPC.

(l2) Do not touch any component which is located on the back side.

(13) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(14) Pins of connector shall not be touched directly with bare hands.

17.2 STORAGE

(1) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃ and relative humidity of less than 70%.

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the stor e.

17.3 OPERATION

(1) Do not connect, disconnect the module in the " Power On" condition.

(2) Power supply should always be turned on/off by following item 8.0 " Power on/off sequence ".

(3) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

(4) The standard limited warranty is only applicable when the module is used for general notebook applications. If used for purposes other than as specified, BOE is not to be held reliable for the defective operations. It is strongly recommended to contact BOE to find out fitness for a particular purpose.

17.4 OTHERS

(1) Avoid condensation of water. It may result in improper operation or disconnection of electrode.

(2) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation, Variation in part contents and environmental temperature, so on) Otherwise the module may be damaged.

(3) If the module displays the same pattern continuously for a long period of time, it can be the situation when The " image sticks" to the screen.

(4) This module has its circuitry PCB's on the rear or bottom side and should be handled carefully to avoid being stressed.

Appendix A

The Measurement Methods for the Dimensions of Module

Caliper:
a. Length of Outline
b. Width of Outline (Without/With PCB)
c. Thickness of Outline (Without/ With PCB)

Coordinate Measuring Machine:
CF Polarizer Size
Active Area Size
Active Area to Outline (Without Tape Wrinkle or Bulged)
Active Area to CF Polarizer
The Distance of Bracket Holes
P-Cover to Outline (Without Tape Wrinkle or Bulged)
Length of P-Cover
Connector Pin 1 to Outline (Without Tape Wrinkle or Bulged)

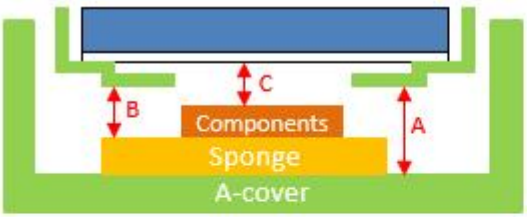
Height Gauge: The Different Height of Root and Top on the Bracket
(Need to Calculate From Bracket Angle Spec.)

Feeler Gauge: The Warpage Spec. of Module

Notes:
Except the Critical Dimensions as Above, Other Dimensions are Measured by Coordinate Measuring Machine If Necessary.

Appendix B

LCM to A-Cover / sponges Z-gap

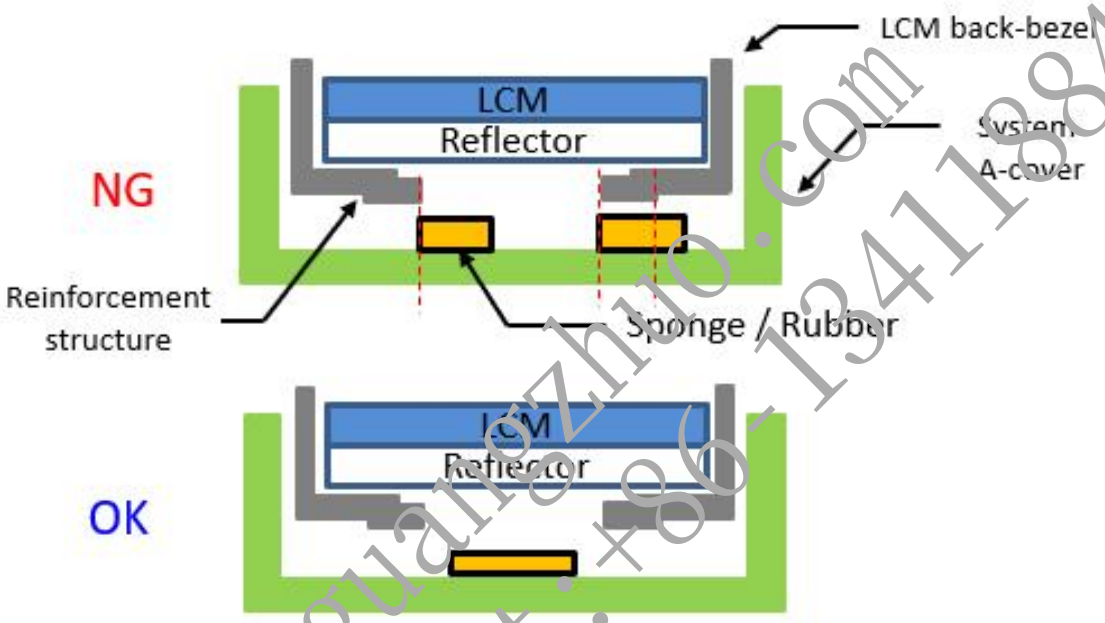


	Plastic Cover	Metal Cover
A	≥ 1.0mm	≥ 0.8mm
B	≥ 0mm	
C	> 0.5mm	

Purpose	The reflector area is very sensitive, BOE would suggest that design enough z-gap to decrease the risk of water ripple, white spots and other abnormal display

Appendix B

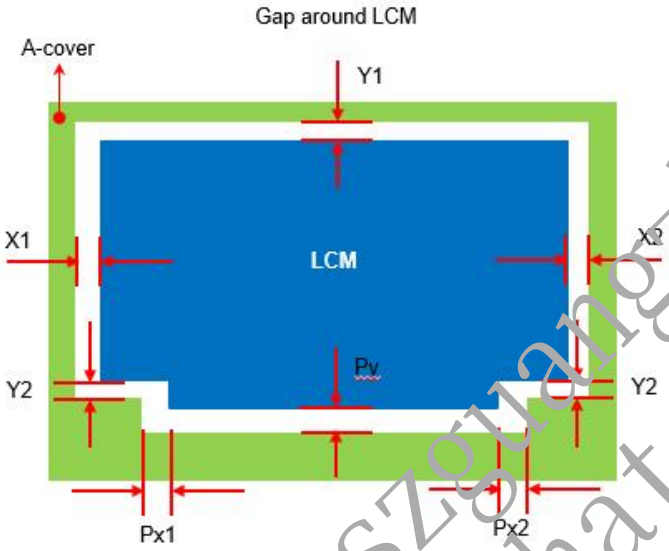
LCM to A-Cover / sponges z-gap



Purpose	If attach sponges or rubbers which correspond to white reflector area, it may cause white spot, pooling or other relative issues. BOE would suggest that attach wide range sponges / rubbers which can cover the LCM back-bezel opening

Appendix B

LCM to side wall / protrusions

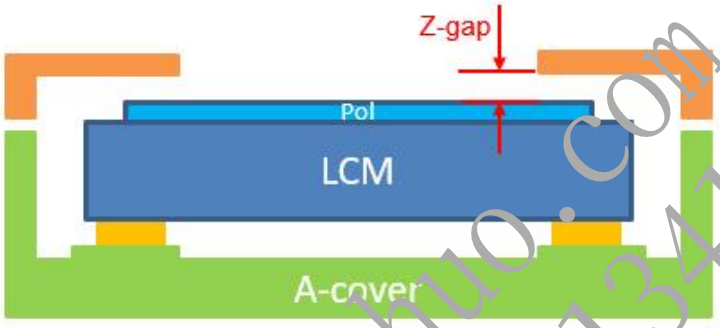


	Normal border (screws)	Narrow border (fix by tapes)
X1 / X2	Min: 0.45mm	Min: 0.35mm
Y1 / Y2	Min: 0.45mm	Min: 0.35mm
Px1 / Px2	Min: 0.55mm	
Py		

Purpose	BOE would suggest that design enough gap around LCM to prevent shock test failure, or interference, cell crack, abnormal display…etc. in the reliability test

Appendix B

LCM to B-cover z-gap

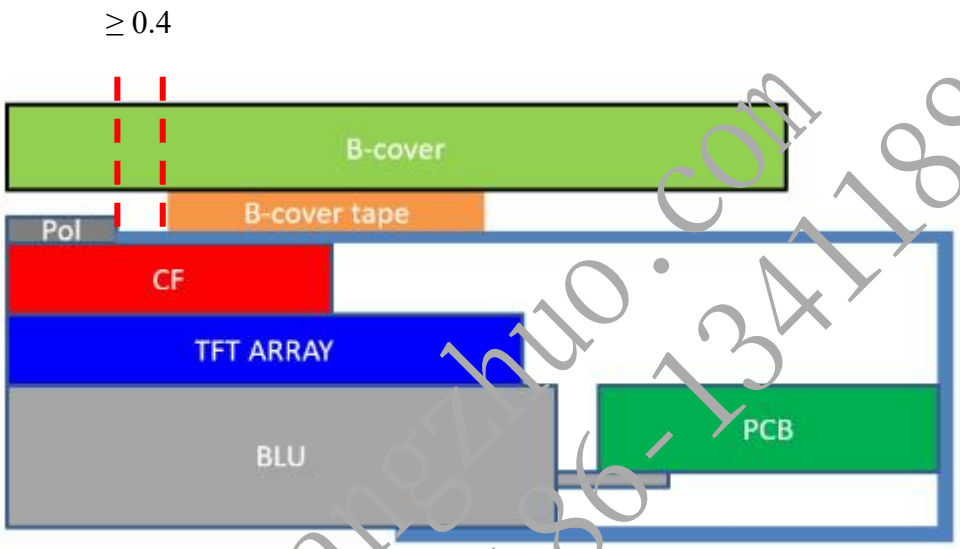


Bezel Tape	Z-Gap
Without	0.15 ~ 0.25mm
With	0.15 ~ 0.20mm

Purpose	Too less z-gap between system B-cover and LCM top pol has high risk that may cause cell crack, pooling, light leakage and other issues

Appendix B

B-cover tape to top pol edge

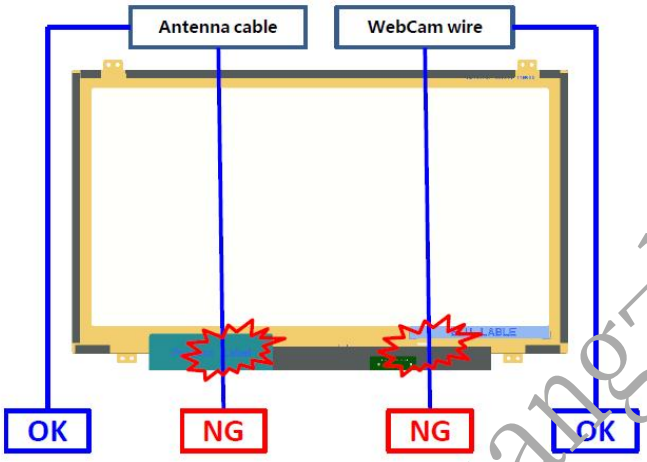


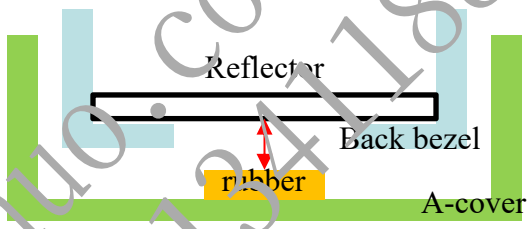
If attach b-cover and LCM with tapes,
Please let tapes to be located out of top pol edges 0.4mm away on 4 sides

Purpose	To avoid the B-cover tape override top pol then cause pooling or light leakage issue

Appendix B

Antenna Cable & Webcam wire



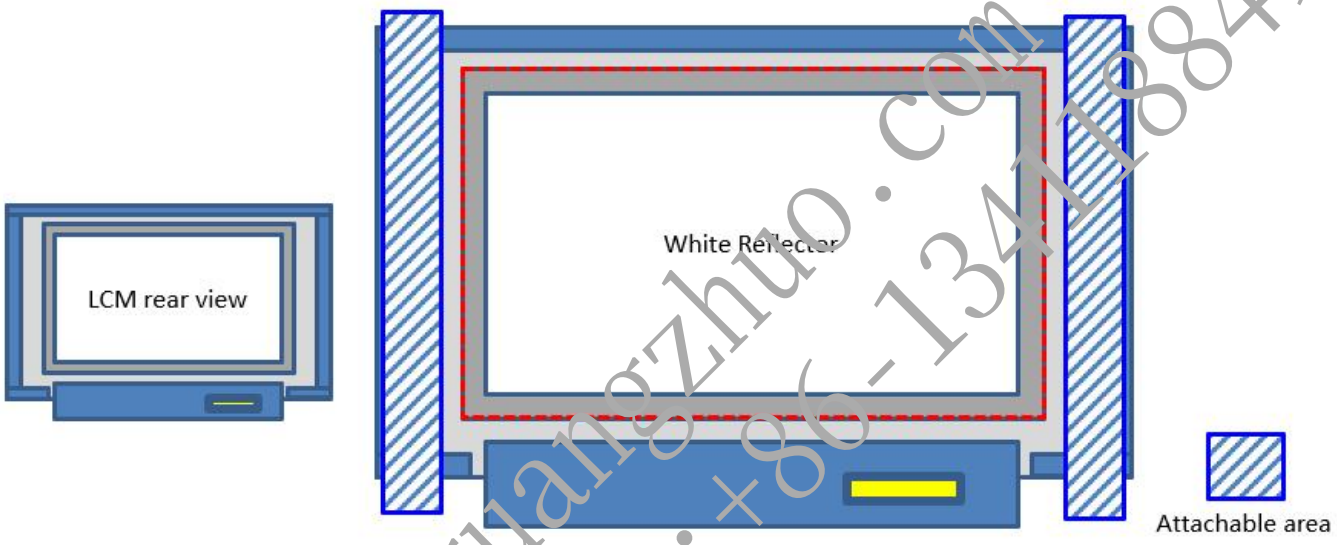


If sponge within the reflector area is necessary, we suggest that the gap between reflector and sponge is more than 0.5mm

Purpose	1. BOE would suggest that do not set Antenna or WebCam cable / wire go behind LCM to avoid backpack test, hinge test ,twist test or pogo test with abnormal display 2. If the cable / wire is necessary to go behind LCM, please make a groove with rounds or chamfers to protect the cable / wire, or attach with higher sponges / rubbers adjacent to the cable / wire route 3. Suggest that attach the cable / wire with tapes to A-cover 4. Do not attach anything with LCM reflector area. If attach cable / wire with LCM reflector area, it may cause pooling, white spot, light leakage and other related issues

Appendix B

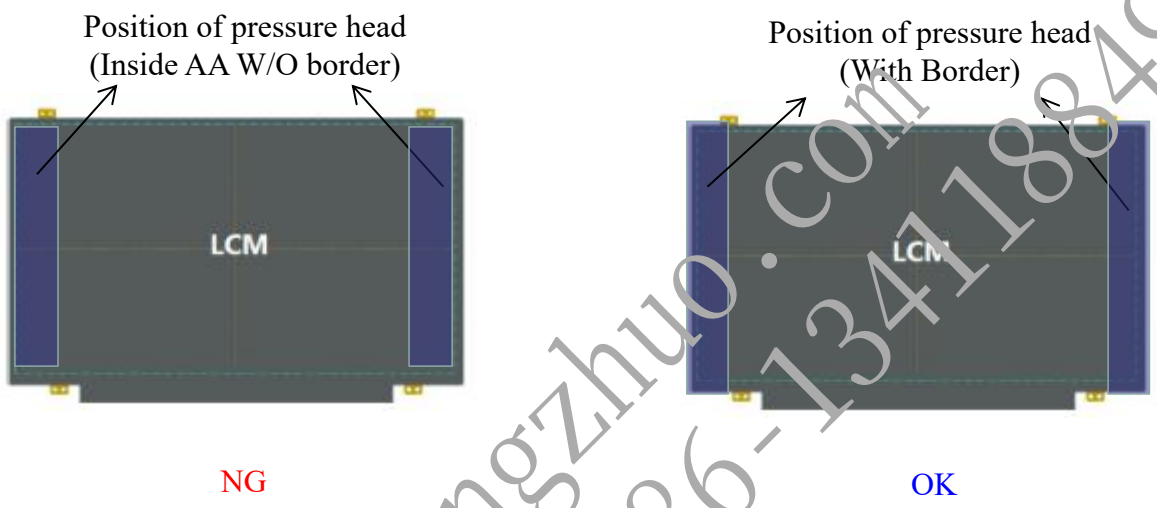
LCM paste area



Purpose	If use the stretch remove tapes to fix LCM with A-cover, please set the stretch remove tapes correspond to the LCM back-bezel and do not let the tapes override the back-bezel's level step of opening

Appendix B

LCM pressable area



NG OK

Purpose	1. If LCM is fixed on A-cover by using the press jig during assembling. 2. To avoid panel broken the design of pressure head of press jig can not only pin on cell panel. The pressure head needs to pin on the LCM frame, which the LCM frame can share the pressure of the pressing head.

Appendix B

Wire setting

Purpose	Wires should be placed between protrusions/side wall and A-cover. If place the wires between LCM and Protrusions/side wall, it may interfere with LCM when assembling, or even cause LCM broken in reliability test.

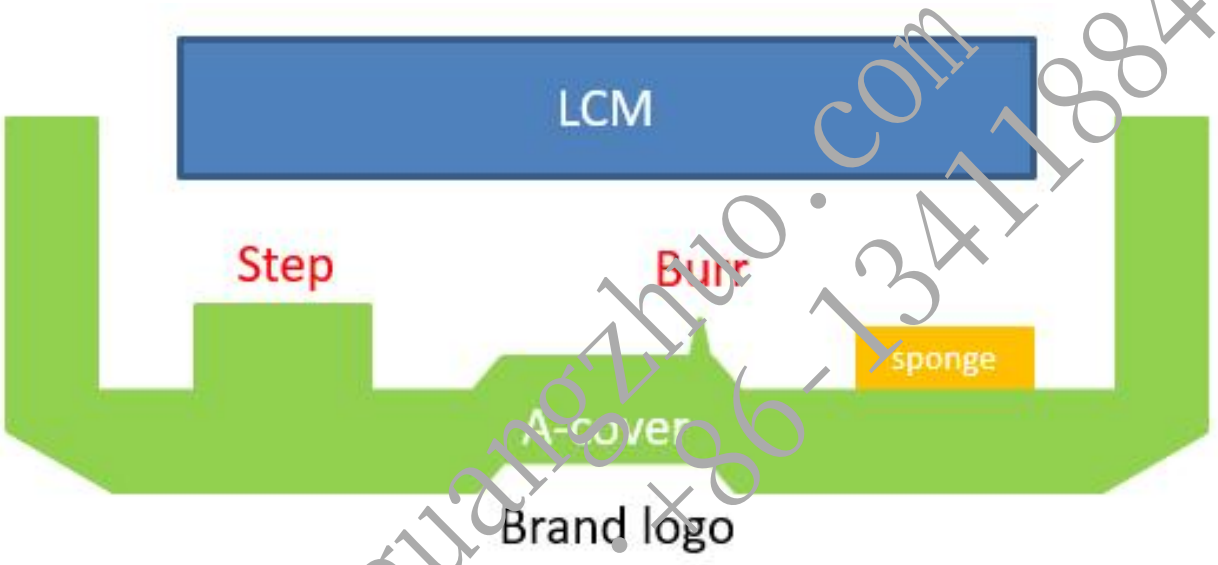
Appendix B

A-cover strength

Purpose	1. BOE would recommend that structural Rib/Bracket height is higher than LCM, in order to avoiding pressures to LCM. 2. The L-shape Bracket is recommended.

Appendix B

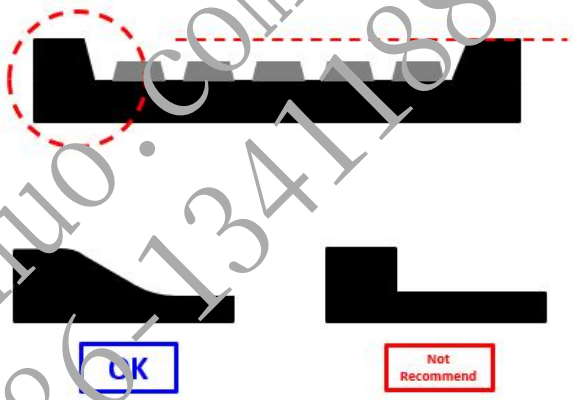
System A-cover Inner Surface



Purpose	There should not exist any burr, segment gap or protrusions beside Logo, which may cause White Spot or Glass Broken by stress concentration.

Appendix B

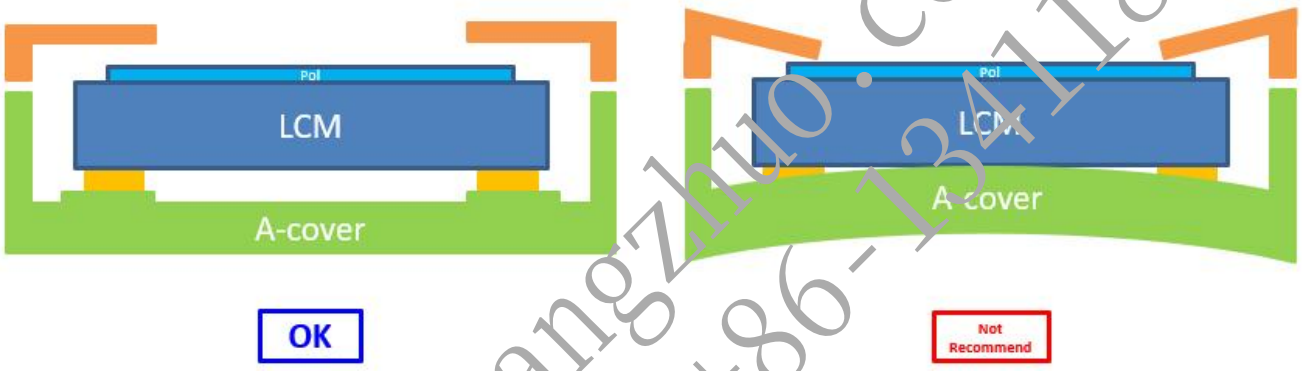
Keyboard area & Mouse pad



Purpose	The transition surface between keyboard and mouse pad should be smooth and without vertical steps\ too large level steps

Appendix B

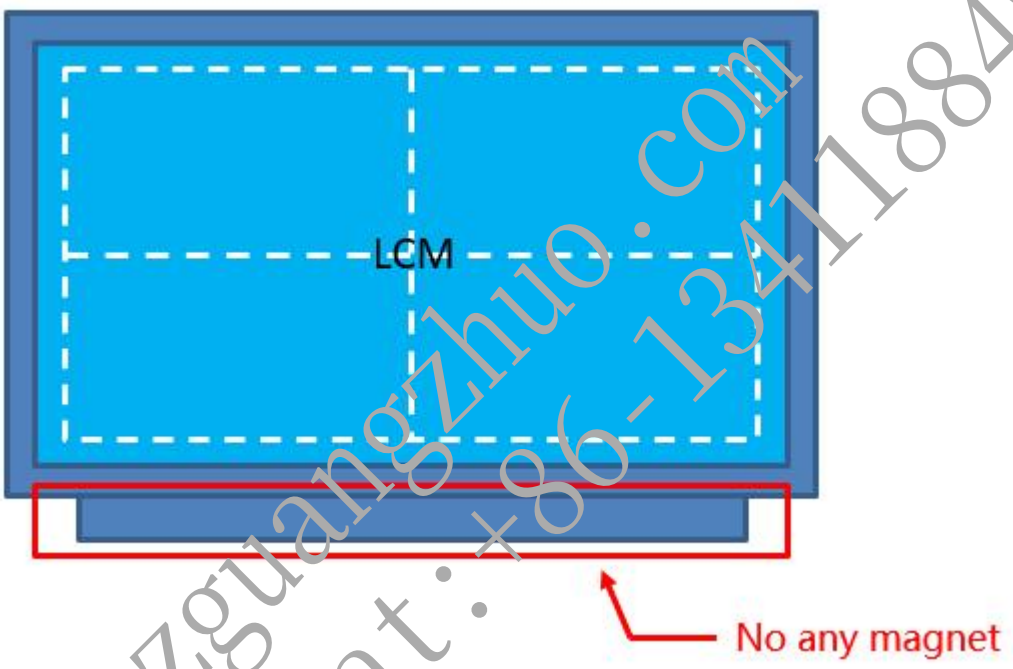
System cover reliability



Purpose	1. No interference between system and LCM in assembly process except compressible grounding gaskets 2. The permanent deformation which caused by Reliability test is not allowed to contact LCM

Appendix B

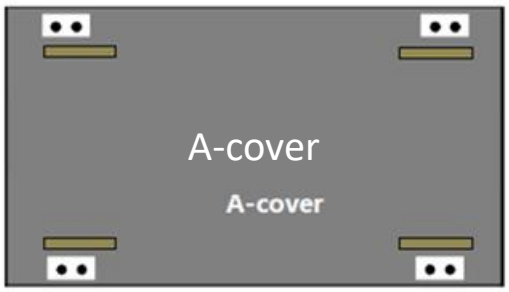
A/B-cover near LCD PCBA

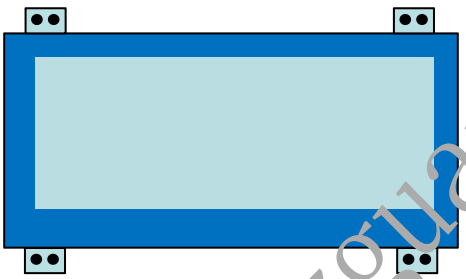


Purpose	There should not been any magnet object close to LCM PCBA, it may cause physical or electricity noise issue

Appendix B

A-cover add sponges on Boss side wall

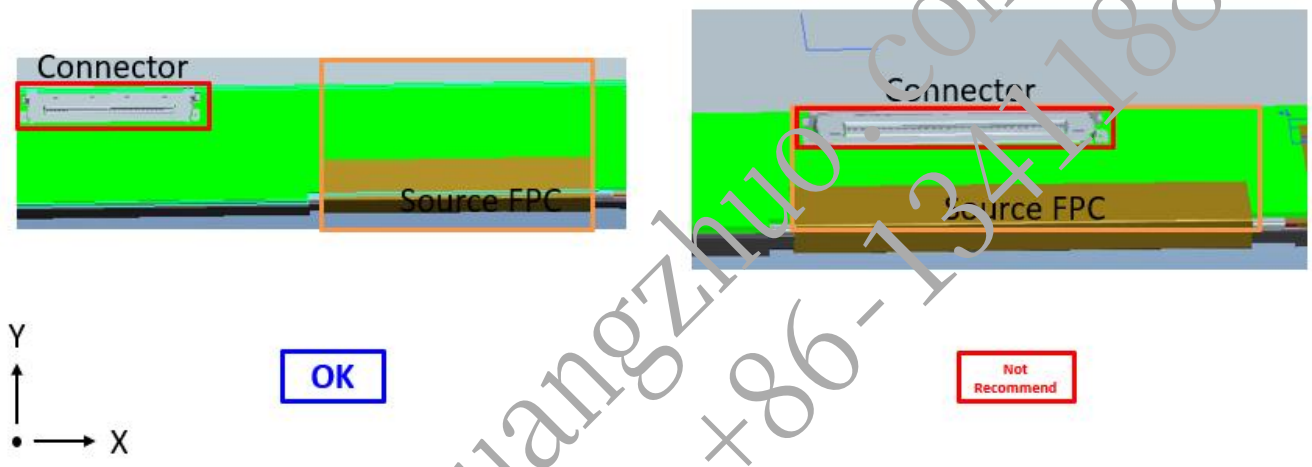




Purpose	BOE would suggest to attach Sponges to the side-wall of the Boss column of A-cover to reduce the risk of panel broken in assembling process.

Appendix B

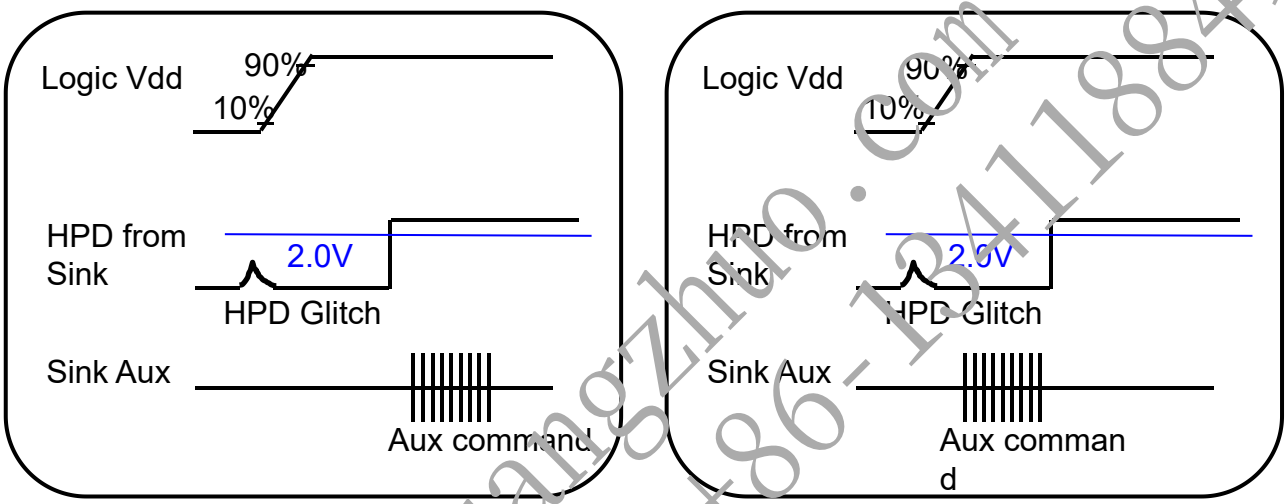
LCM to A-Cover / sponges z-gap



Purpose	Bent type product: The System Connector should not overlap with LCM FPC in X-direction, it may cause FPC lead broken during system connector plug and un-plug process (Panel FPC Bonding location is related to Mask and can not be changed easily)

Appendix C

HPD Signal recognition



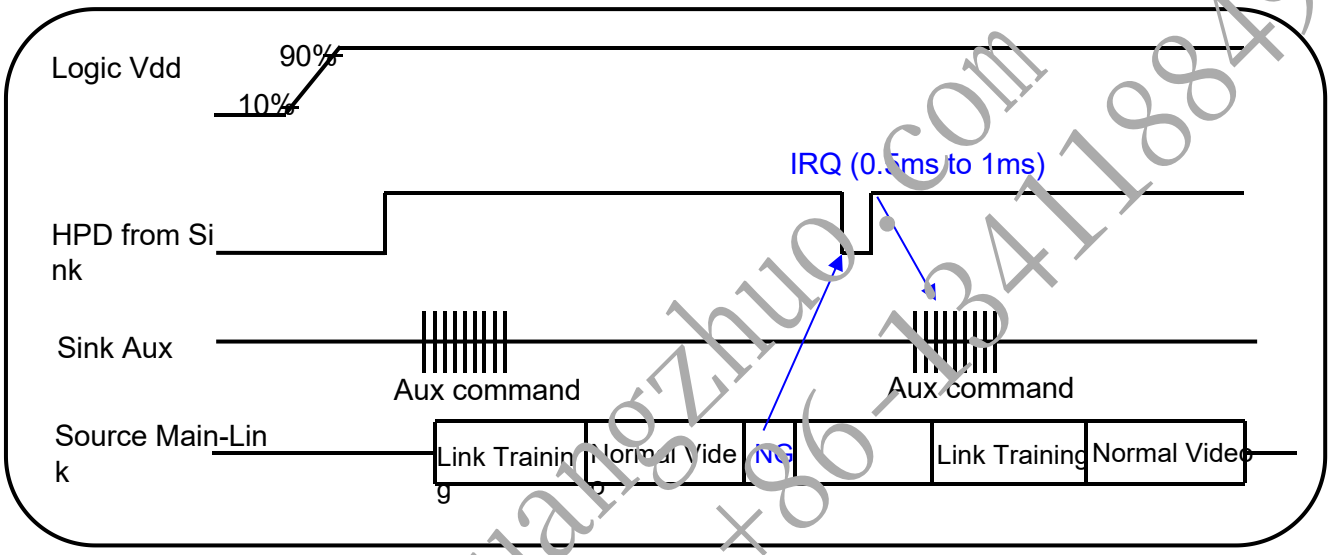
Normal Signal (Ignore HPD Glitch)

Abnormal Signal

Purpose	When HPD glitch voltage less than 2.0(V), system signal can't output AUX command data.

Appendix C

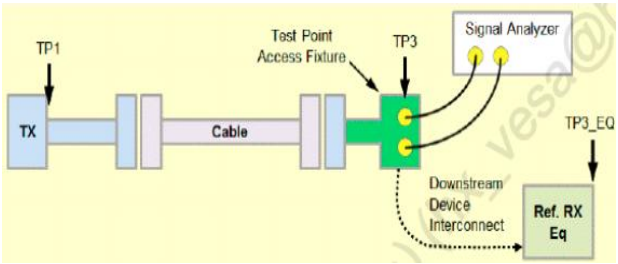
HPD Signal Definition IRQ (Interrupt Request)



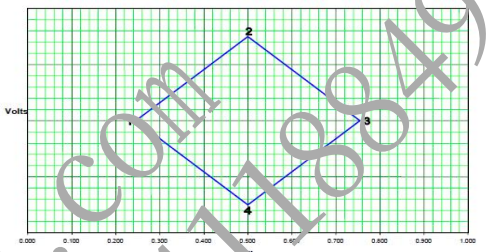
Purpose	When HPD signal low than 0.5ms to 1ms, the source device should check sink status field from the DPCD and take link training again.

Appendix C

Main link eye diagram of TP3



Measured TP3 on LCM connector.



Downstream Device Mask at TP3

	UI	Voltage
1	0.246	0
2	0.5	0.075
3	0.755	0
4	0.5	-0.075

Eye for TP3 at HBR

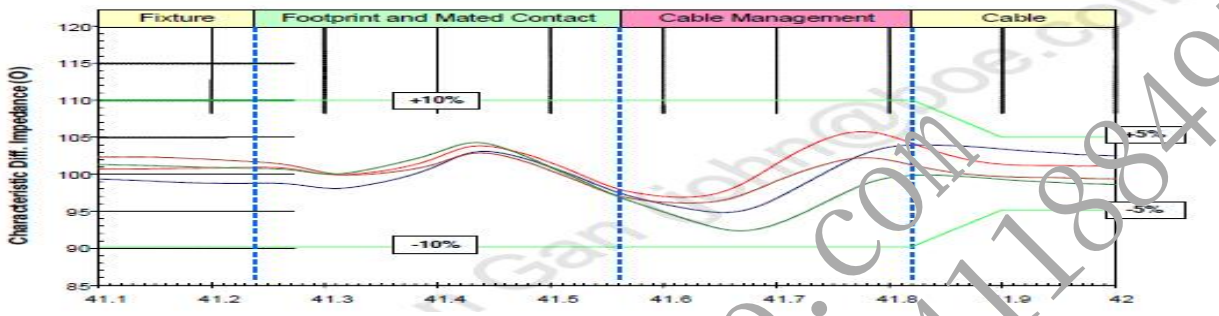
	UI	Voltage
1	0.375	0
2	0.5	0.023
3	0.625	0
4	0.5	-0.023

Eye for TP3 at RBR

Purpose	1. Main Link EYE Diagram should meet TP3 point of VESA. 2. The measure method is through access fixture.

Appendix C

Impedance Profile through a DP Connector



Differential Impedance Profile Measurement Data Example

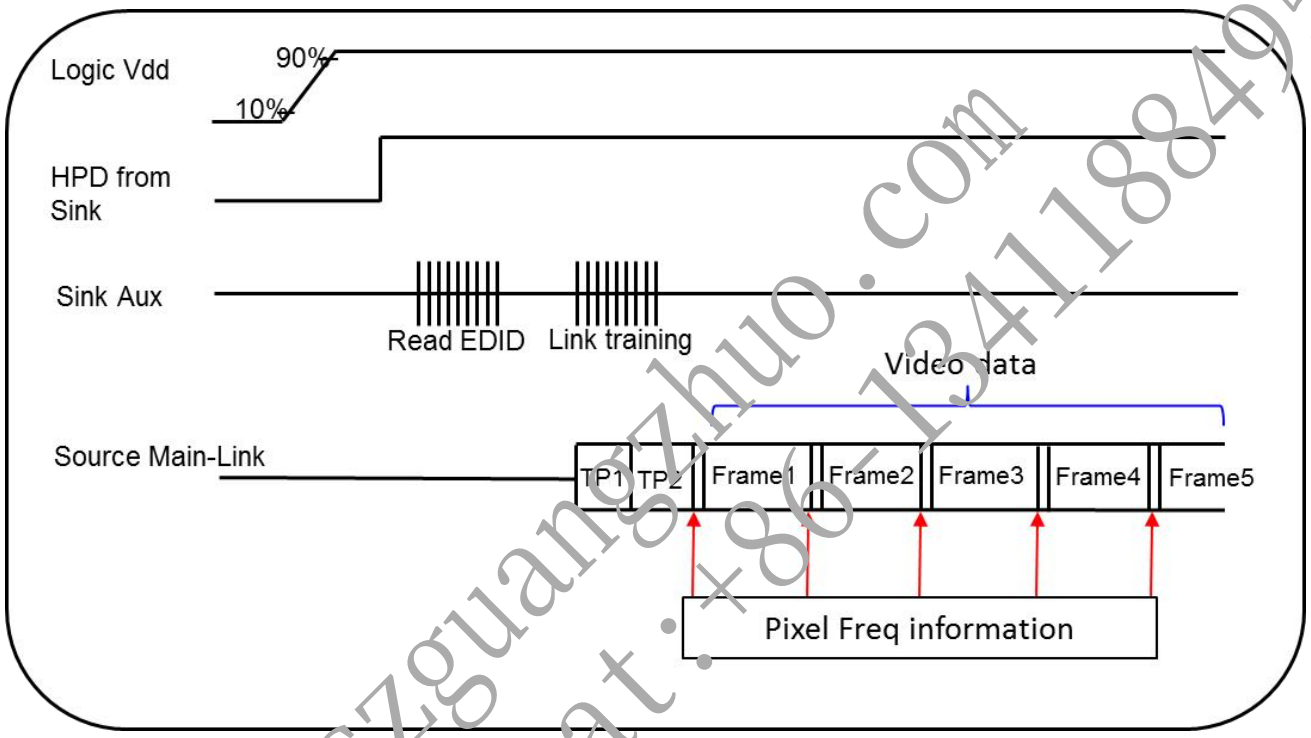
Segment	Differential Impedance Value	Maximum Tolerance
Fixture	100Ω/VESA	±10%
Connector	100Ω/VESA	±10%
Wire management	100Ω/VESA	±10%
Cable	100Ω/VESA	±5%

Impedance Profile Values for Cable Assembly

Purpose	Cable Impedance Profile 100ohm for Cable Assembly

Appendix C

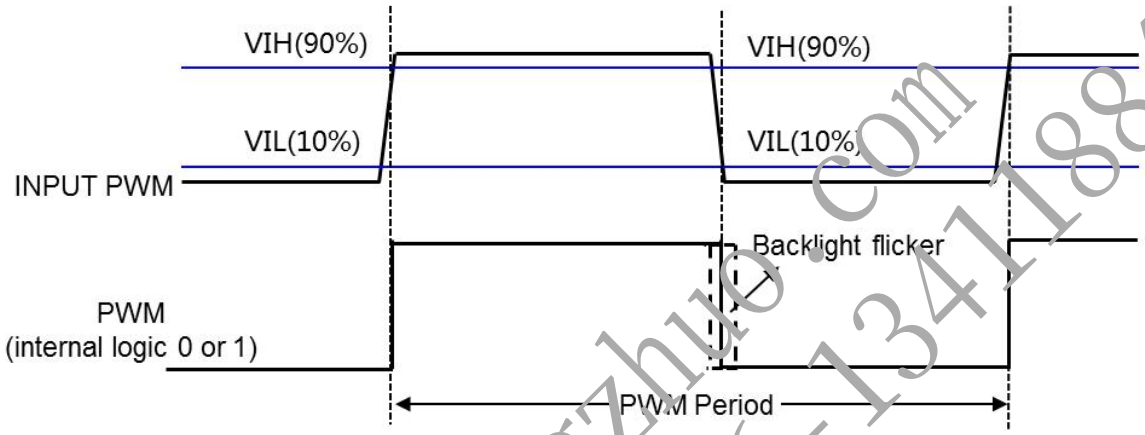
Main Link Pixel Freq information value of MSA data



Purpose	1. It need to fix pixel freq information value of MSA data output to prevent the initial abnormal pixel freq information value from incoming after power on. 2. BOE can read DPCD to check this value. Ex: BIOS is 1.62G , but into windows is 2.7G.

Appendix C

System Input PWM Rising/Falling time



Example:

Freq	Cycle Time	PWM Rising Time	PWM Falling Time
200Hz	5ms	≤1us	≤1us
1KHz	1ms	≤200ns	≤200ns

Purpose	1. LED driver need to calculate the duty cycle of input PWM signal. 2. To avoid backlight flicker visible on LCD, system input PWM suggest : PWM rising ≤ 200ppm*cycle time ; PWM falling ≤ 200ppm*cycle time.