

TITLE : NE156FHM-NX6 V18.0

Customer: ASUS

Product Specification

Rev. 0

BOE Optoelectronics Technology Co., Ltd

SPEC. NUMBER

PRODUCT GROUP

Rev.

ISSUE DATE

PAGE

S8-64-8E-072

TFT-LCD

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2023.06.26

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1.0 GENERAL DESCRIPTION

1.1 Introduction

NE156FHM-NX6 V18.0 is a color active matrix TFT LCD module using Oxide TFT's (Thin Film Transistors) as an active switching devices. This module has a 15.6 inch diagonally measured active area with FHD resolutions (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical Stripe and this module can display 16.7M colors.In this TFT-LCD panel, color filters for excellent color performance is incorporated to realize brighter and clearer pictures, making this Module optimum for use in multi-media applications. All input signals are eDP 1.3 interface compatible.

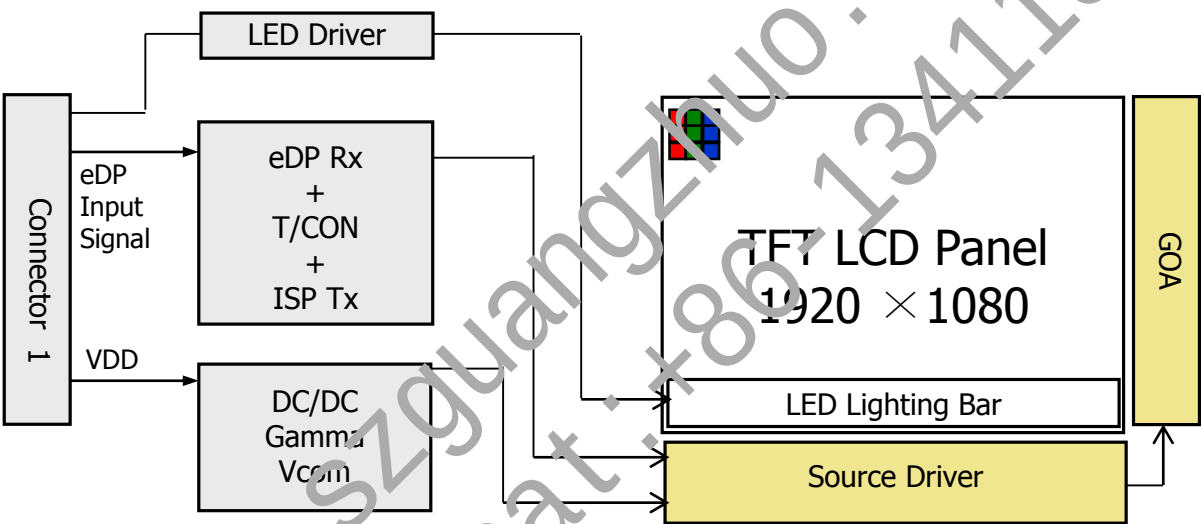


Figure 1. Drive Architecture

1.2 Features

- Frame rate support range: 1~4Hz;
- 4lane eDP1.3 Interface with 2.7Gbps Link Rates
- 8-bit color depth, display 16.7M colors
- LED driving mode is DC driving mode
- Data enable signal mode
- Green Product (RoHS & Halogen free product)
- On board LED Driving circuit
- Low driving voltage and low power consumption
- On board EDID chip
- DPCD Version 1.2 Function :
- PSR1/SDRRS/Free sync/G-sync/BIST

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1.3 Application

- Notebook PC (Wide type)

1.4 General Specification

The followings are general specifications at the model NE156FHM-NX6 V18.0. (listed in Table 1)

<Table 1. General Specifications>

Parameter	Specification	Unit	Remarks
Active area	344.16 (H) × 193.59 (V)	mm	
Number of pixels	1920 (H) × 1080 (V)	pixels	
Pixel pitch	179.25(H) × 179.25(V)	um	
Pixel arrangement	RGB Vertical stripe		
Display colors	16.7M(8Bit)		
Color gamut	sRGB 100% (typ.), RGB 95%(min.)		
Display mode	Normally black		
Dimensional outline	350.66 ± 0.3(H)*205.25 ± 0.3(V)(W/O PCB)*3.2(Max) 350.66 ± 0.3(H)*214.75 ± 0.5(V) (W/PCB)*3.2(Max)	mm	
Weight	365(max)	g	
Surface treatment	Anti-Glare		
Surface hardness	3H		
Back-light	Bottom edge side, 1-LED lighting bar type		Note 1
Power consumption	P _D : 1.35(Max.) @144Hz	W	@Mosaic
	P _{BL} : 3.85 (Max.)	W	@VLED= 12V
	P _{Total} : 5.2(Max.)	W	@Mosaic

Notes : 1. LED Lighting Bar (45*LED Array)

2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Absolute Maximum Ratings>

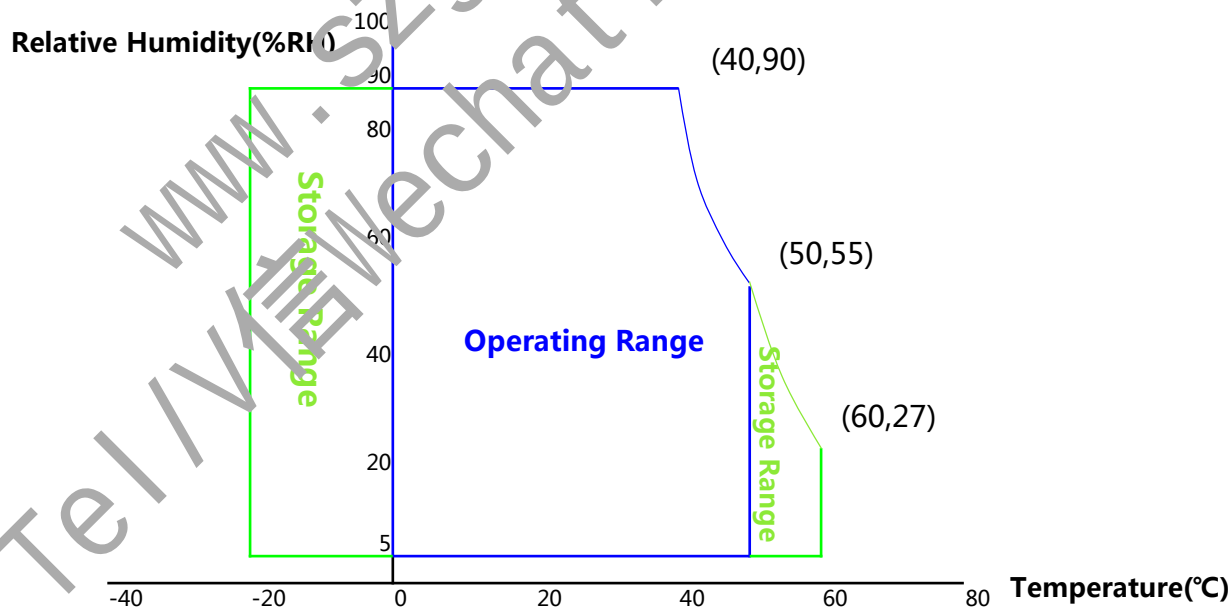
Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-0.3	4.0	V	Note 1
eDP input Voltage	V_{eDP}	0	2.0	V	
Logic Supply Voltage	V_{IN}	$V_{SS}-0.3$	$V_{DD}+0.3$	V	
Operating Temperature	T_{OP}	0	+50	°C	Note 2
Storage Temperature	T_{ST}	-20	+60	°C	

Notes :

1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.

2. Temperature and relative humidity range are shown in the figure below.

95 % RH Max. (40 °C ≥ Ta) Maximum wet - bulb temperature at 39 °C or less. (Ta > 40 °C) No condensation.



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3.0 ELECTRICAL SPECIFICATIONS							
3.1 Electrical Specifications							
< Table 3. Electrical specifications >						[Ta =25±2 °C]	
Parameter			Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage		V _{DD}	3.0	3.3	3.6	V	Note 1
Permissible Input Ripple Voltage		V _{RF}	-10% VDD	-	+10% VDD	V	Note 2
BIST Control Level		High Level	1.35	-	3.3	V	@V _{DDIO} =1.8
		Low Level	0	-	0.36	V	
Power Supply Inrush Current		Inrush	-	-	2	A	
Power Supply Current	Mosaic	I _{DD}	-	272	409	mA	Note 1
	R/G/B		-	272	409	mA	
	Heavy Pattern		-	424	470	mA	Note 1 Only for reference
Power Consumption	Mosaic	P _M	-	0.9	1.35	W	Note 1
	R/G/B	P _{P/Color}	-	0.9	1.35	W	
	Heavy Pattern	Ph	-	1.4	1.55	W	Note 1 Only for reference
	BLU	P _{BL}	-	-	3.85	W	Note 3
	Total	P _{Total}	-	-	5.2	W	@Mosaic
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3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

Notes :

1. The supply voltage is measured and specified at the interface connector of LCM.

The current draw and power consumption specified is for 3.3V at 25 °C.

- a) Mosaic pattern 8*8
 - b) R/G/B patterns
 - c) Heavy pattern(maximum logic power consumption) : H 1line
- The pattern and Power Consumption is shown for reference only

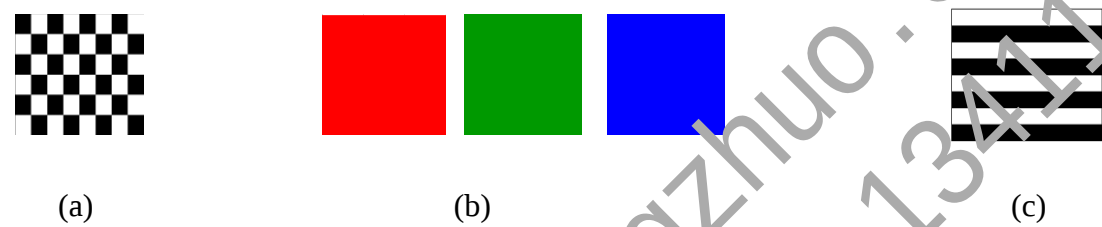


Figure 3. Power Measure Patterns

2. Calculated value for reference ($V_{LED} \times I_{LED}$) , The power consumption with LED Driver are under the $V_{LED} = 12.0V$, 25°C, PWM Duty 100% .

3. Measure condition (Figure 4)

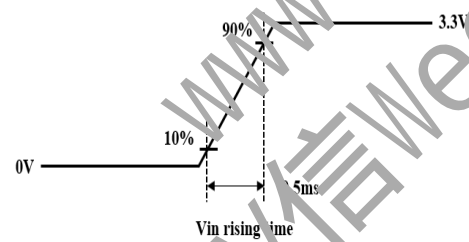


Figure 4. Inrush Measure Condition

4. Input voltage range:3.0~3.6V.Test condition: Oscilloscope bandwidth 20MHz, AC coupling

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3.2 Back-Light Unit

< Table 4. LED Driving guideline specifications >

[Ta =25±2 °C]

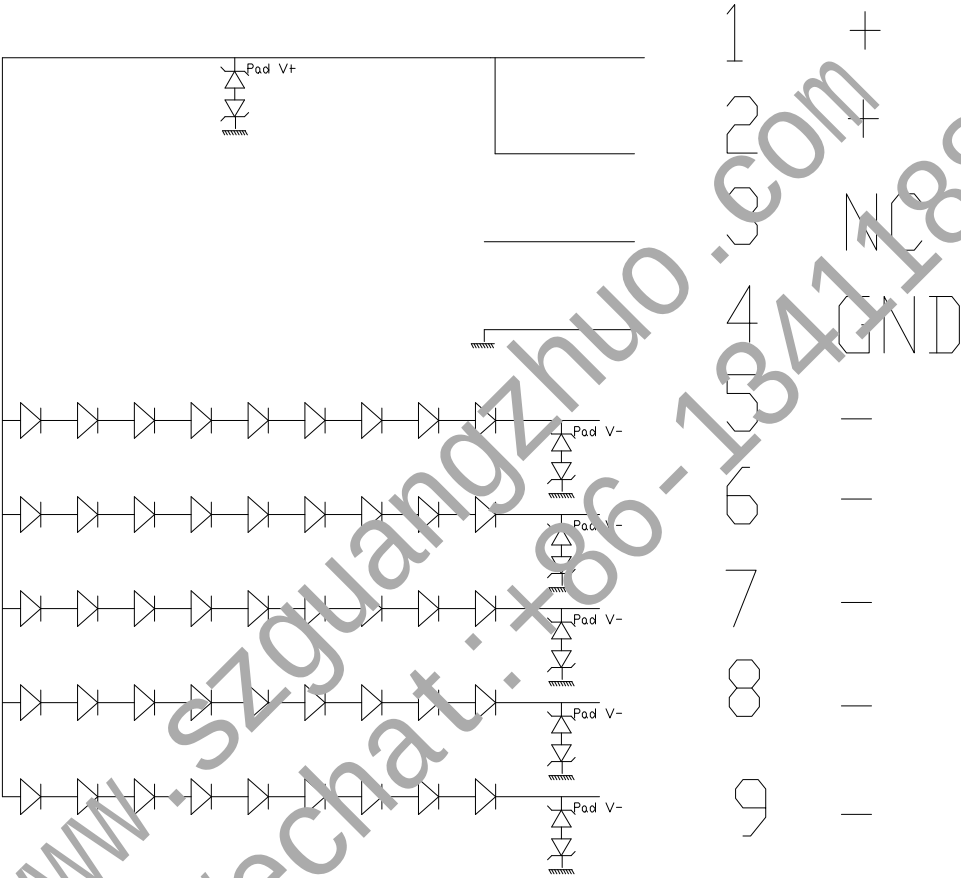
Parameter		Min.	Typ.	Max.	Unit	Remarks
LED Forward Voltage		V _F	-	-	2.9	V
LED Forward Current		I _F	-	20	-	mA
LED Power Consumption		P _{LED}	-	-	3.85	W
LED Life-Time		N/A	15,000	-	-	Hour
Power supply voltage for LED Driver		V _{LED}	5	12	21	V
EN Control Level	Backlight on	V _{BL_EN}	1.2	-	3.6	V
	Backlight off		0	-	0.5	V
PWM Control Level	PWM High Level	V _{BL_PWM}	1.35	-	3.3	V
	PWM Low Level		0	-	0.36	V
PWM Control Frequency		F _{PW}	200	-	2,000	Hz
Duty Ratio			5	-	100	%

Notes :

1. Power supply voltage 12V for LED driver.
Calculator value for reference IF × VF × 45 /driver efficiency = PLED
2. The LED life-time define as the estimated time to 50% degradation of initial luminous.

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3.3 LED Structure



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3.3 Pin assignment for LED Bar

Connector : (STM) MSK24036P9

< Table5. Pin assignment for LED Bar >

Pin No	Symbol	Description	Remarks
1	VLED	LED Anode Power Supply	
2	VLED	LED Anode Power Supply	
3	NC	NC	
4	GND	GND	
5	LED5	LED Cathode Power Supply	
6	LED4	LED Cathode Power Supply	
7	LED3	LED Cathode Power Supply	
8	LED2	LED Cathode Power Supply	
9	LED1	LED Cathode Power Supply	

4.0 OPTICAL SPECIFICATION

4.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = $25\pm 2^{\circ}\text{C}$) with the equipment of luminance meter) and test unit shall be located at an approximate distance 50cm from the LCD surface at a visystem (SR-3AR&GRTewing angle of θ and Φ equal to 0° . We refer to $\theta\theta=0$ ($=03$) as the 3 o'clock direction (the "right"), $\theta\theta=90$ ($=012$) as the 12 o'clock direction ("upward"), $\theta\theta=180$ ($=09$) as the 9 o'clock direction ("left") and $\theta\theta=270$ ($=06$) as the 6 o'clock direction ("bottom"). While scanning θ and/or Φ , the center of the measuring spot on the display surface shall stay fixed. The backlight should be operating for 30 minutes prior to the measurement. VDD shall be $3.3\pm 0.3\text{V}$ at 25°C . Optimum viewing angle direction is o'clock.

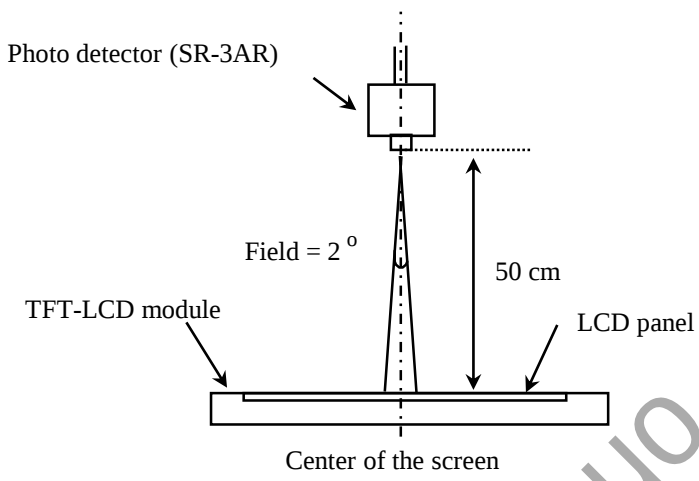
4.2 Optical Specifications

<Table 5. Optical Specifications>

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ_3	CR > 10	80	-	89	Deg.	Note 1
		Θ_9		80	-	89	Deg.	
	Vertical	Θ_{12}		80	-	89	Deg.	
		Θ_6		80	-	89	Deg.	
Luminance Contrast Ratio		CR	$\Theta = 0^{\circ}$	640	300	-		Note 2
Luminance of White	5 Points	Y_w	$\Theta = 0^{\circ}$ IF = 20mA	211	250	-	cd/m ²	Note 3
White Luminance Uniformity	5 Points	ΔY_5		80	-	-	%	Note 4
	13 Points	ΔY_{13}		66.7	-	-	%	
White Chromaticity		W_x	$\Theta = 0^{\circ}$	0.283	0.313	0.343		Note 5
		W_y		0.299	0.329	0.359		
Reproduction of Color	Red	R_x	$\Theta = 0^{\circ}$	Typ.-0.03	0.640	Typ.+0.03		
		R_y			0.330			
	Green	G_x			0.300			
		G_y			0.600			
	Blue	B_x			0.150			
		B_y			0.060			
Color Gamut				95	100	-	%	sRGB
Response Time (Rising + Falling)		T_{RT}	Ta= 25°C $\Theta = 0^{\circ}$	-	20	25	ms	Note 6
Cross Talk		CT	$\Theta = 0^{\circ}$	-	-	2.0	%	Note 7
Gamma		-	-	2.0	2.2	2.4	-	

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Notes : 1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 7). 2. Contrast measurements shall be made at viewing angle of $\Theta = 0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see Figure 7) Luminance Contrast Ratio (CR) is defined mathematically. CR = Luminance when displaying a white raster Luminance when displaying a black raster 3. Center Luminance of white is defined as luminance values of 5 point average across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 8 for a total of the measurements per display. 4. The White luminance uniformity on LCD surface is then expressed as : $\Delta Y = \text{Minimum Luminance of 5(or 13) points} / \text{Maximum Luminance of 5(or 13) points.}$(see Figure 8 and Figure 9). 5. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel. 6. The electro-optical response time measurements shall be made as Figure 10 by switching the “data” input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_r, and 90% to 10% is T_f. 7. Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark. (See Figure 11).			
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4.3 Optical Measurements



Optical characteristics measurement setup

Figure 7. Measurement Set Up

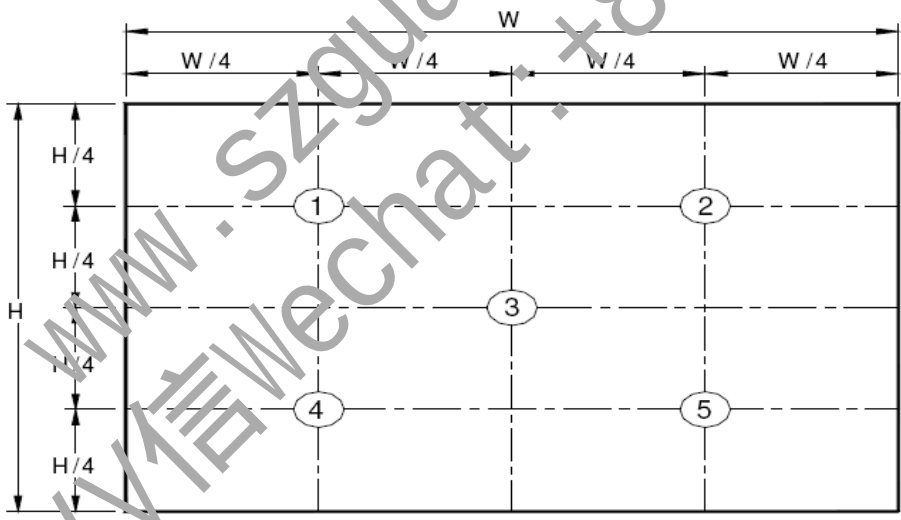


Figure 8. White Luminance and Uniformity Measurement Locations (5 points)

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Center Luminance of white is defined as luminance values of center 5 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 7 for a total of the measurements per display.

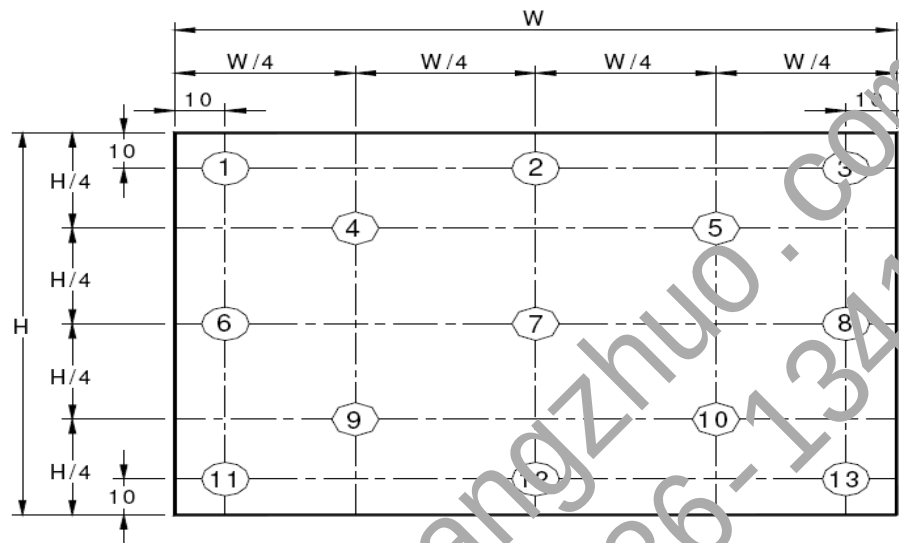


Figure 9. Uniformity Measurement Locations (13 points)

The White luminance uniformity on LCD surface is then expressed as : $\Delta Y5$ = Minimum Luminance of five points / Maximum Luminance of five points (see Figure 8) , $\Delta Y13$ = Minimum Luminance of 13 points /Maximum Luminance of 13 points (see Figure 9).

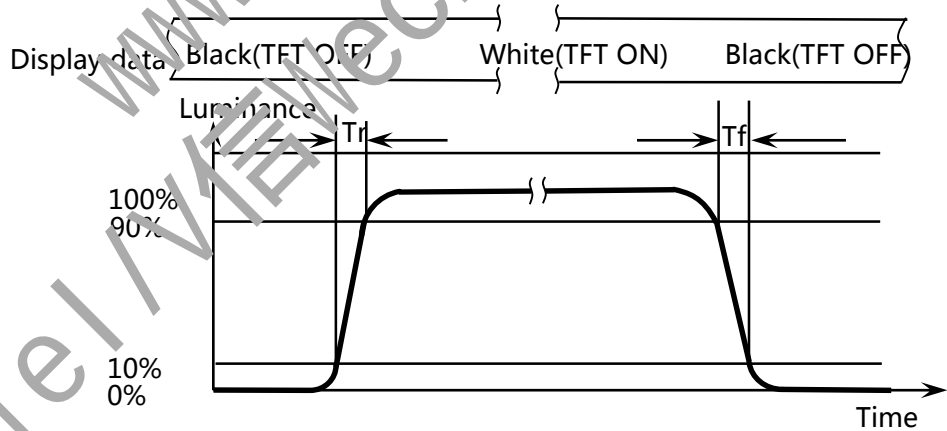
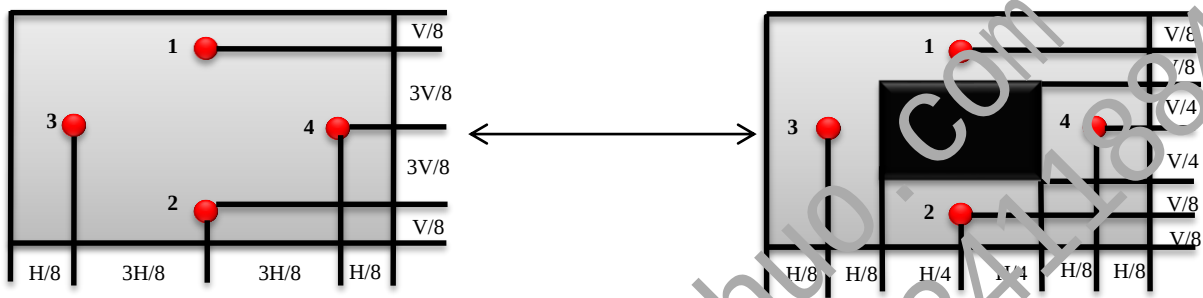


Figure 10. Response Time Testing

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The electro-optical response time measurements shall be made as shown in Figure 10 by switching the “data” input signal ON and OFF. Tr: The luminance to change from 10% to 90% ,Tf: The luminance to change from 90% to 10% .

The test system : GRT



Cross Talk (%) = $\left| \frac{Y_B - Y_A}{Y_A} \right| \times 100$

Figure 11. Cross Talk Modulation Test Description

Where:

- Y_A = Initial luminance of measured area (cd/m²)
- Y_B = Subsequent luminance of measured area (cd/m²)

The location 1/2/3/4 measured will be exactly the same in both patterns. The test background gray is from L64 to L192.Take the largest data as the result.

Cross Talk on one area of the LCD surface by another shall be measured by comparing the luminance (Y_A) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (Y_B) of that same area when any adjacent area is driven dark.(Refer to Figure 11)

The test system: SR-3AR

5.0 INTERFACE CONNECTION.

5.1 Electrical Interface Connection

The connector interface pin assignments are listed in Table 7.

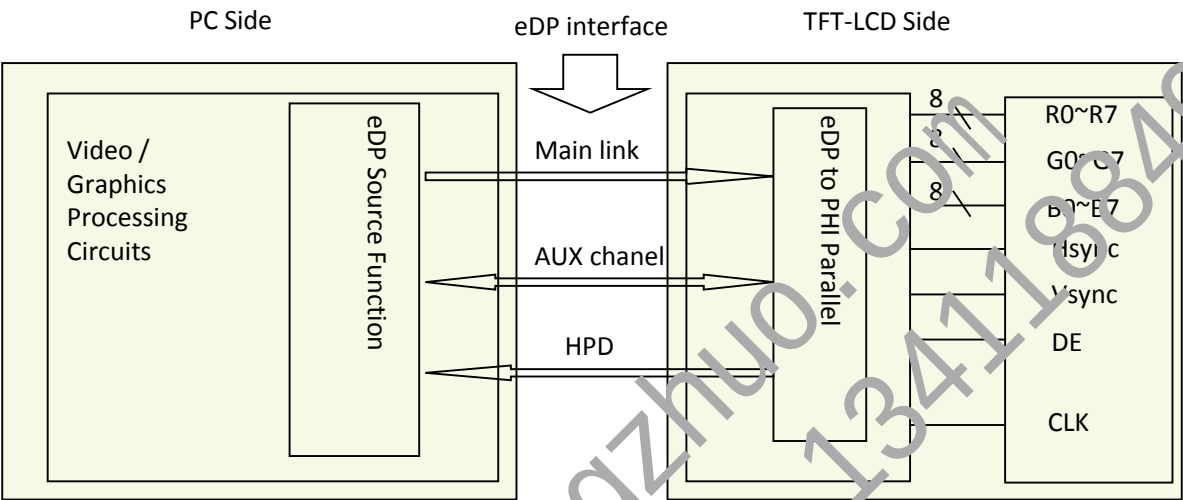
<Table 7. Pin Assignments for the Interface Connector>

Terminal	Symbol	Function	Remark
PIN No.	Symbol		
1	DDS_SCL	DDS I2C	
2	H_GND	High Speed Ground	Note1
3	Lane3_N	Complement Signal Link Lane 3	
4	Lane3_P	True Signal Link Lane 3	
5	H_GND	High Speed Ground	
6	Lane2_N	Complement Signal Link Lane 2	
7	Lane2_P	True Signal Link Lane 2	
8	H_GND	High Speed Ground	
9	Lane1_N	Complement Signal Link Lane 1	
10	Lane1_P	True Signal Link Lane 1	
11	H_GND	High Speed Ground	
12	Lane0_N	Complement Signal Link Lane 0	
13	Lane0_P	True Signal Link Lane 0	
14	H_GND	High Speed Ground	
15	AUX_CH_P	True Signal Auxiliary Channel	
16	AUX_CH_N	Complement Signal Auxiliary Channel	
17	H_GND	High Speed Ground	
18	LCD_VCC	LCD logic and driver power(3.3V)	
19	LCD_VCC	LCD logic and driver power(3.3V)	
20	LCD_VCC	LCD logic and driver power(3.3V)	
21	LCD_VCC	LCD logic and driver power(3.3V)	
22	BIST	BIST PIN	
23	LCD_GND	LCD logic and driver ground	
24	LCD_GND	LCD logic and driver ground	
25	LCD_GND	LCD logic and driver ground	
26	LCD_GND	LCD logic and driver ground	
27	HPD	HPD Signal	
28	BL_GND	Backlight ground	
29	BL_GND	Backlight ground	
30	BL_GND	Backlight ground	

31	BL_GND	Backlight ground	
32	BL_ENABLE	Backlight on/off	
33	BL_PWM_DIM	System PWM	
34	DDS_SDA	DDS_I2C	
35	NC	NC	Note2
36	BL_PWR	Backlight power	
37	BL_PWR	Backlight power	
38	BL_PWR	Backlight power	
39	BL_PWR	Backlight power	
40	NC	NC	Note2

Note : 1. The shielding case is connected with signal GND
Connector used :STM MSAK24025P40
Corresponding connector :I-PEX 20454 04 V1
2.Don't input any signals or any power into a NC pin. Keep the NC pin open.

5.2. eDP Interface



5.3.eDP Input signal

Lane 0	Lane 1	Lane 2	Lane 3
R0-7:0	R1-7:0	R2-7:0	R3-7:0
G0-7:0	G1-7:0	G2-7:0	G3-7:0
B0-7:0	B1-7:0	B2-7:0	B3-7:0
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-7:0	G5-7:0	G6-7:0	G7-7:0
B4-7:0	B5-7:0	B6-7:0	B7-7:0
R8-7:0	R9-7:0	R10-7:0	R11-7:0
G8-7:0	G9-7:0	G10-7:0	G11-7:0
B8-7:0	B9-7:0	B10-7:0	B11-7:0

6.0 SIGNAL TIMING SPECIFICATION

6.1 The NE156FHM-NX6 Is Operated By The DE Only

< Table 8. Signal Timing Specification >

Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	-	346.9	-	MHz
Frame Period		Tv	-	1158	-	lines
			-	144	-	Hz
			-	6.94	-	ms
Vertical Display Period		Tvd	-	1080	-	lines
One line Scanning Period		Th	-	2080	-	clocks
Horizontal Display Period		Thd	-	1920	-	clocks

Note : The above is as optimized setting.

6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 8.

<Table 9. eDP Rx Interface Timing Specification>

Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock	SSC	-	-	0.5	%	
Differential peak-to-peak input voltage at package pins	VRX-DIFFp-p	90	-	1200	mV	
Rx input DC common mode voltage	VRX_DC_CM	0	-	2	V	
Differential termination resistance	RRX-DIFF	80	90	100	Ω	
Single-ended termination resistance	RRX-SE	40	-	50	Ω	
Rx short circuit current limit	IRX_SHORT	-	-	50	mA	
Intra-pair skew at Rx package pins (HBR) RX intra-pair skew tolerance at HBR	LRX_SKEW_INTRA_PAIR		-	50	ps	

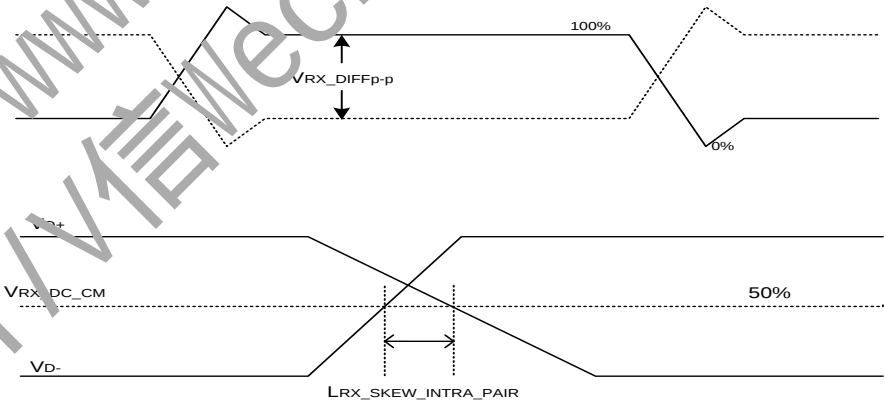


Figure 15. VRX-DIFFp-p & LRX_SKEW_INTRA_PAIR

<Table 10. HPD Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
HPD voltage	V _{HPD}	2.25	-	3.6	V	
Hot Plug Detection Threshold	-	2.0	-	-	V	Source side Detecting
Hot Unplug Detection Threshold	-	-	-	0.8	V	
HPD_IRQ Pulse Width	HPD_IRQ	0.5	-	1	ms	
HPD_TimeOut	-	2.0	-	-	ms	

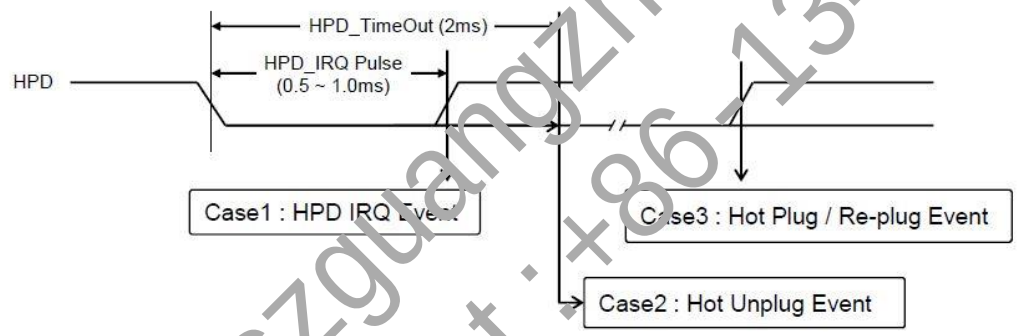


Figure 16. HPD Events

<Table 11. AUX Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
AUX unit interval	UIAUX	0.4	0.5	0.6	Us	
AUX peak-to-peak input differential voltage	VAUX-RX-DIFFp-p	0.29	-	1.38	V	
AUX CH termination DC resistance	RAUX-TERM	80	90	100	Ω	
AUX DC common mode voltage	VAUX-DC-CM	0	-	2	V	
AUX turn around common mode voltage	VAUX-TURN-CM	-	-	0.3	V	
AUX short circuit current limit	IAUX-SHORT	-	-	50	mA	
AUX AC Coupling Capacitor	CSOURCE-AUX	75	-	200	nf	Source side

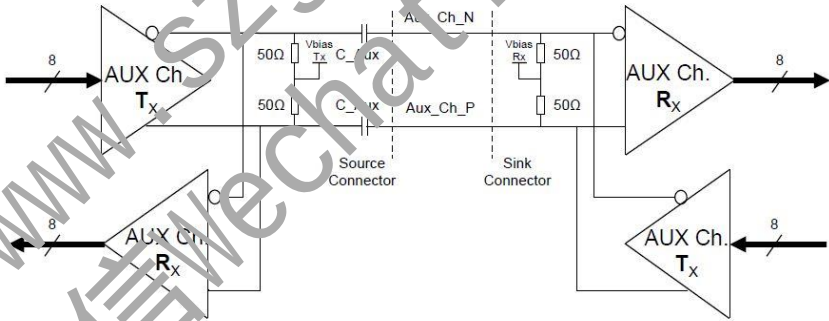


Figure 17. AUX differential pair

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7.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

	Colors & Gray scale	Data signal																							
		R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Light Blue	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Purple	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△																								
	▽																								
	Brighter	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▽	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△																								
	▽																								
	Brighter	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	▽	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	△																								
	▽																								
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Gray scale of White & Black	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	△																								
	▽																								
	Brighter	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1
	▽	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

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8.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below.

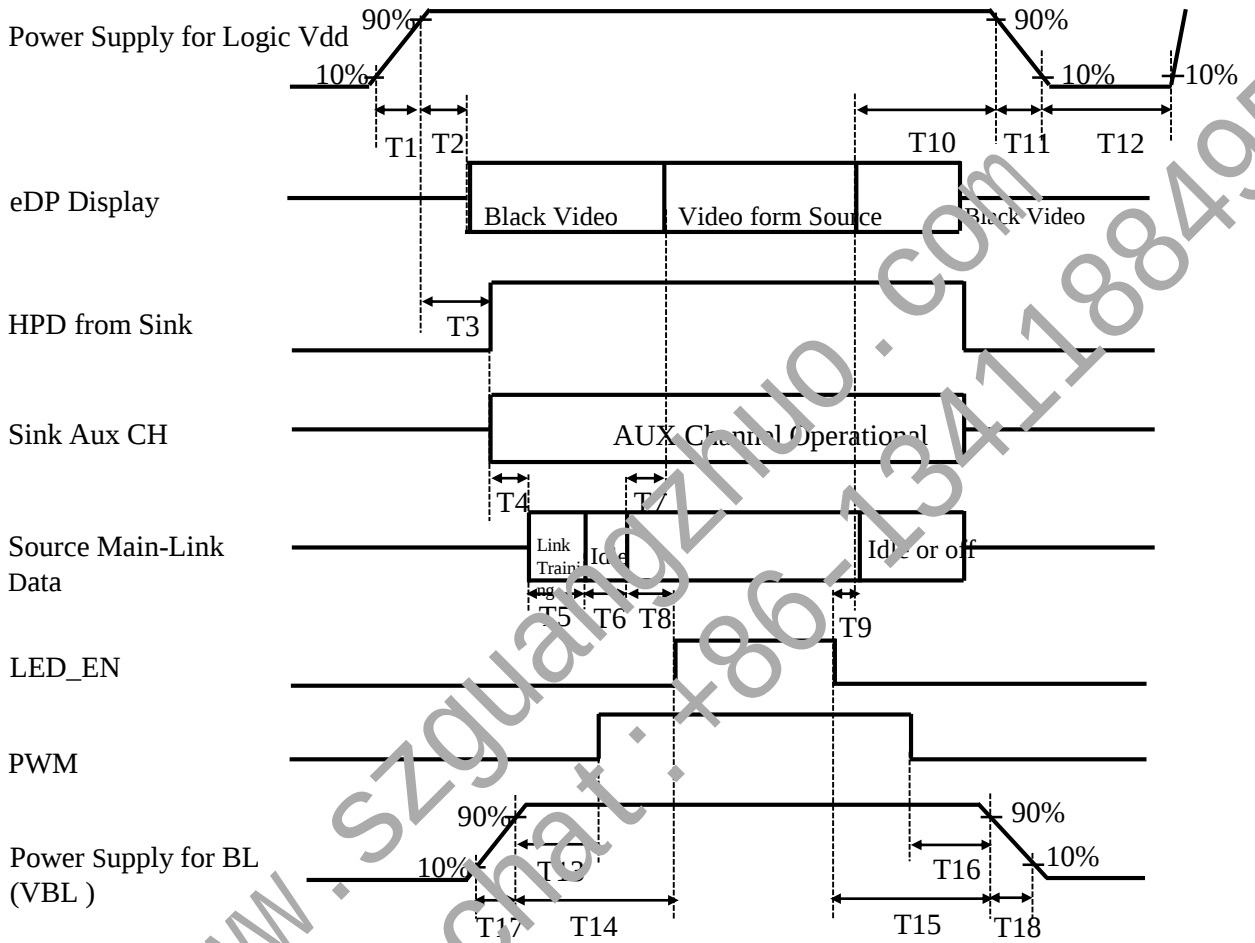


Figure 18. Power Sequence

- 0.5ms ≤ T1 ≤ 10 ms
 - 0ms < T2 ≤ 200 ms
 - 0ms < T3 ≤ 200 ms
 - T4+T5+T6+T7>80ms
 - 0ms < T7 ≤ 50ms
 - 50ms < T8
 - 0ms < T9
- 100ms < T10 < 500 ms
 - 0.5ms ≤ T11 ≤ 10 ms
 - 500ms ≤ T12
 - 0ms < T13
 - 0ms < T14
 - 0ms < T15
 - 0ms < T16
- 0.5ms ≤ T17
 - 0.5ms ≤ T18

Notes

1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal are valid.

9.0 Connector Description

Physical interface is described as for the connector on LCM.

These connectors are capable of accommodating the following signals and will be following components.

9.1 TFT LCD Module

Connector Name /Description	For Signal Connector
Manufacturer	STM or Compatible
Type/ Part Number	MSAK24025M40G or Compatible
Mating Housing/ Part Number	20451-040T or Compatible

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10.0 MECHANICAL CHARACTERISTICS

10.1 Dimensional Requirements

Figure 23 shows mechanical outlines for the model NE156FHM-NX6 V18.0.
Other parameters are shown in Table 14.

<Table 14. Dimensional Parameters>

Parameter	Specification	Unit
Active Area	344.16 (H) × 193.59 (V)	mm
Number of pixels	1920 (H) × 1080 (V) (1 pixel = R + G + B dots)	pixels
Pixel pitch	179.25(H) × 179.25(V)	um
Pixel arrangement	RGB Vertical stripe	
Display colors	16.7M(8bit)	
Display mode	Normally Black	
Dimensional outline	350.66 ± 0.3(H) * 205.25 ± 0.3(V) (W/O PCB) * 3.2(Max) 350.66 ± 0.3(H) * 214.75 ± 0.5 V (W/PCB) * 3.2(Max)	mm
Weight	365 (max)	g

10.2 Mounting

See Figure 24.

10.3 Anti-Glare and Polarizer Hardness

The surface of the LCD has an Anti-Glare coating to minimize reflection and a 3H hardness coating to reduce scratching.

10.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 350lux.

11.0 RELIABILITY TEST

The reliability test items and its conditions are shown in below.

<Table 15. Reliability Test>

No	Test Items	Conditions	Remark
1	High temperature storage test	Ta = 60°C , 240 hrs	
2	Low temperature storage test	Ta = -20°C , 240 hrs	
3	High temperature & high humidity operation test	Ta = 50°C , 80%RH, 240 hrs	
4	High temperature operation test	Ta = 50°C , 240 hrs	
5	Low temperature operation test	Ta = 0°C , 240 hrs	
6	Thermal shock	Ta = -20 °C (0.5 hr), ↔ 60 °C (0.5 hr), 100 cycle, switching time 5min	
7	Vibration test (non-operating)	Ta = 25°C , 60%RH, 1.5G, 10~500Hz, Sine wave, 30min/cycle, 1cycle for each X,Y,Z	Note 1
8	Shock test (non-operating)	Ta = 25°C , 60%RH, 220G, Half Sine Wave 2msec ± X, ± Y, ± Z Once for each direction	Note 1
9	Electro-static discharge test (operating)	Air : 150 pF, 330Ω, ± 15 KV Contact : 150 pF, 330Ω, ± 8 KV Ta = 25°C , 60%RH,	Note 2

Notes :

1. The fixture must be hard enough, so that the module would not be twisted or bent.
2. Self- recovery and restart recovery is allowed. No hardware failures.

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12.0 HANDLING & CAUTIONS

- (1) Cautions when taking out the module

 - Pick the pouch only, when taking out module from a shipping package.
- (2) Cautions for handling the module

 - As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
 - As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
 - As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
 - Do not pull the interface connector in or out while the LCD module is operating.
 - Put the module display side down on a flat horizontal plane.
 - Handle connectors and cables with care.
- (3) Cautions for the operation

 - When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
 - Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.
- (4) Cautions for the atmosphere

 - Dew drop atmosphere should be avoided.
 - Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.
- (5) Cautions for the module characteristic

 - Do not apply fixed pattern data signal to the LCD module at product aging.
 - Applying fixed pattern for a long time may cause image sticking.
- (6) Other cautions

 - Do not disassemble and/or re-assemble LCD module.
 - Do not re-adjust variable resistor or switch etc.
 - When returning the module for repair or etc. Please pack the module not to be broken. We recommend to use the original shipping packages.

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13.0 LABEL

(1) Product Label

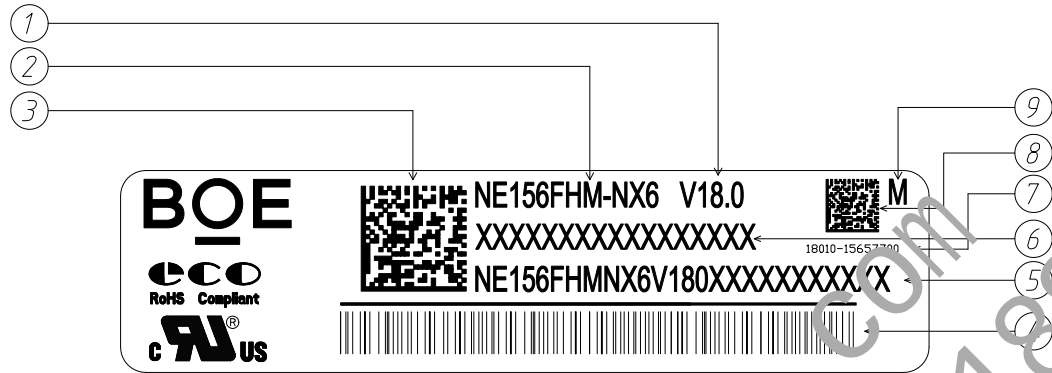


Figure 20. Product Label

Serial number marked part needs to print, show as follows:

- 1. Version
- 2. FG-CODE (Before 12 bit)
- 3. ASUS Gamming ID (2D barcode)
- 4. Module ID barcode
- 5. ASUS Gamming ID
- 6. Module ID
- 7. PN
- 8. PN (2D barcode)
- 9. M(Mass production)

Module ID Naming Rule:

<Table 16. Module ID Naming Rule>

Digit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Code	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Description	Product Name		Product Grade	Facility Code	Year		Month	Model Extension Code (Last 4 Digits FG Code)				Serial NO.					

(2) Box label

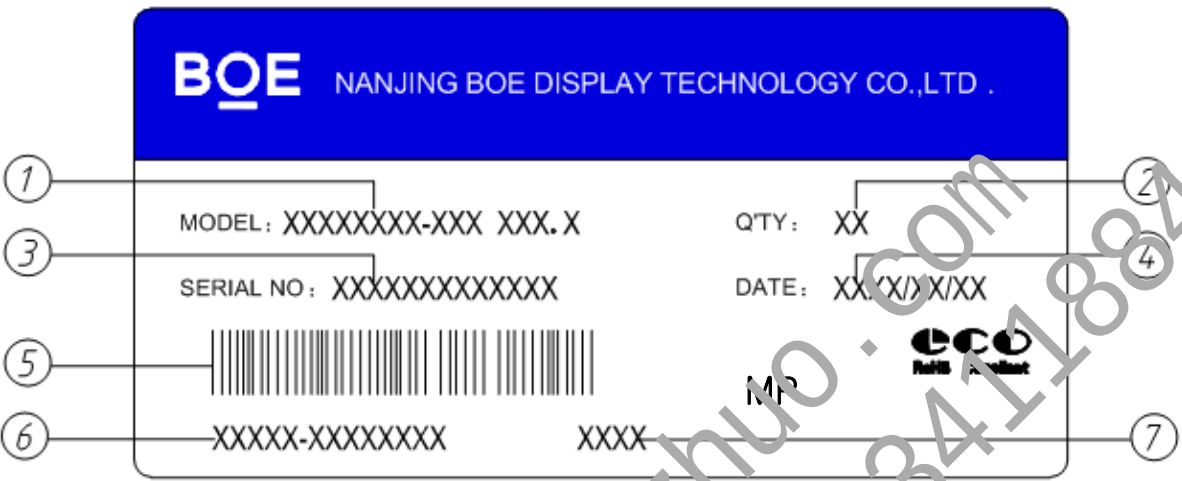


Figure 22. Box Label

Serial number marked part needs to print, show as follow:

- 1. FG-CODE
 - 2. Product Quantity (XX per Carton)
 - 3. BOX ID
 - 4. Date of Packing
 - 5. Barcode (Box ID)
 - 6. Customer FN.
 - 7. FG-Code After four
- Total Size:100*50mm

Box ID Naming Rule:

<Table 17. Box Label Naming Rule >

Digit	1	2	3	4	5	6	7	8	9	10	11	12	13
Code	X	X	X	X	X	X	X	X	X	X	X	X	X
Description	Product Name		Product Grade	Facility Code	Year		Month	Revision	Box Serial NO.				

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14.0 PACKING INFORMATION

14.1 Packing Order

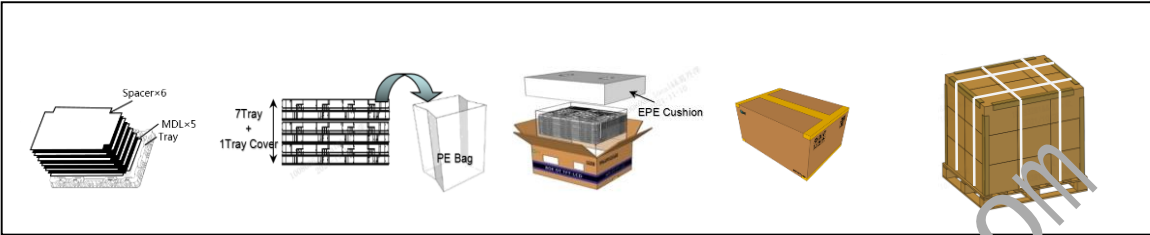


Figure 23. Packing Order

- Put 1 pcs spacer in tray and 1 pcs MDL on spacer.
5pcs MDL/Tray,6pcs Spacer/Tray
- Put 7 pcs tray and 1 pcs tray cover in PE bag.
- Put PE bag with 2 EPE Cushion in the inner box.
- 35pcs/Box,18Box/Pallet,630pcs MDL/Pallet.

14.2 Note

- Box dimension: 478mm*358mm*309mm
- Package quantity in one box: 35pcs
- Total weight: 15.0±1.5kg/Box

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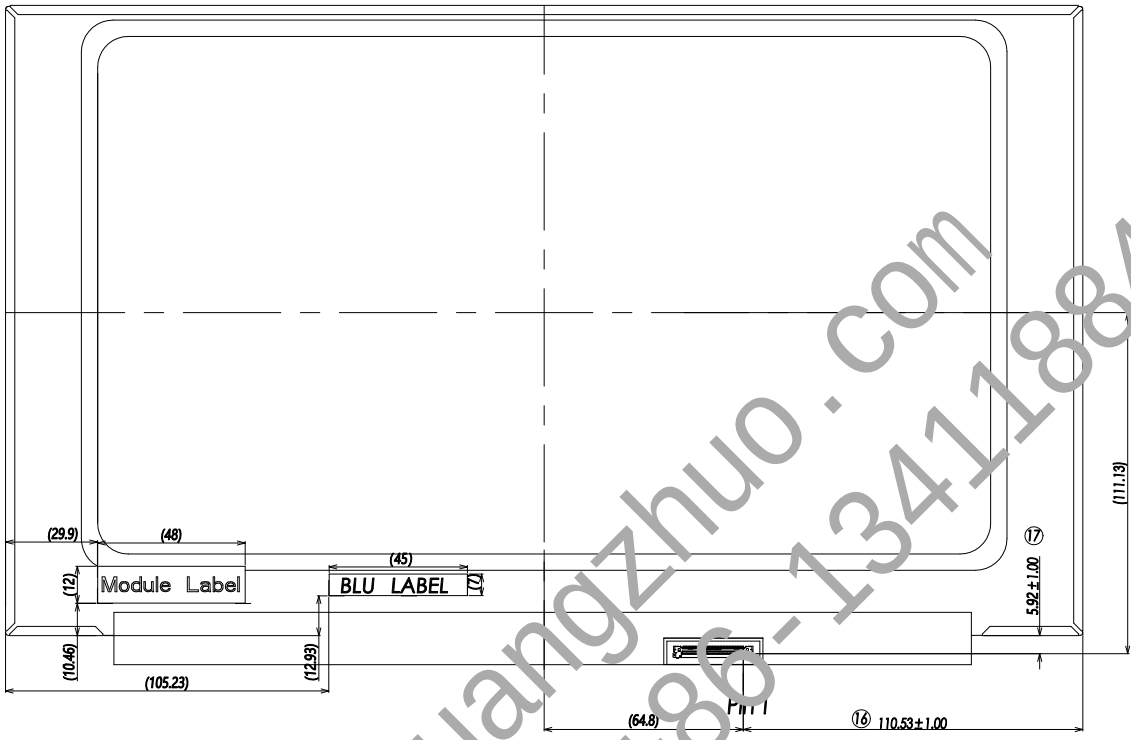


Figure 26.7 FT-LCD Module Outline Dimensions (Rear view)

- Notes:
1. Warpage and deformation Spec.: 0.5mm Max..
 2. The eDP connector is measured at PIN 1 and mating line.
 3. Unspecified tolerance refer to 0.3 mm.
 4. The measurement method for the dimension of module, please refer to product spec.
 5. Top polarizer is the highest portion.
 6. “0” means the reference dimensions.
 7. Critical dimension: ① ~ ⑱
- CPK: ① ~ ②

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16.0 EDID Table

Address (HEX)	Function	Hex	Dec	crc	Input values.	Notes
00	Header	00	0		0	EDID Header
01		FF	255		255	
02		FF	255		255	
03		FF	255		255	
04		FF	255		255	
05		FF	255		255	
06		FF	255		255	
07		00	0		0	
08	ID Manufacturer Name	09	9		BOE	ID = BOE
09		E5	229			
0A	ID Product Code	70	112		2928	ID = 2928
0B		0B	11			
0C	32-bit serial No.	00	0		0	
0D		00	0		0	
0E		00	0		0	
0F		00	0		0	
10	Week of manufacture	1E	30		30	
11	Year of Manufacture	20	32		2022	Manufactured in 2022
12	EDID Structure Ver.	01	1		1	EDID Ver 1.0
13	EDID revision #	04	4		4	EDID Rev. 0.4
14	Video input definition	A5	165		-	Refer to right table
15	Max H image size	22	34		34	34 cm (Approx)
16	Max V image size	13	19		19	19 cm (Approx)
17	Display Gamma	78	120		2.2	Gamma curve = 2.2
18	Feature support	03	3		-	Refer to right table
19	Red/Green low bits	EE	238		-	Red / Green Low Bits
1A	Blue/White low bits	95	149		-	Blue / White Low Bits
1B	Red x high bits	A3	163	655	0.640	Red (x) = 10100011 (0.64)
1C	Red y high bits	54	84	338	0.330	Red (y) = 01010100 (0.33)
1D	Green x high bits	4C	76	307	0.300	Green (x) = 01001100 (0.3)
1E	Green y high bits	99	153	314	0.600	Green (y) = 10011001 (0.6)
1F	Blue x high bits	26	38	154	0.150	Blue (x) = 00100110 (0.15)
20	BLue y high bits	05	5	61	0.060	Blue (y) = 00001111 (0.06)
21	White x high bits	59	80	321	0.313	White (x) = 01010000 (0.313)
22	White y high bits	54	84	337	0.329	White (y) = 01010100 (0.329)
23	Established timing 1	00	0		-	Refer to right table
24	Established timing 2	00	0		-	
25	Established timing 3	00	0		-	
26	Standard timing #1	01	1			Not Used
27		01	1			
28		01	1			
29	Standard timing #1	01	1			Not Used
2A		01	1			
2B		01	1			
2C	Standard timing #3	01	1			Not Used
2D		01	1			
2E		01	1			
2F	Standard timing #5	01	1			Not Used
30		01	1			
31		01	1			
32	Standard timing #6	01	1			Not Used
33		01	1			
34		01	1			
35	Standard timing #8	01	1			Not Used

16.0 EDID Table

36	Detailed timing/monitor descriptor #1	74	116		144.5	144.52MHz Main clock
37		38	56			
38		80	128		1920	Hor Active = 1920
39		A0	160		160	Hor Blanking = 160
3A		70	112		-	4 bits of Hor. Active + 4 bits of Hor. Blanking
3B		38	56		1080	Ver Active = 1080
3C		4E	78		78	Ver Blanking = 78
3D		40	64		-	4 bits of Ver. Active + 4 bits of Ver. Blanking
3E		30	48		48	Hor Sync Offset = 48
3F		20	32		32	H Sync Pulse Width = 32
40		35	53		3	V Sync Offset = 3 line
41		00	0		5	V Sync Pulse width : 5 line
42		58	88		344	Horizontal Image Size = 744 mm (Low 8 bits)
43		C2	194		194	Vertical Image Size = 194 mm (Low 8 bits)
44		10	16		-	4 bits of Hor Image Size + 4 bits of Ver Image Size
45		00	0		0	Hor Border (pixels)
46		00	0		0	Vertical Border (Lines)
47		1A	26		-	Refer to right table
48	Detailed timing/monitor descriptor #2	00	0		0	
49		00	0		0	
4A		00	0		0	
4B		FD	253		253	Tag Number for Display Range Limits Descriptor
4C		00	0		0	Vertical/Horizontal Rate Offset are zero
4D		3C	60		60	Minimum Vertical Rate :60Hz
4E		90	144		144	Maximum Vertical Rate :144Hz
4F		A7	167		167	Minimum Horizontal Rate : 167KHz
50		A7	167		167	Maximum Horizontal Rate : 167KHz
51		23	35		347	Maximum Pixel Clock : 346.85MHz
52		00	1		1	Range Limits Only
53		0A	10		10	Display Range Limits & CVT Support Definition
54		20	32		32	
55		20	32		32	
56		20	32		32	
57		20	32		32	
58		20	32		32	
59		20	32		32	
5A	Detailed timing/monitor descriptor #3	00	0			Indicates descriptor #4 is a display Descriptor
5B		00	0			Reserved
5C		00	0			Reserved
5D		FC	252			Tag : ASCII String
5E		00	0			Reserved
5F		4E	78		N	Model name : NE156FHM-NX6
60		45	69		E	
61		31	49		1	
62		35	53		5	
63		36	54		6	
64		46	70		F	
65		48	72		H	
66		4D	77		M	
67		2D	45		-	
68		4E	78		N	
69		58	88		X	
6A		36	54		6	
6B		0A	10			

16.0 EDID Table

6C	Detailed timing/monitor descriptor #4	00	0			Indicates descriptor #4 is a display Descriptor
6D		00	0			
6E		00	0			Reserved
6F		00	0			Tag : ASCII String
70		00	0			Reserved
71		00	0			Model name :
72		00	0			
73		00	0			
74		00	0			
75		00	0			
76		00	0			
77		00	0			
78		00	0			
79		00	0			
7A		00	0			
7B		00	0			
7C		00	0			
7D		00	0			
7E	Extension flag	01	1		?	0 : 1个EDID; N: N+1个EDID
7F	Checksum	D3	211	211	.	

16.0 EDID Table

80	DID Extension Header	70	112		112	DisplayID EDID Extension Block tag
81		20	32		32	DisplayID Version/Revision = 2.0
82		79	121		121	Section Size (byte) = 121 bytes
83		02	2		2	Display Product Primary Use Case
84		00	0		0	Extension count
85	DID Block #1 Header	22	34		34	DID2.0 Data block tag[22h] =Detailed Timing Data Block
86		00	0		0	Block revision = Revision 0
87		14	20		20	Number of Payload Bytes in block= 40 Bytes
88	DID DATA Block #1 detail timing	DB	219		346.8	Pixel Clock (Low bit, Range = 0.001Mhz (000000h) ~ 16,777.216Mhz (FFFFFh))
89		4A	74			Minium Pixel Clock (Middle bit)
8A		05	5			Minium Pixel Clock (High bit)
8B		84	132		132	timing options
8C		7F	127			
8D		07	7		1920	H-Active
8E		9F	159			
8F		00	0		160	H-Blanking
90		2F	47			
91		00	0		48	H-offset
92		1F	31			
93		00	0		32	H-sync pulse width
94		37	55			
95		04	4		1080	V-Active
96		4D	77			
97		00	0		70	V-Blanking
98		02	2			
99		00	0		3	V-offset
9A	DID Extension Header	04	4			
9B		00	0		5	V-sync pulse width
9C		2B	43		43	DID2.1 Data block tag[2Bh] = Adaptive-Sync Data Block
9D		00	0		0	Block revision = Revision 0
9E	DID Block #1 Header Adaptive Sync	06	6		6	Number of Payload Bytes in block= 6 Bytes
9F		27	39		39	Adaptive-Sync Operation and Range Information
A0		00	0		0	Flicker performance is met in any duration decrease within the refresh rate range without jitter impact.
A1	DID Block #1 Header Adaptive Sync	3C	60		60	Min. Vertical Rate : 60 Hz
A2		8F	143		143	Maximum Refresh Rate7:0
A3		00	0		0	bit1:0 =01: Maximum Refresh Rate9:8
A4	DID DATA Block #1	00	0		0	Flicker performance is met in any duration decrease within the refresh rate range without jitter impact.
A5		00	0		-	Unused
A6		00	0		-	Unused
A7		00	0		-	Unused
A8		00	0		-	Unused
A9		00	0		-	Unused
AA		00	0		-	Unused
AB		00	0		-	Unused
AC		00	0		-	Unused
AD		00	0		-	Unused
AE		00	0		-	Unused
AF		00	0		-	Unused

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16.0 EDID Table

B0		00	0	-	Unused
B1		00	0	-	Unused
B2		00	0	-	Unused
B3		00	0	-	Unused
B4		00	0	-	Unused
B5		00	0	-	Unused
B6		00	0	-	Unused
B7		00	0	-	Unused
B8		00	0	-	Unused
B9		00	0	-	Unused
BA		00	0	-	Unused
BB		00	0	-	Unused
BC		00	0	-	Unused
BD		00	0	-	Unused
BE		00	0	-	Unused
BF		00	0	-	Unused
C0		00	0	-	Unused
C1		00	0	-	Unused
C2		00	0	-	Unused
C3		00	0	-	Unused
C4		00	0	-	Unused
C5		00	0	-	Unused
C6		00	0	-	Unused
C7		00	0	-	Unused
C8		00	0	-	Unused
C9		00	0	-	Unused
CA		00	0	-	Unused
CB		00	0	-	Unused
CC		00	0	-	Unused
CD		00	0	-	Unused
CE		00	0	-	Unused
CF		00	0	-	Unused
D0		00	0	-	Unused
D1		00	0	-	Unused
D2		00	0	-	Unused
D3		00	0	-	Unused
D4		00	0	-	Unused
D5		00	0	-	Unused
D6		00	0	-	Unused
D7		00	0	-	Unused
D8		00	0	-	Unused
D9		00	0	-	Unused
DA		00	0	-	Unused
DB		00	0	-	Unused
DC		00	0	-	Unused
DD		00	0	-	Unused
DE		00	0	-	Unused
DF		00	0	-	Unused

16.0 EDID Table

E0		00	0	-	Unused
E1		00	0	-	Unused
E2		00	0	-	Unused
E3		00	0	-	Unused
E4		00	0	-	Unused
E5		00	0	-	Unused
E6		00	0	-	Unused
E7		00	0	-	Unused
E8		00	0	-	Unused
E9		00	0	-	Unused
EA		00	0	-	Unused
EB		00	0	-	Unused
EC		00	0	-	Unused
ED		00	0	-	Unused
EE		00	0	-	Unused
EF		00	0	-	Unused
F0		00	0	-	Unused
F1		00	0	-	Unused
F2		00	0	-	Unused
F3		00	0	-	Unused
F4		00	0	-	Unused
F5		00	0	-	Unused
F6		00	0	-	Unused
F7		00	0	-	Unused
F8		00	0	-	Unused
F9		00	0	-	Unused
FA		00	0	-	Unused
FB		00	0	-	Unused
FC		00	0	-	Unused
FD		00	0	-	Unused
FE		5D	93	47	DisplayID section checksum (81h~FDh)
FF		90	144	144	Extended block checksum (80h~FEh)

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17.0 GENERAL PRECAUTIONS

17.1 HANDLING

- (1) When the module is assembled, It should be attached to the system firmly using every mounting holes.
Be careful not to twist or bend the modules.
- (2) Refrain from strong mechanical shock or any force to the module. Otherwise, it may cause improper operation or damage to the module.
- (3) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than 1 HB pencil lead.
- (4) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.
- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth .In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static , it may cause damage to the module.
- (9) Use fingerstalls with soft gloves to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Do not pull or fold the LED FPC.
- (12) Do not touch any component which is located on the back side.
- (13) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (14) Pins of connector shall not be touched directly with bare hands.

17.2 STORAGE

- (1) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃ and relative humidity of less than 70%.
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.

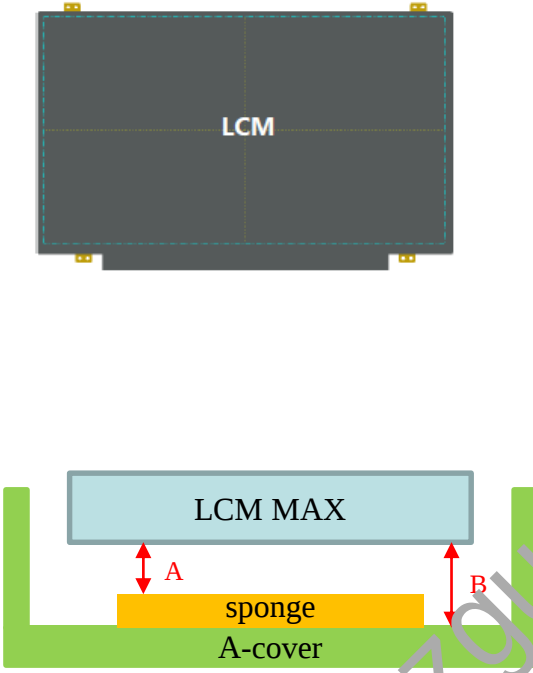
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17.3 OPERATION (1) Do not connect, disconnect the module in the “ Power On” condition. (2) Power supply should always be turned on/off by following item 8.0 “ Power on/off sequence “. (3) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference. (4) The standard limited warranty is only applicable when the module is used for general notebook applications. If used for purposes other than as specified, BOE is not to be held reliable for the defective operations. It is strongly recommended to contact BOE to find out fitness for a particular purpose. 17.4 OTHERS (1) Avoid condensation of water. It may result in improper operation or disconnection of electrode. (2) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation, Variation in part contents and environmental temperature, etc.) Otherwise the module may be damaged. (3) If the module displays the same pattern continuously for a long period of time, it can be the situation when The “ image sticks” to the screen. (4) This module has its circuitry PCB’s on the rear or bottom side and should be handled carefully to avoid being stressed.				
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Appendix A The Measurement Methods for the Dimensions of Module Caliper: Thickness of Outline (Without/With PCB For Flat Project) (Without PCB For Bend Project) Micrometer: Thickness with PCB For Bend Project (Without FPC/COF Air Gap Effect) Coordinate Measuring Machine: Length of Outline (Without Tape Wrinkle or Bulged) Width of Outline (Without PCB) (Without Tape Wrinkle or Bulged) Width of Outline (With PCB) CF Polarizer Size Active Area (Or AA_BM) Size Active Area to Outline (Without Tape Wrinkle or Bulged) Active Area to CF Polarizer The Distance of Bracket Holes P-Cover to Outline (Without Tape Wrinkle or Bulged) Length of P-Cover Connector Pin 1 to Outline (Without Tape Wrinkle or Bulged) Height Gauge: The Different Height of Foot and Top on the Bracket (Need to Calculate From Bracket Angle Spec.) Feeler Gauge: The Warpage Spec. of Module Notes: Except the Critical Dimensions as Above, Other Dimensions are Measured by Coordinate Measuring Machine If Necessary.				
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Appendix B

LCM to A-Cover / sponges z-gap



	Plastic Cover (LCM Thickness: Max)	Metal Cover (LCM Thickness: Max)
A	>0mm	>0mm
B	Min: 1.0mm	Min: 0.8mm
Without the open area of back cover		

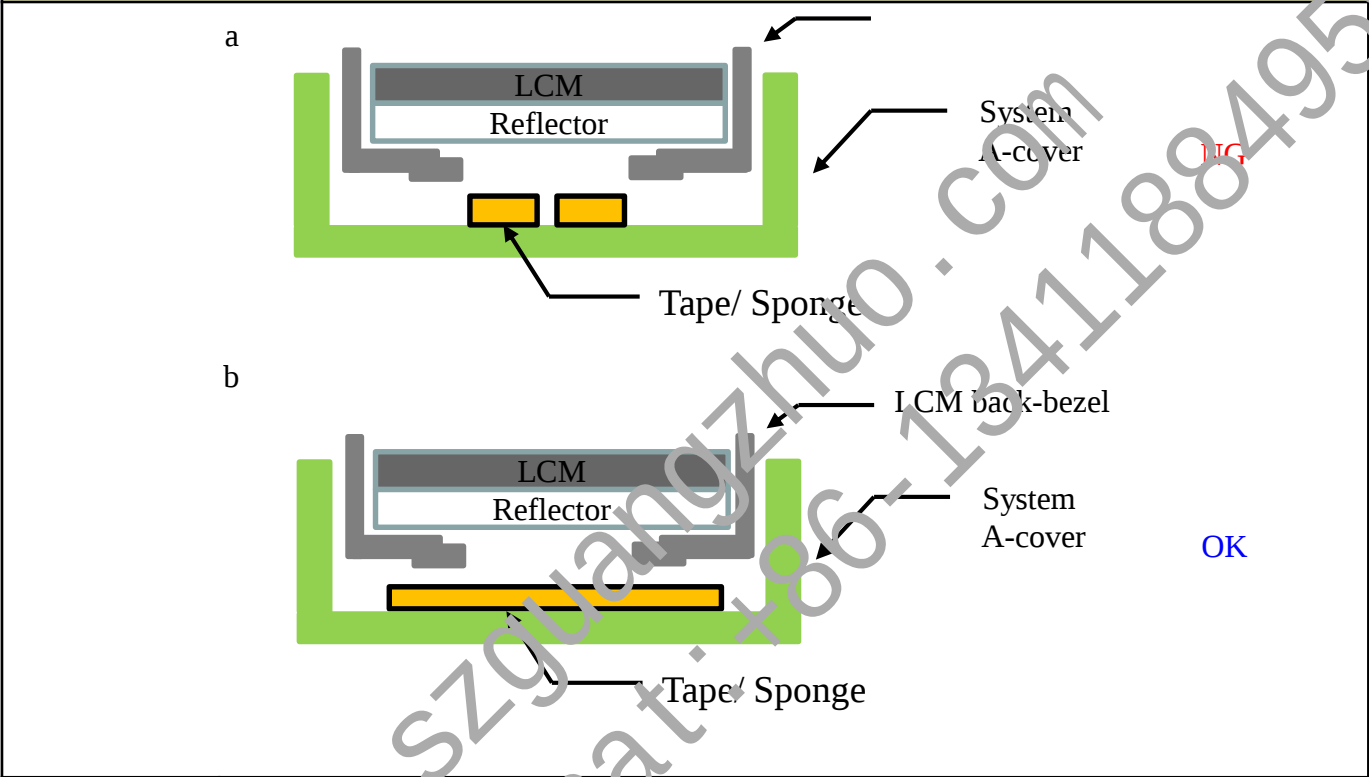
Purpose

The reflector area is very sensitive, we suggest that design enough z-gap to decrease the risk of water upple, white spot and other abnormal display

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LCM to A-Cover / sponges z-gap

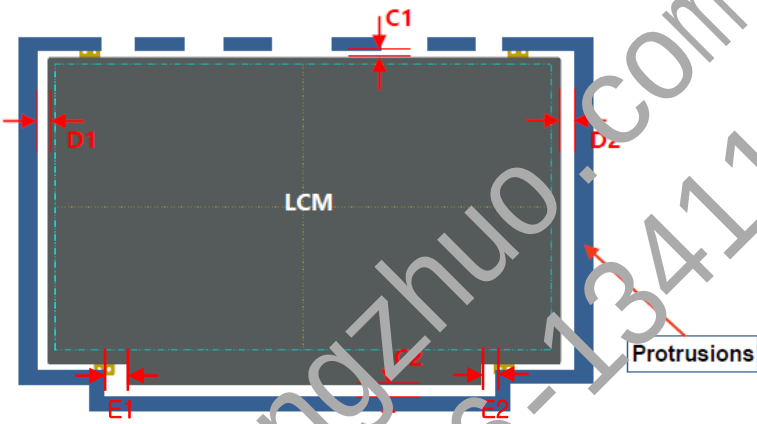


Purpose	If attach sponges or rubbers which correspond to white reflector area, it may cause white spot, pooling or other relate issues. We suggest that attach wide range sponges / rubbers which can cover the LCM back-bezel opening
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Appendix B

LCM to side wall / protrusions

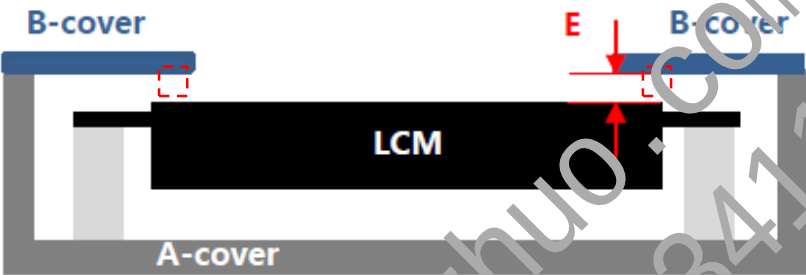


	Normal border	Narrow border
D1/D2	Min: 0.45mm	Min: 0.35mm
C1	Min: 0.50mm	
C2	Min: 0.50mm	
E1/E2	Min: 0.55mm	

Purpose	We suggest that design enough gap around LCM to prevent shock test failure, or interference, cell crack, abnormal display...etc. in the reliability test
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Appendix B

LCM to B-cover z-gap



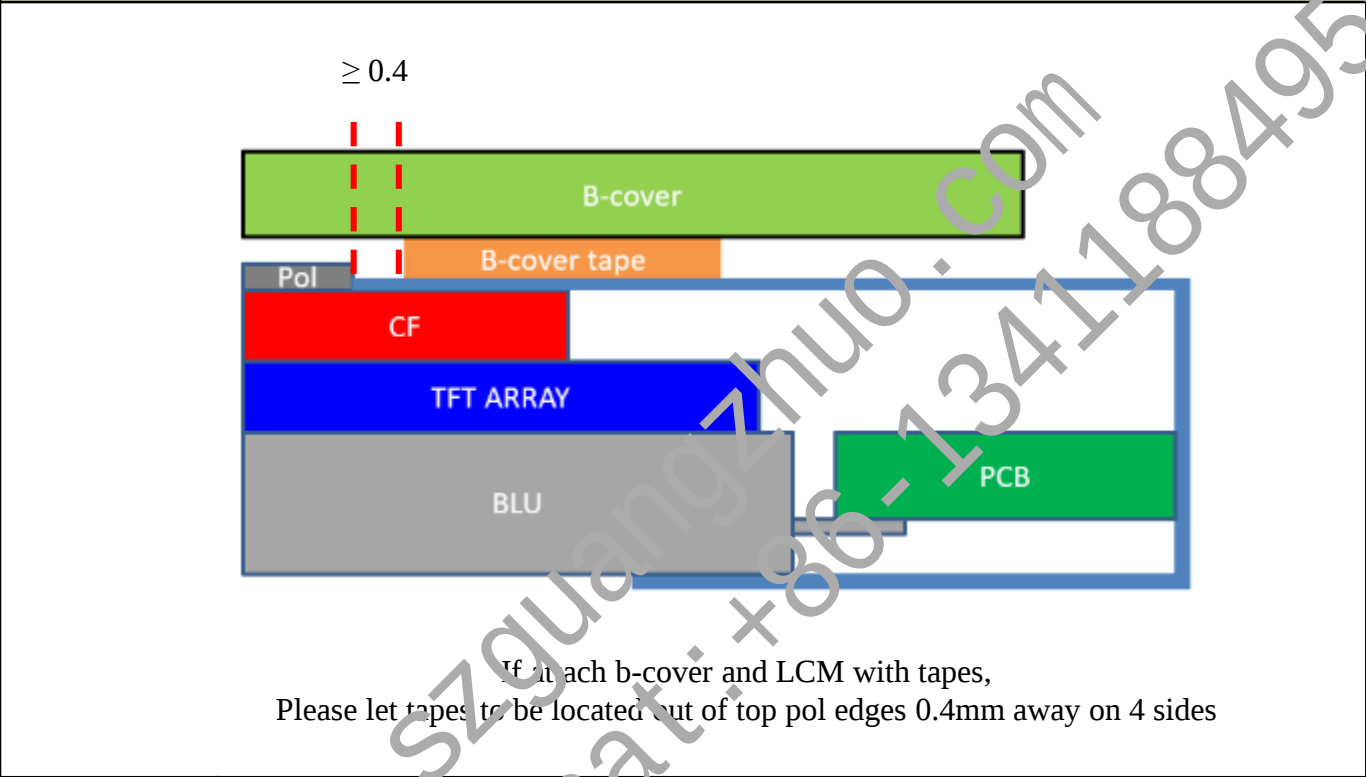
B-cover Tape	Gap
Without	0.15 ~ 0.25mm
With	0.15 ~ 0.20mm

Purpose	Too less z-gap between system B-cover and LCM top pol has high risk to cause cell crack, pooling, light leakage and other issues
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Appendix B

B-cover tape to top pol edge



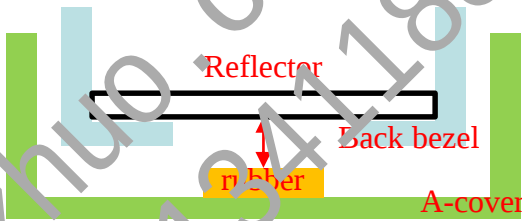
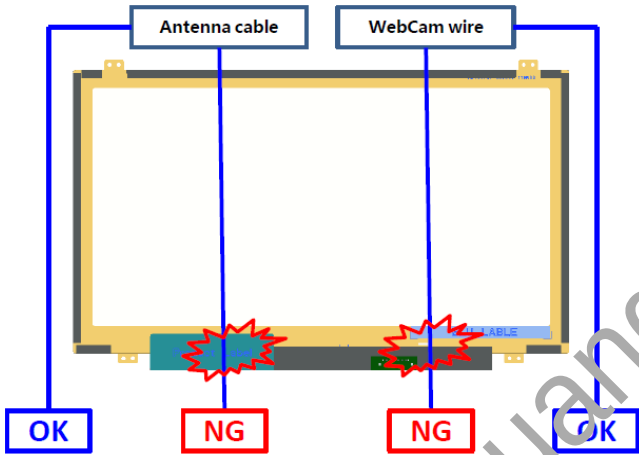
If attach b-cover and LCM with tapes,
Please let tapes to be located out of top pol edges 0.4mm away on 4 sides

Purpose	To avoid the B-cover tape override top pol and cause pooling or light leakage issue
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Appendix B

Antenna Cable & Webcam wire



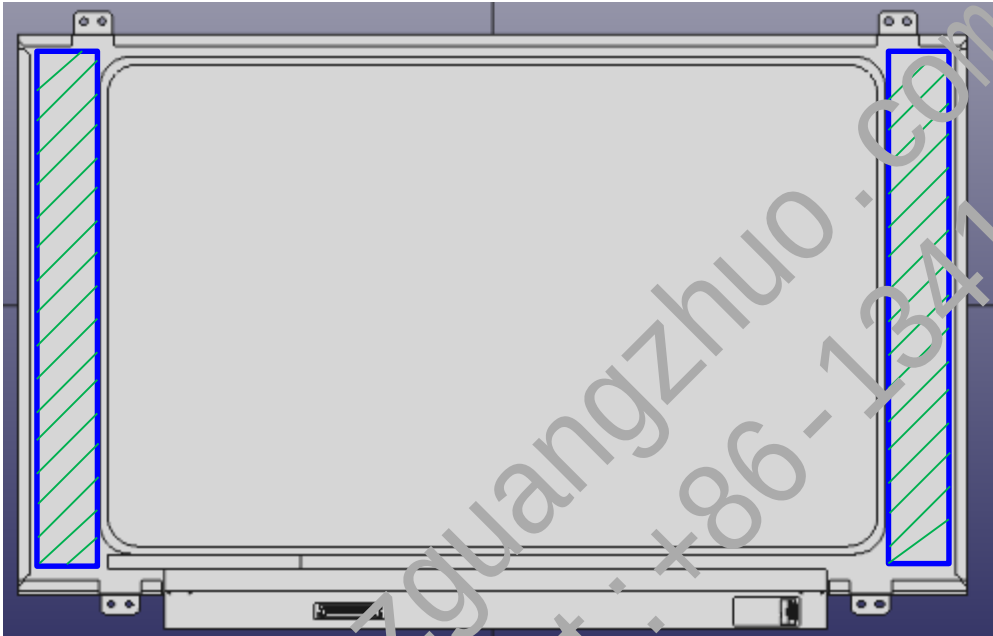
If sponge within the reflector area is necessary, we suggest that the gap between reflector and sponge is more than 0.5mm

Purpose	1. We suggest that do not set Antenna or WebCam cable / wire go behind LCM to avoid backpack test, hinge test ,twist test or pogo test with abnormal display 2. If the cable / wire is necessary to go behind LCM, please make a groove with rounds or chamfers to protect the cable / wire, or attach with higher sponge / rubber adjacent to the cable / wire route 3. Suggest that attach the cable / wire with tapes to A-cover 4. Do not attach anything with LCM reflector area. If attach cable / wire with LCM reflector area, it may cause pooling, white spot, light leakage and other related issues
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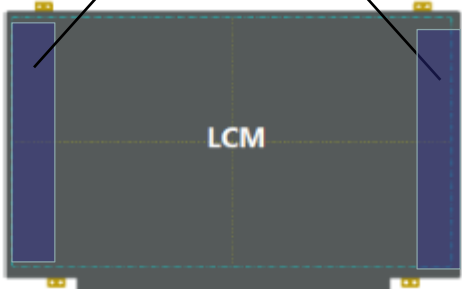
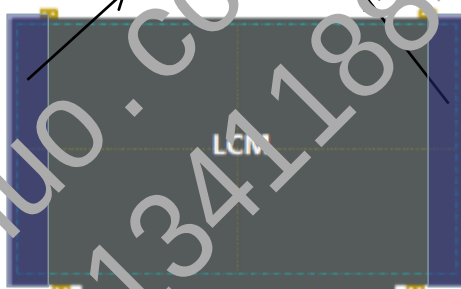
Appendix B

LCM paste area



Attachment area

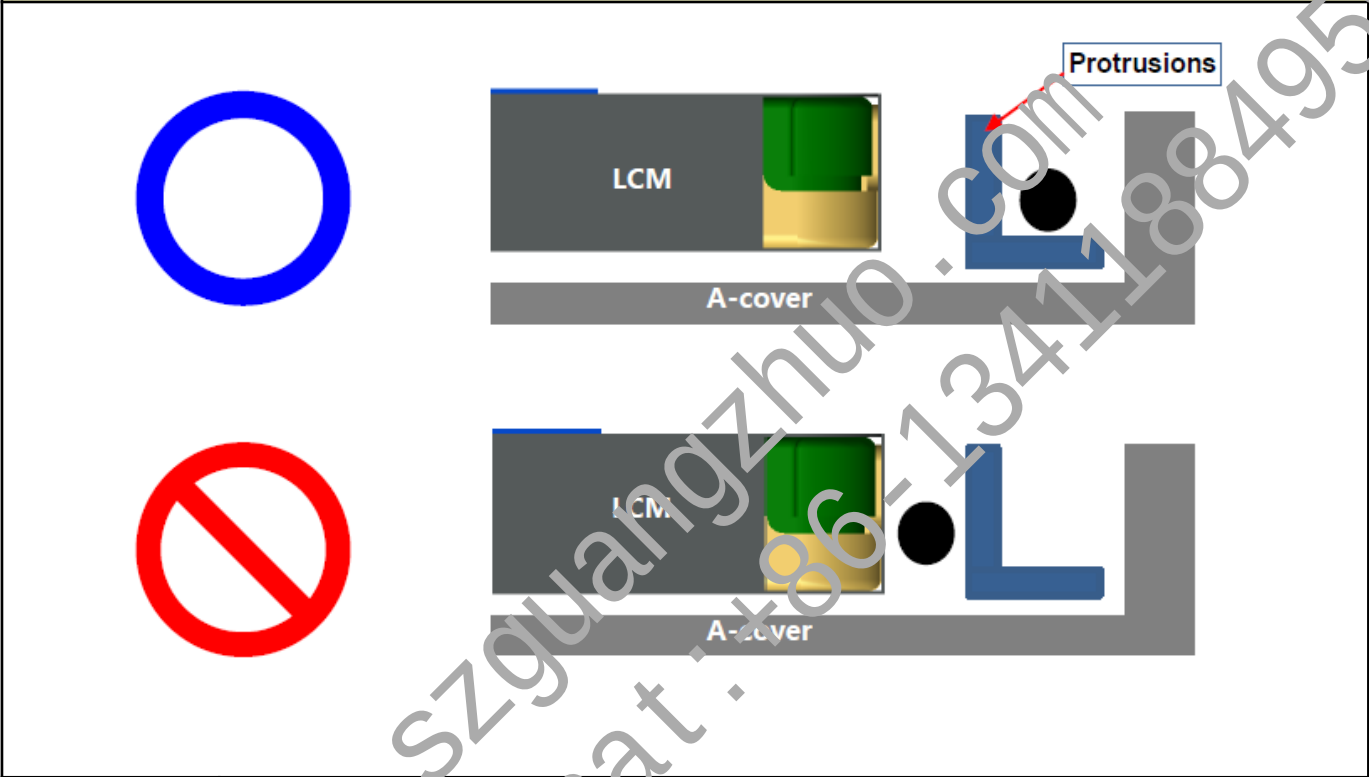
Purpose	If use the stretch remove tapes to fix LCM with A-cover, please set the stretch remove tapes correspond to the LCM back-bezel and do not let the tapes override the back-bezel's level step of opening
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LCM pressable area				
Position of pressure head  NG Position of pressure head  OK				
Purpose	1. LCM is fixed on A-cover by double-sided tap which can stick LCM after using the press jig stress LCM during assembling. 2. To avoid panel broken the design of pressure head of press jig can not only pin on cell panel. The pressure head needs to pin on the LCM frame, which the LCM frame can share the pressure of the pressing head.			
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Wire setting

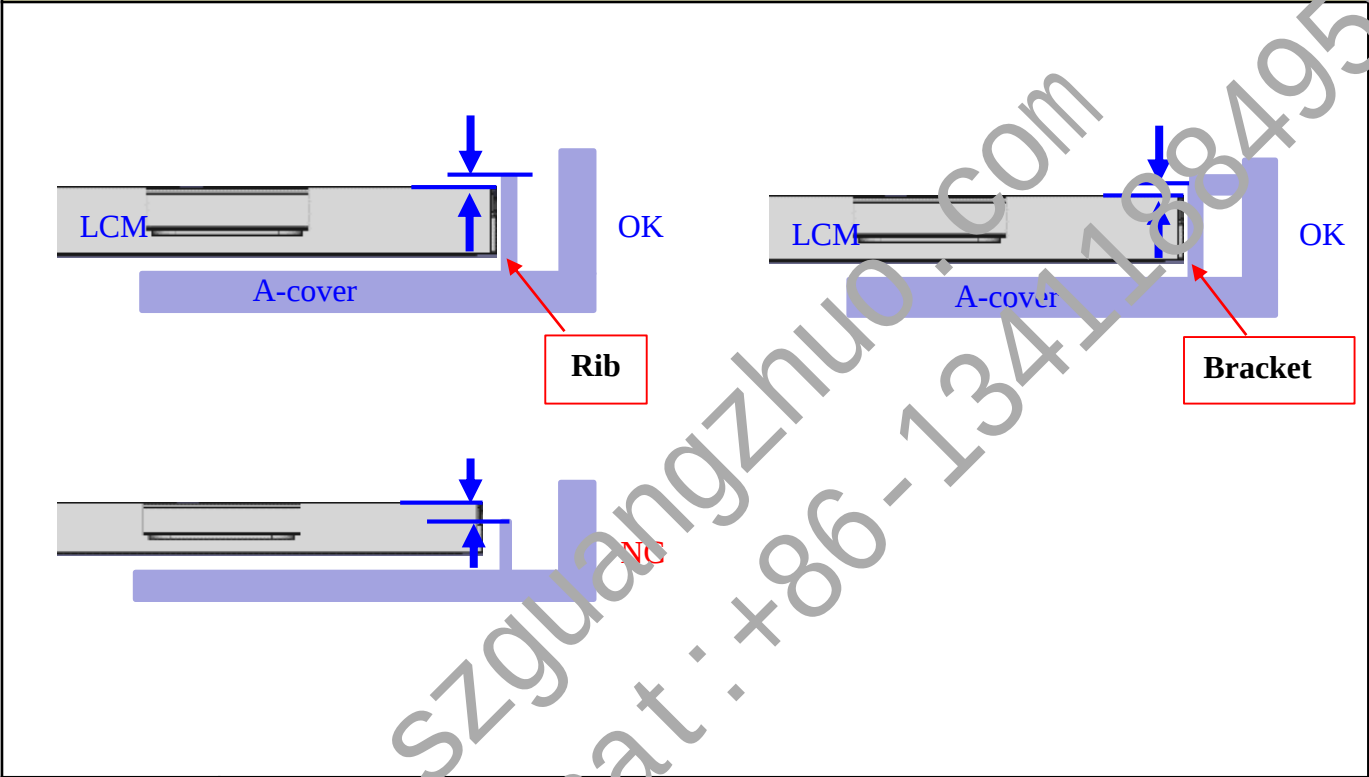


Purpose	Wire should be placed between Protrusions and A-cover. If place the wire between LCM and Protrusions, it may interfere with LCM when assembling B-covers, or even cause LCM breakage in reliability test.
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Appendix B

A-cover strength



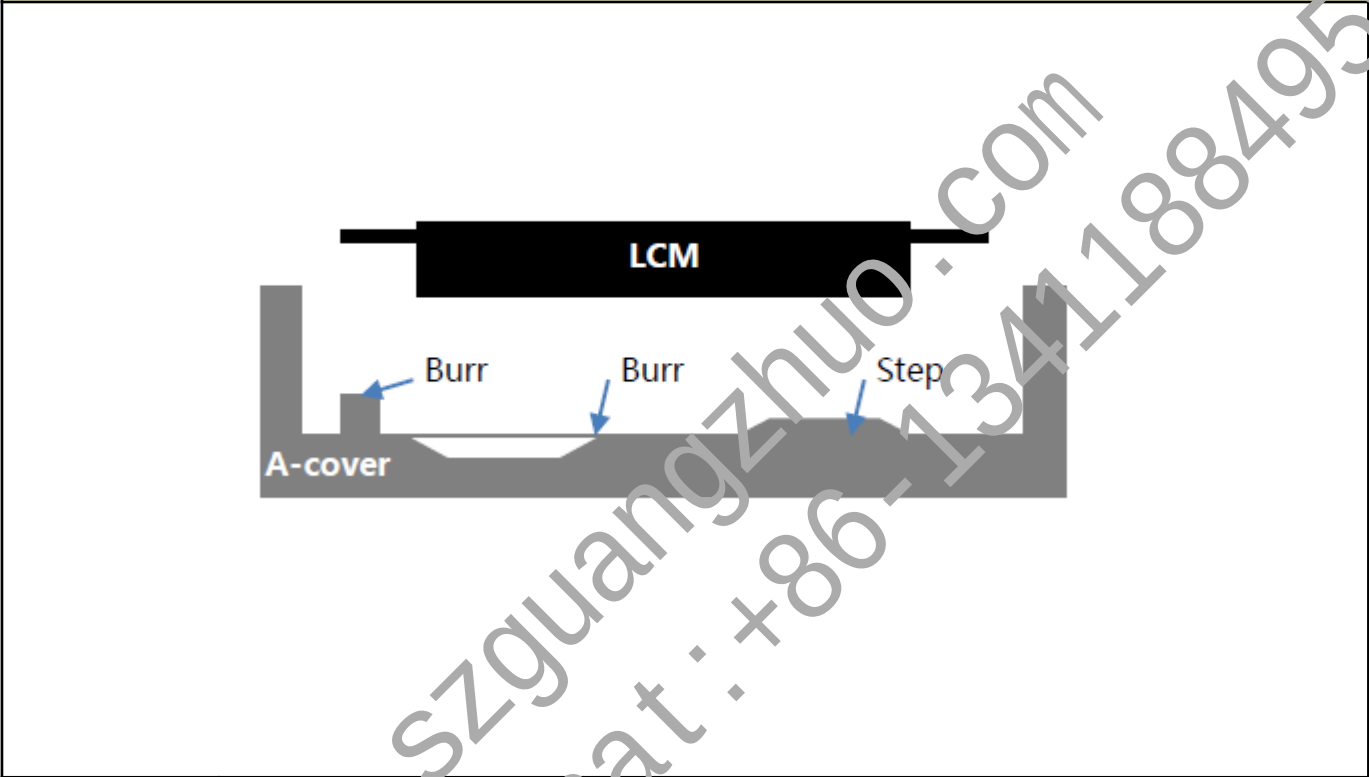
Purpose	1. It is recommended that Rib height is higher than LCM, in order to avoiding press on LCM edge panels. 2. As for LCM is more stronger than Rib, the L Bracket is be recommended.
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Appendix B

System A-cover Inner Surface



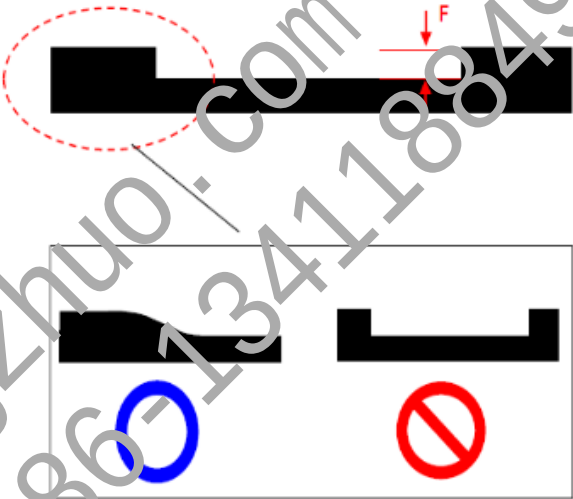
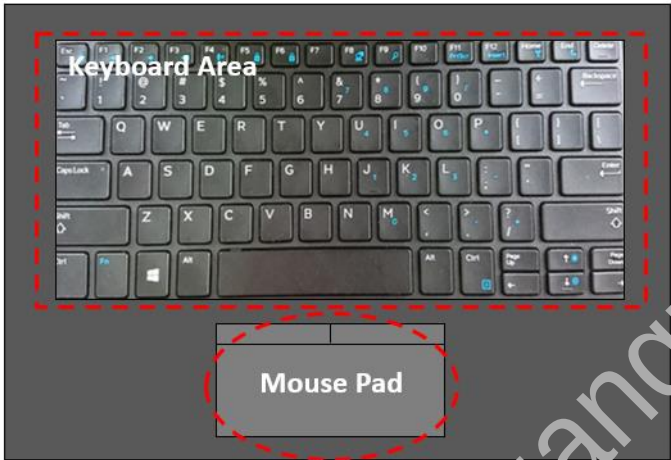
Purpose	There should not exist any burr, segment gap or protrusions beside Logo, which would cause White Spot or Glass Broken by stress concentration.
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Appendix B

Keyboard area & Mouse pad



F: max 0.3mm

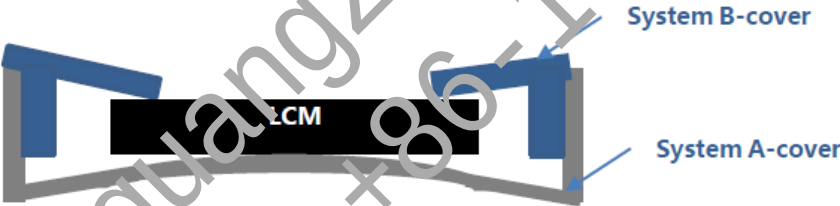
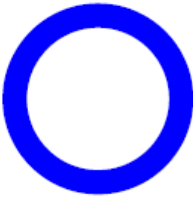
Purpose	In order to avoiding I.C.M fragments in reliability test, the step surface of Keyboard and Mouse pad transmits smoothly, and should not be right-angle. For example, when Foge testing, if the broken hole is done in this location, it is easy to produce fragments.
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Appendix B

System cover reliability

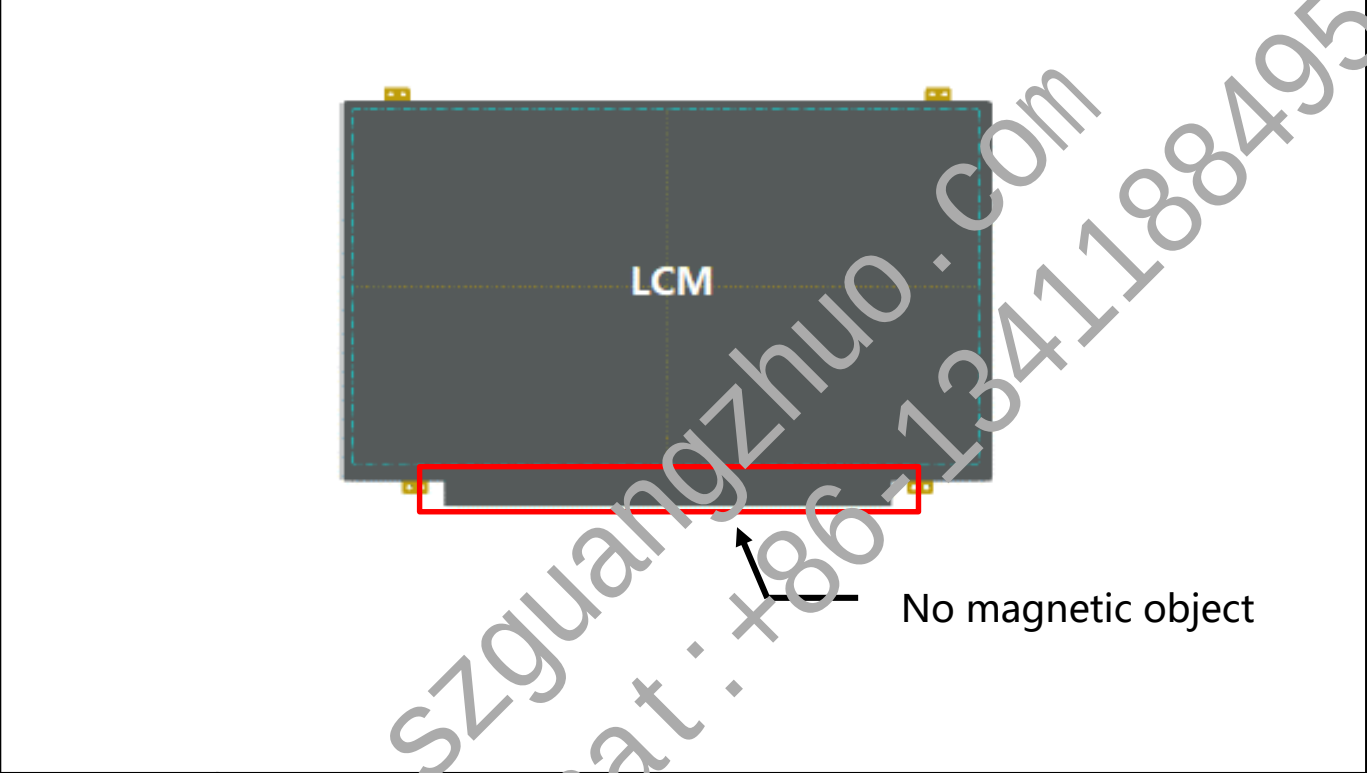


Purpose	The permanent deformation part of System cover after the reliability test, including sponge and other structures or components, can not touch LCM.
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A/B-cover near LCD PCBA

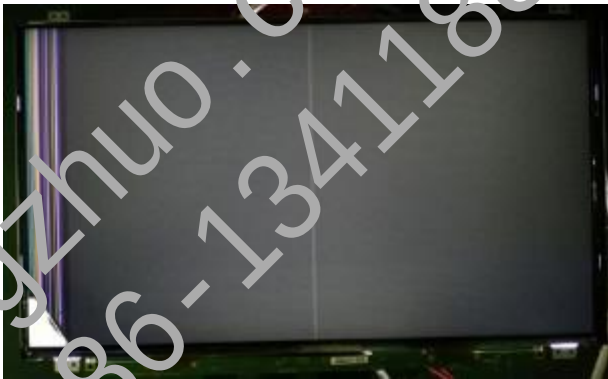
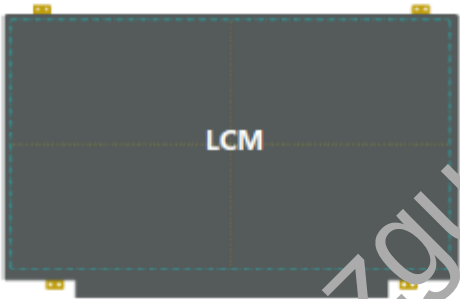


Purpose	There should not have magnet object near LCM PCBA, which is prone to cause physical or electricity noise issue
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A-cover add sponges on Boss side wall



Purpose

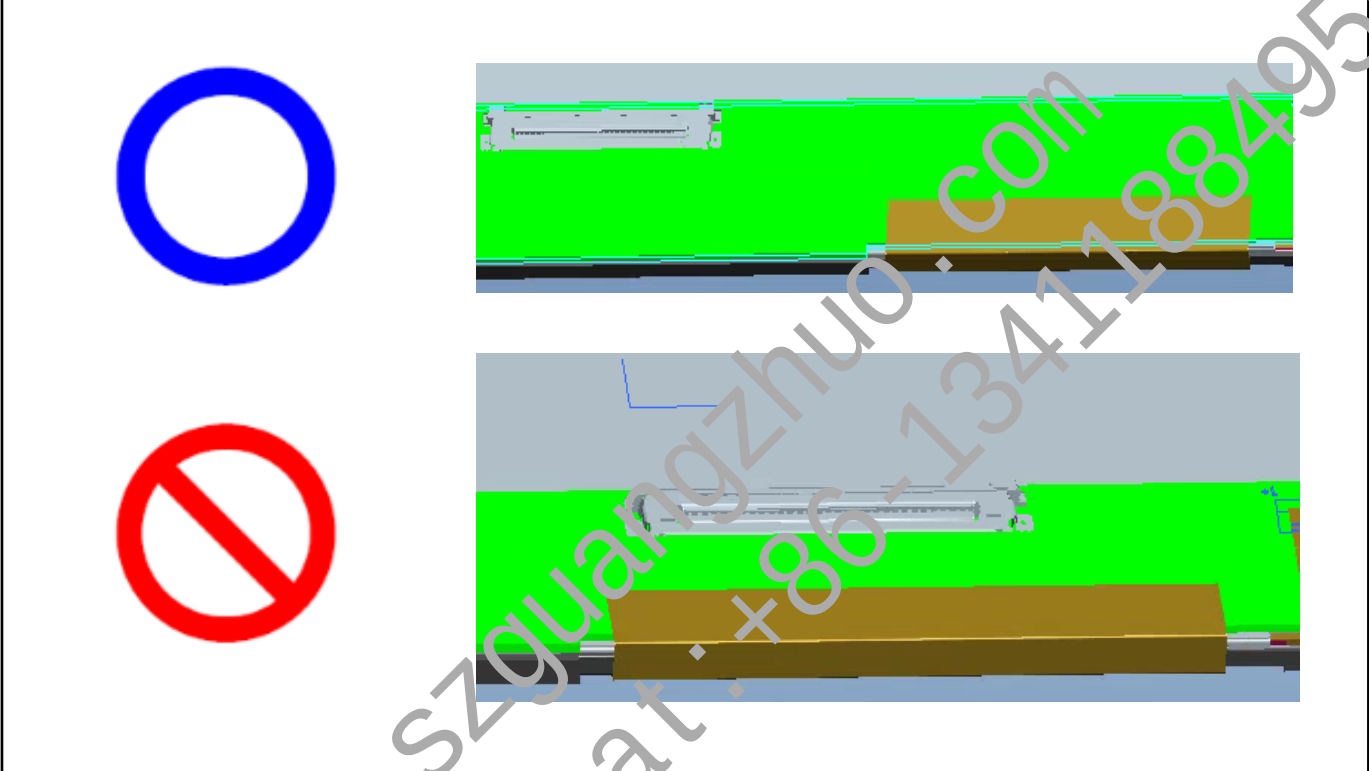
We suggest to attach Sponges to the side of the Boss column of A-cover to reduce the panel broken possibility in assembly. It is recommended to this design synchronously.

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LCM to A-Cover / sponges z-gap



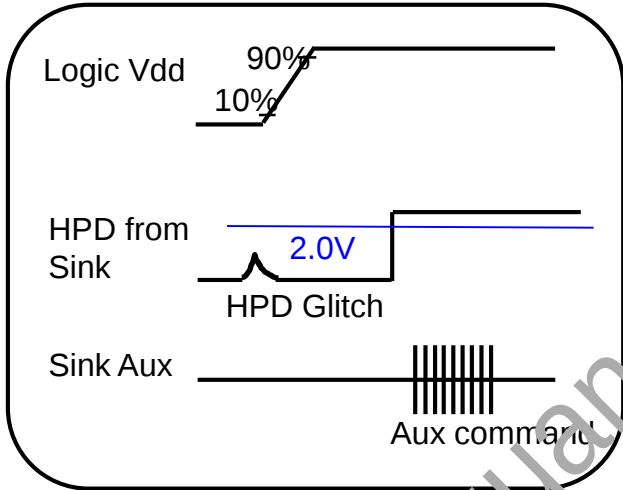
Purpose	Bent product: The position of system connector and FPC should be staggered in X direction. Otherwise, when testing, the system Cable line extrudes FPC, leading to FPC Crack; (Panel FPC Bonding location is related to Mask and can not be changed easily)
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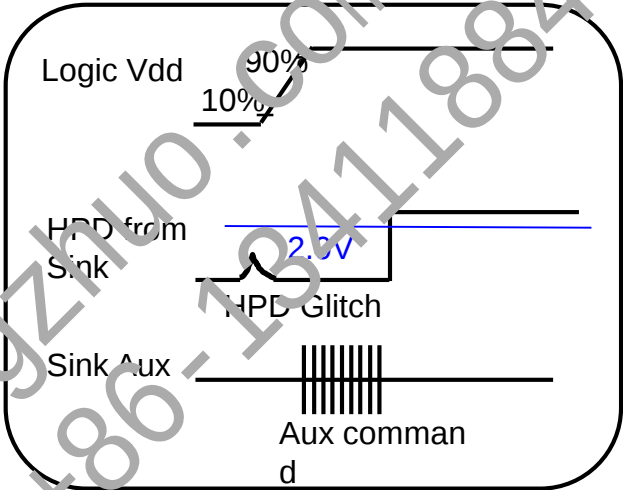
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Appendix C

HPD Signal recognition



Normal Signal (Ignore HPD Glitch)

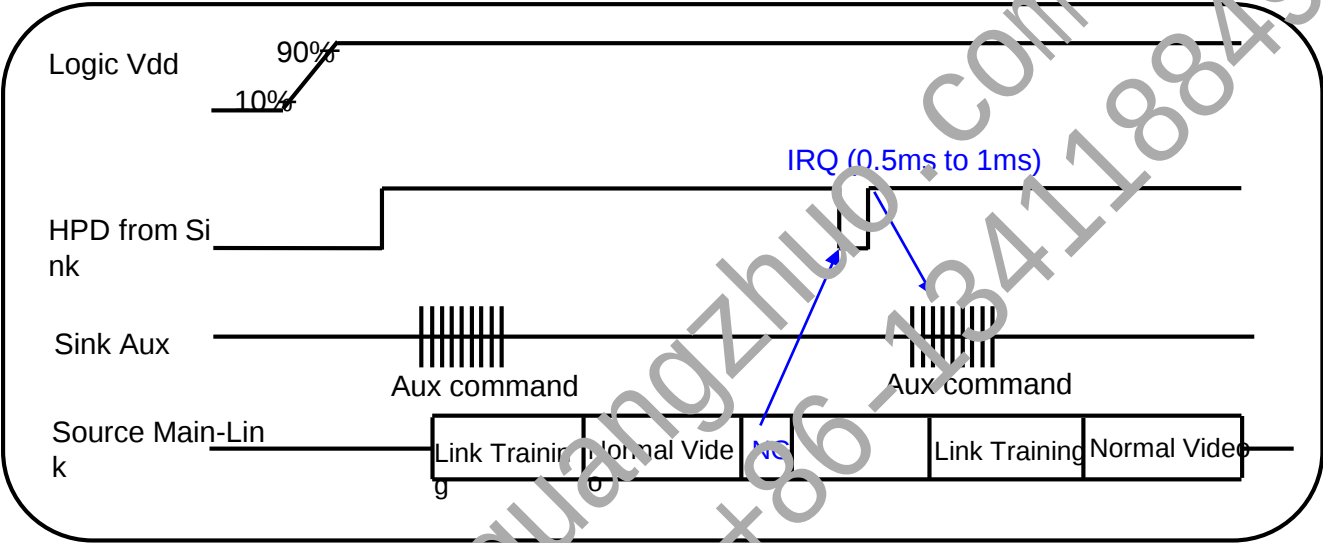


Abnormal Signal

Purpose	When HPD glitch voltage less than 2.0(V), system signal can't output AUX command data.
---------	--

Appendix C

HPD Signal Definition IRQ (Interrupt Request)

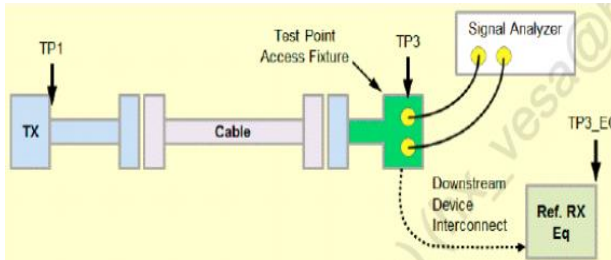


Purpose

When HPD signal low than 0.5ms to 1ms, the source device should check sink status field from the DPCD and take link training again.

Appendix C

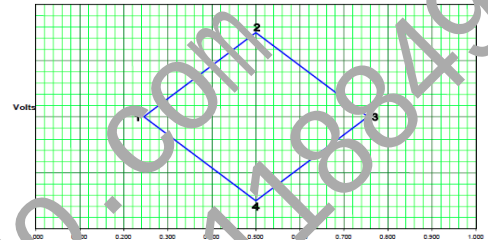
Main link eye diagram of TP3



Measured TP3 on LCM connector.

	UI	Voltage
1	0.246	0
2	0.5	0.075
3	0.755	0
4	0.5	-0.075

Eye for TP3 at LBR



Downstream Device Mask at TP3

	UI	Voltage
1	0.375	0
2	0.5	0.023
3	0.625	0
4	0.5	-0.023

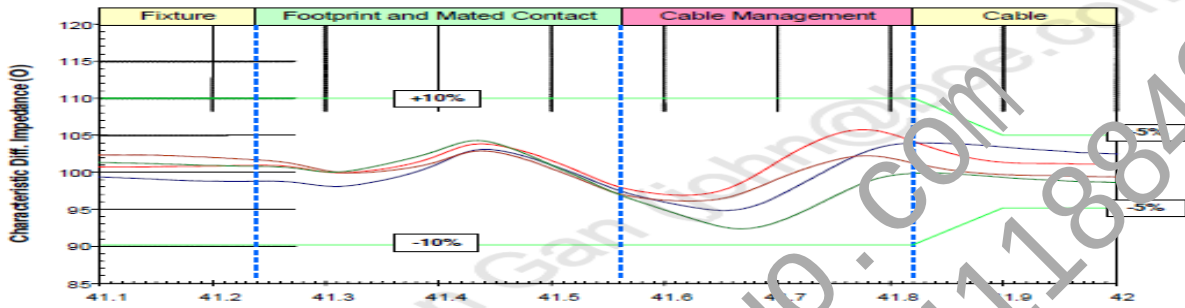
Eye for TP3 at RBR

Purpose

1. Main Link EYE Diagram should meet TP3 point of VESA.
2. The measure method is through access fixture.

Appendix C

Impedance Profile through a DP Connector



Differential Impedance Profile Measurement Data Example

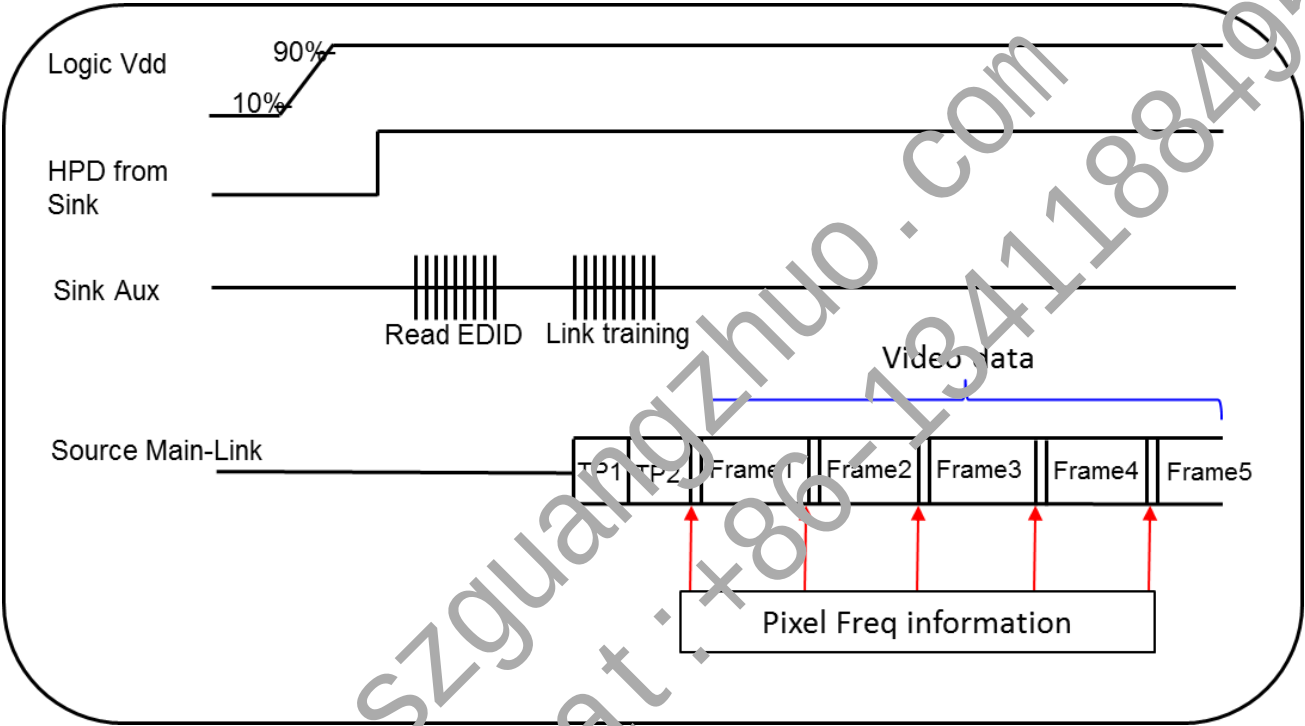
Segment	Differential Impedance Value	Maximum Tolerance
Fixture	100Ω/VESA	±10%
Connector	100Ω/VESA	±10%
Wire management	100Ω/VESA	±10%
Cable	100Ω/VESA	±5%

Impedance Profile Values for Cable Assembly

Purpose	Cable Impedance Profile 100ohm for Cable Assembly
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Appendix C

Main Link Pixel Freq information value of MSA data

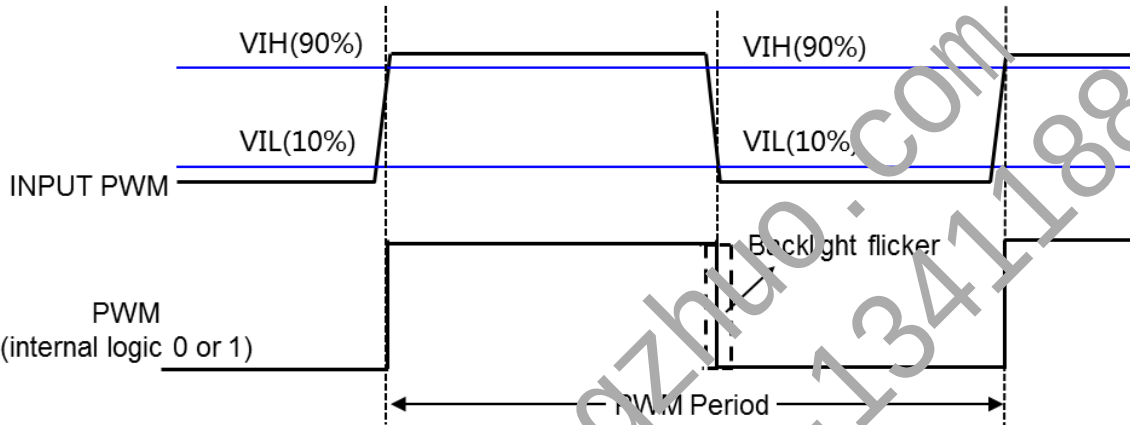


Purpose

- 1. It need to fix pixel freq information value of MSA data output to prevent the initial abnormal pixel freq information value from incoming after power on.
- 2. BOE can read DPCD to check this value. Ex: BIOS is 1.62G , but into windows is 2.7G.

Appendix C

Main Link Pixel Freq information value of MSA data



Example:

Freq	Cycle Time	PWM Rising Time	PWM Falling Time
200Hz	5ms	≤5us	≤1us
1KHz	1ms	≤200ns	≤200ns

Purpose

1. LED driver need to calculate the duty cycle of input PWM signal.
2. To avoid backlight flicker visible on LCD, system input PWM suggest :
PWM rising $\leq 200 \text{ ppm} \times \text{cycle time}$; PWM falling $\leq 200 \text{ ppm} \times \text{cycle time}$.