

TITLE : NE156FHM-NX1 V18.0

Customer: ASUS

Product Specification

Rev. P0

BOE Optoelectronics Technology Co., Ltd

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TFT-LCD P0 2021.03.08 1 OF 66

REVISION HISTORY

(√)Preliminary Specification
()Final Specification

Revision No.	Page	Description of Changes	Date	Prepared
P0	66	Preliminary Specification	2021.03.08	Li Qiang

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1.0 GENERAL DESCRIPTION

1.1 Introduction

NE156FHM-NX1 is a color active matrix TFT LCD module using Oxide TFT's (Thin Film Transistors) as an active switching devices. This module has a 15.6 inch diagonally measured active area with FHD resolutions (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical Stripe and this module can display 16.7M colors.In this TFT-LCD panel, color filters for excellent color performance is incorporated to realize brighter and clearer pictures, making this Module optimum for use in multi-media applications. All input signals are eDP interface compatible.

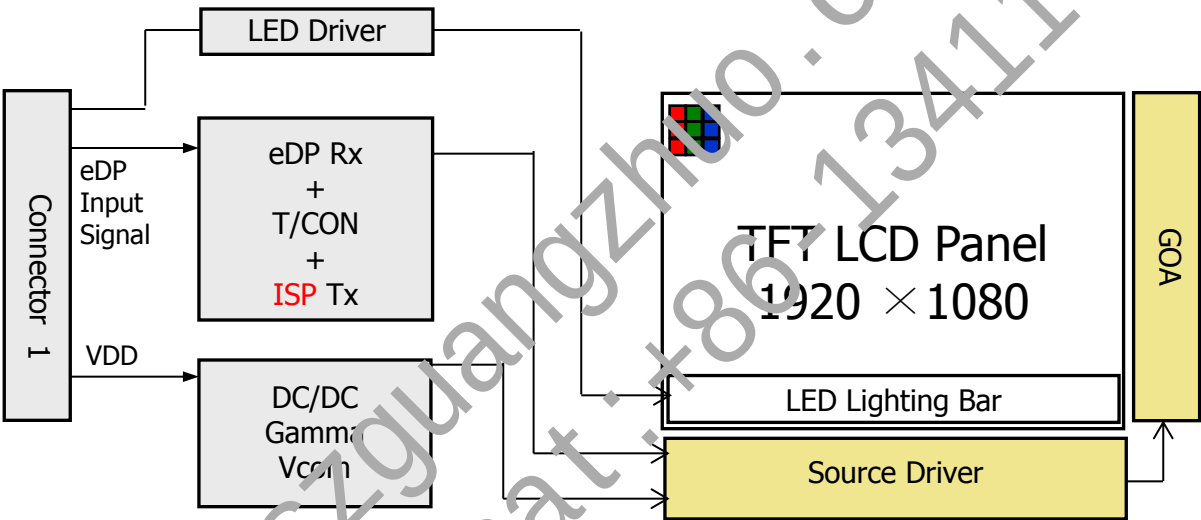


Figure 1. Drive Architecture

1.2 Features

- Frame rate support range: 144Hz;
- 4 lane eDP1.3 Interface with 2.7Gbps Link Rates
- 8-bit color depth, display 16.7M colors
- LED driving mode is DC driving mode
- Data enable signal mode
- Support PSR1/Static DRRS
- Green Product (RoHS & Halogen free product)
- On board LED Driving circuit
- Low driving voltage and low power consumption
- On board EDID chip

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1.3 Application

- Notebook PC (Wide type)

1.4 General Specification

The followings are general specifications at the model NE156FHM-NX1. (listed in Table 1)

<Table 1. General Specifications>

Parameter	Specification	Unit	Remarks
Active area	344.16 (H) × 193.59 (V)	mm	
Number of pixels	1920 (H) × 1080 (V)	pixels	
Pixel pitch	179.25(H) × 179.25(V)	um	
Pixel arrangement	RGB Vertical stripe		
Display colors	16.7M(6Bit+FRC)		
Color gamut	NTSC 45% (typ.)		
Display mode	Normally Black		
Dimensional outline	350.66 ± 0.3(H) * 216.245 ± 0.5(V)(W/O PCB)*3.2(Max) 350.66 ± 0.3(H)*216.245 ± 0.5(V) (W/PCB)*3.2(Max)	mm	
Weight	360(max)	g	
Surface treatment	Anti-Glare		
Surface hardness	3H		
Back-light	Bottom edge side, 1-LED lighting bar type		Note 1
Power consumption	P _D : 1.35(Max.)	W	@Mosaic
	P _{BL} : 3.25(Max.)	W	@VLED= 12V
	P _{Total} : 4.6(Max.)	W	@Mosaic

Notes : 1. LED Lighting Bar (45*LED Array)

2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Absolute Maximum Ratings>

Ta=25+/-2℃

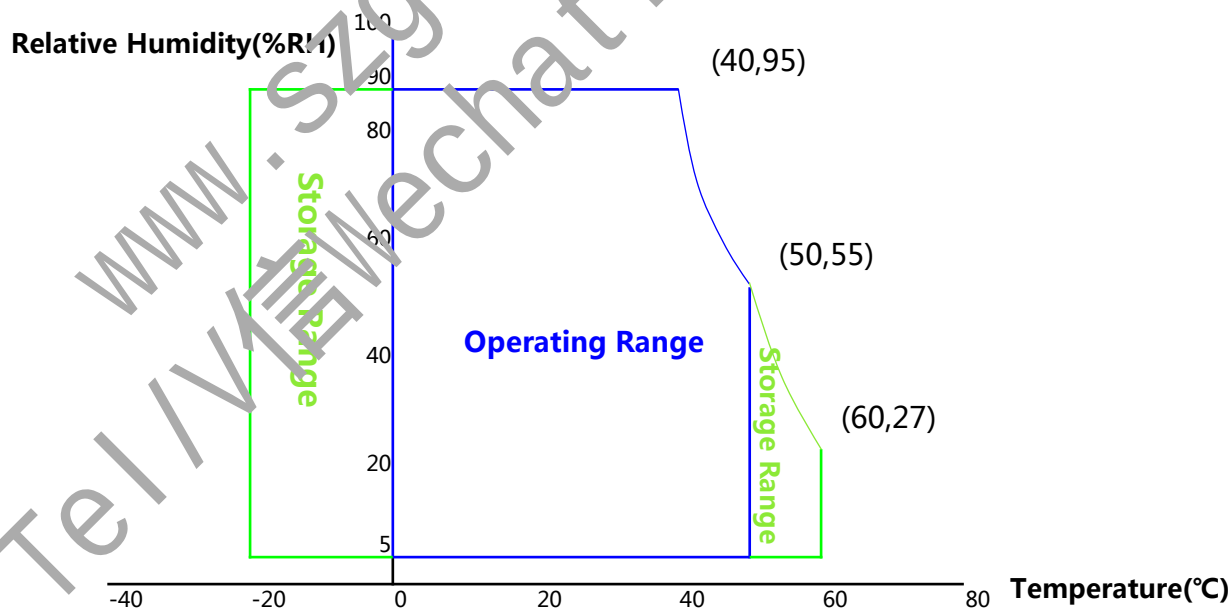
Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V _{DD}	-0.3	4.0	V	Note 1
eDP input Voltage	V _{eDP}	0	2.0	V	
Logic Supply Voltage	V _{IN}	V _{SS} -0.3	V _{DD} +0.3	V	
Operating Temperature	T _{OP}	0	+50	℃	Note 2
Storage Temperature	T _{ST}	-20	+60	℃	

Notes :

1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.

2. Temperature and relative humidity range are shown in the figure below.

95 % RH Max. (40 °C ≥ Ta) Maximum wet - bulb temperature at 39 °C or less. (Ta > 40 °C) No condensation.



3.0 ELECTRICAL SPECIFICATIONS

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3.1 Electrical Specifications

< Table 3. Electrical specifications >

[Ta = 25±2 °C]

Parameter		Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V _{DD}	3.0	3.3	3.6	V	Note 1
Permissible Input Ripple Voltage	V _{RF}	-	-	300	mV	At V _{DD} = 3.3V
Power Supply Current	I _{DD}	-	318		mA	Note 1
LX Current Limit	I _{LX}			2	A	
Positive-going Input Threshold Voltage	V _{IT+}	-		100	mV	V _{cm} = 1.2V typ.
Negative-going Input Threshold Voltage	V _{IT-}	-100	-	-	mV	
BIST Control Level	High Level	0.7*V _{DDIO}		-	V	@V _{DDIO} =2.5
	Low Level	-	-	0.25*V _{DDIO}	V	
Differential Input Voltage	V _{ID}	200	-	600	mV	
Power Consumption	P _D	-	1.05	1.35	W	Note 1
	P _{BL}	-		3.25	W	Note 2
	P _{total}	-		4.6	W	

Notes : 1. The supply voltage is measured and specified at the interface connector of LCM. The current draw and power consumption specified is for 3.3V at 25 °C by Mosaic pattern.

2. Calculated value for reference (VLED × ILED)

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3.2 Back-Light Unit

< Table 4. LED Driving guideline specifications >

[Ta = 25±2 °C]

Parameter		Min.	Typ.	Max.	Unit	Remarks
LED Forward Voltage	V_F	-	-	3	V	
LED Forward Current	I_F	-	20	-	mA	
LED Power Consumption	P_{LED}	-	-	3.25	W	
LED Life-Time	N/A	15,000	-	-	Hour	IF = 20mA
Power supply voltage for LED Driver	V_{LED}	5	12	21	V	
EN Control Level	Backlight on	1.2	-	VDD	V	
	Backlight off	0	-	0.6	V	
PWM Control Level	PWM High Level	1.75	-	VDD	V	
	PWM Low Level	0	-	0.625	V	
PWM Control Frequency	F_{PWM}	200	-	2000	Hz	
Duty Ratio	-	5	-	100	%	

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3.3 Pin assignment for LED Bar

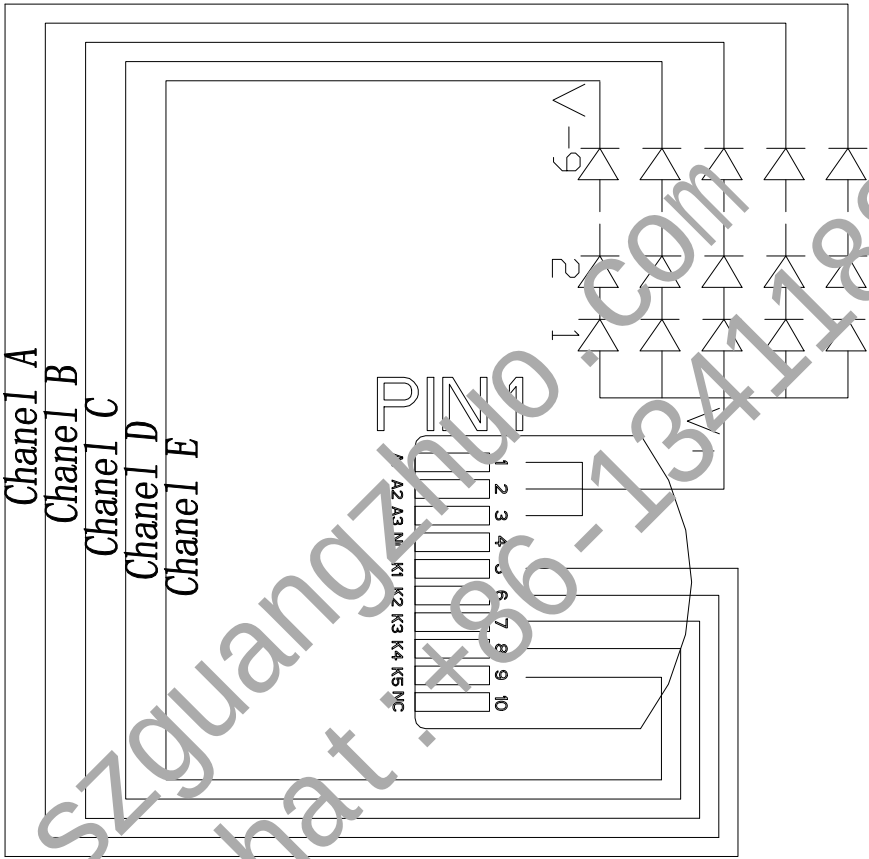
Connector : I-PEX 20542-010E-01 (I-PEX)

< Table5. Pin assignment for LED Bar >

Pin No	Symbol	Description	Remarks
1	VLED	LED Anode Power Supply	
2	VLED	LED Anode Power Supply	
3	VLED	LED Anode Power Supply	
4	NC	NC	
5	FB1	LED Cathode Power Supply	
6	FB2	LED Cathode Power Supply	
7	FB3	LED Cathode Power Supply	
8	FB4	LED Cathode Power Supply	
9	FB5	LED Cathode Power Supply	
10	FB6	LED Cathode Power Supply	

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3.3 LED Structure



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4.0 OPTICAL SPECIFICATION

4.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2℃) with the equipment of luminance meter system (PR730&PR810) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to θ=0 (=03) as the 3 o'clock direction (the “right”), θ=90 (=012) as the 12 o'clock direction (“upward”), θ=180 (=09) as the 9 o'clock direction (“left”) and θ=270(=06) as the 6 o'clock direction (“bottom”). While scanning θand/or Ø, the center of the measuring spot on the display surface shall stay fixed. The backlight should be operating for 30 minutes prior to the measurement. VDD shall be 3.3+/- 0.3V at 25℃. Optimum viewing angle direction is 0° clock.

4.2 Optical Specifications

<Table 5. Optical Specifications>

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ_3	CR > 10	80	85	-	Deg.	Note 1
		Θ_9		80	85	-	Deg.	
	Vertical	Θ_{12}		80	85	-	Deg.	
		Θ_6		80	85	-	Deg.	
Luminance Contrast Ratio		CR	$\Theta = 0^\circ$	960	200	-		Note 2
Luminance of White	5 Points	Y_w	$\Theta = 0^\circ$ ILED = 21mA	2125	250	-	cd/m ²	Note 3
White Luminance Uniformity	5 Points	ΔY_5		80	-	-	%	Note 4
	13 Points	ΔY_{13}	62.5	-	-	%		
White Chromaticity		W_x	$\Theta = 0^\circ$	0.283	0.313	0.343		Note 5
		W_y		0.299	0.329	0.359		
Reproduction of Color	Red	R_x	$\Theta = 0^\circ$	Typ.-0.03	0.595	Typ.+0.03		
		R_y			0.362			
	Green	G_x			0.346			
		G_y			0.555			
	Blue	B_x			0.158			
		B_y			0.107			
Color Gamut				35	45	-	%	DCI-P3 coverage
Response Time (Rising + Falling)		T_{RT}	Ta= 25°C $\Theta = 0^\circ$	-	25	30	ms	Note 6
GTF ave.		-	Ta= 25°C $\Theta = 0^\circ$	-	16	-	ms	OD on Note 8
Cross Talk		CT	$\Theta = 0^\circ$	-	-	2.0	%	Note 7
Gamma		-	-	2.0	2.2	2.4	-	

Notes :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 7).
2. Contrast measurements shall be made at viewing angle of $\Theta = 0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see Figure 7) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Center Luminance of white is defined as luminance values of 5 point average across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 8 for a total of the measurements per display.
4. The White luminance uniformity on LCD surface is then expressed as : $\Delta Y = \text{Minimum Luminance of 5(or 13) points} / \text{Maximum Luminance of 5(or 13) points.}$ (see Figure 8 and Figure 9).
5. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels, first in red, green, blue and white. Measurements shall be made at the center of the panel.
6. The electro-optical response time measurements shall be made as Figure 10 by switching the “data” input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_r , and 90% to 10% is T_f .
7. Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark. (See Figure 11).

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8. Response time 9*9 matrix

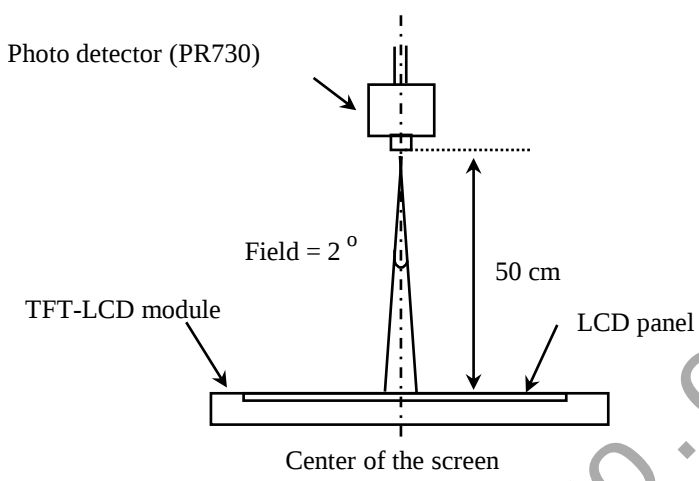
Response time 9*9 matrix

Response Time		To								
From		L0	L32	L64	L96	L128	L159	L191	L223	L255
	L0									
	L32									
	L64									
	L96									
	L128									
	L159									
	L191									
	L223									
	L255									

Response time (Tr + Tf) = L0 to L255 + L255 to L0

Response time (gray to gray) average = average time in 9*9 matrix

4.3 Optical Measurements



Optical characteristics measurement setup

Figure 7. Measurement Set Up

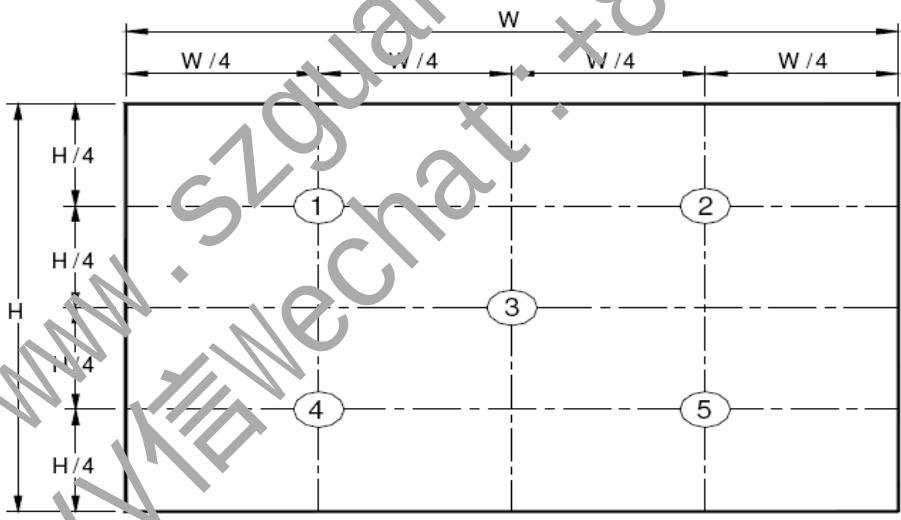


Figure 8. White Luminance and Uniformity Measurement Locations (5 points)

Center Luminance of white is defined as luminance values of center 5 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 7 for a total of the measurements per display.

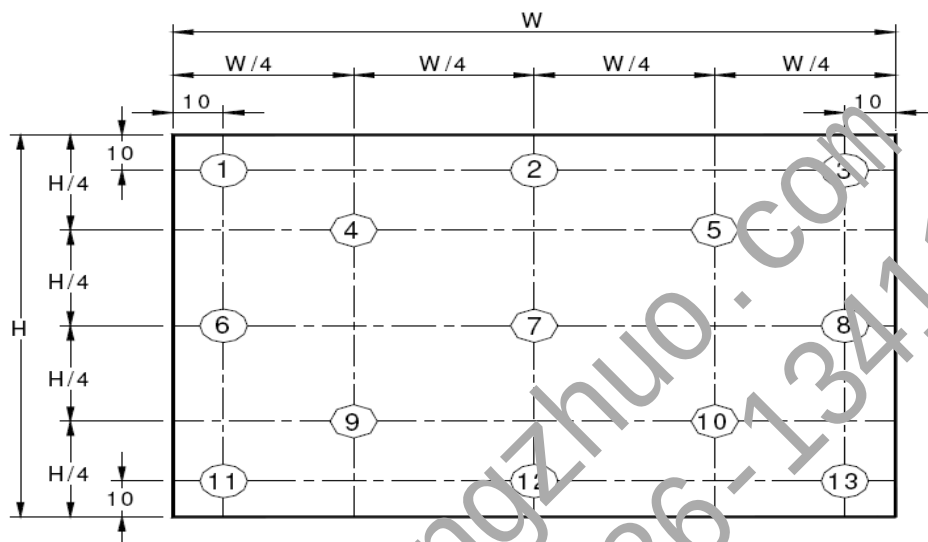


Figure 9. Uniformity Measurement Locations (13 points)

The White luminance uniformity on LCD surface is then expressed as : $\Delta Y5$ = Minimum Luminance of five points / Maximum Luminance of five points (see Figure 8) , $\Delta Y13$ = Minimum Luminance of 13 points / Maximum Luminance of 13 points (see Figure 9).

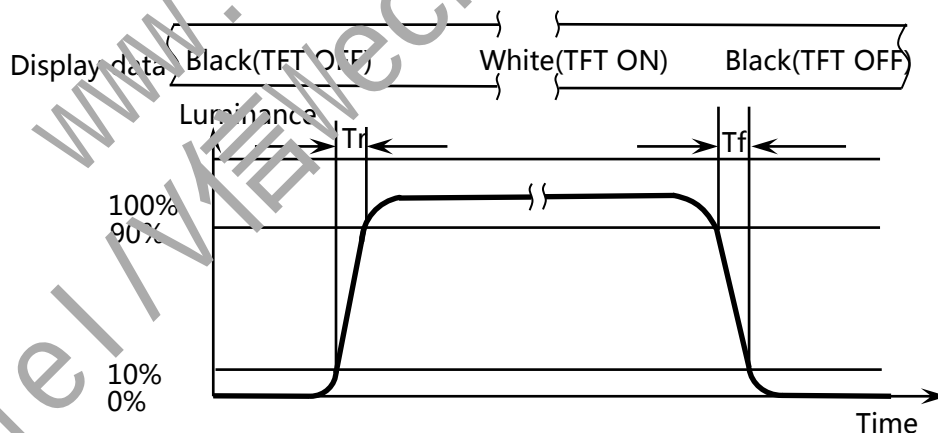
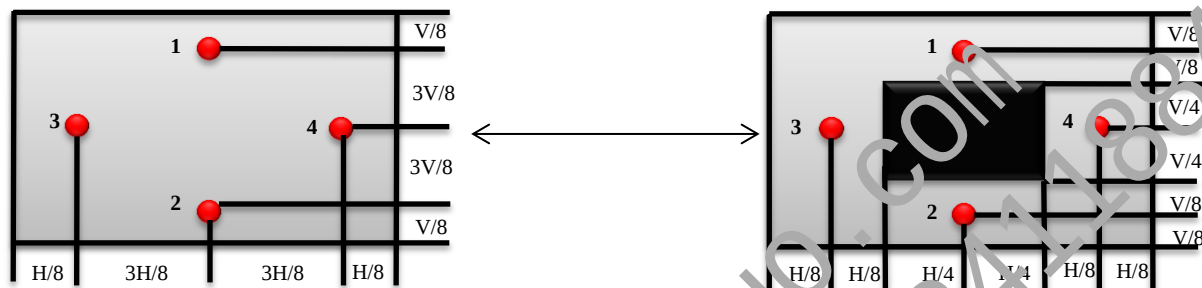


Figure 10. Response Time Testing

The electro-optical response time measurements shall be made as shown in Figure 10 by switching the “data” input signal ON and OFF. Tr: The luminance to change from 10% to 90% ,Tf: The luminance to change from 90% to 10% .

The test system : LMS PR810



$$\text{Cross Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_A} \right| \times 100$$

Figure 11. Cros. Talk Modulation Test Description

Where:

Y_A = Initial luminance of measured area (cd/m²)

Y_B = Subsequent luminance of measured area (cd/m²)

The location 1/2/3/4 measured will be exactly the same in both patterns. The test background gray is from L64 to L192.Take the largest data as the result.

Cross Talk on one area of the LCD surface by another shall be measured by comparing the luminance (Y_A) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (Y_B) of that same area when any adjacent area is driven dark.(Refer to Figure 11)

The test system: PR730

5.0 INTERFACE CONNECTION.

5.1 Electrical Interface Connection

The connector interface pin assignments are listed in Table 7.

<Table 7. Pin Assignments for the Interface Connector>

Terminal	Symbol	Function	Remark
PIN No.	Symbol		
1	NC	Reserved for LCD for manufacturer's use	Note2
2	H_GND	High Speed Ground	Note1
3	Lane3_N	Complement Signal Link Lane 3	
4	Lane3_P	True Signal Link Lane 3	
5	H_GND	High Speed Ground	
6	Lane2_N	Complement Signal Link Lane 2	
7	Lane2_P	True Signal Link Lane 2	
8	H_GND	High Speed Ground	
9	Lane1_N	Complement Signal Link Lane 1	
10	Lane1_P	True Signal Link Lane 1	
11	H_GND	High Speed Ground	
12	Lane0_N	Complement Signal Link Lane 0	
13	Lane0_P	True Signal Link Lane 0	
14	H_GND	High Speed Ground	
15	AUX_CH_P	True Signal Auxiliary Channel	
16	AUX_CH_N	Complement Signal Auxiliary Channel	
17	H_GND	High Speed Ground	
18	LCD_VCC	LCD logic and driver power(3.3V)	
19	LCD_VCC	LCD logic and driver power(3.3V)	
20	LCD_VCC	LCD logic and driver power(3.3V)	
21	LCD_VCC	LCD logic and driver power(3.3V)	
22	BIST	BIST PIN	
23	LCD_GND	LCD logic and driver ground	
24	LCD_GND	LCD logic and driver ground	
25	LCD_GND	LCD logic and driver ground	
26	LCD_GND	LCD logic and driver ground	
27	HPD	HPD Signal	Note3
28	BL_GND	Backlight ground	
29	BL_GND	Backlight ground	

30	BL_GND	Backlight ground	
31	BL_GND	Backlight ground	
32	BL_ENABLE	Backlight on/off	Note4
33	BL_PWM_DIM	System PWM	Note5
34	NC	Reserved for LCD for manufacturer's use	Note2
35	NC	Reserved for LCD for manufacturer's use	
36	BL_PWR	Backlight power	
37	BL_PWR	Backlight power	
38	BL_PWR	Backlight power	
39	BL_PWR	Backlight power	
40	NC	NC	

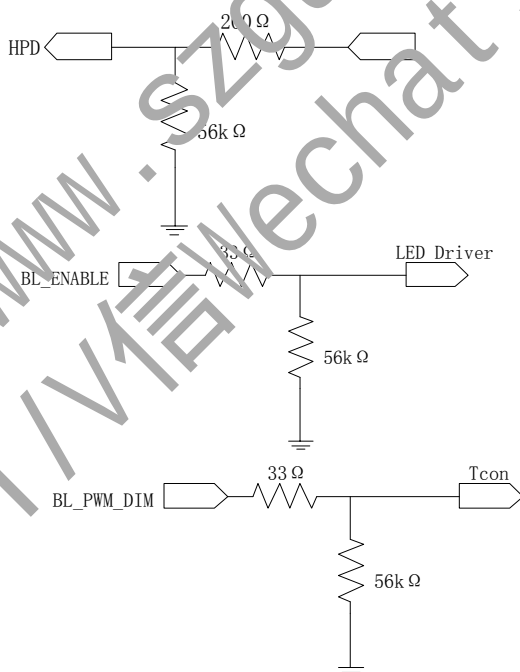
Note : 1. The shielding case is connected with signal GND.

Connector used :20455-040E-76 (I-PEX)

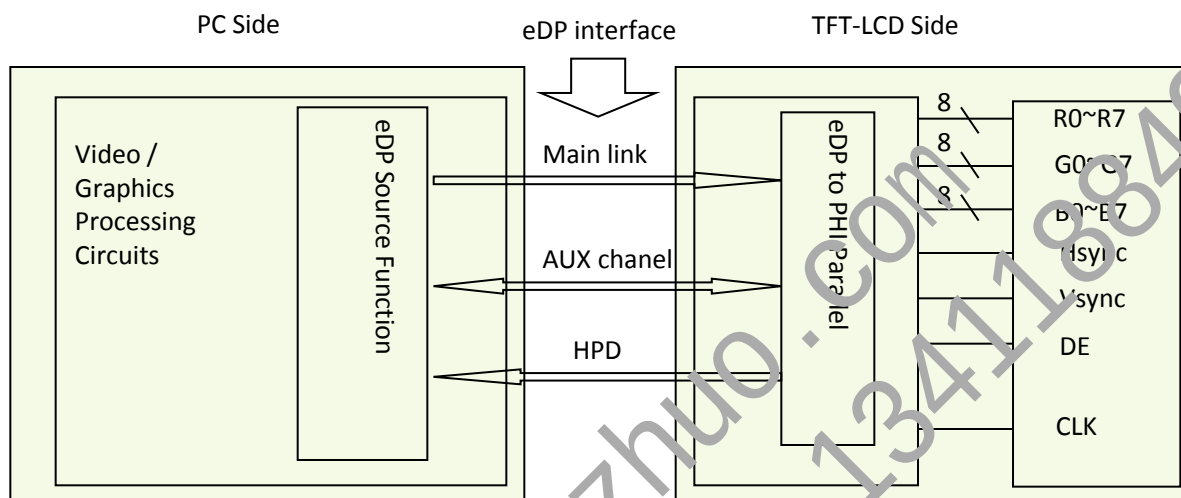
Corresponding connector :20455-040T (I-PEX)

2.Don't input any signals or any powers into a NC pin. Keep the NC pin open.

3. The equivalent circuit figure of the terminal.



5.2. eDP Interface



5.3.eDP Input signal

Lane 0	Lane 1	Lane 2	Lane 3
R0-7:0	R1-7:0	R2-7:0	R3-7:0
G0-7:0	G1-7:0	G2-7:0	G3-7:0
B0-7:0	B1-7:0	B2-7:0	B3-7:0
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-7:0	G5-7:0	G6-7:0	G7-7:0
B4-7:0	B5-7:0	B6-7:0	B7-7:0
R8-7:0	R9-7:0	R10-7:0	R11-7:0
G8-7:0	G9-7:0	G10-7:0	G11-7:0
B8-7:0	B9-7:0	B10-7:0	B11-7:0

6.0 SIGNAL TIMING SPECIFICATION

6.1 Timing Parameters

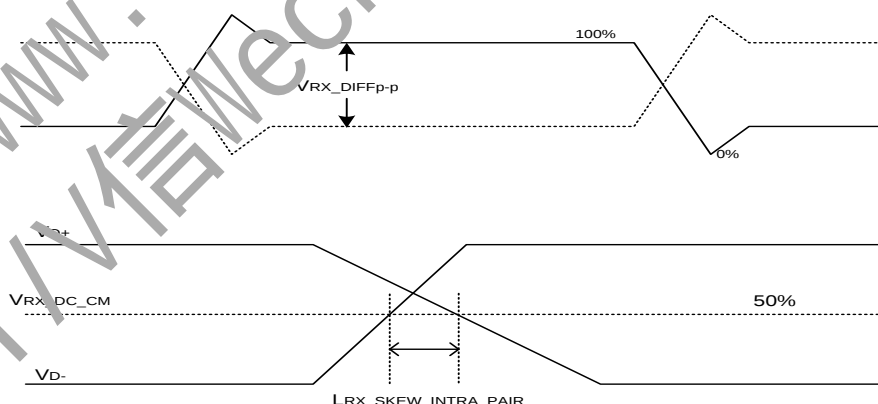
Item	Min	Typ	Max	Unit
Pixel clk	147.81	354.73		M
H effective time	1920	1920	1920	
H blank time	220	260	480	
H total time	2140	2180	2300	
V effective time	1080	1080	1080	
V blank time	20	50	2260	
V total time	1100	1130	3340	

6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 8.

<Table 9. eDP Rx Interface Timing Specification>

Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock	SSC	-	-	0.5	%	
Differential peak-to-peak input voltage at package pins	VRX-DIFFp-p	90	-	1200	mV	
Rx input DC common mode voltage	VRX_DC_CM	-	GND	-	V	
Differential termination resistance	RRX-DIFF	-	100	-	Ω	
Single-ended termination resistance	RRX-SE	40	-	60	Ω	
Rx short circuit current limit	IRX_SHORT	-	-	50	mA	
Intra-pair skew at Rx package pins (HBR) RX intra-pair skew tolerance at HBR	LRX_SKEW_INTRA_PAIR	-	-	50	ps	



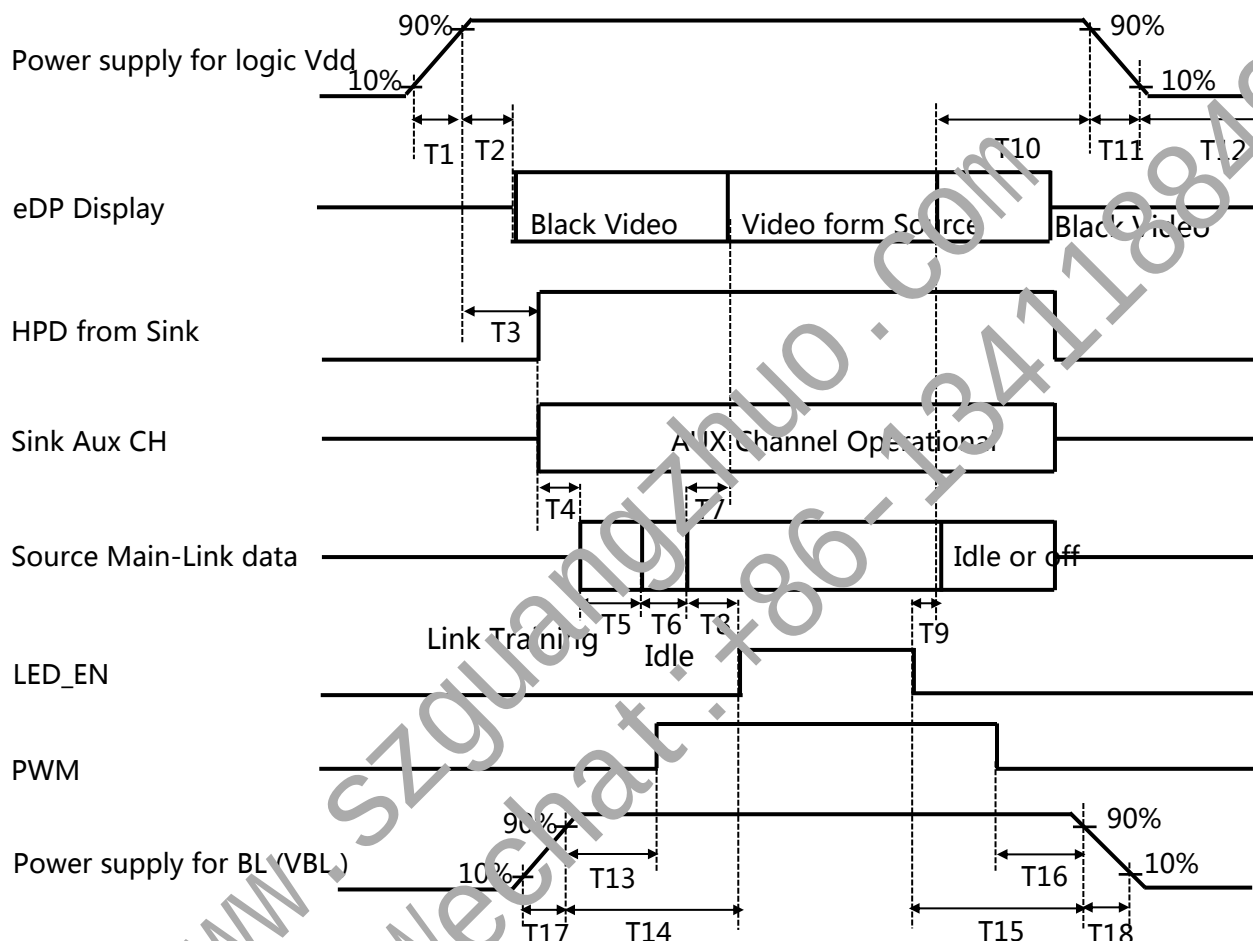
7.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

	Colors & Gray scale	Data signal																											
		R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7				
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	
	Light Blue	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Purple	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	△	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Darker	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	△	↑								↑								↑											
	▽	↓								↓								↓											
	Brighter	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	▽	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Gray scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	△	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Darker	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	△	↑								↑								↑											
	▽	↓								↓								↓											
	Brighter	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	
	▽	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	
Gray scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	
	△	↑								↑								↑											
	▽	↓								↓								↓											
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	
Gray scale of White & Black	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	△	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	
	Darker	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	
	△	↑								↑								↑											
	▽	↓								↓								↓											
	Brighter	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	
	▽	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

8.0 POWER SEQUENCE

23

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below



- $0.5\text{ms} \leq T1 \leq 10\text{ms}$
- $0\text{ms} \leq T2 \leq 200\text{ms}$
- $0\text{ms} \leq T3 \leq 250\text{ms}$
- $0\text{ms} \leq T13 \leq 10\text{ms}$
- $0.5\text{ms} \leq T14 \leq 10\text{ms}$
- $0\text{ms} \leq T17 \leq 100\text{ms}$
- $0\text{ms} \leq T21 \leq 100\text{ms}$
- $0\text{ms} \leq T7 \leq 50\text{ms}$
- $0\text{ms} \leq T10 \leq 500\text{ms}$
- $1\text{ms} \leq T11 \leq 10\text{ms}$
- $500\text{ms} \leq T12 \leq 100\text{ms}$
- $100\text{ms} \leq T15 \leq 100\text{ms}$
- $0\text{ms} \leq T16 \leq 100\text{ms}$
- $0.1\text{ms} \leq T20 \leq 100\text{ms}$

Notes:

1. As for the power off sequence for VDD (t11), be sure to keep above mentioned timing. If the VDD power off sequence timing is other than shown above, LCD may cause permanent damage.

2. As for the power sequence for backlight, it is recommended to apply above mentioned input timing.

9.0 Connector Description

Physical interface is described as for the connector on LCM.

These connectors are capable of accommodating the following signals and will be following components.

9.1 TFT LCD Module

Connector Name /Description	For Signal Connector
Manufacturer	I-PEX
Mating housing/ Part Number	20455-040E-76 (I-PEX)

	www.szguangzhuo.com 广卓液晶屏 echodeng61@hotmail.com jimei@jimeihk.com +86-13411884959	PRODUCT GROUP	REV	ISSUE DATE
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10.0 MECHANICAL CHARACTERISTICS

10.1 Dimensional Requirements

Figure 23 shows mechanical outlines for the model NE160QAM-NX1.
Other parameters are shown in Table 14.

<Table 14. Dimensional Parameters>

Parameter	Specification	Unit
Active Area	344.6784 (H) × 215.424 (V)	mm
Number of pixels	3840 (H) X 2400 (V) (1 pixel = R + G + B dots)	pixels
Pixel pitch	89.76(H) × 89.76 (V)	um
Pixel arrangement	RGB Vertical stripe	
Display colors	16 TM (6bit+FRC)	
Display mode	Normally Black	
Dimensional outline	350.66±0.3(H)*216.245±0.5(V) (W/O PCB)*3.2(Max) 350.66±0.3(H)*216.245±0.5(V) (W/PCB)*3.2(Max)	mm
Weight	360 (max)	g

10.2 Mounting

See Figure 24.

10.3 Anti-Glare and Polarizer Hardness

The surface of the LCD has an Anti-Glare coating to minimize reflection and a 3H hardness coating to reduce scratching.

10.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 350lux.

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11.0 RELIABILITY TEST

The reliability test items and its conditions are shown in below.

<Table 15. Reliability Test>

No	Test Items	Conditions	Remark
1	High temperature storage test	Ta = 60°C , 240 hrs	
2	Low temperature storage test	Ta = -20°C , 240 hrs	
3	High temperature & high humidity operation test	Ta = 50°C , 80%RH, 240 hrs	
4	High temperature operation test	Ta = 50°C , 240 hrs	
5	Low temperature operation test	Ta = 0°C , 240 hrs	
6	Thermal shock	Ta = -20 °C(0.5 hr). ↔ 60 °C (0.5 hr), 100 cycles	
7	Vibration test (non-operating)	Ta = 25°C , 60%RH, 1.5G, 10~500Hz, Sine wave, 30min/cycle, 1cycle for each X,Y,Z	Note 1
8	Shock test (non-operating)	Ta = 25°C , 60%RH, 220G, Half Sine Wave 2msec ± X, ± Y, ± Z Once for each direction	Note 1
9	Electro-static discharge test (operating)	Air : 150 pF, 330Ω, ± 15 KV Contact : 150 pF, 330Ω, ± 8 KV Ta = 25°C , 60%RH,	Note 2

Notes :

1. The fixture must be hard enough , so that the module would not be twisted or bent.
2. Self- recovery and restart recovery is allowed. No hardware failures.

12.0 HANDLING & CAUTIONS

(1) Cautions when taking out the module

- Pick the pouch only, when taking out module from a shipping package.

(2) Cautions for handling the module

- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation

- When the module is operating, do not lose CLK, ENA/B signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

(4) Cautions for the atmosphere

- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristic

- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions

- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc. Please pack the module not to be broken. We recommend to use the original shipping packages.

13.0 LABEL

(1) Product Label

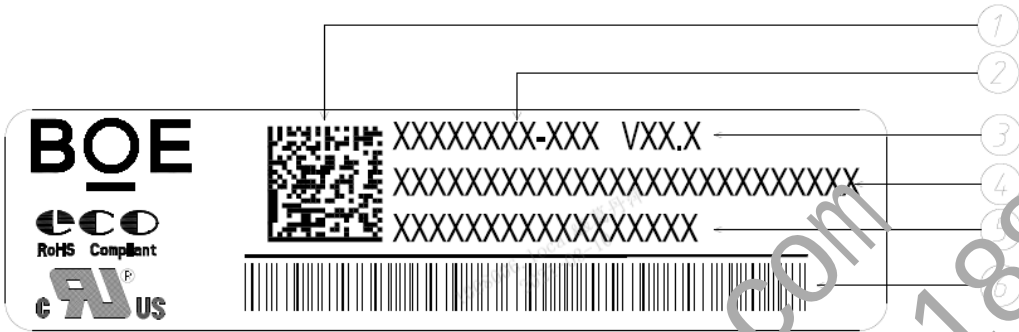


Figure 20. Product Label

Serial number marked part needs to print, show as follows:

1. ASUS Gamming ID (2D barcode)
2. FG-CODE (Before 12 bit)
3. Version
4. ASUS Gamming ID
5. Module ID
6. Module ID barcode

Module ID Naming Rule:

<Table 16. Module ID Naming Rule>

Digit Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Code	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Description	Product Name		Product Grade	Facility Code	Year		Month	Model Extension Code (Last 4 Digits FG Code)				Serial NO.					

(2) Box label

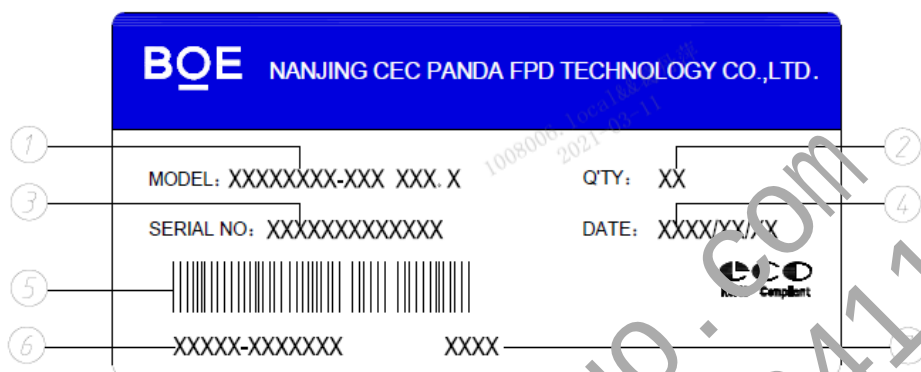


Figure 22. Box Label

Serial number marked part needs to print, show as follow:

1. FG-CODE (Before 12 bit)
 2. Product Quantity (XX pc/ Carton)
 3. BOX ID
 4. Date of Packing
 5. Barcode (Box ID)
 6. Customer NO.
 7. FG-Code After four
- Total Size: 80*60mm

Box ID Naming Rule:

<Table 17. Box Label Naming Rule >

Digit Code	1	2	3	4	5	6	7	8	9	10	11	12	13
Code	X	X	X	X	X	X	X	X	X	X	X	X	X
Description	Product Name		Product Grade	Facility Code	Year		Month	Revision	Box Serial NO.				

BOE	www.szguangzhuo.com 广卓液晶屏 echodeng61@hotmail.com jimei@jimeihk.com +86-13411884959	PRODUCT GROUP	REV	ISSUE DATE
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14.0 PACKING INFORMATION

14.1 Packing Order

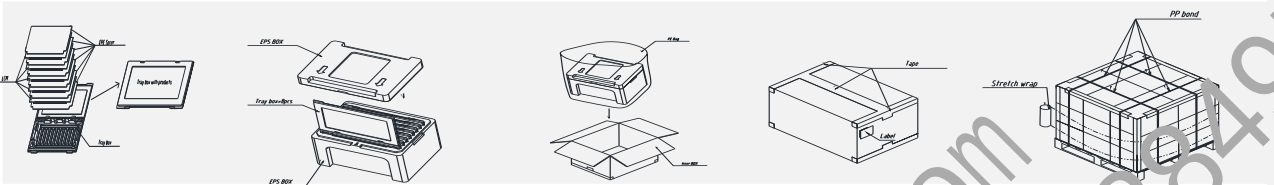


Figure 23. Packing Order

- Put 1pcs EPE Spacer, 1pcs LCM, 1pcs EPE Spacer ... Totally 5pcs LCM and 6 pcs EPE Spacer in one Tray box.
Capacity:5pcs LCM/Tray box, 6pcs EPE Spacer/Tray Box;
- Put the tray box in EPS Box. Totally 8 pcs Tray box/ EPS Box.
Capacity:40pcs LCM/EPS box, 8pcs Tray box/ EPS box;
- Put 1pcs EPS box in the PE Bag and put it in the inner box together.
Capacity: 8pcs Tray box/PE bag, 1pcs PE bag/ Inner box;
- Use Packing Tape to Seal inner box, Stick the box label onto inner box and align it to the label mark.
- Put 18 Inner box on the Pallet, Secure with strapping tape, wrap around film, paper protection Angle.
Capacity:6 Inner box/Layer, 3Layer, 720pcs LCM/Pallet

14.2 Note

- Box dimension: 485mm*375mm*345mm
- Package quantity in one box: 40pcs
- Total weight: (18.65 ±10% kg/Box (Typ)

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15.0 MECHANICAL OUTLINE DIMENSION

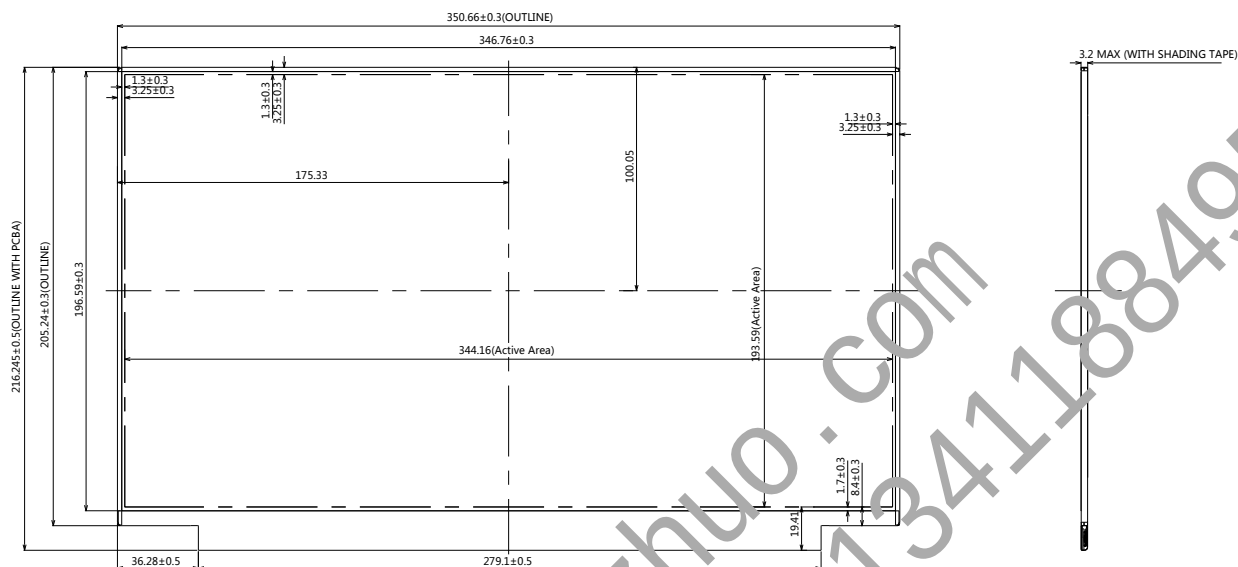


Figure 24. T1 T-LCD Module Outline Dimension (Front View)

Notes:

1. Warpage and deformation Spec.: 0.5mm Max..
2. The eDP connector is measured at PIN 1 and mating line.
3. Top polarizer is the highest portion.
4. Do not have light leakage on four corners of module.
5. Measurement method refer to Appendix A
6. System matching refer to Appendix B
7. “()”marks the reference dimensions.

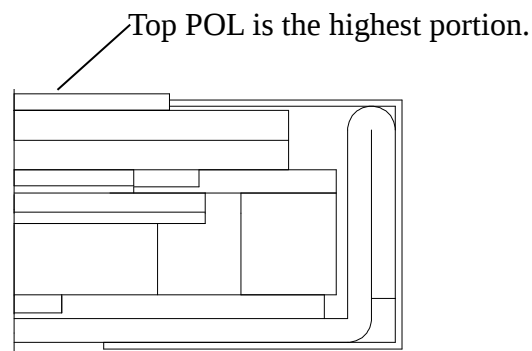


Figure 25. Highest Point Position

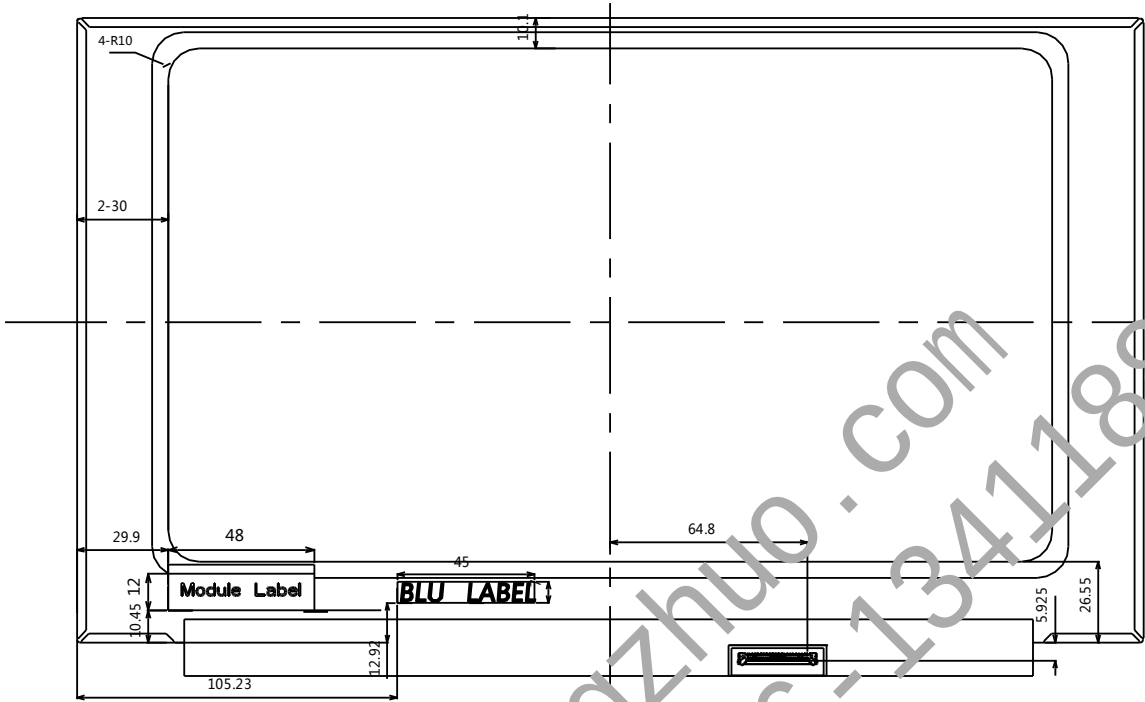


Figure 26. TFT-LCD Module Outline Dimensions (Rear view)

- Notes:
- 1. Warpage and deformation Spec.: 0.5mm Max.
 - 2. The eDP connector is measured at PIN 1 and mating line.
 - 3. Top polarizer is the highest portion.
 - 4. Do not have light leakage on four corners of module.
 - 5. Measurement method refer to Appendix A
 - 6. System matching refer to Appendix B
 - 7. “()”marks the reference dimensions.

16.0 EDID Table

Byte	Byte	Field Name and Comments	Value	Value
(decimal)	(hex)		(hex)	(binary)
0	00	Header	00	00000000
1	01	Header	FF	11111111
2	02	Header	FF	11111111
3	03	Header	FF	11111111
4	04	Header	FF	11111111
5	05	Header	FF	11111111
6	06	Header	FF	11111111
7	07	Header	00	00000000
8	08	EISA manufacture code =NCP	30	00111000
9	09	EISA manufacture code (Compressed ASCII)	70	01110000
10	0A	Product code (LM156LF2F: 77)	4D	01001011
11	0B	Product code (hex,LSB first)	00	00000000
12	0C	LCD Serial No (fixed "0")	00	00000000
13	0D	LCD No (fixed "0")	00	00000000
14	0E	LCD No (fixed "0")	00	00000000
15	0F	LCD No (fixed "0")	00	00000000
16	10	Week of manufacture	33	00110011
17	11	Year of manufacture - 1990 (ex: 2000 - 1990 =10) 2021-1990 = 31	1F	00011111
18	12	EDID structure version # = 1	01	00000001
19	13	EDID revision # = 1	04	00000100
20	14	Video i/p definition = Digital 8bit DFP support	A5	10100101
21	15	Max H image size(cm) = 34cm	22	00100010
22	16	Max V image size(cm) = 19cm	13	00010011
23	17	Display gamma (2.2×100) = 100 = 120	78	01111000
24	18	Feature support(stanby,suspend,RGB color/Prefer Time)	03	00000011
25	19	Red/Green Low bit (Rr/Ry/GxGy)	68	01101000
26	1A	Blue/White Low bit (Bx/By/WxWy)	50	01010000
27	1E	Red X(Rx) (written value 0.595)	98	10011000
28	1C	Red Y(Ry) (written value 0.362)	5C	01011100
29	1D	Green X(Gx) (written value 0.346)	58	01011000
30	1E	Green Y(Gy) (written value 0.555)	8E	10001110
31	1F	Blue X(Bx) (written value 0.158)	28	00101000
32	20	Blue Y(By) (written value 0.107)	1B	00011011
33	21	White X(Wx) (written value 0.313)	50	01010000
34	22	White Y(Wy) (written value 0.329)	54	01010100

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16.0 EDID Table

35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Established timings 3(Manufacture's reserved timing)	00	00000000
38	26	Standard timing ID1	01	00000001
39	27	Standard timing ID1	01	00000001
40	28	Standard timing ID2	01	00000001
41	29	Standard timing ID2	01	00000001
42	2A	Standard timing ID3	01	00000001
43	2B	Standard timing ID3	01	00000001
44	2C	Standard timing ID4	01	00000001
45	2D	Standard timing ID4	01	00000001
46	2E	Standard timing ID5	01	00000001
47	2F	Standard timing ID5	01	00000001
48	30	Standard timing ID6	01	00000001
49	31	Standard timing ID6	01	00000001
50	32	Standard timing ID7	01	00000001
51	33	Standard timing ID7	01	00000001
52	34	Standard timing ID8	01	00000001
53	35	Standard timing ID8	01	00000001
54	36	Detailed timing descriptor #1 fck/10000 (=354.73MHz)	91	10010001
55	37	#1 fck	8A	10001010
56	38	#1 Horizontal active 920=780h 80v	80	10000000
57	39	#1 Horizontal blanking 260=104h 04h	04	00000100
58	3A	#1 Horizontal active/Horizontal blanking 71h	71	01110001
59	3B	#1 Vertical active 1080=430h 38h	38	00111000
60	3C	#1 Vertical blanking 50=32h	32	00110010
61	3D	#1 Vertical active/Vertical blanking 40h	40	01000000
62	3E	#1 Horizontal sync , offset(Thfp)48=030h 30h	30	00110000
63	3F	#1 Horizontal sync , width 32=020h 20h	20	00100000
64	40	#1 Vertical sync,offset / Vertical sync,width (offset=3h/width=5h)	35	00110101
65	41	#1 Horizontal sync offset/width/Vertical sync offset/width	00	00000000
66	42	#1 Horizontal image size 344.16mm=158h 58h	58	01011000
67	43	#1 Vertical image size 193.59mm=0C2h C2h	C2	11000010
68	44	#1 Horizontal image size / Vertical image size 10h	10	00010000

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16.0 EDID Table

69	45	Horizontal boarder	00	00000000
70	46	Vertical boarder	00	00000000
71	47	Flags(Non-interlaced=0/non 3D=00/Digital separate=11/Vsync polarity /Hsyncpolarity=01/Reserved For Stereo Mode=0)	1A	00011010
72	48	#2 Main Clock=147.81MHz	BD	10111101
73	49	#2 fck	39	00111001
74	4A	#2 Horizontal active 1920=780h 80h	80	10000000
75	4B	#2 Horizontal blanking 260=104h 04h	04	00001000
76	4C	#2 Horizontal active/Horizontal blanking 71h	71	00111001
77	4D	#2 Vertical active 1080=438h 38h	38	00111000
78	4E	#2 Vertical blanking 50=32h	32	00110010
79	4F	#2 Vertical active/Vertical blanking 40h	40	01000000
80	50	#2 Horizontal sync , offset(Thfp) =30	30	00110000
81	51	#2 Horizontal sync , width=48	20	00100000
82	52	#2 Vertical sync, offset / Vertical sync, width (offset=3h/width=5h)	35	00110101
83	53	#2 Horizontal sync offset/width/Vertical sync offset/width	00	00000000
84	54	#2 Horizontal image size 344.16mm=158h 58h	58	01011000
85	55	#2 Vertical image size 193.59mm=0C2h 02h	C2	11000010
86	56	#2 Horizontal image size / Vertical image size 10h	10	00010000
87	57	Horizontal boarder	00	00000000
88	58	Vertical boarder	00	00000000
89	59	Flags(Non-interlaced=0/non 3D=00/Digital separate=11/Vsync polarity/Hsyncpolarity=01/Reserved For Stereo Mode=0)	1A	00011010
90	5A	Flag	00	00000000
91	5B	Flag	00	00000000
92	5C	Flag	00	00000000
93	5D	Date Type Tag: Alphanumeric Date String(ASCII)	FD	11111101
94	5E	Flag	00	00000000
95	5F	Extension flag	30	00110000
96	60	Extension flag	90	10010000
97	61	Extension flag	A3	10100011
98	62	Extension flag	A3	10100011
99	63	Extension flag	23	00100011
100	64	Extension flag	01	00000001
101	65	Extension flag	0A	00001010
102	66	Flag	20	00100000

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16.0 EDID Table

103	67	Flag	20	00100000
104	68	Flag	20	00100000
105	69	Flag	20	00100000
106	6A	Flag	20	00100000
107	6B	Flag	20	00100000
108	6C	Flag	00	00000000
109	6D	Flag	00	00000000
110	6E	Flag	00	00000000
111	6F	Data Type Tag: Manufacturer Specified Data 00	FE	11111110
112	70	Flag	00	00000000
113	71	Manufacturer PN 1st Character(N)	4E	01001110
114	72	Manufacturer PN 2nd Character(E)	45	01000101
115	73	Manufacturer PN 3rd Character(1)	31	00110001
116	74	Manufacturer PN 4th Character(5)	35	00110101
117	75	Manufacturer PN 5th Character(6)	36	00110110
118	76	Manufacturer Name 6th Character(F)	46	01000110
119	77	Manufacturer Name 7th Character(F)	48	01001000
120	78	Manufacturer Name 8th Character(M)	4D	01001101
121	79	Manufacturer Name 9th Character(-)	2D	00101101
122	7A	Manufacturer Name 10th Character(N)	4E	01001110
123	7B	Manufacturer Name 11th Character(X)	58	01011000
124	7C	Manufacturer Name 12th Character(1)	31	00110001
125	7D	Flag	0A	00001010
126	7E	Extension flag	00	00000000
127	7F	Checksum	F4	11110100

17.0 GENERAL PRECAUTIONS

17.1 HANDLING

- (1) When the module is assembled, It should be attached to the system firmly using every mounting holes.
Be careful not to twist or bend the modules.
- (2) Refrain from strong mechanical shock or any force to the module. Otherwise, it may cause improper operation or damage to the module.
- (3) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than 1 HB pencil lead.
- (4) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.
- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth .In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static , it may cause damage to the module.
- (9) Use fingerstalls with soft gloves to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Do not pull or fold the LED FPC.
- (12) Do not touch any component which is located on the back side.
- (13) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (14) Pins of connector shall not be touched directly with bare hands.

17.2 STORAGE

- (1) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃ and relative humidity of less than 70%.
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.

17.3 OPERATION

- (1) Do not connect, disconnect the module in the “ Power On” condition.
- (2) Power supply should always be turned on/off by following item 8.0 “ Power on/off sequence “.
- (3) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
- (4) The standard limited warranty is only applicable when the module is used for general notebook applications. If used for purposes other than as specified, BOE is not to be held reliable for the defective operations. It is strongly recommended to contact BOE to find out fitness for a particular purpose.

17.4 OTHERS

- (1) Avoid condensation of water. It may result in improper operation or disconnection of electrode.
- (2) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation, Variation in part contents and environmental temperature, etc.). Otherwise the module may be damaged.
- (3) If the module displays the same pattern continuously for a long period of time, it can be the situation when The “ image sticks” to the screen.
- (4) This module has its circuitry PCB's on the rear or bottom side and should be handled carefully to avoid being stressed.

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Appendix A

The Measurement Methods for the Dimensions of Module

Caliper:

- a. Length of Outline
- b. Width of Outline (Without/With PCB)
- c. Thickness of Outline (Without/ With PCB)

Coordinate Measuring Machine:

- CF Polarizer Size
- Active Area Size
- Active Area to Outline (Without Tape Wrinkle or Bulged)
- Active Area to CF Polarizer
- The Distance of Bracket Holes
- P-Cover to Outline (Without Tape Wrinkle or Bulged)
- Length of P-Cover
- Connector Pin 1 to Outline (Without Tape Wrinkle or Bulged)

Height Gauge: The Different Height of Root and Top on the Bracket
(Need to Calculate From Bracket Angle Spec.)

Feeler Gauge: The Warpage Spec. of Module

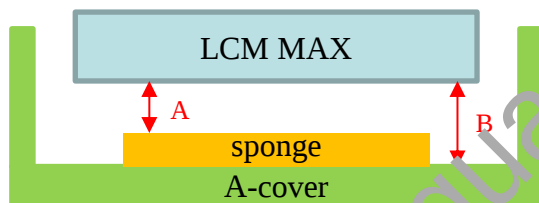
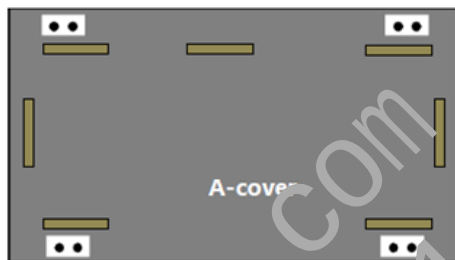
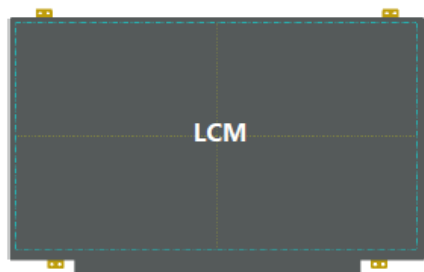
Notes:

Except the Critical Dimensions as Above, Other Dimensions are Measured by Coordinate Measuring Machine If Necessary.

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Appendix B

LCM to A-Cover / sponges z-gap



	Plastic Cover (LCM Thickness: Max)	Metal Cover (LCM Thickness: Max)
A	>0mm	>0mm
B	Min: 1.0mm	Min: 0.8mm
Without the open area of back cover		

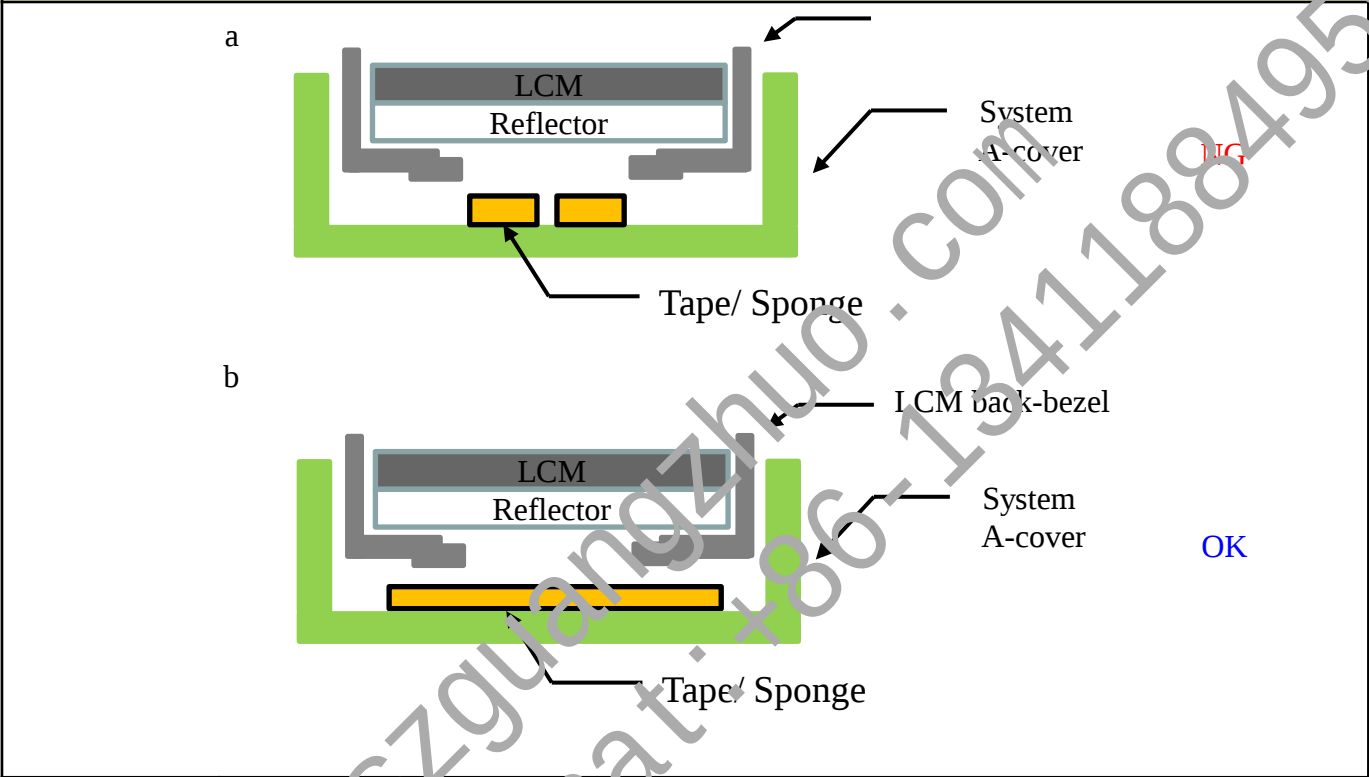
Purpose

The reflector area is very sensitive, we suggest that design enough z-gap to decrease the risk of water upple, white spot and other abnormal display

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Appendix B

LCM to A-Cover / sponges z-gap



Purpose	If attach sponges or rubbers which correspond to white reflector area, it may cause white spot, pooling or other relate issues. We suggest that attach wide range sponges / rubbers which can cover the LCM back-bezel opening
---------	---

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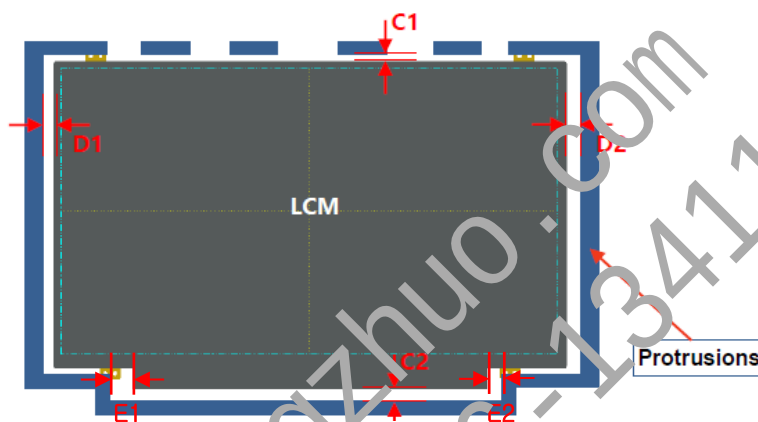
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Appendix B

LCM to side wall / protrusions



	Normal border	Narrow border
D1/D2	Min: 0.45mm	Min: 0.35mm
C1	Min: 0.50mm	
C2	Min: 0.50mm	
E1/E2	Min: 0.55mm	

Purpose

We suggest that design enough gap around LCM to prevent shock test failure, or interference, cell crack, abnormal display...etc. in the reliability test

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Appendix B

LCM to B-cover z-gap



B-cover Tape	Gap
Without	0.15 ~ 0.25mm
With	0.15 ~ 0.20mm

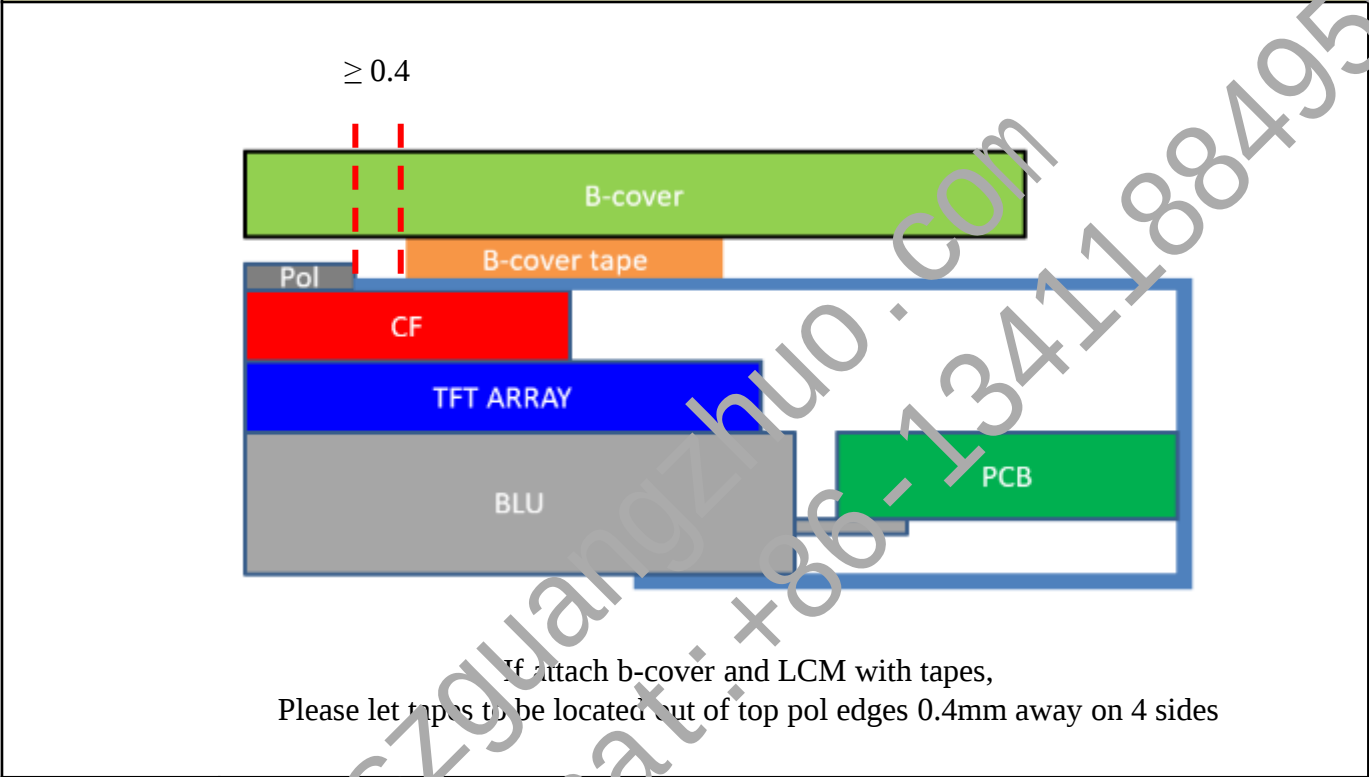
Purpose

Too less z-gap between system B-cover and LCM top pol has high risk to cause cell crack, pooling, light leakage and other issues

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Appendix B

B-cover tape to top pol edge

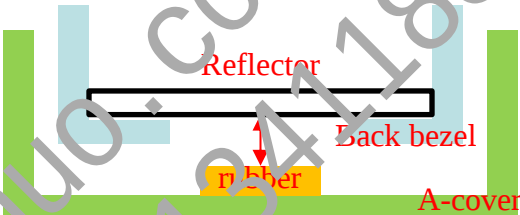
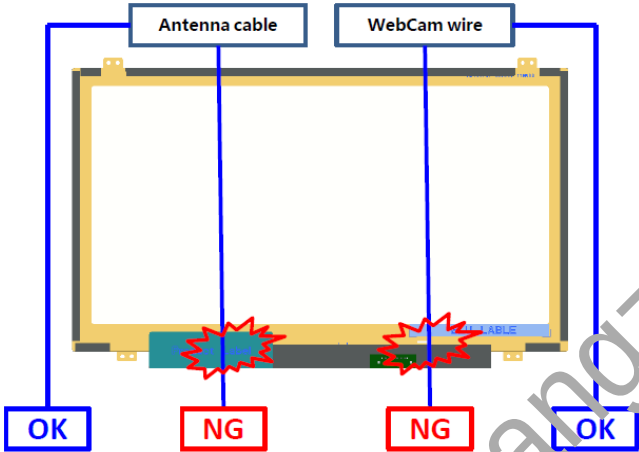


Purpose	To avoid the B-cover tape override top pol and cause pooling or light leakage issue
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Appendix B

Antenna Cable & Webcam wire



If sponge within the reflector area is necessary, we suggest that the gap between reflector and sponge is more than 0.5mm

Purpose

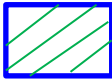
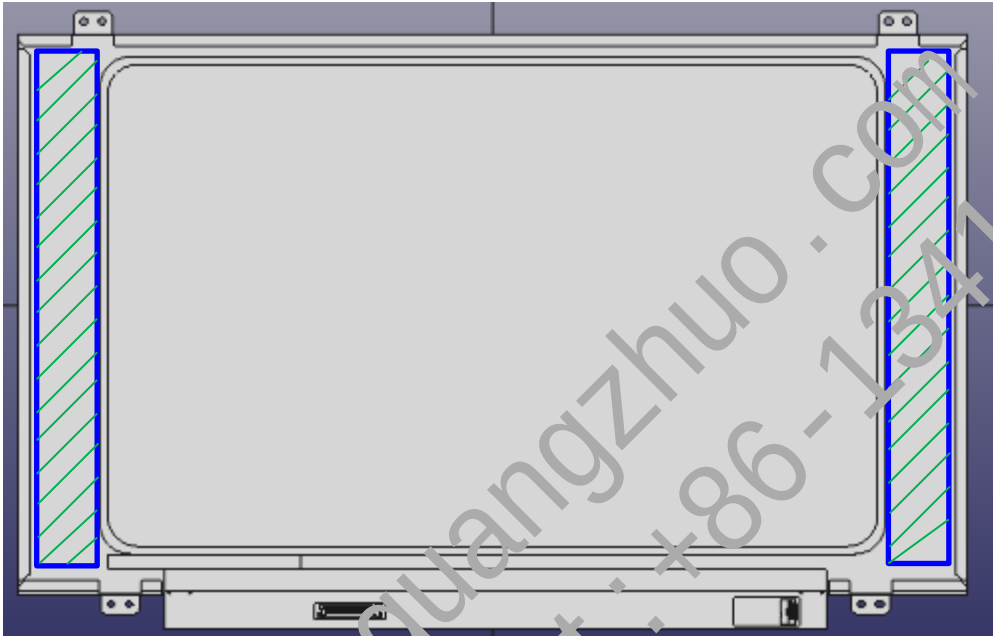
1. We suggest that do not set Antenna or WebCam cable / wire go behind LCM to avoid backpack test, hinge test ,twist test or pogo test with abnormal display
2. If the cable / wire is necessary to go behind LCM, please make a groove with rounds or chamfers to protect the cable / wire, or attach with higher sponge / rubber adjacent to the cable / wire route
3. Suggest that attach the cable / wire with tapes to A-cover
4. Do not attach anything with LCM reflector area. If attach cable / wire with LCM reflector area, it may cause pooling, white spot, light leakage and other related issues

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Appendix B

LCM paste area



Attachment area

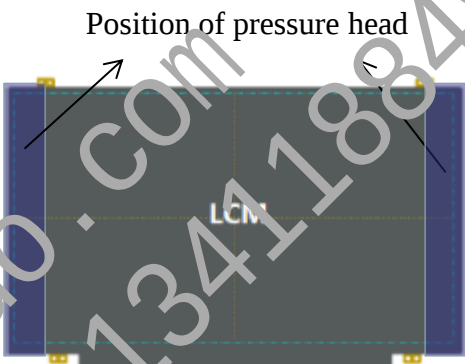
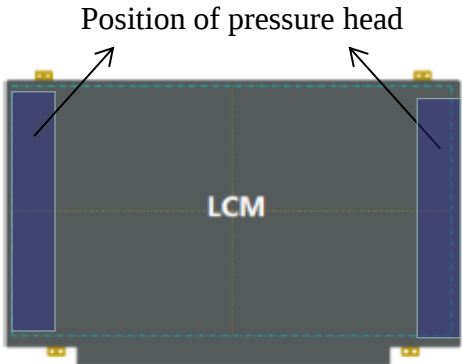
Purpose	If use the stretch remove tapes to fix LCM with A-cover, please set the stretch remove tapes correspond to the LCM back-bezel and do not let the tapes override the back-bezel's level step of opening
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LCM pressable area



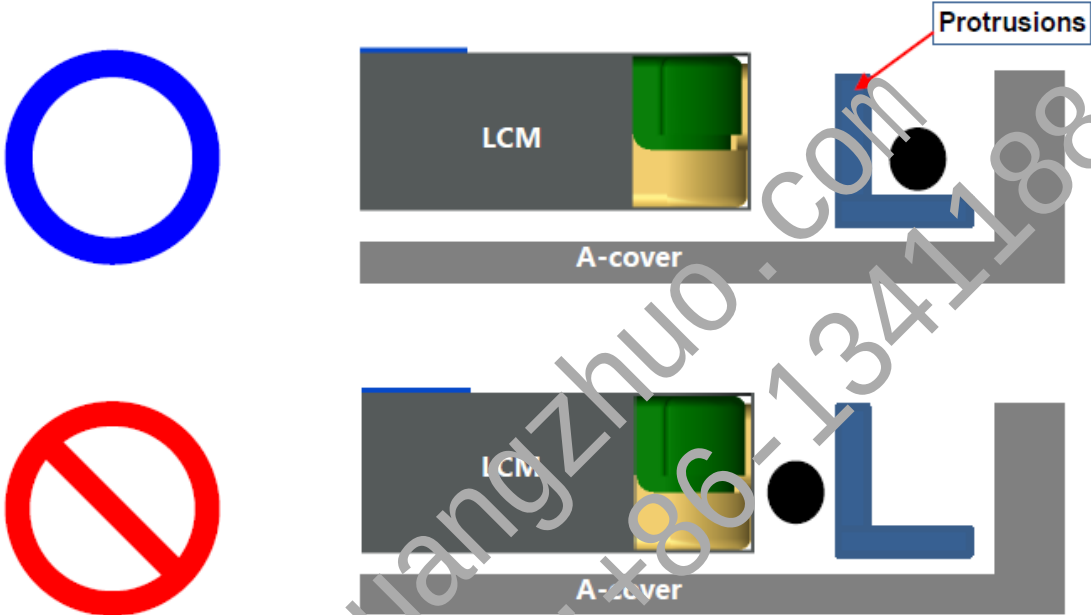
Purpose	1. LCM is fixed on A-cover by double-sided tap which can stick LCM after using the press jig stress LCM during assembling. 2. To avoid panel broken the design of pressure head of press jig can not only pin on cell panel. The pressure head needs to pin on the LCM frame, which the LCM frame can share the pressure of the pressing head.
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Wire setting



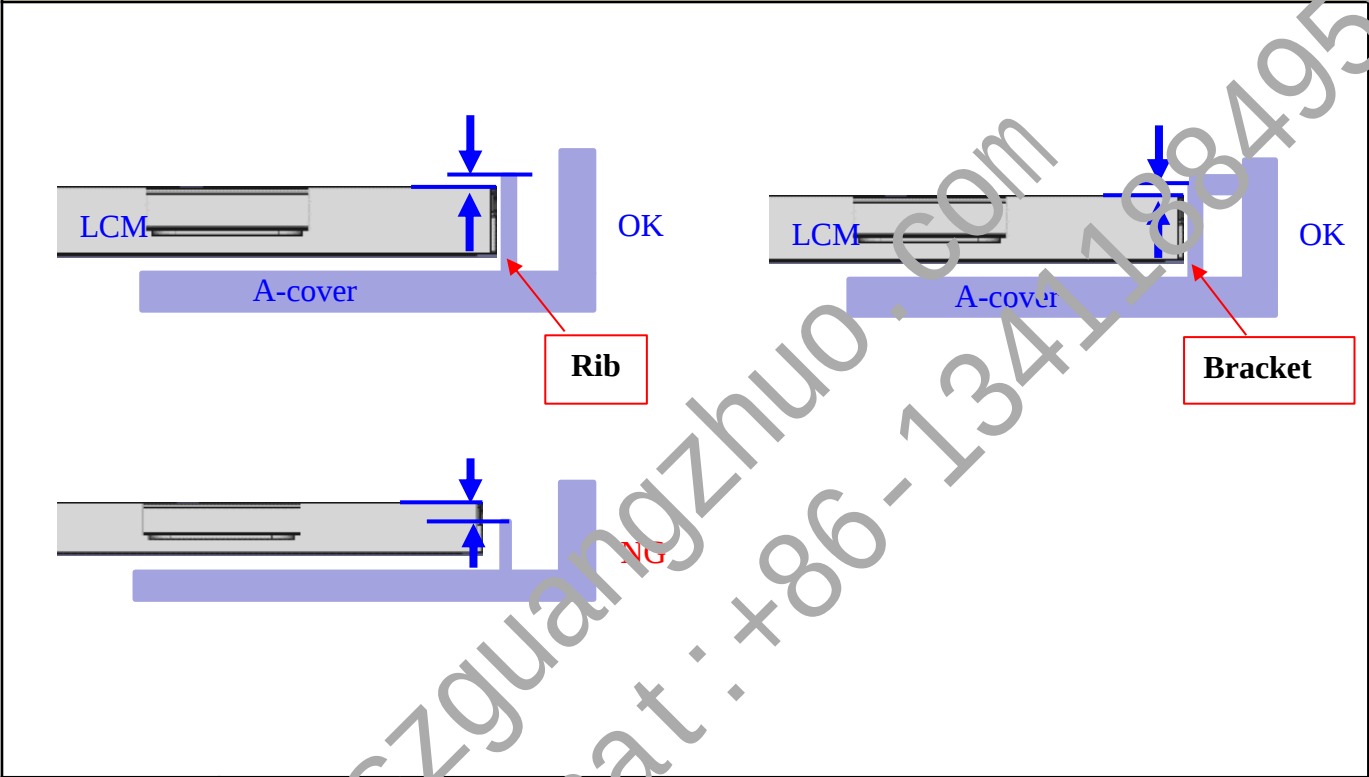
Purpose	Wire should be placed between Protrusions and A-cover. If place the wire between LCM and Protrusions, it may interfere with LCM when assembling B-covers, or even cause LCM breakage in reliability test.
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A-cover strength



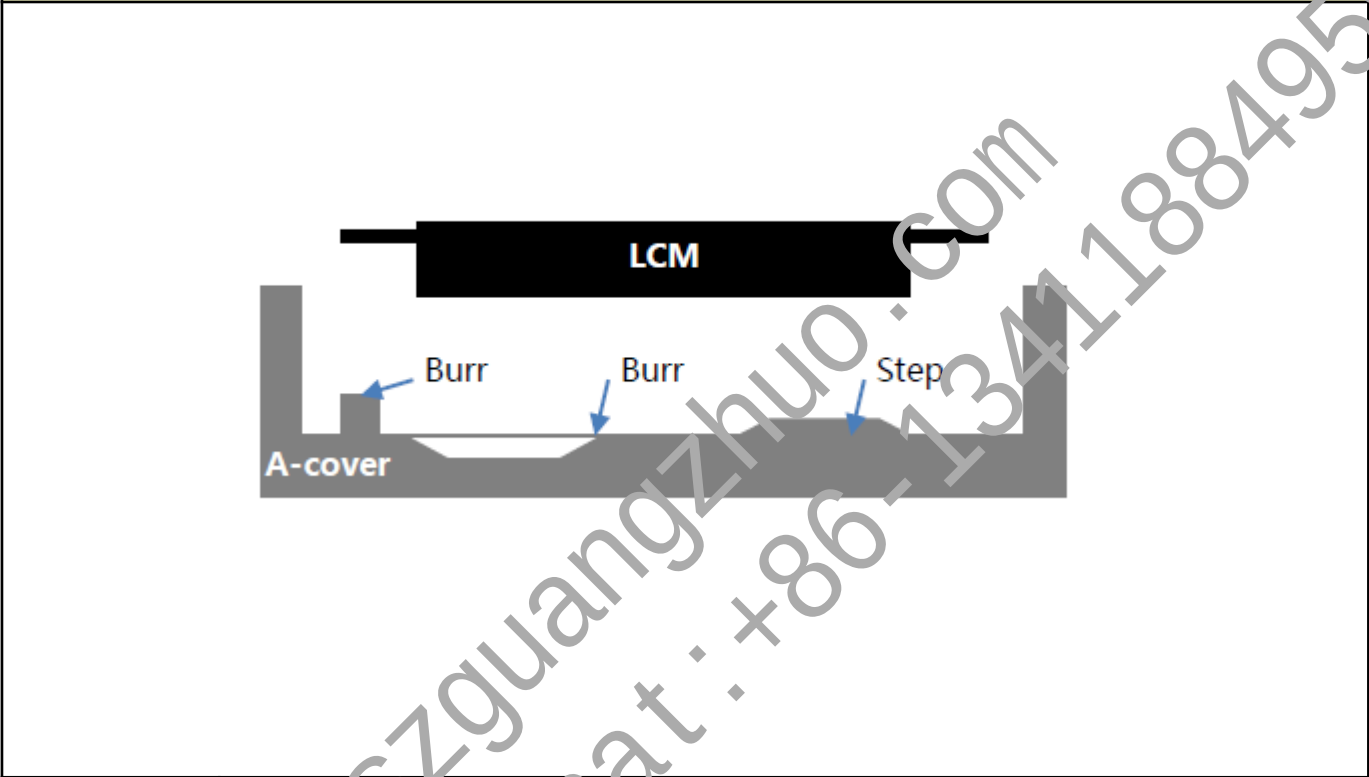
Purpose	1. It is recommended that Rib height is higher than LCM, in order to avoiding press on LCM edge panels. 2. As for LCM is more stronger than Rib, the L Bracket is be recommended.
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System A-cover Inner Surface



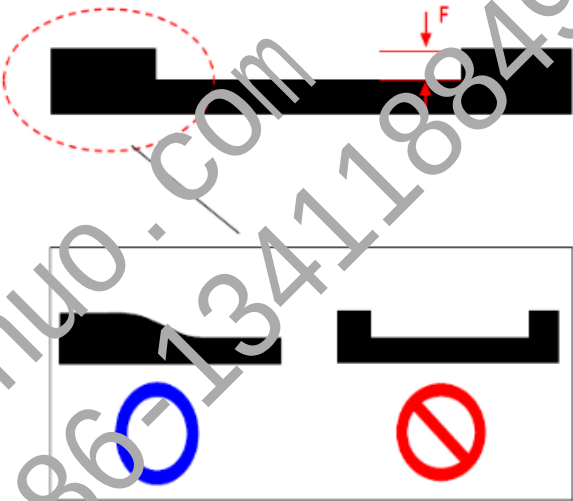
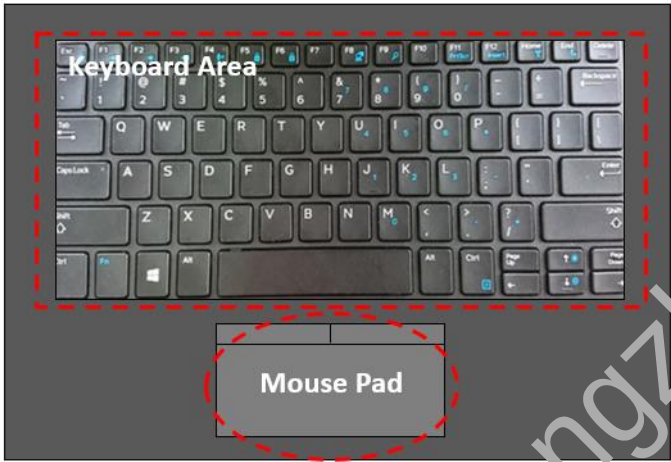
Purpose	There should not exist any burr, segment gap or protrusions beside Logo, which would cause White Spot or Glass Broken by stress concentration.
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Keyboard area & Mouse pad



max 0.3mm

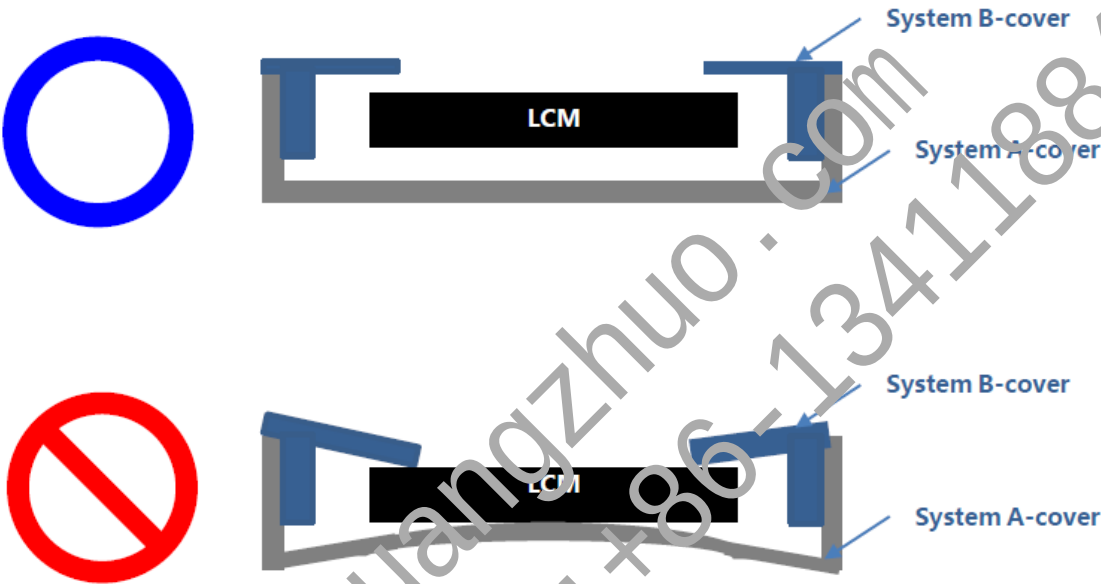
Purpose	In order to avoiding I.C.M fragments in reliability test, the step surface of Keyboard and Mouse pad transmits smoothly, and should not be right-angle. For example, when Foge testing, if the broken hole is done in this location, it is easy to produce fragments.
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System cover reliability



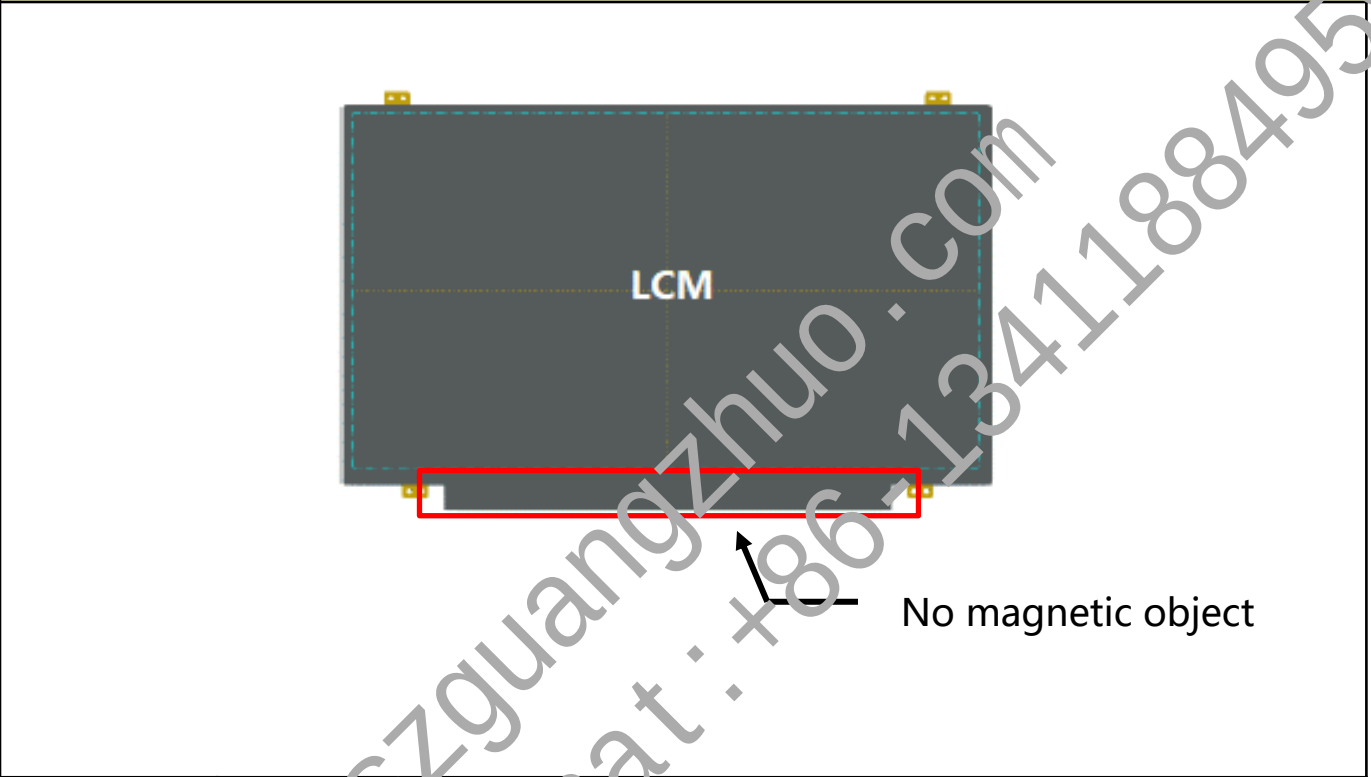
Purpose	The permanent deformation part of System cover after the reliability test, including sponge and other structures or components, can not touch LCM.
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A/B-cover near LCD PCBA



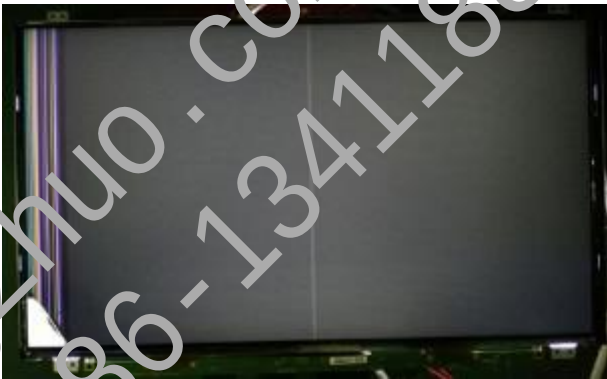
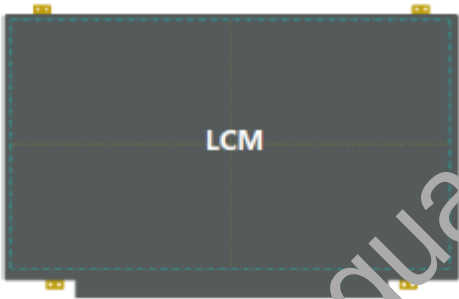
Purpose	There should not have magnet object near LCM PCBA, which is prone to cause physical or electricity noise issue
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Appendix B

A-cover add sponges on Boss side wall



Purpose

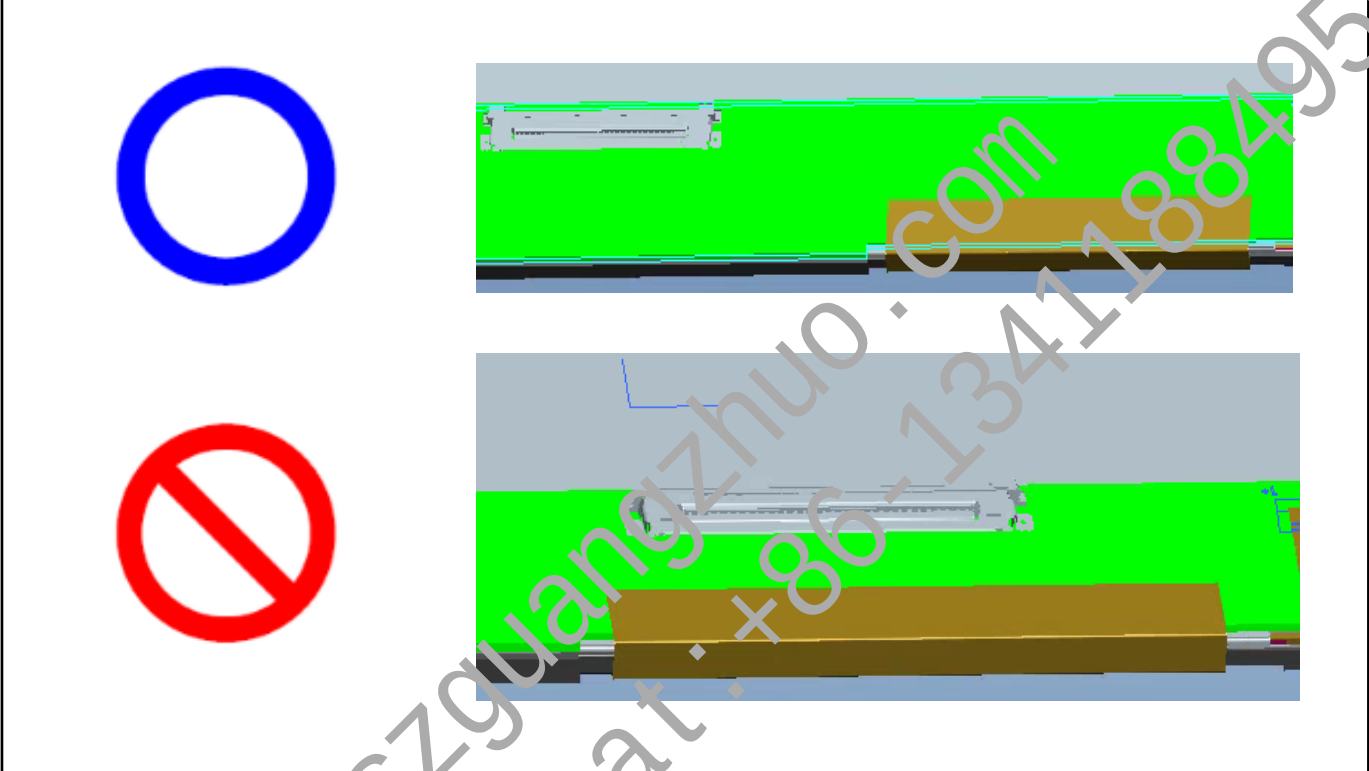
We suggest to attach Sponges to the side of the Boss column of A-cover to reduce the panel broken possibility in assembly. It is recommended to this design synchronously.

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Appendix B

LCM to A-Cover / sponges z-gap

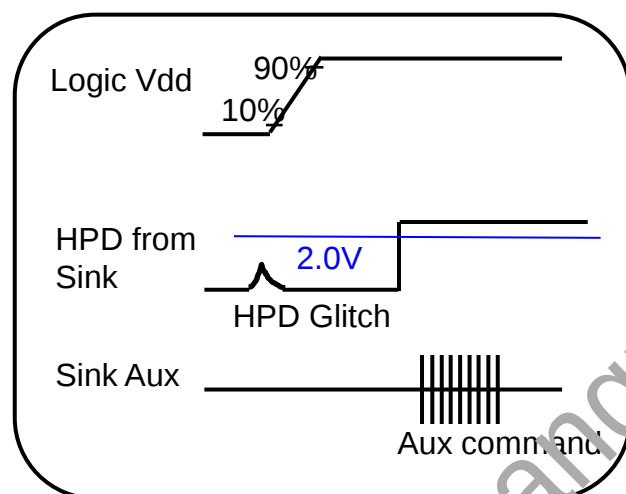


Purpose	Bent product: The position of system connector and FPC should be staggered in X direction. Otherwise, when testing, the system Cable line extrudes FPC, leading to FPC Crack; (Panel FPC Bonding location is related to Mask and can not be changed easily)
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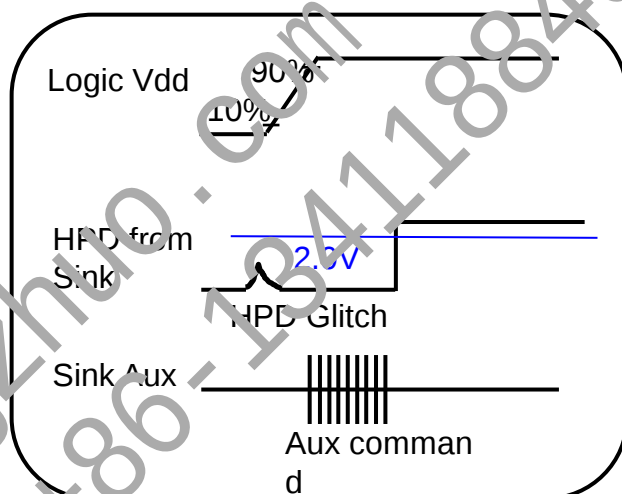
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Appendix C

HPD Signal recognition



Normal Signal (Ignore HPD Glitch)



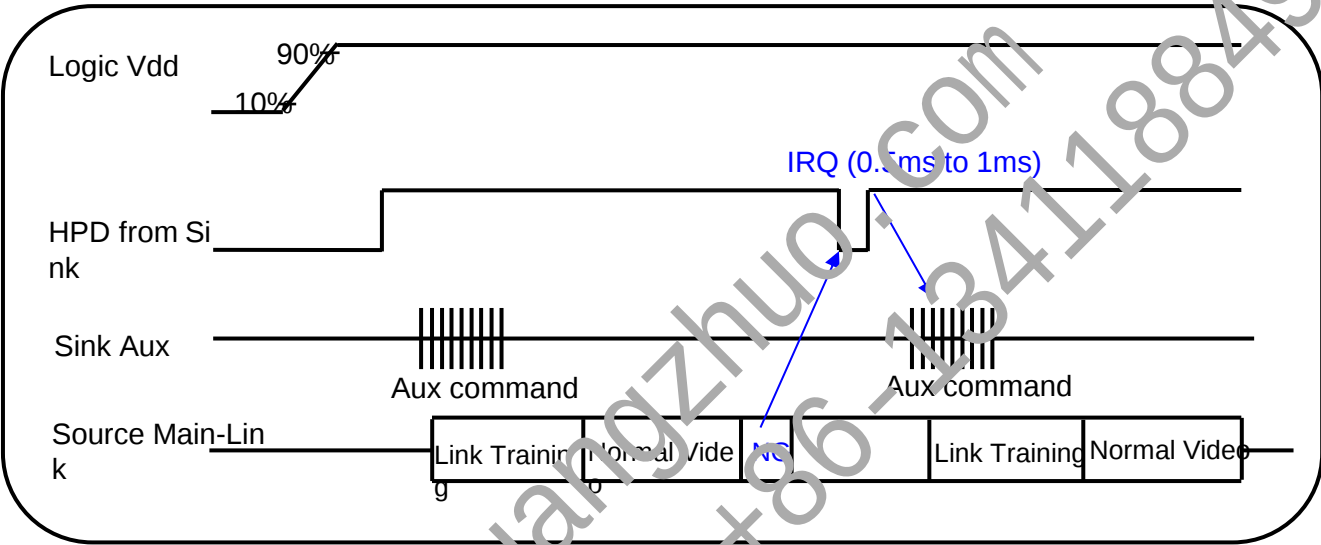
Abnormal Signal

Purpose

When HPD glitch voltage less than 2.0(V), system signal can't output AUX command data.

Appendix C

HPD Signal Definition IRQ (Interrupt Request)

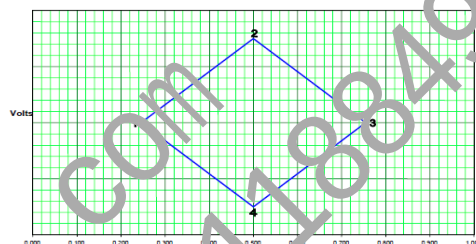
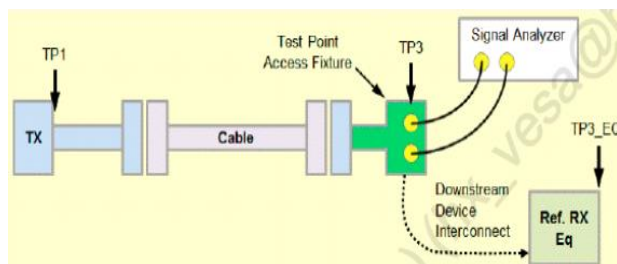


Purpose

When HPD signal low than 0.5ms to 1ms, the source device should check sink status field from the DPCD and take link training again.

Appendix C

Main link eye diagram of TP3



Measured TP3 on LCM connector.

Downstream Device Mask at TP3

	UI	Voltage
1	0.246	0
2	0.5	0.075
3	0.755	0
4	0.5	-0.075

Eye for TP3 at RBR

	UI	Voltage
1	0.375	0
2	0.5	0.023
3	0.625	0
4	0.5	-0.023

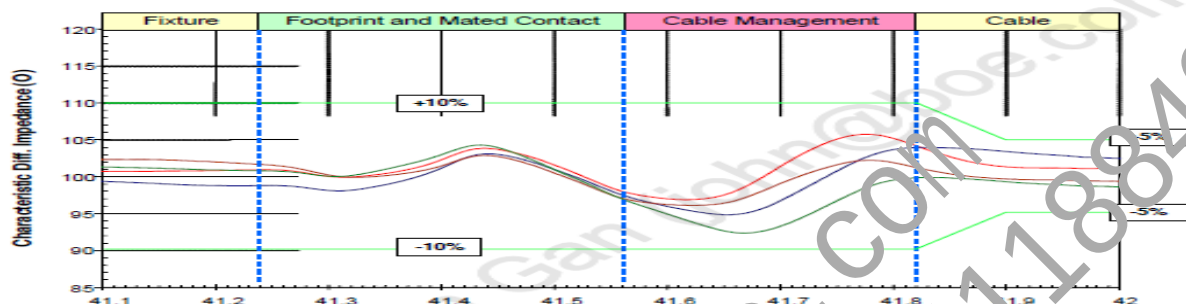
Eye for TP3 at RBR

Purpose

1. Main Link EYE Diagram should meet TP3 point of VESA.
2. The measure method is through access fixture.

Appendix C

Impedance Profile through a DP Connector



Differential Impedance Profile Measurement Data Example

Segment	Differential Impedance Value	Maximum Tolerance
Fixture	100Ω/VESA	±10%
Connector	100Ω/VESA	±10%
Wire management	100Ω/VESA	±10%
Cable	100Ω/VESA	±5%

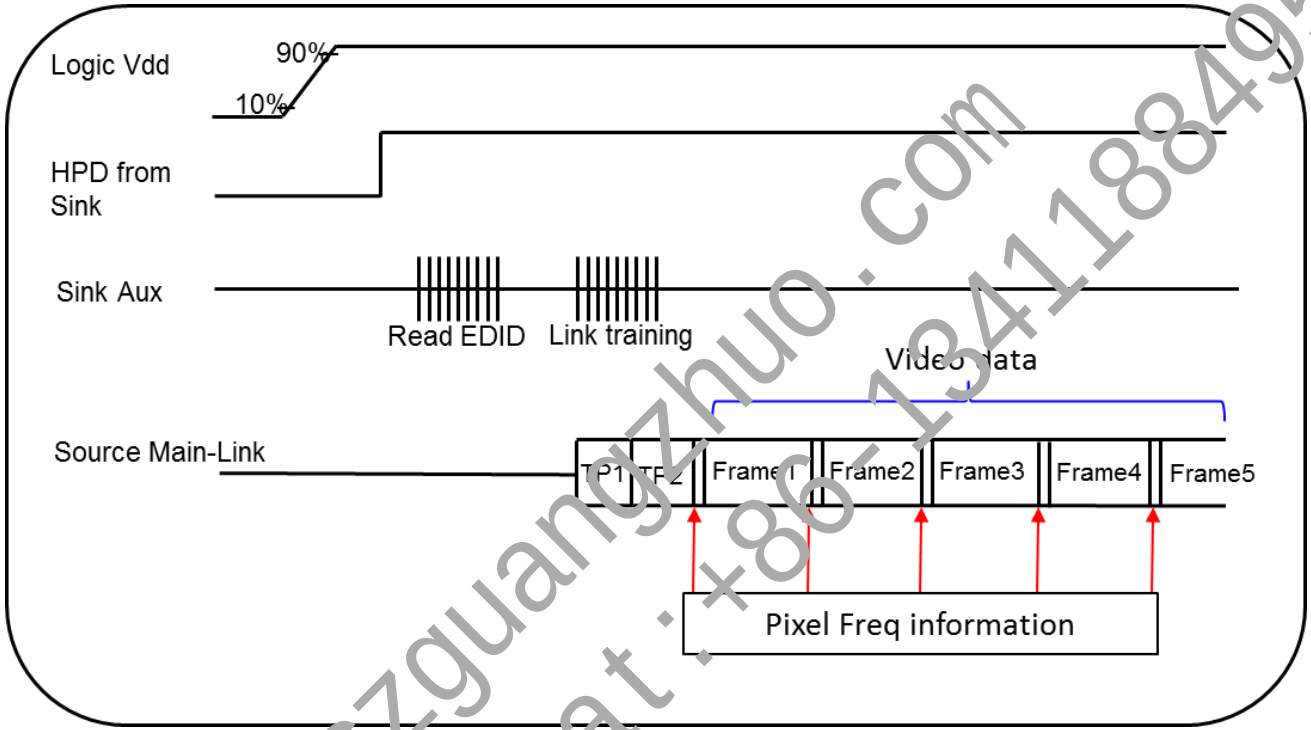
Impedance Profile Values for Cable Assembly

Purpose

Cable Impedance Profile 100ohm for Cable Assembly

Appendix C

Main Link Pixel Freq information value of MSA data

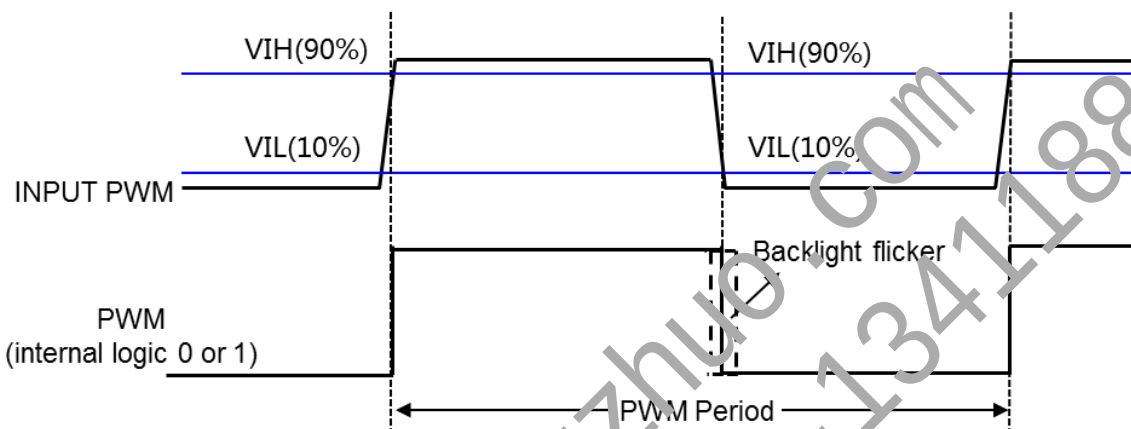


Purpose

- 1. It need to fix pixel freq information value of MSA data output to prevent the initial abnormal pixel freq information value from incoming after power on.
- 2. BOE can read DPCD to check this value. Ex: BIOS is 1.62G , but into windows is 2.7G.

Appendix C

Main Link Pixel Freq information value of MSA data



Example:

Freq	Cycle Time	PWM Rising Time	PWM Falling Time
200Hz	5ms	≤5us	≤1us
1KHz	1ms	≤200ns	≤200ns

Purpose

1. LED driver need to calculate the duty cycle of input PWM signal.
2. To avoid backlight flicker visible on LCD, system input PWM suggest :
PWM rising $\leq 200\text{ppm} \times \text{cycle time}$; PWM falling $\leq 200\text{ppm} \times \text{cycle time}$.