Doc. Number:

■ Tentative Specification
☐ Preliminary Specification
☐ Approval Specification

MODEL NO.: N160GME
SUFFIX: GQC
DPN: Rev.:C1

Customer:

APPROVED BY SIGNATURE

Name / Title
Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By

CONTENTS

REVISION HISTORY

Version	Date	Page	Description
0.0	Nov. 19, 2021	All	Tentative Spec Ver.0.0 was first issued

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N160GME-GQC is a 16” TFT Liquid Crystal NB Display module with LED Backlight unit and 40 pins eDP interface. This module supports 2560 x 1600 QHD model and can display 16,777,216 colors. This panel complies with TUV Rheinland low blue light method 2 and is certified as a component under certain conditions.

1.2 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Screen Size	16” diagonal	-	-
Driver Element	IGZO	-	-
Frame Rate	240	Hz	-
Pixel Number	2560 x R.G.B. x 1600	pixel	-
Pixel Pitch	0.13464 (H) x 0.13464 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Interface	eDP 1.4		
Display Colors	16,777,216	color	-
Transmissive Mode	Normally black	-	-
Surface Treatment	Hard coating (3H), High resolution Adaptable AG	-	-
Luminance, White	300	Cd/m2	-
Color Gamut	DCI-P3 100%	%	-
Power Consumption	Total (7.2) W (Max.) @ cell (2.8) W (Max.), BL (4.4) W (Max.)		-

Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, fv = 165 Hz, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 ºC, whereas MOSAIC pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Glass	Thickness		0.25		mm	
Polarizer	Thickness		0.077/0.103		mm	
Module Size	Horizontal(H)	349.38	349.68	349.98	mm	(1) (2)
	Vertical(V) w/o PCB and Hinge	224.63	223.93	224.23	mm	
	Vertical(V) with PCB	233.93	234.43	234.93	mm	
	Thickness (T) w/o sponge	-	2.05	2.20	mm	
Boze Area	Horizontal	346.88	347.08	347.28	mm	
	Vertical	217.62	217.82	218.02	mm	
Active Area	Horizontal	344.58	344.68	344.78	mm	
	Vertical	215.32	215.42	215.52	mm	
Weight		-	355	370	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Dimensions are measured by caliper.

Note (3) Panel thickness is measured with calipers clamping mylar or tape tightly

2.1 CONNECTOR TYPE

Please refer Appendix Outline Drawing for detail design.

Connector Part No.: IPEX-20682-040E-02

User's connector Part No:IPEX-20679-040T-01

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

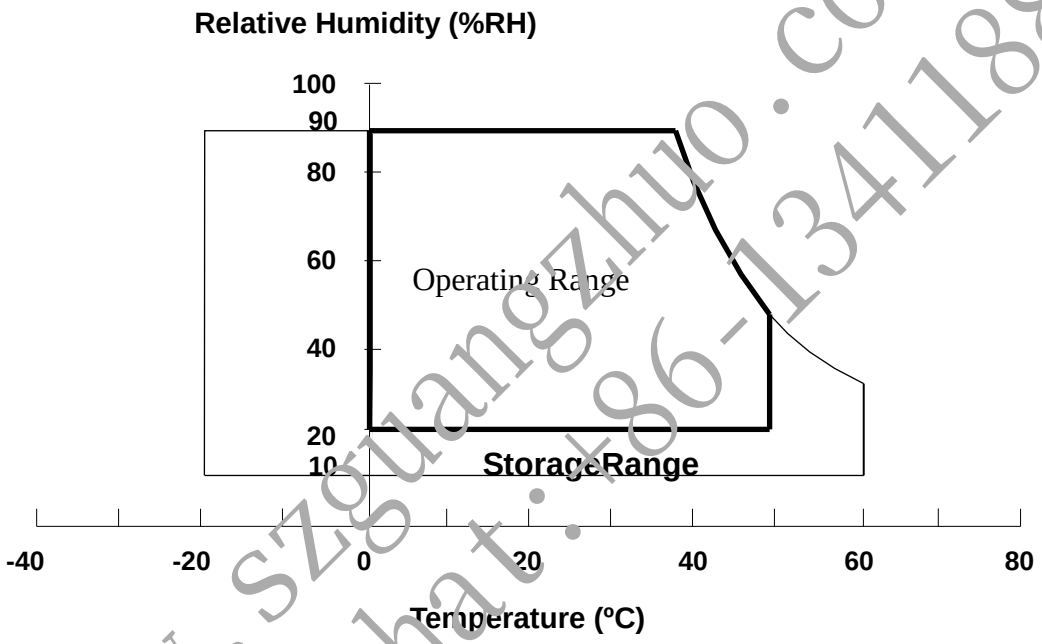
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)

Note (1) (a) 90 %RH Max. (Ta < 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta < 40 ºC).

(c) No condensation.

Note (2) The temperature of panel surface should be 0 ºC min. and 60 ºC max.



3.2 ELECTRICAL ABSOLUTE RATINGS

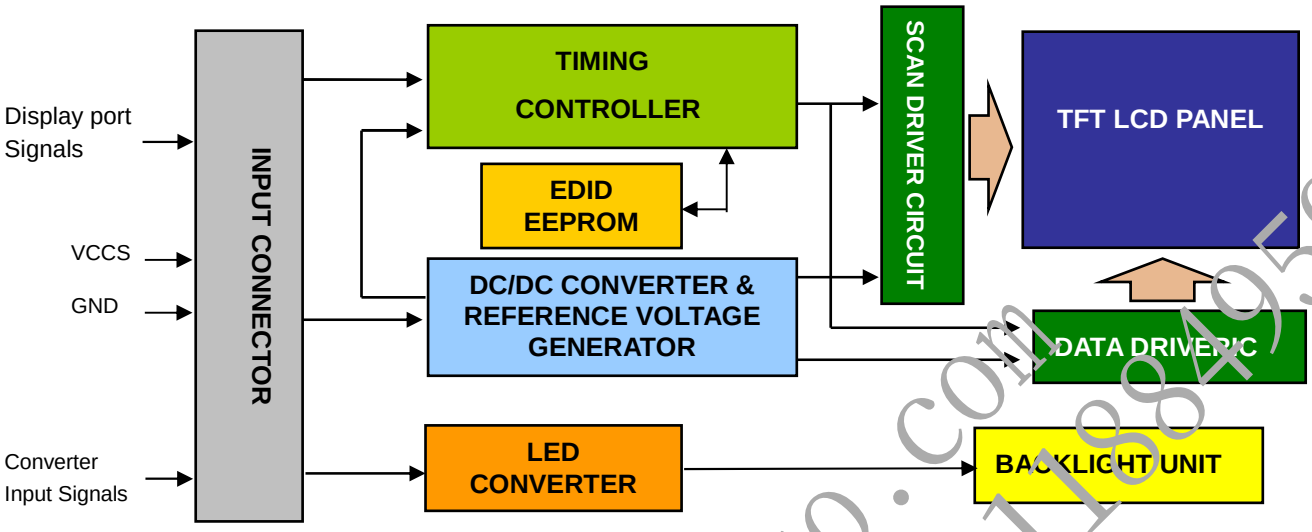
3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	+4.0	V	
Converter Input Voltage	LED_VCCS	-0.3	26	V	(1)
Converter Control Signal Voltage	LED_PWM,	-0.3	5	V	(1)
Converter Control Signal Voltage	LED_EN	-0.3	5	V	(1)

Note (1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “ELECTRICAL CHARACTERISTICS”.

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



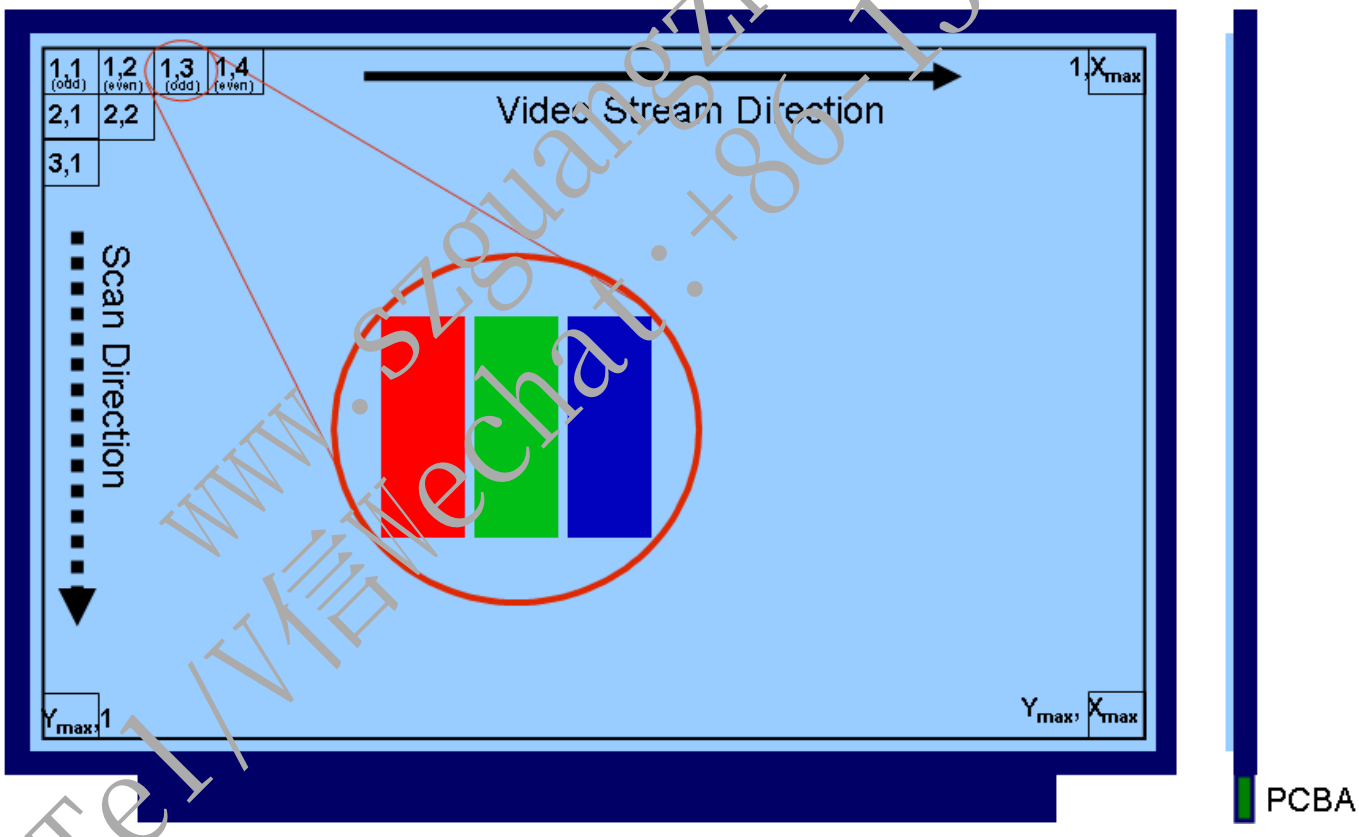
4.2 INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	DDS_SCL	Nvidia DDS, I2C (SCL)	
2	H_GND	High Speed Ground	
3	Lane3_N	Complement Signal Link Lane3	
4	Lane3_P	True Signal Link Lane3	
5	H_GND	High Speed Ground	
6	Lane2_N	Complement Signal Link Lane2	
7	Lane2_P	True Signal Link Lane2	
8	H_GND	High Speed Ground	
9	Lane1_N	Complement Signal Link Lane 1	
10	Lane1_P	True Signal Link Lane 1	
11	H_GND	High Speed Ground	
12	Lane0_N	Complement Signal Link Lane 0	
13	Lane0_P	True Signal Link Lane 0	
14	H_GND	High Speed Ground	
15	AUX_CH_P	True Signal Auxiliary Channel	
16	AUX_CH_N	Complement Signal Auxiliary Channel	
17	H_GND	High Speed Ground	
18	VCCS	LCD logic and driver power	
19	VCCS	LCD logic and driver power	
20	VCCS	LCD logic and driver power	
21	VCCS	LCD logic and driver power	
22	BIST_EN	Panel Built In Self Test Enable	
23	GND	Ground	
24	GND	Ground	
25	GND	Ground	

26	GND	Ground	
27	HPD	Hot Plug Detect	
28	BL_GND	Backlight ground	
29	BL_GND	Backlight ground	
30	BL_GND	Backlight ground	
31	BL_GND	Backlight ground	
32	LED_EN	BL_Enable Signal of LED Converter	
33	LED_PWM	PWM Dimming Control Signal of LED Converter	
34	DDS_SDA	Nvidia DDS, I2C (SDA)	
35	PSR_EN	PSR Enable signal of TCON	PSR disable@ default/High. PSR enable@ Low
36	LED_VCCS	Backlight power	(Support 6.0 ~ 21V)
37	LED_VCCS	Backlight power	(Support 6.0 ~ 21V)
38	LED_VCCS	Backlight power	(Support 6.0 ~ 21V)
39	LED_VCCS	Backlight power	(Support 6.0 ~ 21V)
40	OD_EN	OD Enable signal of TCON	OD function (Disable @ default/High, Enable @ Low)

Note (1) The first pixel is odd as shown in the following figure



Note (2) The setting of BIST, OD and PSR function are as follows.

Pin	Enable	Disable
BIST_EN	Hi	Lo
OD_EN	Hi	Lo
PSR_EN	Lo	High

Hi = High level, Lo = Low level.

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICSSPECIFICATION

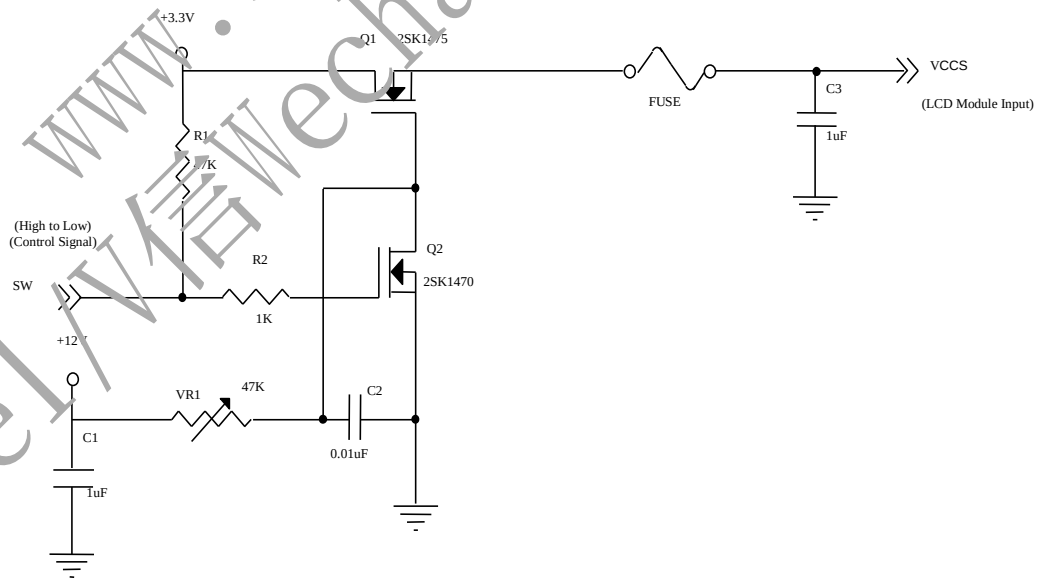
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)
HPD	High Level		2.25	-	3.6	V	(6)
	Low Level		0	-	0.8	V	(6)
HPD Impedance		R_{HPD}	30K	-	-	ohm	(5)
Ripple Voltage		V_{RP}	-	50	-	mV	(1)
BIST_EN Input Voltage	High Level	V_{IHCABC}	2.3	-	3.6	V	(5)
	Low Level	V_{ILCABC}	0	-	0.5	V	(5)
BIST_EN Impedance		R_{CABC_EN}	30K	-	-	ohm	(5)
Inrush Current		I_{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Mosaic	Icc	-	(790)	(850)	mA	(3)
	Black		-	(790)	(850)	mA	(3)
	Solid Pattern		-	(790)	(850)	mA	(3)
	Mosaic@PSR		-	(790)	(850)	mA	(3)
	Solid Pattern@PSR		-	(790)	(850)	mA	(3)
Power per EBL WG		P_{EBL}	-	(3.68)	-	W	(4)

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

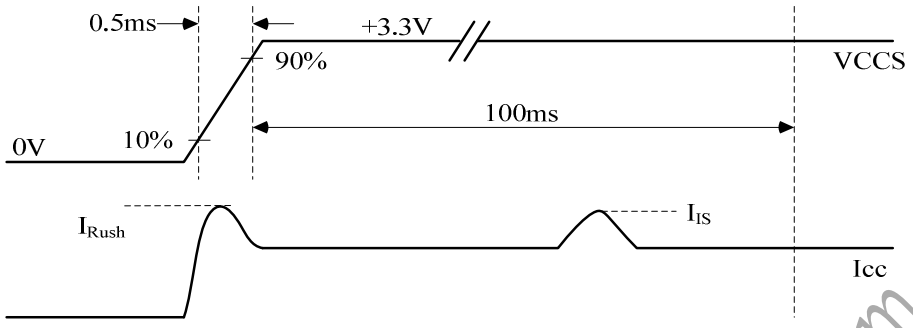
Note (2) I_{RUSH}: the maximum current when VCCS is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.

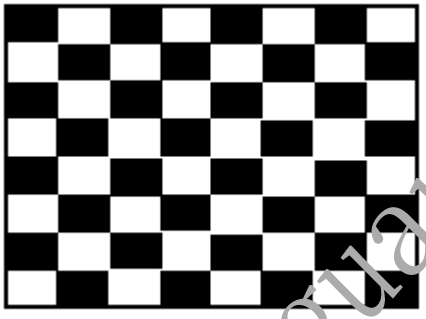


VCCS rising time is 0.5ms



Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ºC, DC Current and f_v = 240Hz, OD enable, whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern



Active Area

b. The solid pattern is the largest one of R/G/B pattern.

c. The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ºC, DC Current and PSR mode enable, whereas a power dissipation check pattern is displayed.

Note (4) The specified power are the sum of LCD panel electronics input power and the converter input power. Test conditions are as follows.

(a) VCCS = 3.3 V, Ta = 25 ± 2 ºC, f_v = 240 Hz,

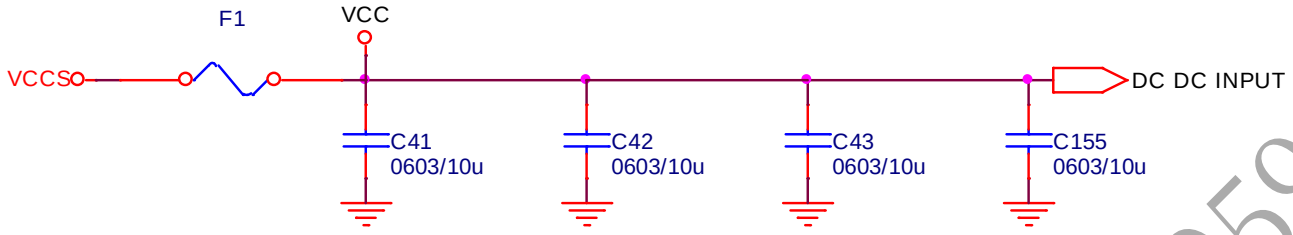
(b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.

(c) Luminance: 60 nits

Note (5) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. Please refer to Note (4) of 4.3.2 LED CONVERTER SPECIFICATION to obtain more information.

Note (6) When a source detects a low-going HPD pulse, it must be regarded as a HPD event. Thus, the source must read the link / sink status field or receiver capability field of the DPCD and take corrective action

Note (7) Input VCC Circuit is as below



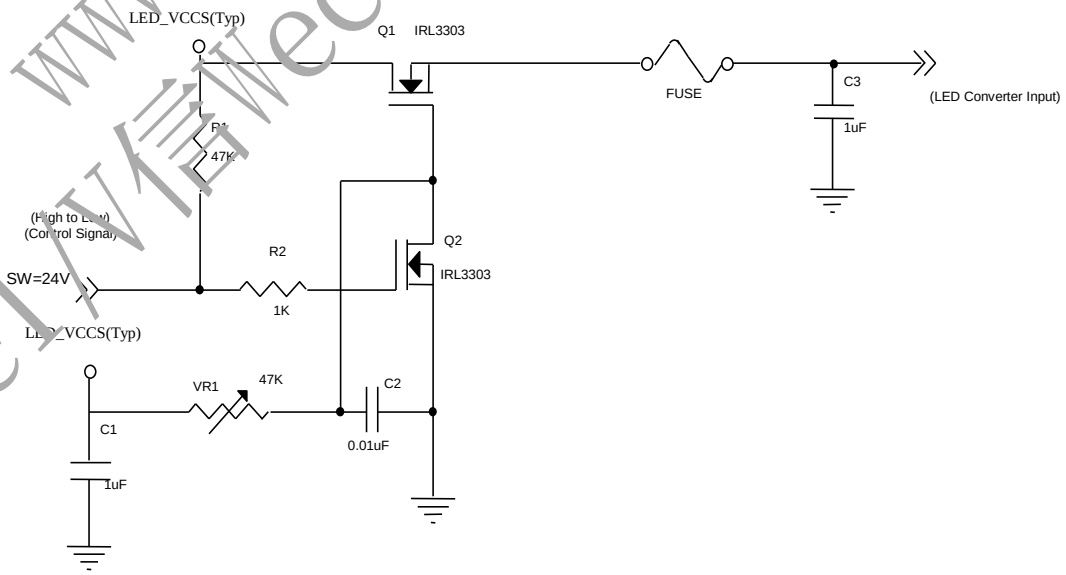
4.3.2 LED CONVERTER SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input Power Supply Voltage		LED_Vccs	6.0	12.0	21.0	V	
Converter Inrush Current		$ILED_{RUSH}$	-	-	1.5	A	(1)
LED_EN Control Level	Backlight On		2.2	-	5.0	V	(4)
	Backlight Off		0	-	0.6	V	(4)
LED_EN Impedance		R_{LED_EN}	30K	-		ohm	(4)
PWM Control Level	PWM High Level		2.2	-	5	V	(4)
	PWM Low Level		0	-	0.6	V	(4)
PWM Impedance		R_{PWM}	30K			ohm	(4)
PWM Control Duty Ratio			5	-	100	%	(5)
PWM Control Permissive Ripple Voltage		V_{PWM_pp}	-	-	100	mV	
PWM Control Frequency		f_{PWM}	190	-	2K	Hz	(2)
LED Power Current	LED_VCCS =Typ.	ILED	(240)	(353)	(366)	mA	(3)

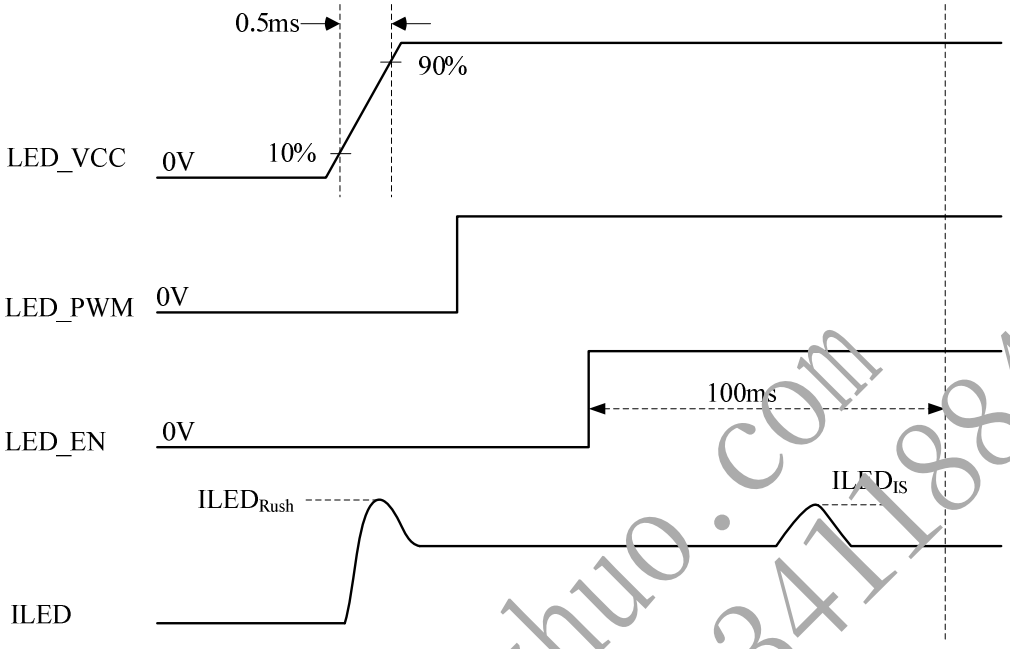
Note (1) $ILED_{RUSH}$: the maximum current when LED_VCCS is rising,

$ILED_{IS}$: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.



VLED rising time is 0.5ms



Note (2) If PWM control frequency is applied in the range less than 1KHz, the "waterfall" phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

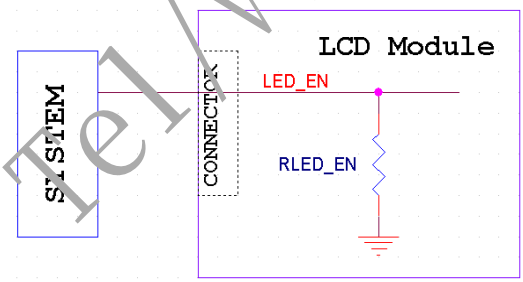
$$(N + 0.33) * f \leq f_{PWM} \leq (N + 0.66) * f$$

N : Integer $(N \geq 3)$

f : Frame rate

Note (3) The specified LED power supply current is under the conditions at "LED_VCCS = Typ.", Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.

Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. For example, the figure below describes the equivalent pull down impedance of LED_EN (if it exists). The rest pull down impedances of other signals (eg. HPD, PWM …) are in the same concept.



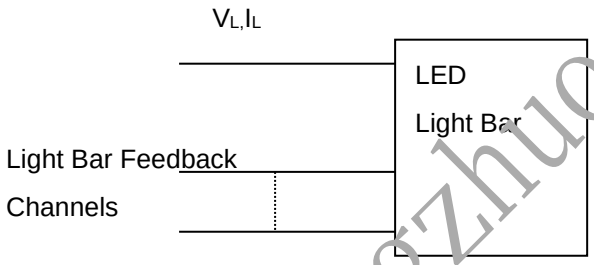
Note (5) If the cycle-to-cycle difference of PWM duty exceeds 0.1%, especially when the PWM duty is low, slight brightness change might be observed.

4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	28.6	30.8	31.9	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L	-	118.4	-	mA	(3)
Power Consumption	P_L		3.647	3.777	W	
LED Life Time	L_{BL}	15000	-	-	Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$(Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 ºC and I_L = 14.8 mA(Per EA) until the brightness becomes ≦ 50% of its original value.

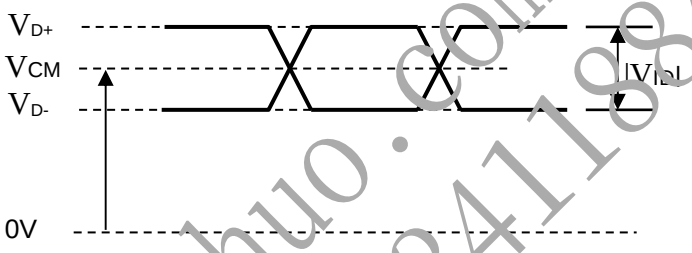
4.4 DISPLAYPORTSIGNAL TIMING SPECIFICATION

4.4.1 ELECTRICAL SPECIFICATIONS

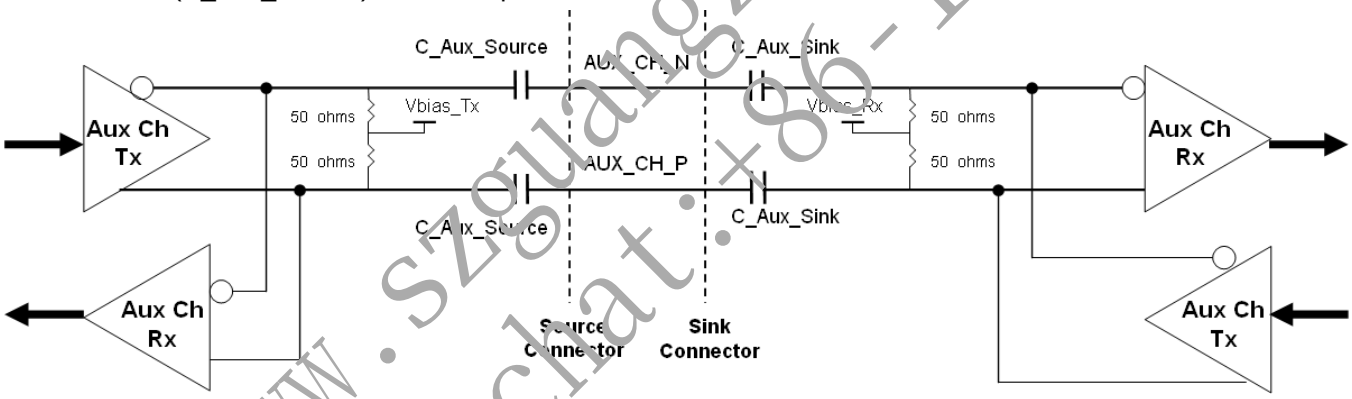
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Signal Common Mode Voltage(MainLink and AUX)	VCM	0		2	V	(1)(4)
AUX AC Coupling Capacitor	C_Aux_Source	75		200	nF	(2)
Main Link AC Coupling Capacitor	C_ML_Source	75		200	nF	(3)

Note (1)Display port interface related AC coupled signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2. There are many optional items described in eDP1.2. If some optional item is requested, please contact us

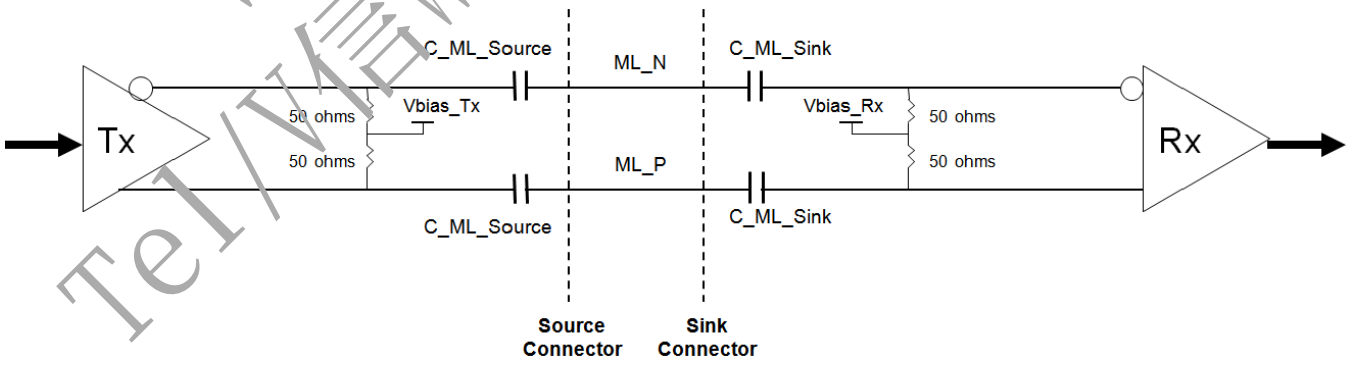
Single Ended



(2) Recommended eDP AUX Channel topology is as below and the AUX AC Coupling Capacitor (C_Aux_Source) should be placed on the source device.



(3) Recommended Main Link Channel topology is as below and the Main Link AC Coupling Capacitor (C_ML_Source) should be placed on the source device.



(4) The source device should pass the test criteria described in DisplayPortCompliance Test Specification (CTS) 1.1

4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Refresh Rate 240Hz

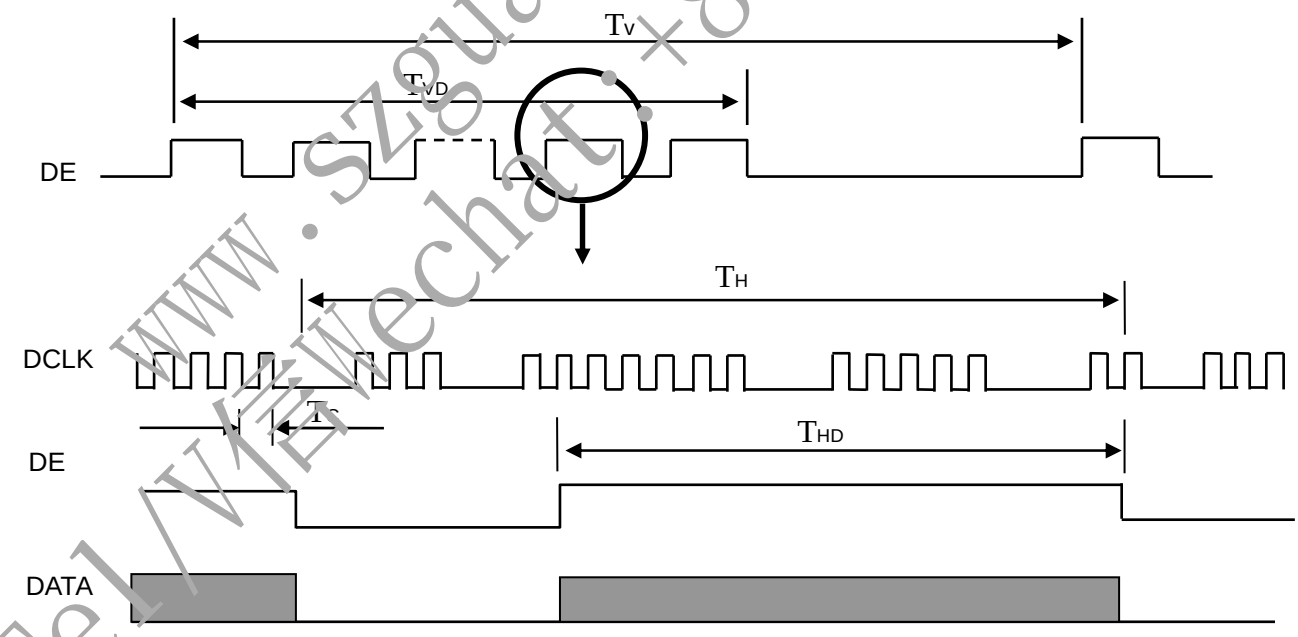
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	(1163)	(1175)	(1186.7)	MHz	-
DE	Vertical Total Time	TV	1796	1800	1804	TH	-
	Vertical ActiveDisplayPeriod	TVD	1600	1600	1600	TH	-
	Vertical ActiveBlankingPeriod	TVB	TV-TVD	200	TV-TVD	TH	-
	Horizontal Total Time	TH	2700	2720	2740	Tc	-
	Horizontal ActiveDisplayPeriod	THD	2560	2560	2560	Tc	-
	Horizontal ActiveBlankingPeriod	THB	TH-THB	(160)	TH-THB	Tc	-

Refresh rate 60Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	279.93	282.67	285.39	MHz	-
DE	Vertical Total Time	TV	1728	1732	1736	TH	-
	Vertical ActiveDisplayPeriod	TVD	1600	1600	1600	TH	-
	Vertical ActiveBlankingPeriod	TVB	TV-TVD	132	TV-TVD	TH	-
	Horizontal Total Time	TH	2700	2720	2740	Tc	-
	Horizontal ActiveDisplayPeriod	THD	2560	2560	2560	Tc	-
	Horizontal ActiveBlankingPeriod	THB	TH-THB	(160)	TH-THB	Tc	-

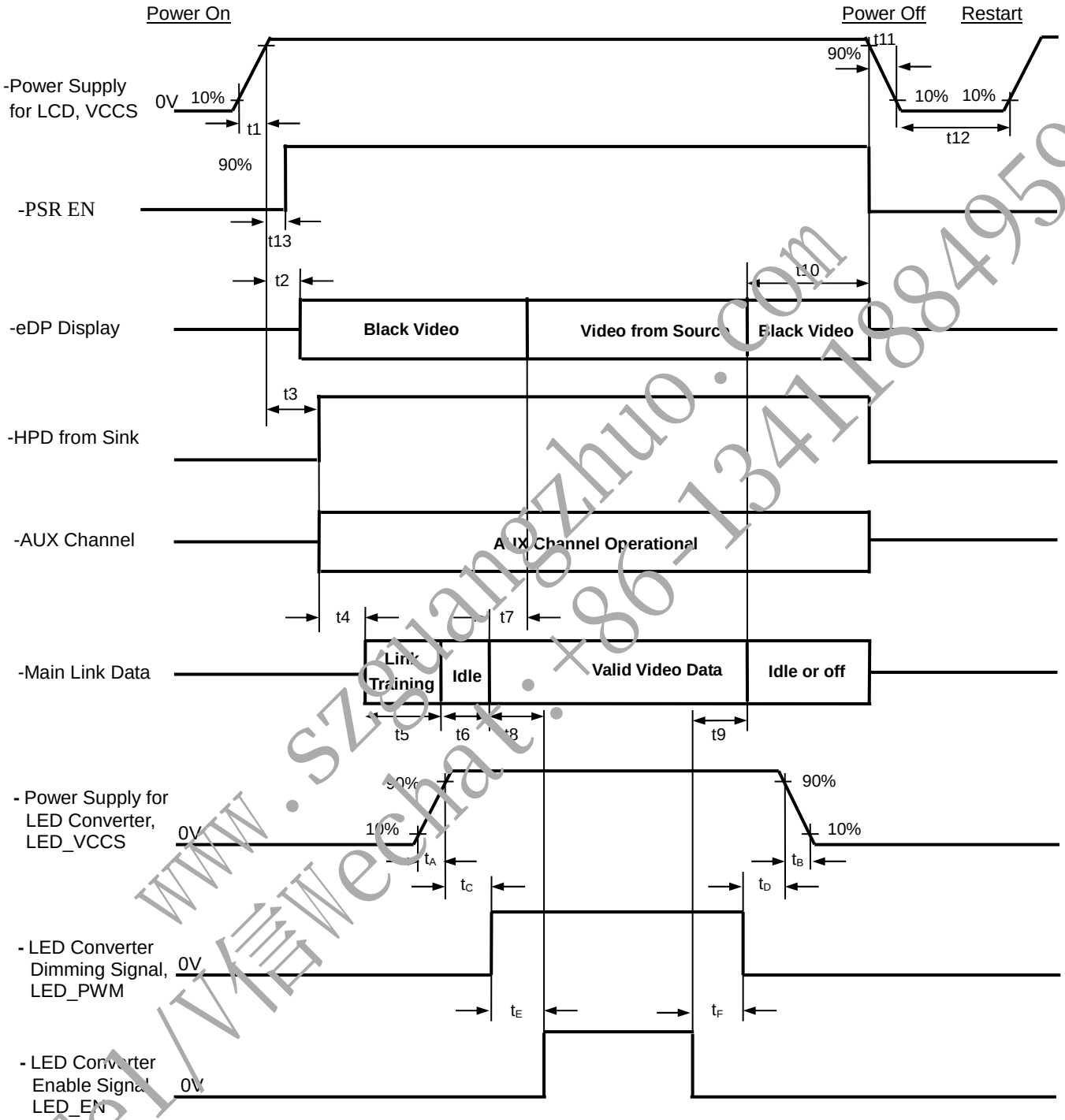
Note (1) The panel can operate at 480Hz normal mode and power saving mode, respectively. All reliability tests are based on specific timing of 480Hz refresh rate. We can only assure the panel's electrical function at power saving mode.

INPUT SIGNAL TIMING DIAGRAM



4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.



Timing Specifications

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	Power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t2	Delay from LCD,VCCS to black video generation	Sink	0	200	ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source (see Notes:2 and 3 below)
t3	Delay from LCD,VCCS to HPD high	Sink	0	200	ms	Sink AUX Channel must be operational upon HPD high (see Note:4 below)
t4	Delay from HPD high to link training initialization	Source	0	-	ms	Allows for Source to read Link capability and initialize
t5	Link training duration	Source	0		ms	Dependant on Source link training protocol
t6	Link idle	Source	0	-	ms	Min Accounts for required BS-Idle pattern. Max allows for Source frame synchronization
t7	Delay from valid video data from Source to video on display	Sink	0	50	ms	Max value allows for Sink to validate video data and timing. At the end of T7, Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and Sink will no longer generate automatic Black Video
t8	Delay from valid video data from Source to backlight on	Source	80	-	ms	Source must assure display video is stable *: Recommended by INX. To avoid garbage image.
t9	Delay from backlight off to end of valid video data	Source	50	-	ms	Source must assure backlight is no longer illuminated. At the end of T9, Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and Sink will automatically display Black Video. (See Notes: 2 and 3 below) *: Recommended by INX. To avoid garbage image.
t10	Delay from end of valid video data from Source to power off	Source	0	500	ms	Black video will be displayed after receiving idle or off signals from Source
t11	VCCS power rail fall time, 90% to 10%	Source	0.5	10	ms	-

t12	VCCS Power off time	Source	500	-	ms	-
t13	Delay from LCD,VCCS to PSR_EN high	Source	(0)	(5)	ms	PSR function select time
t_A	LED power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t_B	LED power rail fall time, 90% to 10%	Source	0	10	ms	-
t_C	Delay from LED power rising to LED dimming signal	Source	1	-	ms	-
t_D	Delay from LED dimming signal to LED power falling	Source	1	-	ms	-
t_E	Delay from LED dimming signal to LED enable signal	Source	0	-	ms	-
t_F	Delay from LED enable signal to LED dimming signal	Source	0	-	ms	-

Note (1) Please don't plug or unplug the interface cable when system is turned on.Before LCD_VCCS and LED_VCCS are ready, it is recommended to pull down the backlight control signals.

Note (2) The Sink must include the ability to automatically generate Black Video autonomously. The Sink must automatically enable Black Video under the following conditions:

- Upon LCDVCC power-on (within T2 max)
- When the "NoVideoStream_Flag" (VB-ID Bit 3) is received from the Source (at the end of T9)

Note (3) The Sink may implement the ability to disable the automatic Black Video function, as described in Note (2), above, for system development and debugging purposes.

Note (4) The Sink must support AUX Channel polling by the Source immediately following LCDVCC power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to response to an AUX Channel transaction with the time specified within T3 max.

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

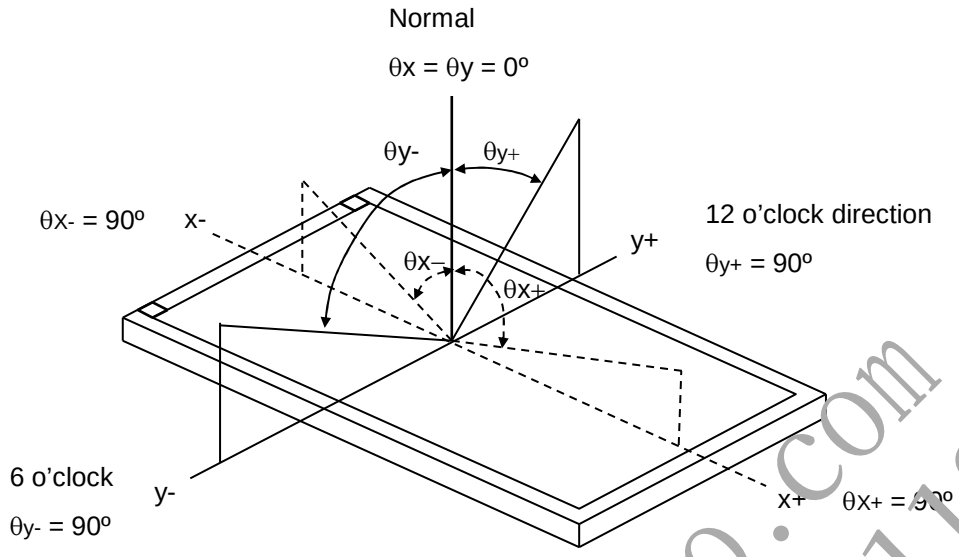
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	118.4	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	800	1000	-	-	(2), (5) ,(7)
Response Time		T_R		-	5	7	ms	(3) ,(7)
		T_F		-	4	5	ms	
		TGtG (OD OFF)			3	5		
		TGtG (OD ON)		-	7	9	ms	
Average Luminance of White		LAVE		255	300	-	cd/m²	(4), (6) ,(7)
Color Chromaticity	Red	Rx		Typ – 0.03	0.680	Typ + 0.03	-	(1) ,(7)
		Ry			0.320		-	
	Green	Gx			0.265		-	
		Gy			0.690		-	
	Blue	Bx			0.150		-	
		By			0.060		-	
	White	Wx			0.313		-	
		Wy			0.329			
Viewing Angle	Horizontal	θ_x+	CR≥10	80	89	-	Deg.	(1),(5) , (7)
		θ_x-		80	89	-		
	Vertical	θ_Y+		80	89	-		
		θ_Y-		80	89	-		
White Variation		δW_{5p}	θ_x=0°, θ_Y =0°	80	90		-	(5),(6) , (7)
		δW_{13p}	θ_x=0°, θ_Y =0°	65	75		-	
Low Blue Light		BLR	θ_x=0°, θ_Y =0°	-	-	50	%	1), (5), (7), (8) (9)
		CCT		5500	6500	7000	K	
		BLTF				0.085		

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

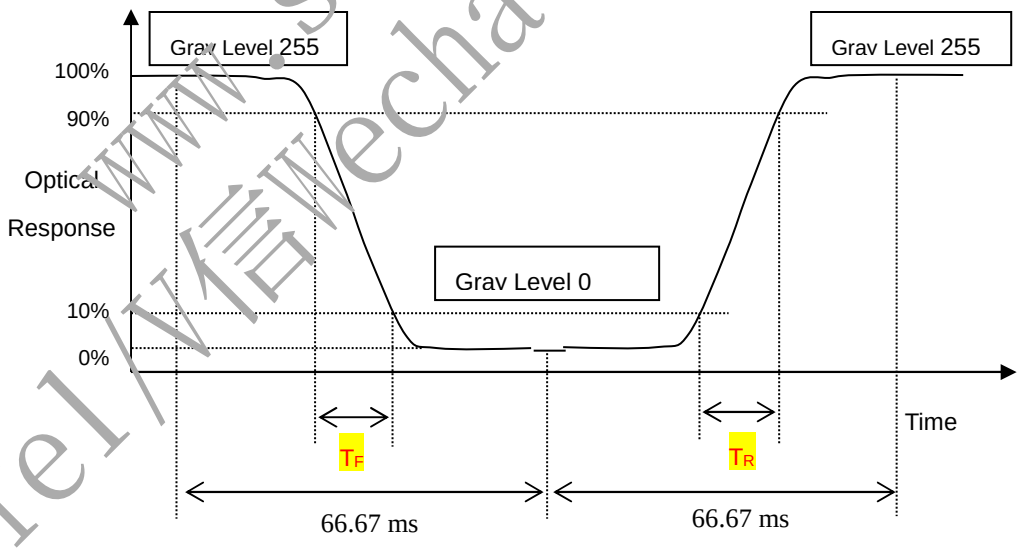
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note(6).

Note (3) Definition of Response Time (T_R, T_F):



-The TGtG is the response time means the transition time from "Gray N" to "Gray M" (N,M=0~255).

- T_{GtG_AVE} is the total average of the T_{GtG} data (Measured by INX GTG instrument)

- The gray (N,M) stands for the (0,32,64,~255) as the following table.

* It depends on Overshoot rate

Gray to gray		M								
		0	32	64	96	128	160	192	224	255
N	0									
	32									
	64									
	96									
	128									
	160									
	192									
	224									
	255									

Note (4) Definition of Average Luminance of White (L_{AVE}):

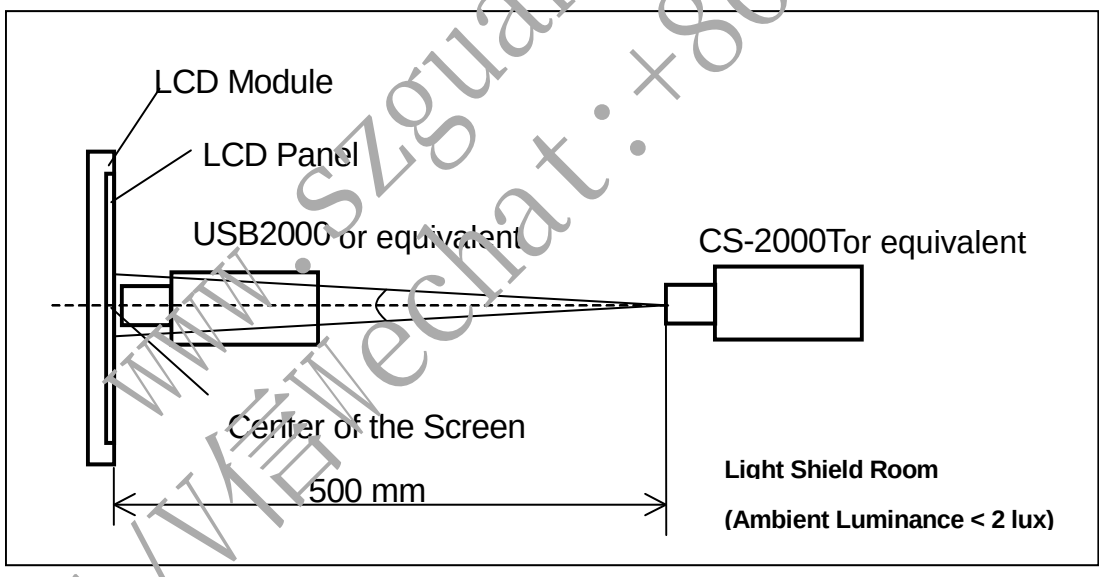
Measure the luminance of White at 5 points

L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note(5)

Note (5) MeasurementSetup:

The LCD module should be stabilized at given temperature for20 minutes to avoid abrupt temperature change during measuring.In order to stabilize the luminance, the measurement should be executed after lighting Backlight for20 minutes in a windless room.

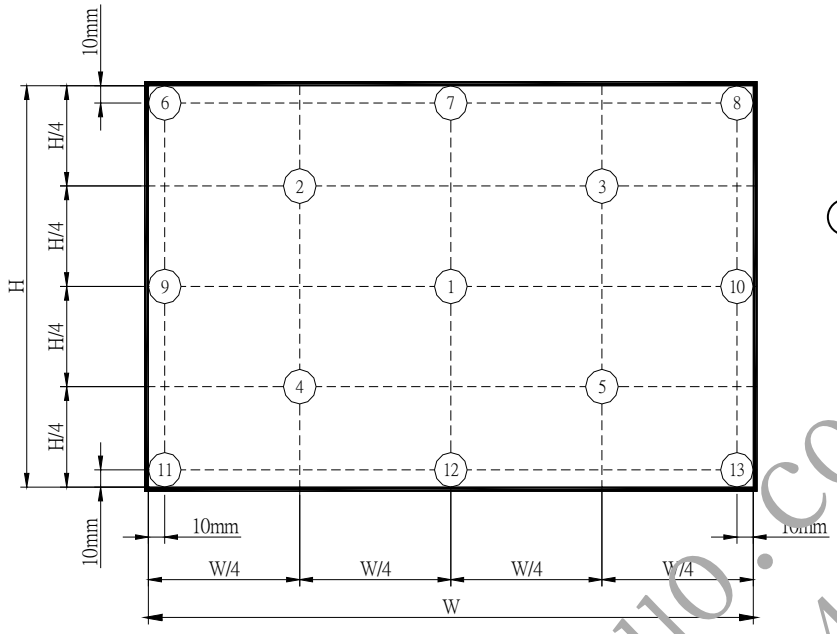


Note (6) Definition of White Variation(δW):

Measure theluminance of gray level 255 at 5 points / 13 points

δW_{5p}={Minimum [L (1) ~ L (5)] / Maximum [L (1) ~ L (5)]}*100%

δW_{13p}={Minimum [L (1) ~ L (13)] / Maximum [L (1) ~ L (13)]}*100%



Ⓧ : Test Point

X=1 to 13

Note(7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted

Note (8) Definition of Blue Light Ratio (BLR)

Measure the luminance of gray level 255 at center points

$$Blue\ Light\ Ratio(BLR) = \left[\frac{Range\ (415\sim455\ nm)}{Range\ (400\sim500\ nm)}\right] x\ 100\%$$

Range (415~455 nm): Light intensity between 415 nm and 455 nm

Range (400~500 nm): Light intensity between 400 nm and 500 nm

BLR = BLR (1)

BLR (X) is corresponding to the Blue Light Ratio of the point X at Figure in Note (6)

Note (9) Definition of Blue light toxicity

Measure the luminance of gray level 255 at center points

$$BLTF = \frac{100}{683} x \int_{380}^{780} L(\lambda) x B(\lambda) x \Delta\lambda \Big/ \int_{380}^{780} L(\lambda) x g(\lambda) x \Delta\lambda$$

in which:

Δ λ = 1

L(λ): spectral irradiance in μW·cm-2·nm-1

B(λ): Blue-Light Hazard Function

g(λ): CIE 1931 RGB luminosity function

683 - maximum spectral luminous efficacy constant (683 lumens per Watt at 555 nm)

6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60ºC, 240 hours	(1) (2)
Low Temperature Storage Test	-20ºC, 240 hours	
Thermal Shock Storage Test	-20ºC, 0.5hour←→60℃, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	50ºC, 240 hours	
Low Temperature Operation Test	0ºC, 240 hours	
High Temperature & High Humidity Operation Test	50℃, 80% RH, 240 hours	
ESD Test (Operation)	150pF, 330Ω, 1sec/cycle Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±15KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave, 1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect.

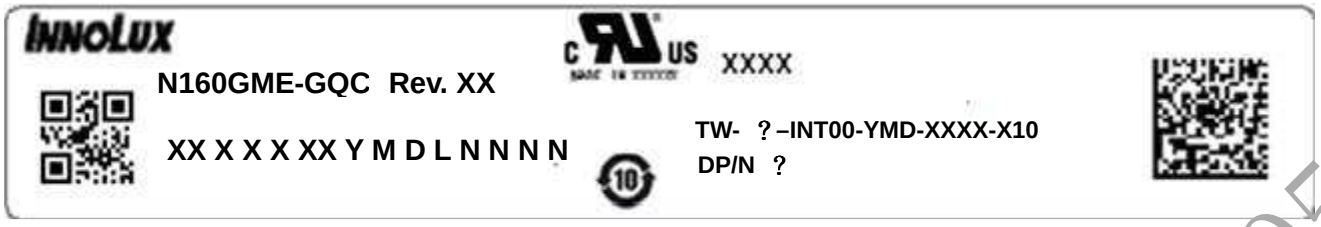
Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

7. PACKING

7.1 MODULE LABEL

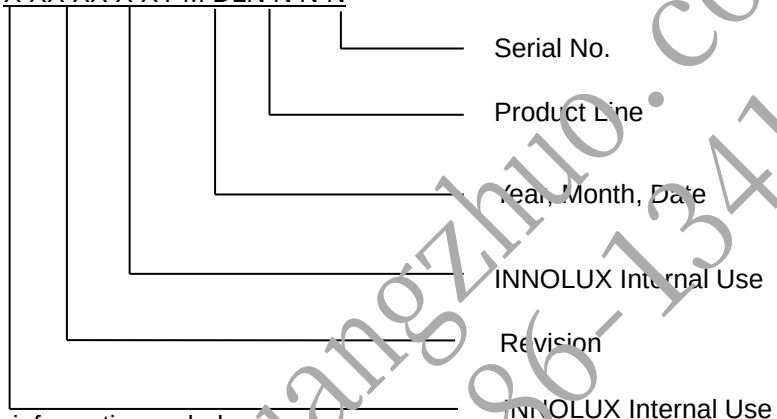
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: N160GME-GQC

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X XX XX X XY M DLN N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year:0~9, for 2010~2019

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

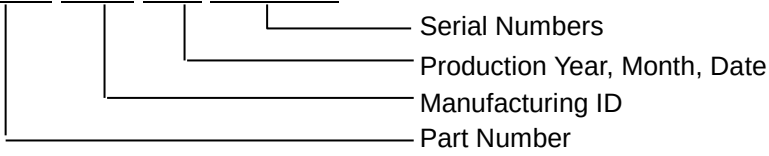
(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

(e) UL Logo : XXXX is UL factory ID.

(f) Dell 2D label contains information as below:

(f-1) Serial ID: TW-0SSSSS-INT00-YMD-XXXX-ZZZ



(f-1-1) Corresponding LCM Fab code XXXXX is as below

-INT00 : Tainan J001 and J003

(f-2) Production location: Made in XXXX.

(f-3) ZZZ:Revision code: X00, X10, X20, A00..etc.

BUILD PHASE	REVISION
SST (WS)	X00, X01, X02, … X09
PT (ES)	X10, X11, X12, … X19
ST (CS)	X20, X21, X23, … X29
XB (MP)	A00, A01, A02, … A99

7.2 DELL Carton LABEL

Dell carton label contains information as below:

(a) PKG ID: 04688-INT00-YMD-XXXXXX-0SSSSS-ZZ

- Dell P/N
- Serial numbers.
- Production Year, Month, Date
- Manufacturing ID

(b) Production location: Made in XXXX.

(c) Revision code: X00, X10, X20, A00..etc.

(d) BOX Quantity:ZZ

(e) DILoc ID&Mfg ID XXXXX INX LCM Fab Code

(e-1)Corresponding LCM Fab code XXXXX is as below.

7.3 CARTON

(1)Box Dimensions : 540(L)*380(W)*315(H)
(2)20 Module/Carton

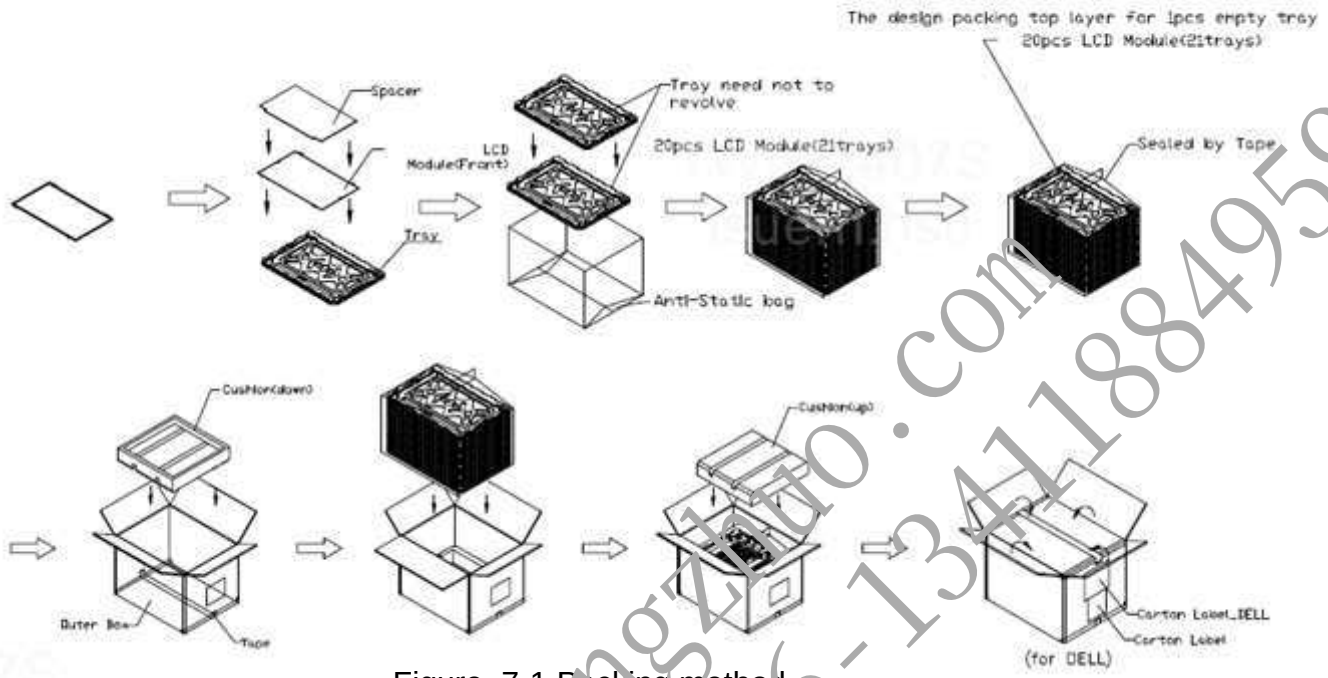


Figure. 7-1 Packing method

7.4 PALLET

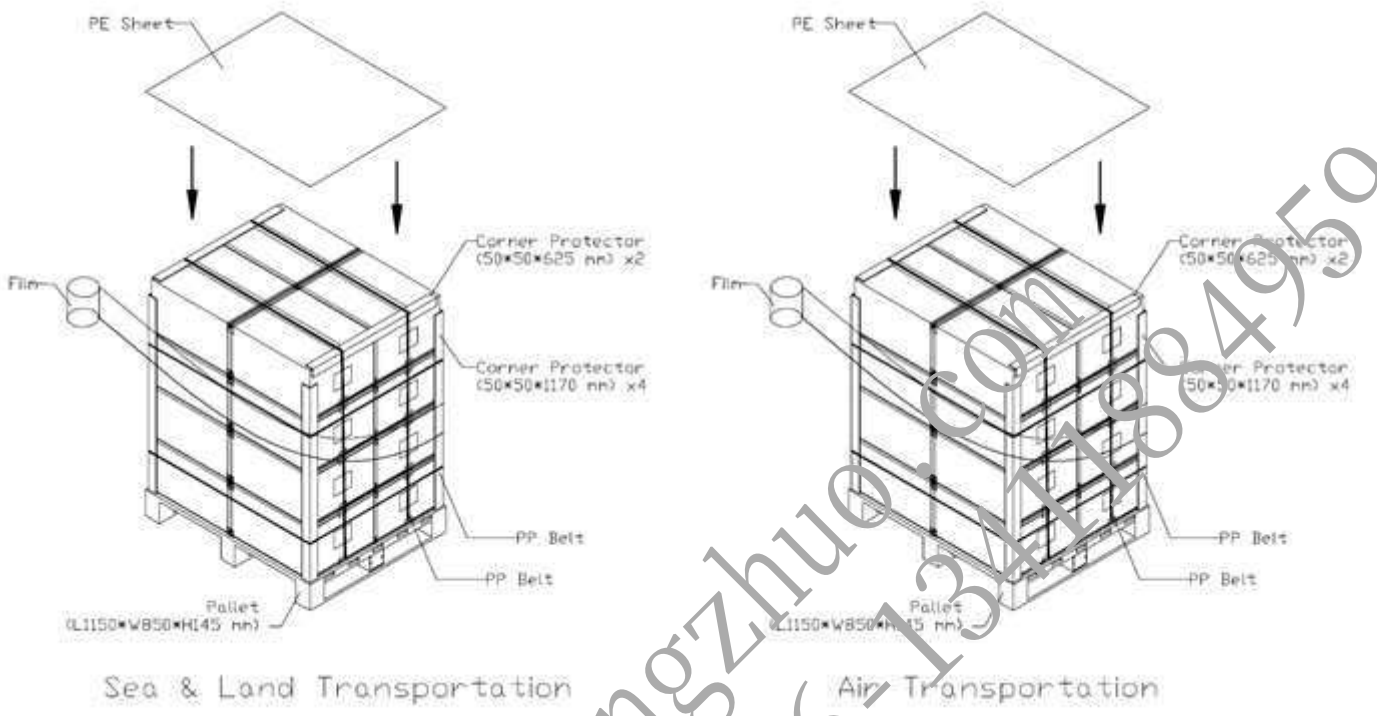


Figure. 7-2 Packing method

7.5 UN-PACKAGING METHOD

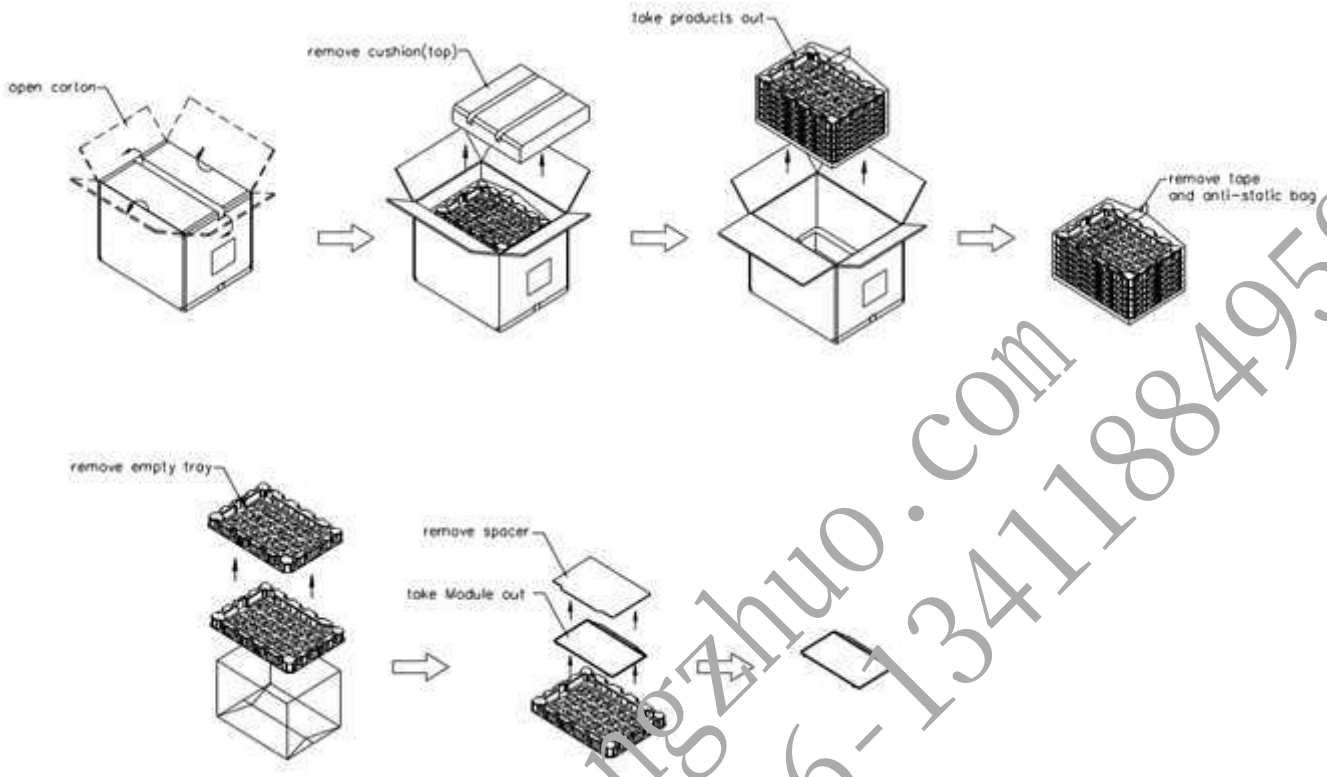


Figure. 7-3 Un-packing method

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

Appendix. EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Appendix. EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
1	00	Header	00	00000000
2	01	Header	FF	11111111
3	02	Header	FF	11111111
4	03	Header	FF	11111111
5	04	Header	FF	11111111
6	05	Header	FF	11111111
7	06	Header	FF	11111111
8	07	Header	00	00000000
9	08	EISA ID manufacturer name ("CMN")	0D	00001101
10	09	EISA ID manufacturer name	AE	10101110
11	0A	ID product code (LSB)	1E	00011110
12	0B	ID product code (MSB)	16	00010110
13	0C	ID S/N (fixed "0")	00	00000000
14	0D	ID S/N (fixed "0")	00	00000000
15	0E	ID S/N (fixed "0")	00	00000000
16	0F	ID S/N (fixed "0")	00	00000000
17	10	Week of manufacture ("09")	09	00001001
18	11	Year of manufacture ("2022")	20	00100000
19	12	EDID structure version ("1")	01	00000001
20	13	EDID revision ("4")	04	00000100
21	14	Video I/P definition ("Digital")	A5	10100101
22	15	Active area horizontal ("34.468cm")	22	00100010
23	16	Active area vertical ("21.542cm")	16	00010110
24	17	Display Gamma (Gamma = "2.2")	78	01111000
25	18	Feature support ("RGB, Continous")	03	00000011
26	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	0F	00001111
27	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	95	10010101
28	1B	Rx=0.68	AE	10101110
29	1C	Ry=0.32	52	01010010
30	1D	Gx=0.265	43	01000011
31	1E	Gy=0.69	B0	10110000
32	1F	Bx=0.15	26	00100110
33	20	By=0.06	0F	00001111
34	21	Wx=0.313	50	01010000
35	22	Wy=0.329	54	01010100
36	23	Established timings 1	00	00000000
37	24	Established timings 2	00	00000000
38	25	Manufacturer's reserved timings	00	00000000
39	26	Standard timing ID # 1	01	00000001
40	27	Standard timing ID # 1	01	00000001
41	28	Standard timing ID # 2	01	00000001
42	29	Standard timing ID # 2	01	00000001

43	2A	Standard timing ID # 3	01	00000001
44	2B	Standard timing ID # 3	01	00000001
45	2C	Standard timing ID # 4	01	00000001
46	2D	Standard timing ID # 4	01	00000001
47	2E	Standard timing ID # 5	01	00000001
48	2F	Standard timing ID # 5	01	00000001
49	30	Standard timing ID # 6	01	00000001
50	31	Standard timing ID # 6	01	00000001
51	32	Standard timing ID # 7	01	00000001
52	33	Standard timing ID # 7	01	00000001
53	34	Standard timing ID # 8	01	00000001
54	35	Standard timing ID # 8	01	00000001
55	36	Detailed timing description # 1 Pixel clock ("282.67"MHz, According to VESA CVT Rev1.4)	6B	01101011
56	37	# 1 Pixel clock (hex LSB first)	6E	01101110
57	38	# 1 H active ("2560")	00	00000000
58	39	# 1 H blank ("160")	A0	10100000
59	3A	# 1 H active : H blank ("2560 : 160")	A0	10100000
60	3B	# 1 V active ("1600")	40	01000000
61	3C	# 1 V blank ("132")	84	10000100
62	3D	# 1 V active : V blank ("1600 : 132")	60	01100000
63	3E	# 1 H sync offset ("48")	30	00110000
64	3F	# 1 H sync pulse width ("32")	20	00100000
65	40	# 1 V sync offset : V sync pulse width ("6 : 10")	6A	01101010
66	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width ("48 : 32 : 6 : 10")	00	00000000
67	42	# 1 H image size ("344 mm")	58	01011000
68	43	# 1 V image size ("215 mm")	D7	11010111
69	44	# 1 H image size : V image size	10	00010000
70	45	# 1 H boarder ("0")	00	00000000
71	46	# 1 V boarder ("0")	00	00000000
72	47	Non-interlaced, Normal Display, Digital separate, Negative Hsync, Negative Vsync	1A	00011010
73	48	# 2 Dummy Descriptor	00	00000000
74	49	# 2 Dummy Descriptor	00	00000000
75	4A	# 2 Dummy Descriptor	00	00000000
76	4B	# 2 Dummy Descriptor Tag Number	10	00010000
77	4C	# 2 Dummy Descriptor	00	00000000
78	4D	# 2 Dummy	00	00000000
79	4E	# 2 Dummy	00	00000000
80	4F	# 2 Dummy	00	00000000
81	50	# 2 Dummy	00	00000000
82	51	# 2 Dummy	00	00000000
83	52	# 2 Dummy	00	00000000
84	53	# 2 Dummy	00	00000000
85	54	# 2 Dummy	00	00000000
86	55	# 2 Dummy	00	00000000
87	56	# 2 Dummy	00	00000000
88	57	# 2 Dummy	00	00000000
89	58	# 2 Dummy	00	00000000
90	59	# 2 Dummy	00	00000000
91	5A	Flag	00	00000000

92	5B	Flag	00	00000000
93	5C	Flag	00	00000000
94	5D	Data Type Tag: Alphanumeric Data String (ASCII)	FE	11111110
95	5E	Flag	00	00000000
96	5F	Dell P/N 1st Character "T"	54	01010100
97	60	Dell P/N 2nd Character "6"	36	00110110
98	61	Dell P/N 3rd Character "G"	47	01000111
99	62	Dell P/N 4th Character "3"	33	00110011
100	63	Dell P/N 5th Character "6"	36	00110110
101	64	EDID Revision	00	00000000
102	65	Manufacturer P/N "1"	31	00110001
103	66	Manufacturer P/N "6"	36	00110110
104	67	Manufacturer P/N "0"	30	00110000
105	68	Manufacturer P/N "G"	47	01000111
106	69	Manufacturer P/N "M"	4D	01001101
107	6A	Manufacturer P/N "E"	45	01000101
108	6B	New line character indicates end of ASCII string	0A	00001010
109	6C	Flag	00	00000000
110	6D	Flag	00	00000000
111	6E	Flag	00	00000000
112	6F	Data Type Tag: Manufacturer Specified Data 00	00	00000000
113	70	Flag	00	00000000
114	71	Color Management	02	00000010
115	72	Panel Type and Revision	41	01000001
116	73	Frame Rate	0F	00001111
117	74	Light Controller Interface and Maximum Luminance	9E	10011110
118	75	Front Surface / Polarizer and Pixel Structure	00	00000000
119	76	Multi-Media Features	00	00000000
120	77	Multi-Media Features	00	00000000
121	78	Special Features	00	00000000
122	79	Special Features	0F	00001111
123	7A	Special Features	41	01000001
124	7B	New line character indicates end of ASCII string	0A	00001010
125	7C	Padding with "Blank" character	20	00100000
126	7D	Padding with "Blank" character	20	00100000
127	7E	Extension flag	01	00000001
128	7F	Checksum	74	01110100
129	80	DisplayID EDID extension block tag	70	01110000
130	81	DisplayID version revision	20	00100000
131	82	section size	79	01111001
132	83	product type identifier	02	00000010
133	84	extension count	00	00000000
134	85	data block tag = type 1 timing detailed	22	00100010
135	86	block revision = 00	00	00000000
136	87	Number of payload bytes in block = (N x 20), 1<=N<=12	14	00010100
137	88	Pixel Clk/1000 [low bit]	00	00000000
138	89	Pixel Clk/1000 [middle bit]	EE	11101110
139	8A	Pixel Clk/1000 [high bit]	11	00010001
140	8B	timing option [prefered 'detailed' timing, No streo, 16:10']	85	10000101
141	8C	Horizontal Active [low bit]	FF	11111111

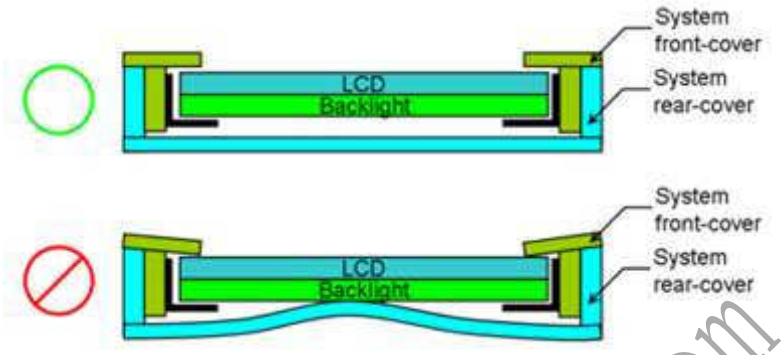
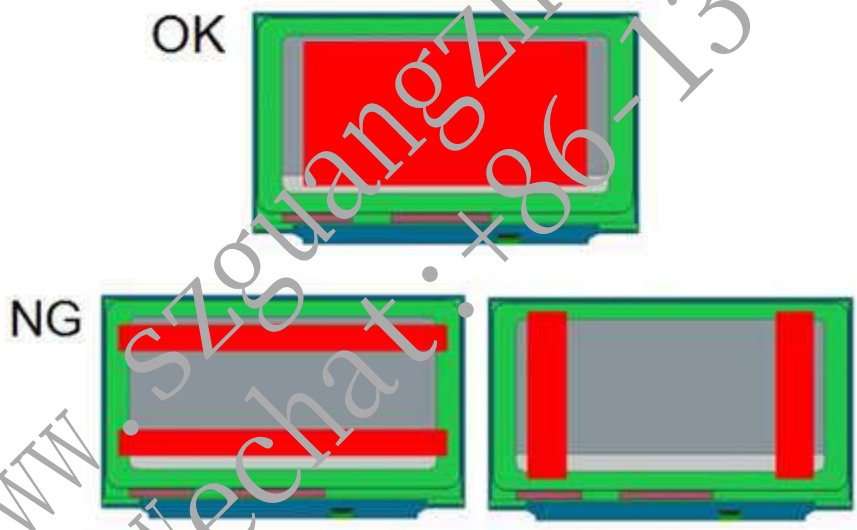
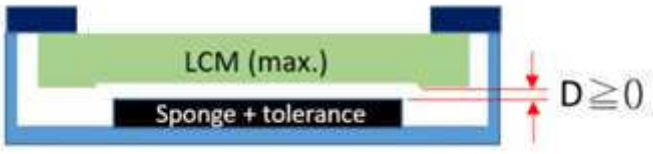
142	8D	Horizontal Active [high bit]	09	00001001
143	8E	Horizontal blank [low bit]	9F	10011111
144	8F	Horizontal blank [high bit]	00	00000000
145	90	Horizontal offset (front porch) [low bit]	2F	00101111
146	91	Horizontal offset (front porch) [high bit] / Horizontal sync polarity = Positive	00	00000000
147	92	Horizontal Sync width [low bit]	1F	00011111
148	93	Horizontal Sync width [high bit]	00	00000000
149	94	Vertical Active [low bit]	3F	00111111
150	95	Vertical Active [high bit]	06	00000110
151	96	Vertical blank [low bit]	C7	11000111
152	97	Vertical blank [high bit]	00	00000000
153	98	Vertical offset (front porch) [low bit]	05	00000101
154	99	Vertical offset (front porch) [high bit] / Vertical sync polarity = Negative	00	00000000
155	9A	Vertical Sync width [low bit]	09	00001001
156	9B	Vertical Sync width [high bit]	00	00000000
157	9C	data block tag = Dynamic Video Timing Range Limits	25	00100101
158	9D	block revision = 01	01	00000001
159	9E	Number of payload bytes in block = 09	09	00001001
160	9F	Minimum Pixel Clk/1,000 [low bit]	00	00000000
161	A0	Minimum Pixel Clk/1,000 [middle bit]	EE	11101110
162	A1	Minimum Pixel Clk/1,000 [high bit]	11	00010001
163	A2	Maximum Pixel Clk/1,000 [low bit]	00	00000000
164	A3	Maximum Pixel Clk/1,000 [middle bit]	EE	11101110
165	A4	Maximum Pixel Clk/1,000 [high bit]	11	00010001
166	A5	Minimum Vertical Refresh Rate	3C	00111100
167	A6	Maximum Vertical Refresh Rate:Bits 7:0	F0	11110000
168	A7	Dynamic Video Timing Range Support Flags/Maximum Vertical Refresh Rate s :Bits 9:8	80	10000000
169	A8	CTA [DID Data block tag:81]	81	10000001
170	A9	Block version :00	00	00000000
171	AA	Number of payload bytes	13	00010011
172	AB	AMD VSDB Header	72	01110010
173	AC	AMD IEEE OUI Value	1A	00011010
174	AD	AMD IEEE OUI Value	00	00000000
175	AE	AMD IEEE OUI Value	00	00000000
176	AF	VSDB Version	03	00000011
177	B0	Free sync Capability	01	00000001
178	B1	Min refresh Rate [Hz]	3C	00111100
179	B2	Max refresh Rate [Hz]	F0	11110000
180	B3	Free sync MCCS VCP Code	00	00000000
181	B4	Supported WCG and HDR feature	00	00000000
182	B5	Max Luminance 1	00	00000000
183	B6	Min Luminance 1	00	00000000
184	B7	Max Luminance 2	00	00000000
185	B8	Min Luminance 2	00	00000000
186	B9	Max refresh Rate [Hz]:Bits 7:0	F0	11110000
187	BA	Max refresh Rate [Hz]:Bist 9:8	00	00000000
188	BB	VSDB Block Reserved	00	00000000
189	BC	VSDB Block Reserved	00	00000000
190	BD	VSDB Block Reserved	00	00000000

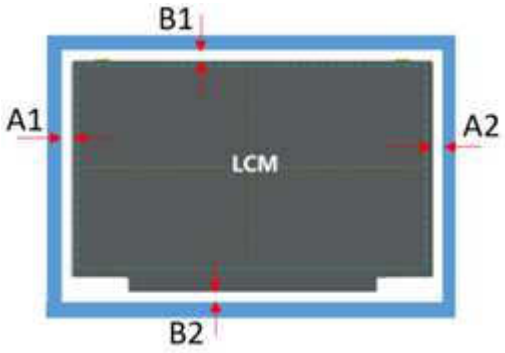
191	BE	Reserved	00	00000000
192	BF	Reserved	00	00000000
193	C0	Reserved	00	00000000
194	C1	Reserved	00	00000000
195	C2	Reserved	00	00000000
196	C3	Reserved	00	00000000
197	C4	Reserved	00	00000000
198	C5	Reserved	00	00000000
199	C6	Reserved	00	00000000
200	C7	Reserved	00	00000000
201	C8	Reserved	00	00000000
202	C9	Reserved	00	00000000
203	CA	Reserved	00	00000000
204	CB	Reserved	00	00000000
205	CC	Reserved	00	00000000
206	CD	Reserved	00	00000000
207	CE	Reserved	00	00000000
208	CF	Reserved	00	00000000
209	D0	Reserved	00	00000000
210	D1	Reserved	00	00000000
211	D2	Reserved	00	00000000
212	D3	Reserved	00	00000000
213	D4	Reserved	00	00000000
214	D5	Reserved	00	00000000
215	D6	Reserved	00	00000000
216	D7	Reserved	00	00000000
217	D8	Reserved	00	00000000
218	D9	Reserved	00	00000000
219	DA	Reserved	00	00000000
220	DB	Reserved	00	00000000
221	DC	Reserved	00	00000000
222	DD	Reserved	00	00000000
223	DE	Reserved	00	00000000
224	DF	Reserved	00	00000000
225	E0	Reserved	00	00000000
226	E1	Reserved	00	00000000
227	E2	Reserved	00	00000000
228	E3	Reserved	00	00000000
229	E4	Reserved	00	00000000
230	E5	Reserved	00	00000000
231	E6	Reserved	00	00000000
232	E7	Reserved	00	00000000
233	E8	Reserved	00	00000000
234	E9	Reserved	00	00000000
235	EA	Reserved	00	00000000
236	EB	Reserved	00	00000000
237	EC	Reserved	00	00000000
238	ED	Reserved	00	00000000
239	EE	Reserved	00	00000000
240	EF	Reserved	00	00000000
241	F0	Reserved	00	00000000

242	F1	Reserved	00	00000000
243	F2	Reserved	00	00000000
244	F3	Reserved	00	00000000
245	F4	Reserved	00	00000000
246	F5	Reserved	00	00000000
247	F6	Reserved	00	00000000
248	F7	Reserved	00	00000000
249	F8	Reserved	00	00000000
250	F9	Reserved	00	00000000
251	FA	Reserved	00	00000000
252	FB	Reserved	00	00000000
253	FC	Reserved	00	00000000
254	FD	Reserved	00	00000000
255	FE	Checksum	83	10000011
256	FF	Checksum	90	10010000

Appendix. OUTLINE DRAWING

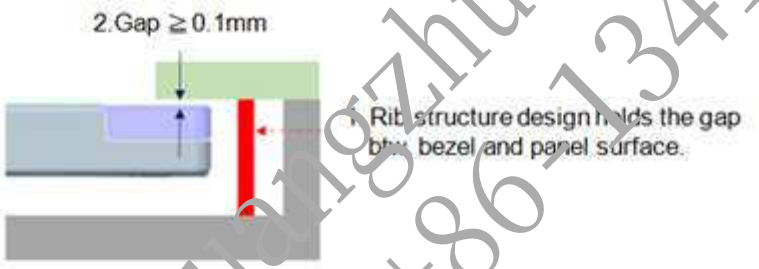
Appendix. SYSTEM COVER DESIGN GUIDANCE

0.	**Permanent deformation of system cover after reliability test**
	
Definition	System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
1	**Sponge area design behind panel**
	
Definition	Sponge area design behind panel can not be across the panel metal rear and the reflector at the same time. It can be on the reflector area only.
2	**Gap between system rear-cover & panel**
	
Definition	The maximum thickness of sponge on the system rear-cover can not interfere to the maximum thickness of panel. Because the interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
3	**Gap Design between panel & around structure**

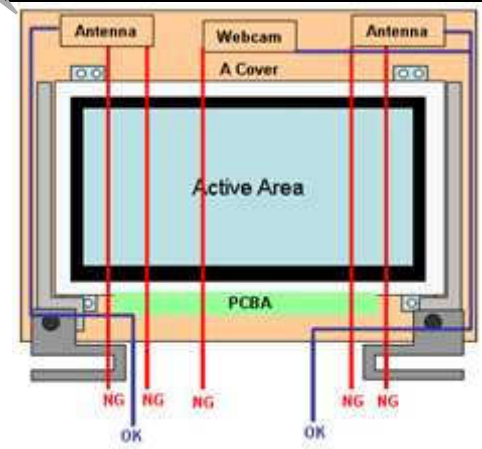


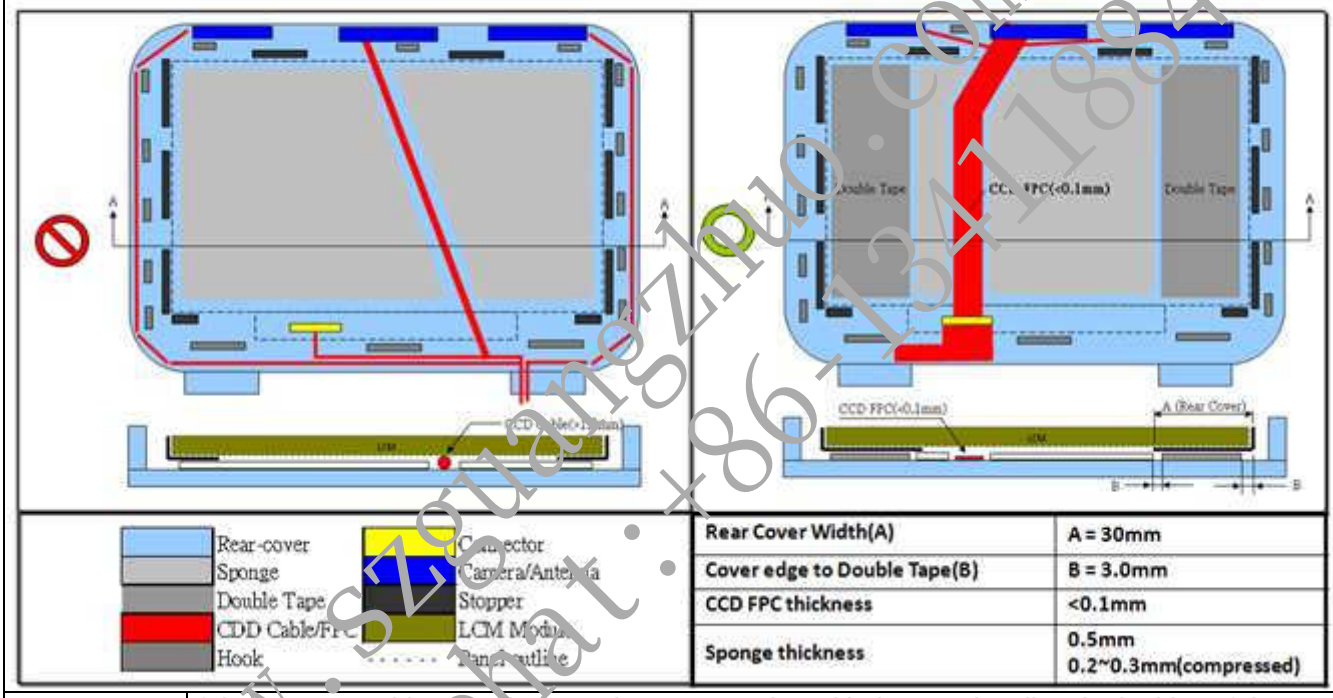
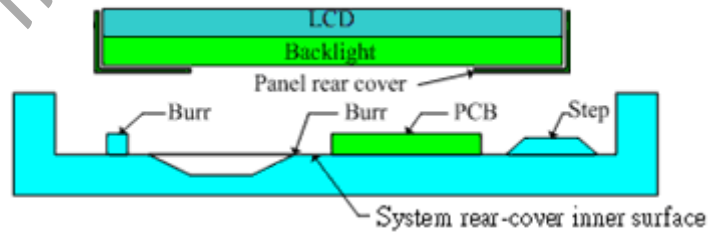
Item	Suggestion	Remark
A1	A1≧0.5	Gap ≧ Panel outline max. tolerance + Assembly max. tolerance
A2	A2≧0.5	
B1	B1≧0.5	
B2	B2≧0.8	

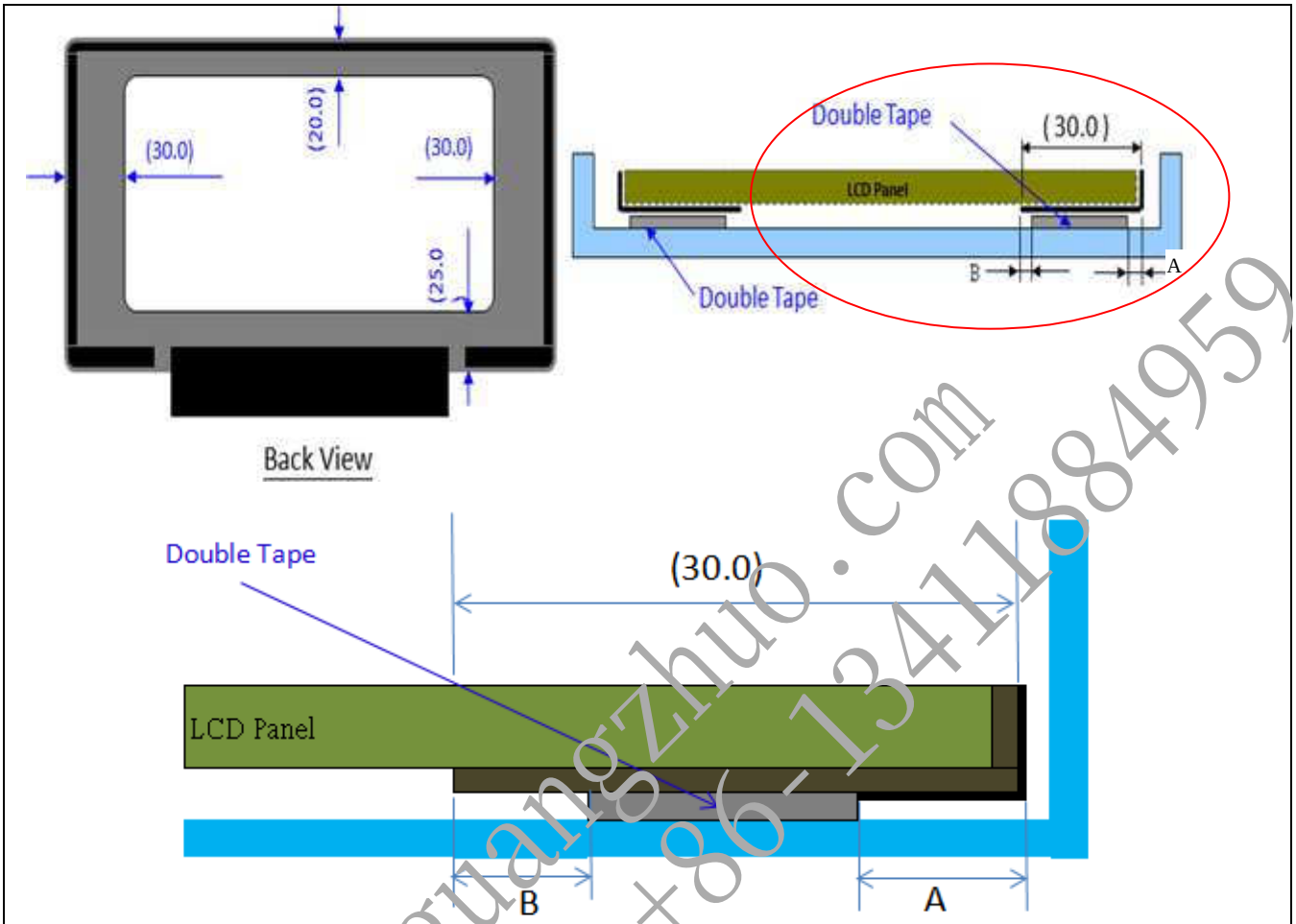
Definition	Gap Design between panel & around structure needs to consider the maximum tolerances of panel outline and assembly at the same time. Gap Design suggestion is shown as A1/A2/B1/B2 on the chart.
4	**Gap between panel & bezel**

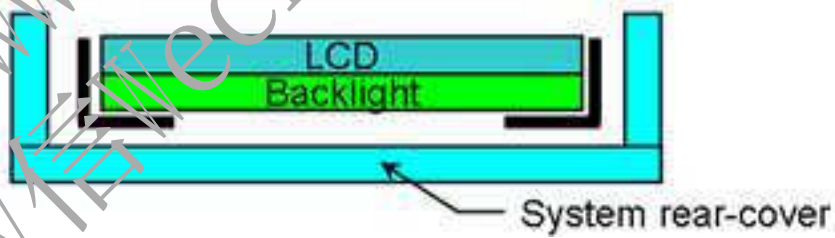


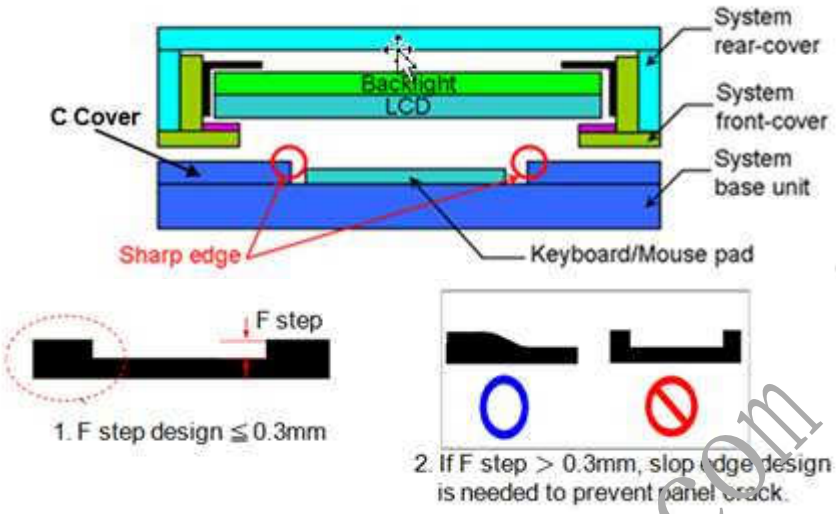
Definition	The gap between system bezel & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system front-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test or during pooling inspection procedure. To remain the sufficient gap, design with system rib higher than maximum panel thickness is recommended. The sufficient gap design is greater or equal to 0.1mm.
5	**Cable routing behind panel**



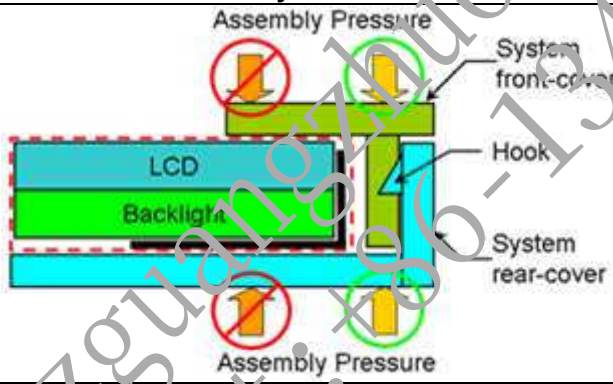
Definition	It is strongly recommended that cables route around the panel outline, not overlap with the panel outline (including PCB). Because issue such as abnormal display & white spot after backpack test, hinge test, twist test or pogo test may occur. If any routings across panel outline are needed, we suggest design as below: -Using FFC/FPC to replace cables. -Routing at the right or left area of panel metal rear. -Avoid any routings at the step of panel or A cover. -No interference to panel. -It should not overlap TCON, COF/FPC, Driver IC
6	**Interference examination of antenna cable and Web Cam wire**
	• To prevent panel damage, we suggest using CCD FPC to replace CCD cable • Using double tape to fix LCM module for no bracket design.  Rear Cover Width(A) A = 30mm Cover edge to Double Tape(B) B = 3.0mm CCD FPC thickness <0.1mm Sponge thickness 0.5mm 0.2~0.3mm(compressed)
	If the antenna cable or Web Cam wire must overlap with the panel outline, both sides of the antenna cable or Web Cam wire must have a sponge(Sponge material can not contain NH3) and sponge require higher antenna cable or Web Cam wire.(Antenna cable or Web Cam wire should not overlap with TCON,COF/FPC,Driver IC) Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
7	**System rear-cover inner surface examination**
	
Definition	Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.
8	**Tape/sponge design on system inner surface**



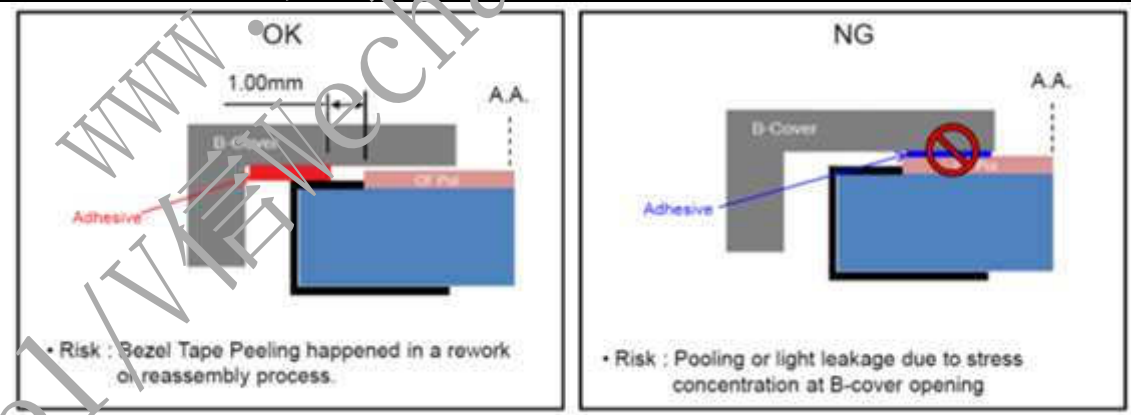
Definition	To prevent peeling the bezel tape in rework process. The length of double tape is 30 – (A+B), A is bezel tape length and B is the double tape attaching tolerance. Ex :A :2mm, B:2mm, the length of double tape is 30-(2+2)=26mm.
9	**Material used for system rear-cover**
	 System rear-cover material: Al-Mg alloy System rear-cover thickness:1.5mm MIN
Definition	System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.
10	**C cover shape design**



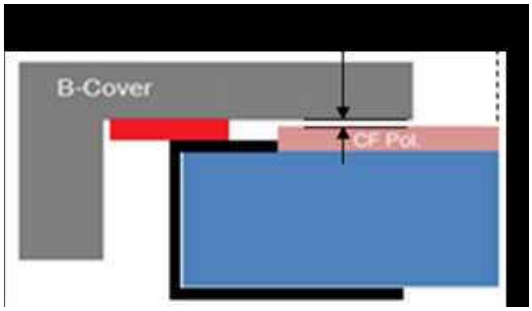
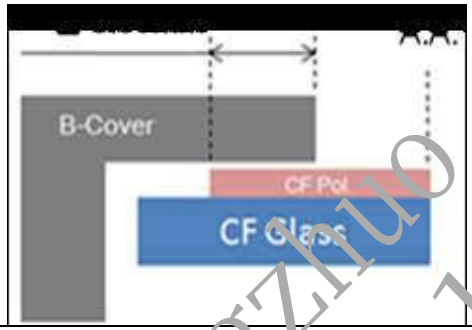
Definition	The F step design on C Cover less than or equal to 0.3mm is recommended. If F step exceeds 0.3mm, the slop edge design is necessary to prevent panel crack.
11	**Assembly SOP examination for system front-cover with Hook design**



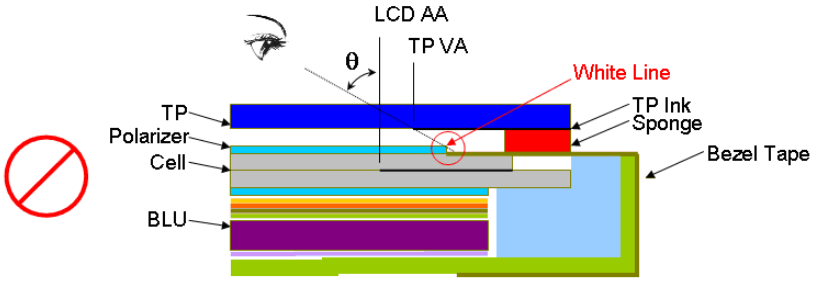
Definition	To prevent panel crack during system front-cover assembly process with hook design, it is not recommended to press panel or any location that related directly to the panel.
12	**Adhesive design between panel & bezel**

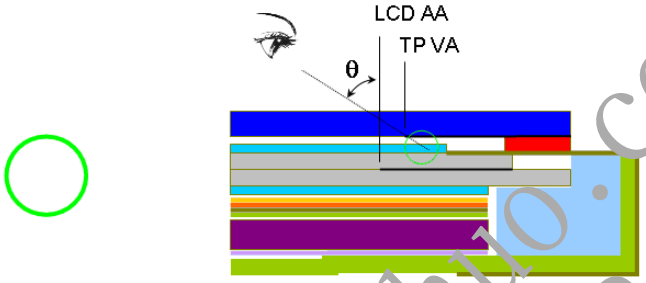


Definition	To prevent panel crack during system front-cover assembly process with double tape design, When system applied adhesive between B-Cover and LCD module, please design a distance 1.00mm between B-Cover's adhesive and CF pol. Do **NOT** put adhesive on CF pol. Adhesive material need be qualified to prevent from doing damage to cell tape after rework. Adhesive material need be qualified to prevent abnormal noise when hinge swinging test.
13	**System front-cover assembly reference with Double tape design**

	
Definition	To prevent system front-cover peeling at double tape contact area, A gap between B-Cover & CF-Pol. Is 0.1mm min.
14	System front-cover opening area reference with TFT-LCD module
	
Definition	To prevent panel the noise of B-cover & CF Pol. Distance from CF Pol. edge to front-cover edge more than 0.65mm.

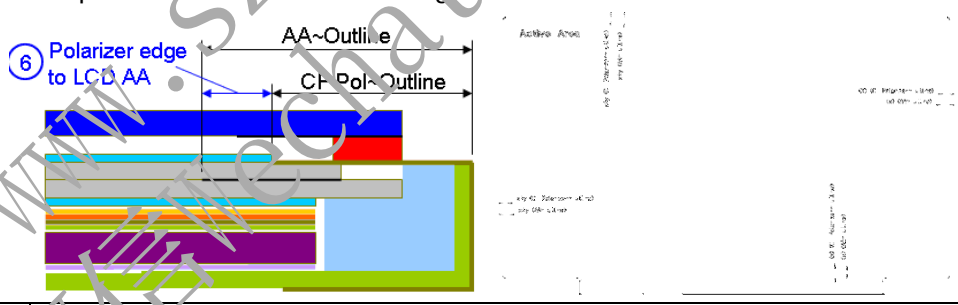
15	Touch Application : TP and LCD Module Combination for White Line Prevention



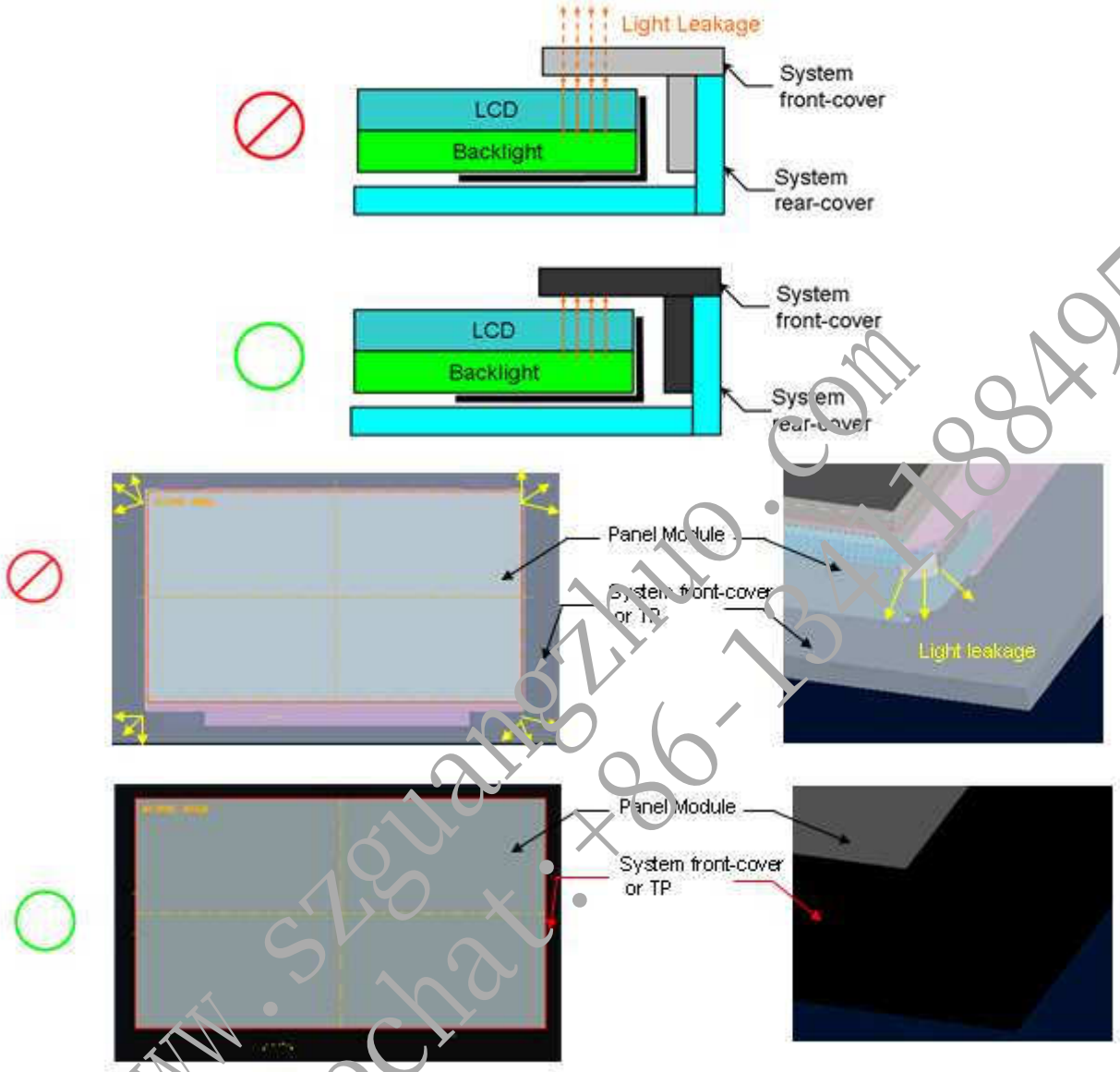


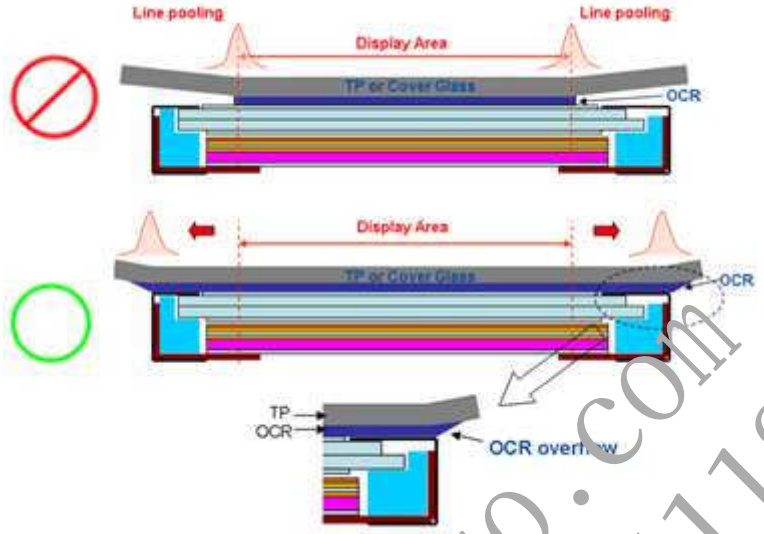
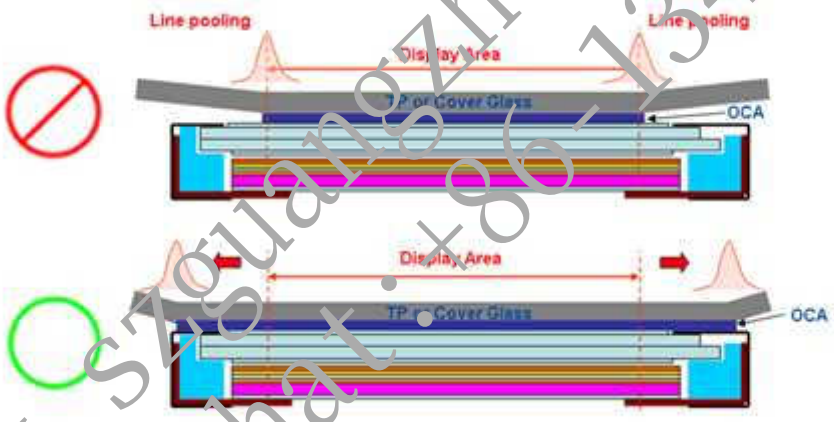
Parameter consideration for White Line Issue :	
1	TP VA to LCD AA distance
2	TP Assembly tolerance
3	TP Ink Printing tolerance
4	Sponge thickness and tolerance
5	Inspection Viewing Angle specification
6	Polarizer edge to LCD AA distance and tolerance

Polarizer edge to LCD AA distance can be derived by “AA~Outline” – “CF Pol~Outline” with respect to INX 2D Outline Drawing on each side.



Definition	For using in Touch Application: to prevent White Line appears between TP and LCD module combination, the maximum inspection angle location must not fall onto LCD polarizer edge, otherwise light line near edge of polarizer will be appear. Parameters such as TP VA to LCD AA distance, TP assembly tolerance, TP Ink printing tolerance, Sponge thickness and tolerance, and Maximum Inspection/Viewing Angle, must be considered with respect to LCD module’s Polarizer edge location and tolerance. This consideration must be taken at all four edges separately. The goal is to find parameters combination that allow maximum inspection angle falls inside polarizer black margin area. Note: Information for Polarizer edge location and its tolerance can be derived from INX 2D Outline Drawing (“AA ~Outline“ - “CF Pol~Outline”). Note: Please feel free to contact INX FAE Engineer. By providing value of parameters above on each side, we can help to verify and pass the white line risk assessment for customer reference.

16	Color of system front-cover material
	
Definition	To prevent light leakage is seen at system front-cover due to material transparency, we suggest using dark color material (black) for system front-cover design.

17	**Use OCR Lamination**
	
Definition	OCR glue as possible beyond module, in order to avoid Line Pooling
18	**Use OCA Lamination**
	
Definition	OCA glue as possible plastered throughout the module, in order to avoid Line Pooling.

Appendix. LCD MODULE HANDLING MANUAL

Purpose	• **This SOP is prepared to prevent panel dysfunction possibility through incorrect handling procedure.** • **This manual provides guide in unpacking and handling steps.** • **Any person which may contact / related with panel, should follow guide stated in this manual to prevent panel loss.**
1.	**Unpacking**

2.	**Panel Lifting**

Use slots at both sides for finger insertion.
Handle panel upward with care.

3.	Do and Don't

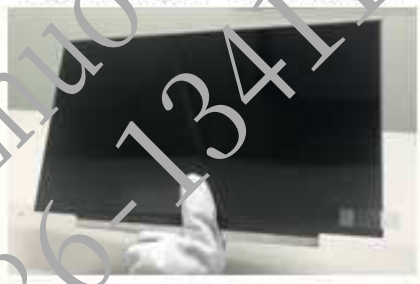
Do :

- Handle with both hands.
- Handle panel at left and right edge.

Don't :

- Lifting with one hand.

- Handle at PCBA side.



Don't :

- Stack panels.

- Press panel.

Don't :

- Put foreign stuff onto panel

- Put foreign stuff under panel

Don't :

- Paste any material unto white reflector sheet

Don't :

- Pull / Push white reflector sheet

Don't :

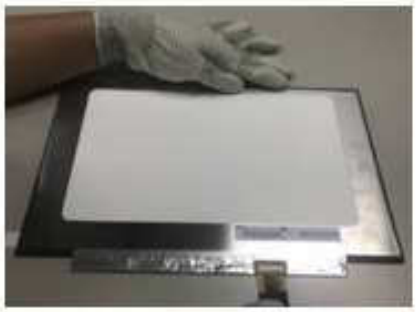
- Hold at panel corner.

Don't :

- Twist panel.

Do :

- Hold panel at top edge while inserting connector.



Don't :

- Press white reflector sheet while inserting connector.

Do :

- Remove panel protector film starts from pull tape

Don't :

- Remove panel protector film From film another side.

Doc. Number:

■ Tentative Specification
☐ Preliminary Specification
☐ Approval Specification

MODEL NO.: N160GME
SUFFIX: GQ1
DPN: Rev.:C1

Customer:

APPROVED BY SIGNATURE

Name / Title
Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By

CONTENTS

REVISION HISTORY

Version	Date	Page	Description
0.0	Nov. 19, 2021	All	Tentative Spec Ver.0.0 was first issued

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N160GME-GQ1 is a 16” TFT Liquid Crystal NB Display module with LED Backlight unit and 40 pins eDP interface. This module supports 2560 x 1600 QHD model and can display 16,777,216 colors. This panel complies with TUV Rheinland low blue light method 2 and is certified as a component under certain conditions.

1.2 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Screen Size	16” diagonal	-	-
Driver Element	IGZO	-	-
Frame Rate	165	Hz	-
Pixel Number	2560 x R.G.B. x 1600	pixel	-
Pixel Pitch	0.13464 (H) x 0.13464 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Interface	eDP 1.4		
Display Colors	16,777,216	color	-
Transmissive Mode	Normally black	-	-
Surface Treatment	Hard coating (3H), High resolution Adaptable AG	-	-
Luminance, White	300	Cd/m2	-
Color Gamut	sRGB 100%	%	-
Power Consumption	Total (6.0) W (Max.) @ cell (2.0)W (Max.), BL (4.0) W (Max.)		-

Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, fv = 165 Hz, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 ºC, whereas MOSAIC pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Glass	Thickness				mm	
Polarizer	Thickness				mm	
Module Size	Horizontal(H)	349.38	349.68	349.98	mm	(1) (2)
	Vertical(V) w/o PCB and Hinge	223.62	223.92	224.22	mm	
	Vertical(V) with PCB	233.92	234.42	234.92	mm	
	Thickness (T) w/o sponge	-	2.45	2.60	mm	
~~Beze Area~~	~~Horizontal~~				~~mm~~	
	~~Vertical~~				~~mm~~	
Active Area	Horizontal	344.58	344.68	344.78	mm	
	Vertical	215.32	215.42	215.52	mm	
Weight		-		325	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Dimensions are measured by caliper.

Note (3) Panel thickness is measured with calipers clamping mylar or tape tightly

2.1 CONNECTOR TYPE

Please refer Appendix Outline Drawing for detail design.

Connector Part No.: IPEX-20682-040E-02

User's connector Part No:IPEX-20679-040T-01

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

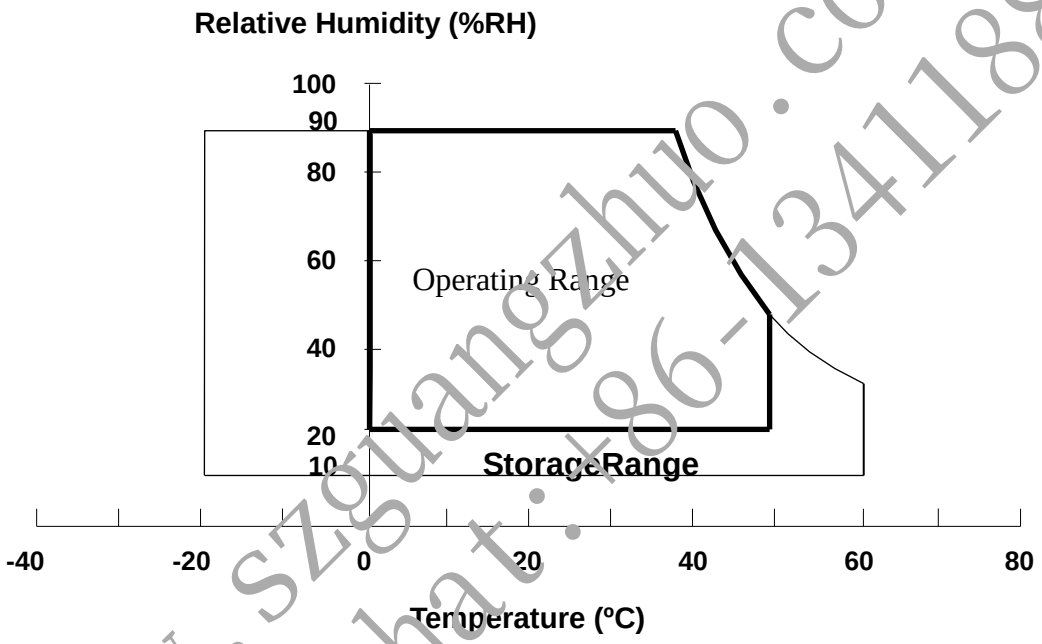
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)

Note (1) (a) 90 %RH Max. (Ta < 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta < 40 ºC).

(c) No condensation.

Note (2) The temperature of panel surface should be 0 ºC min. and 60 ºC max.



3.2 ELECTRICAL ABSOLUTE RATINGS

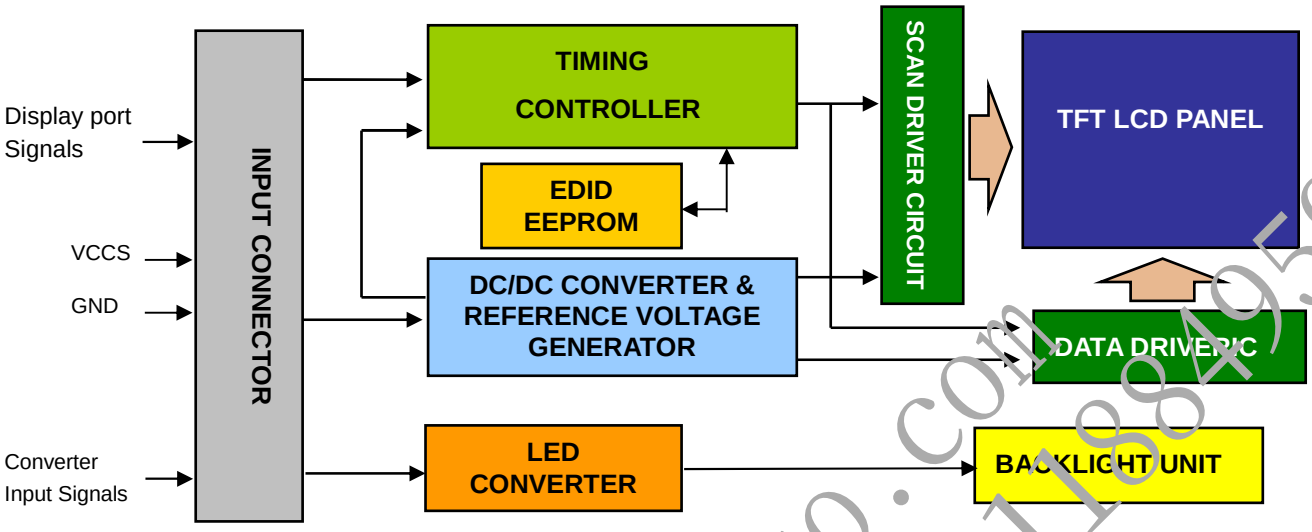
3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	+4.0	V	
Converter Input Voltage	LED_VCCS	-0.3	26	V	(1)
Converter Control Signal Voltage	LED_PWM,	-0.3	5	V	(1)
Converter Control Signal Voltage	LED_EN	-0.3	5	V	(1)

Note (1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “ELECTRICAL CHARACTERISTICS”.

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



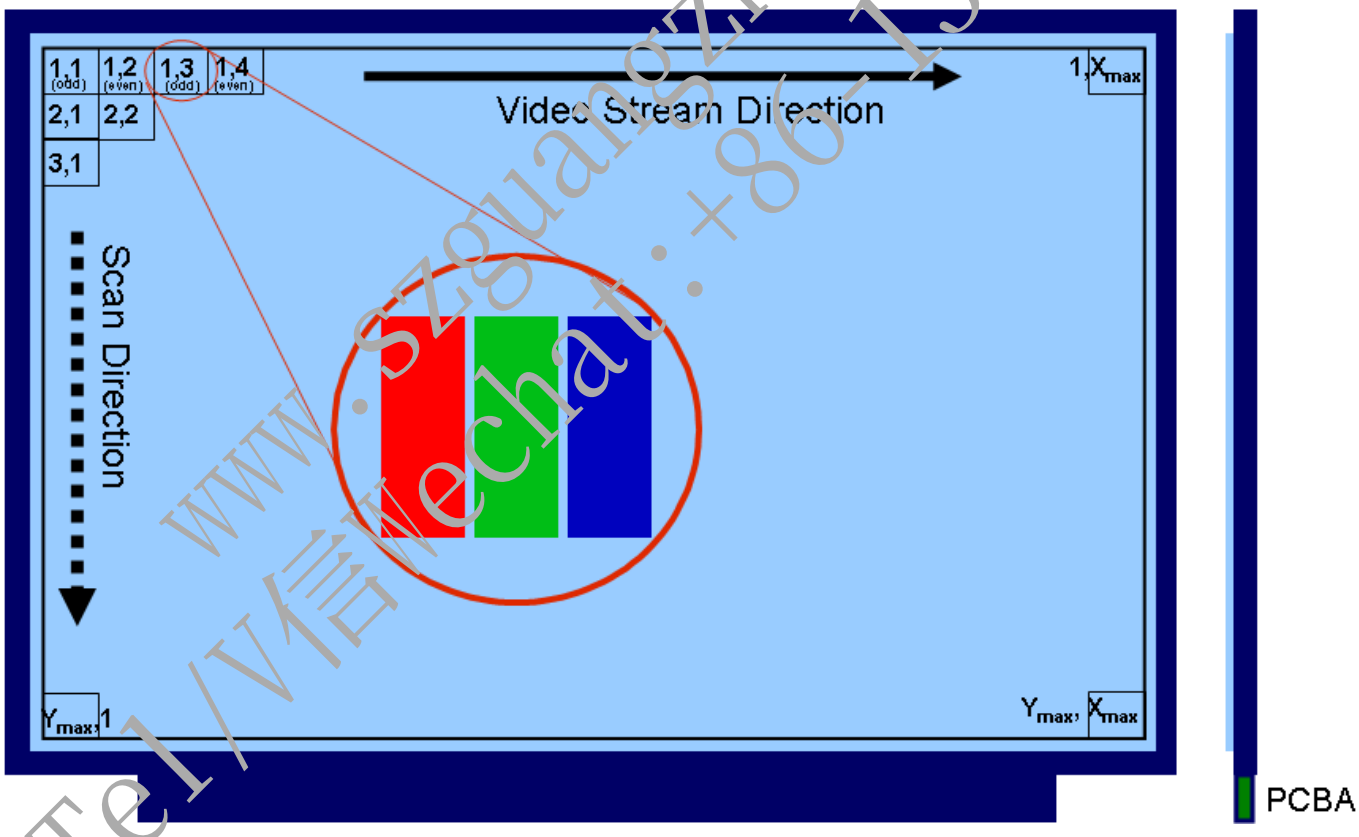
4.2 INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	DDS_SCL	Nvidia DDS, I2C (SCL)	
2	H_GND	High Speed Ground	
3	Lane3_N	Complement Signal Link Lane3	
4	Lane3_P	True Signal Link Lane3	
5	H_GND	High Speed Ground	
6	Lane2_N	Complement Signal Link Lane2	
7	Lane2_P	True Signal Link Lane2	
8	H_GND	High Speed Ground	
9	Lane1_N	Complement Signal Link Lane 1	
10	Lane1_P	True Signal Link Lane 1	
11	H_GND	High Speed Ground	
12	Lane0_N	Complement Signal Link Lane 0	
13	Lane0_P	True Signal Link Lane 0	
14	H_GND	High Speed Ground	
15	AUX_CH_P	True Signal Auxiliary Channel	
16	AUX_CH_N	Complement Signal Auxiliary Channel	
17	H_GND	High Speed Ground	
18	VCCS	LCD logic and driver power	
19	VCCS	LCD logic and driver power	
20	VCCS	LCD logic and driver power	
21	VCCS	LCD logic and driver power	
22	BIST_EN	Panel Built In Self Test Enable	
23	GND	Ground	
24	GND	Ground	
25	GND	Ground	

26	GND	Ground	
27	HPD	Hot Plug Detect	
28	BL_GND	Backlight ground	
29	BL_GND	Backlight ground	
30	BL_GND	Backlight ground	
31	BL_GND	Backlight ground	
32	LED_EN	BL_Enable Signal of LED Converter	
33	LED_PWM	PWM Dimming Control Signal of LED Converter	
34	DDS_SDA	Nvidia DDS, I2C (SDA)	
35	PSR_EN	PSR Enable signal of TCON	PSR disable@ default/High. PSR enable@ Low
36	LED_VCCS	Backlight power	(Support 6.0 ~ 21V)
37	LED_VCCS	Backlight power	(Support 6.0 ~ 21V)
38	LED_VCCS	Backlight power	(Support 6.0 ~ 21V)
39	LED_VCCS	Backlight power	(Support 6.0 ~ 21V)
40	OD_EN	OD Enable signal of TCON	OD function (Disable@ default/High, Enable @ Low)

Note (1) The first pixel is odd as shown in the following figure



Note (2) The setting of BIST, OD and PSR function are as follows.

Pin	Enable	Disable
BIST_EN	Hi	Lo
OD_EN	Hi	Lo
PSR_EN	Lo	High

Hi = High level, Lo = Low level.

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICSSPECIFICATION

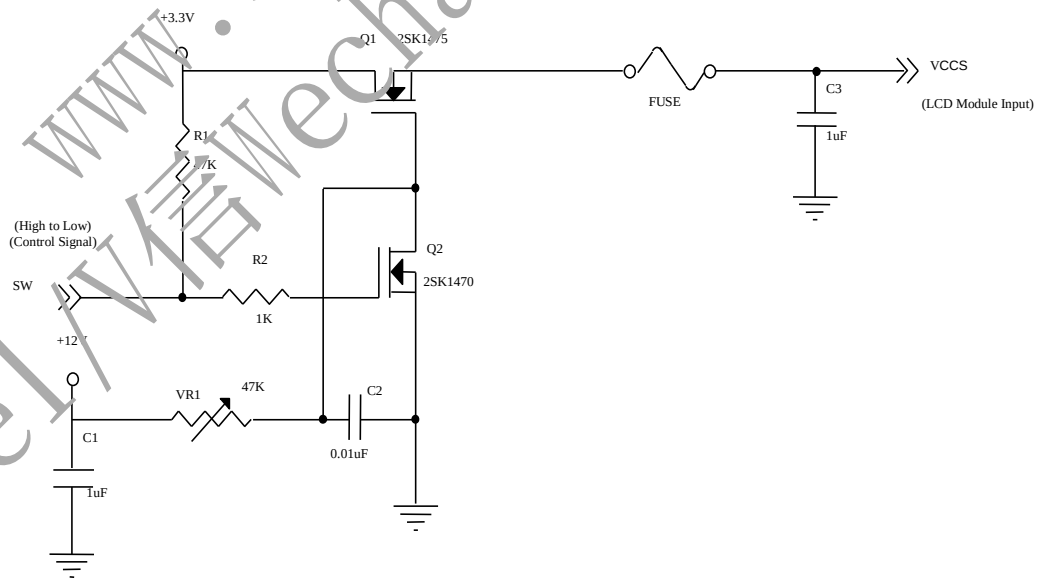
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)
HPD	High Level		2.25	-	3.6	V	(6)
	Low Level		0	-	0.8	V	(6)
HPD Impedance		R_{HPD}	30K	-	-	ohm	(5)
Ripple Voltage		V_{RP}	-	50	-	mV	(1)
BIST_EN Input Voltage	High Level	V_{IHCABC}	2.3	-	3.6	V	(5)
	Low Level	V_{ILCABC}	0	-	0.5	V	(5)
BIST_EN Impedance		R_{CABC_EN}	30K	-	-	ohm	(5)
Inrush Current		I_{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Mosaic	Icc	-	(545)	(606)	mA	(3)
	Black		-	(545)	(606)	mA	(3)
	Solid Pattern		-	(545)	(606)	mA	(3)
	Mosaic@PSR		-	(545)	(606)	mA	(3)
	Solid Pattern@PSR		-	(545)	(606)	mA	(3)
Power per EBL WG		P_{EBL}	-	(2.8)	-	W	(4)

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

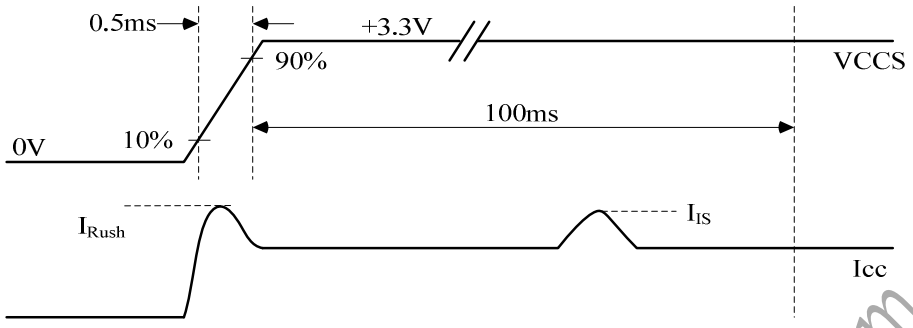
Note (2) I_{RUSH}: the maximum current when VCCS is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.

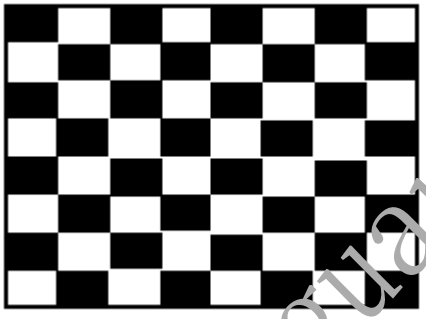


VCCS rising time is 0.5ms



Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ºC, DC Current and f_v = 165Hz, OD enable, whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern



Active Area

b. The solid pattern is the largest one of R/G/B pattern.

c. The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ºC, DC Current and PSR mode enable, whereas a power dissipation check pattern is displayed.

Note (4) The specified power are the sum of LCD panel electronics input power and the converter input power. Test conditions are as follows.

(a) VCCS = 3.3 V, Ta = 25 ± 2 ºC, f_v = 165 Hz,

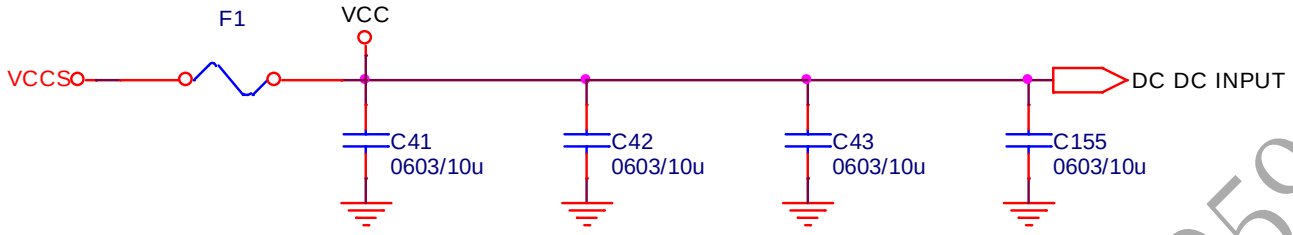
(b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.

(c) Luminance: 60 nits

Note (5) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. Please refer to Note (4) of 4.3.2 LED CONVERTER SPECIFICATION to obtain more information.

Note (6) When a source detects a low-going HPD pulse, it must be regarded as a HPD event. Thus, the source must read the link / sink status field or receiver capability field of the DPCD and take corrective action

Note (7) Input VCC Circuit is as below



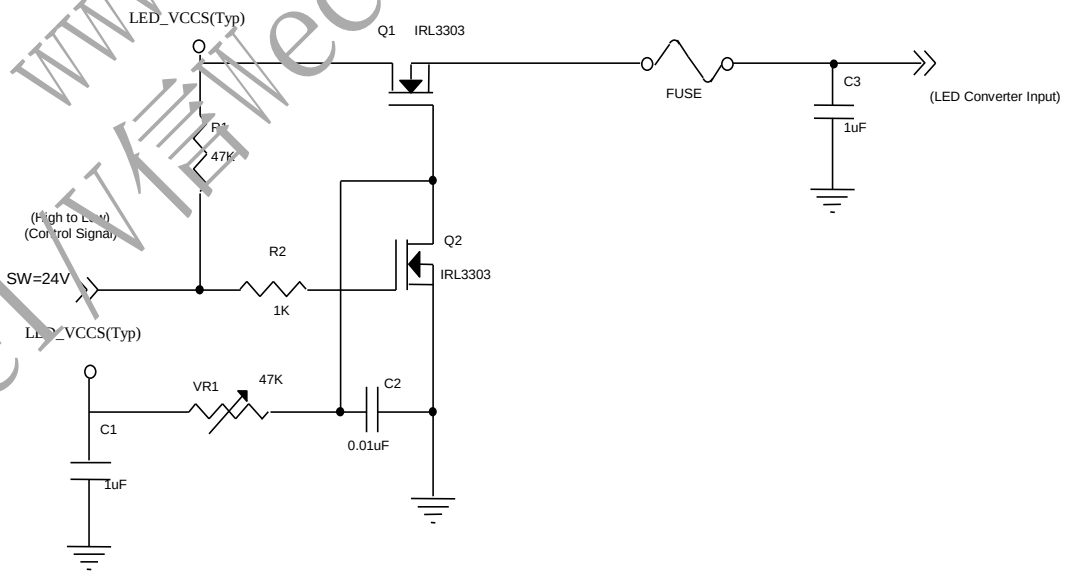
4.3.2 LED CONVERTER SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input Power Supply Voltage		LED_Vccs	6.0	12.0	21.0	V	
Converter Inrush Current		$ILED_{RUSH}$	-	-	1.5	A	(1)
LED_EN Control Level	Backlight On		2.2	-	5.0	V	(4)
	Backlight Off		0	-	0.6	V	(4)
LED_EN Impedance		R_{LED_EN}	30K	-		ohm	(4)
PWM Control Level	PWM High Level		2.2	-	5	V	(4)
	PWM Low Level		0	-	0.6	V	(4)
PWM Impedance		R_{PWM}	30K			ohm	(4)
PWM Control Duty Ratio			5	-	100	%	(5)
PWM Control Permissive Ripple Voltage		V_{PWM_pp}	-	-	100	mV	
PWM Control Frequency		f_{PWM}	190	-	2K	Hz	(2)
LED Power Current	LED_VCCS =Typ.	ILED	(100)	(320)	(333)	mA	(3)

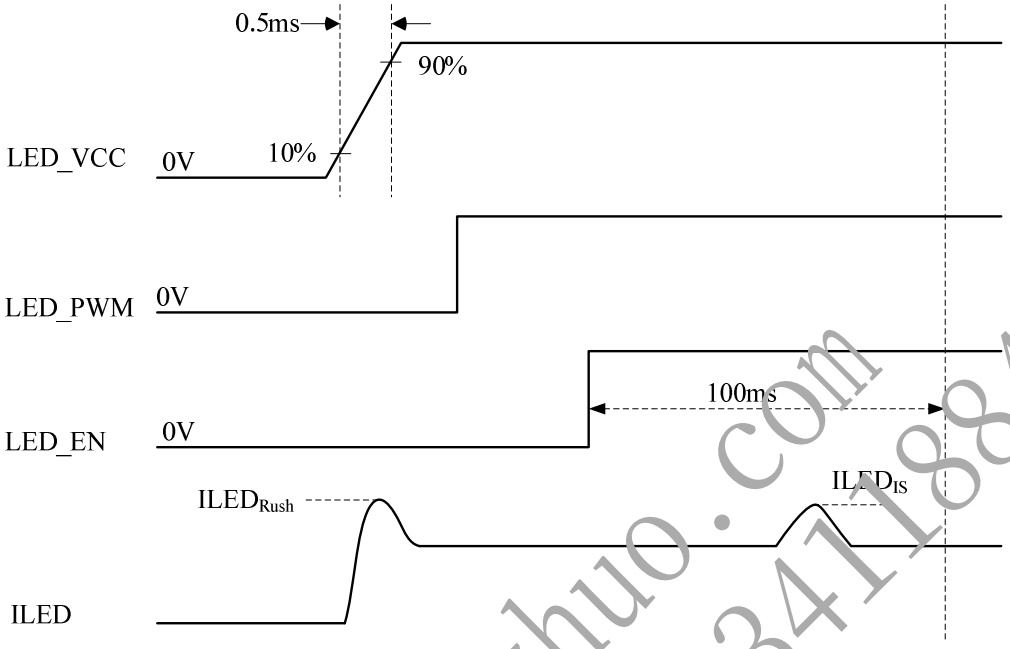
Note (1) $ILED_{RUSH}$: the maximum current when LED_VCCS is rising,

$ILED_{IS}$: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.



VLED rising time is 0.5ms



Note (2) If PWM control frequency is applied in the range less than 1KHz, the "waterfall" phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

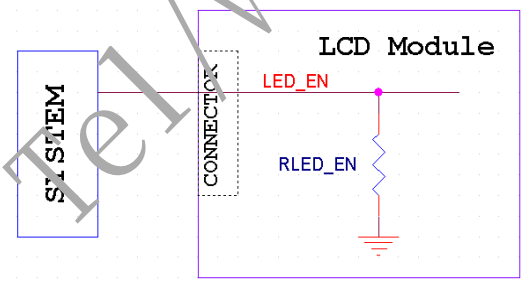
$$(N + 0.33) * f \leq f_{PWM} \leq (N + 0.66) * f$$

N : Integer $(N \geq 3)$

f : Frame rate

Note (3) The specified LED power supply current is under the conditions at "LED_VCCS = Typ.", Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.

Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. For example, the figure below describes the equivalent pull down impedance of LED_EN (if it exists). The rest pull down impedances of other signals (eg. HPD, PWM …) are in the same concept.



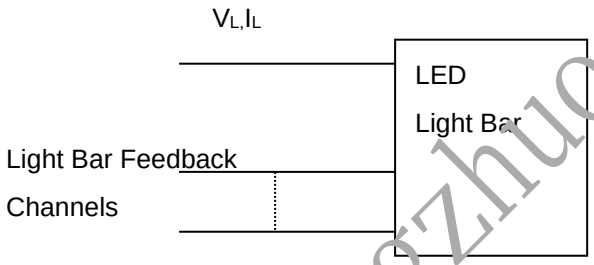
Note (5) If the cycle-to-cycle difference of PWM duty exceeds 0.1%, especially when the PWM duty is low, slight brightness change might be observed.

4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	28.6	30.8	33.0	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L	-	94.4	-	mA	(3)
Power Consumption	P_L		2.908	3.116	W	
LED Life Time	L_{BL}	15000	-	-	Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$(Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 ºC and I_L = 11.8 mA(Per EA) until the brightness becomes ≦ 50% of its original value.

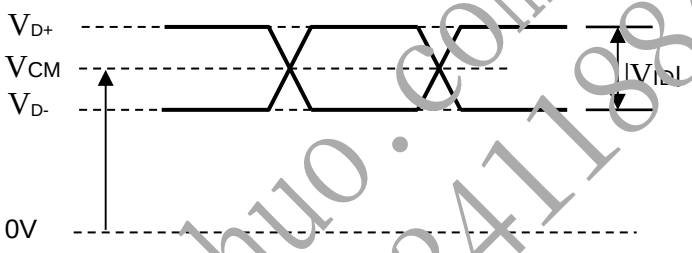
4.4 DISPLAYPORTSIGNAL TIMING SPECIFICATION

4.4.1 ELECTRICAL SPECIFICATIONS

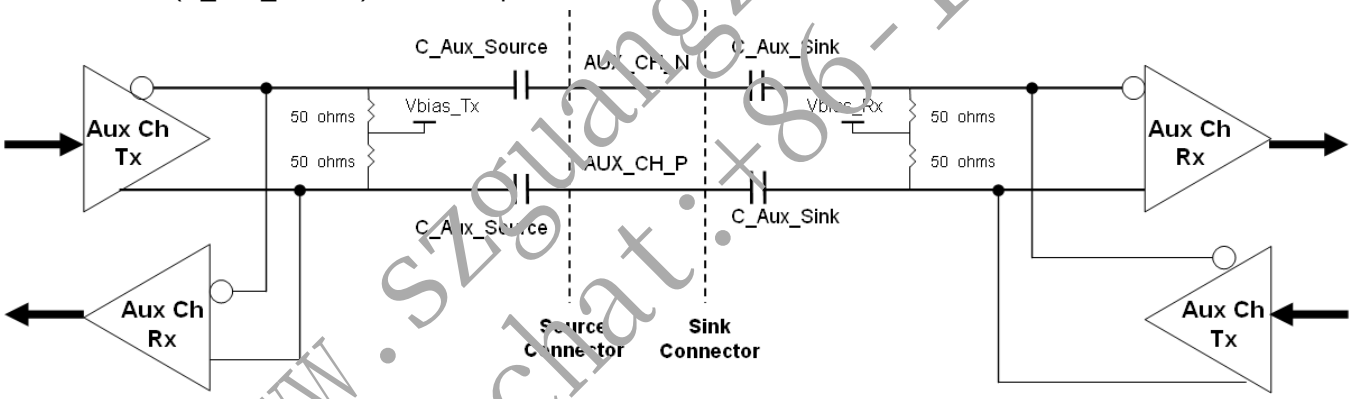
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Signal Common Mode Voltage(MainLink and AUX)	VCM	0		2	V	(1)(4)
AUX AC Coupling Capacitor	C_Aux_Source	75		200	nF	(2)
Main Link AC Coupling Capacitor	C_ML_Source	75		200	nF	(3)

Note (1)Display port interface related AC coupled signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2. There are many optional items described in eDP1.2. If some optional item is requested, please contact us

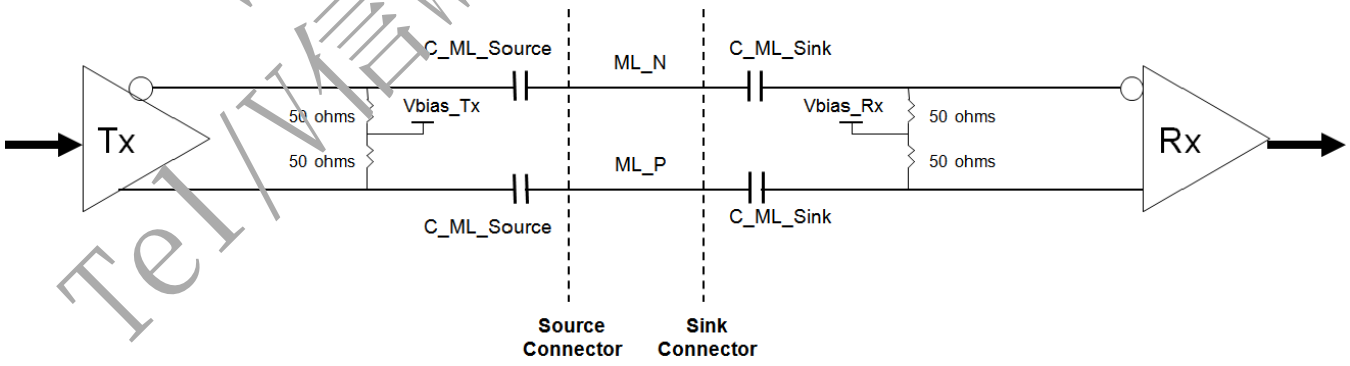
Single Ended



(2) Recommended eDP AUX Channel topology is as below and the AUX AC Coupling Capacitor (C_Aux_Source) should be placed on the source device.



(3) Recommended Main Link Channel topology is as below and the Main Link AC Coupling Capacitor (C_ML_Source) should be placed on the source device.



(4) The source device should pass the test criteria described in DisplayPortCompliance Test Specification (CTS) 1.1

4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Refresh Rate 165Hz

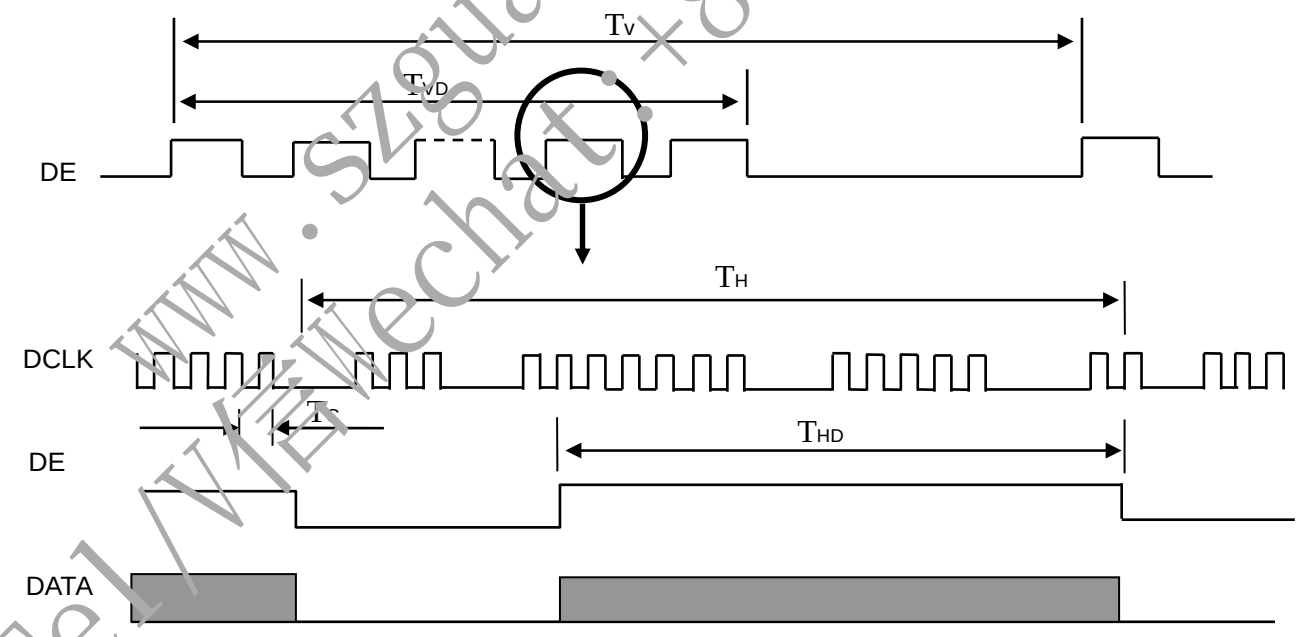
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	769.82	777.32	784.84	MHz	-
DE	Vertical Total Time	TV	1728	1732	1736	TH	-
	Vertical ActiveDisplayPeriod	TVD	1600	1600	1600	TH	-
	Vertical ActiveBlankingPeriod	TVB	TV-TVD	132	TV-TVD	TH	-
	Horizontal Total Time	TH	2700	2720	2740	Tc	-
	Horizontal ActiveDisplayPeriod	THD	2560	2560	2560	Tc	-
	Horizontal ActiveBlankingPeriod	THB	TH-THB	160	TH-THB	Tc	-

Refresh rate 60Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	279.93	282.67	285.39	MHz	-
DE	Vertical Total Time	TV	1728	1732	1736	TH	-
	Vertical ActiveDisplayPeriod	TVD	1600	1600	1600	TH	-
	Vertical ActiveBlankingPeriod	TVB	TV-TVD	132	TV-TVD	TH	-
	Horizontal Total Time	TH	2700	2720	2740	Tc	-
	Horizontal ActiveDisplayPeriod	THD	2560	2560	2560	Tc	-
	Horizontal ActiveBlankingPeriod	THB	TH-THD	160	TH-THD	Tc	-

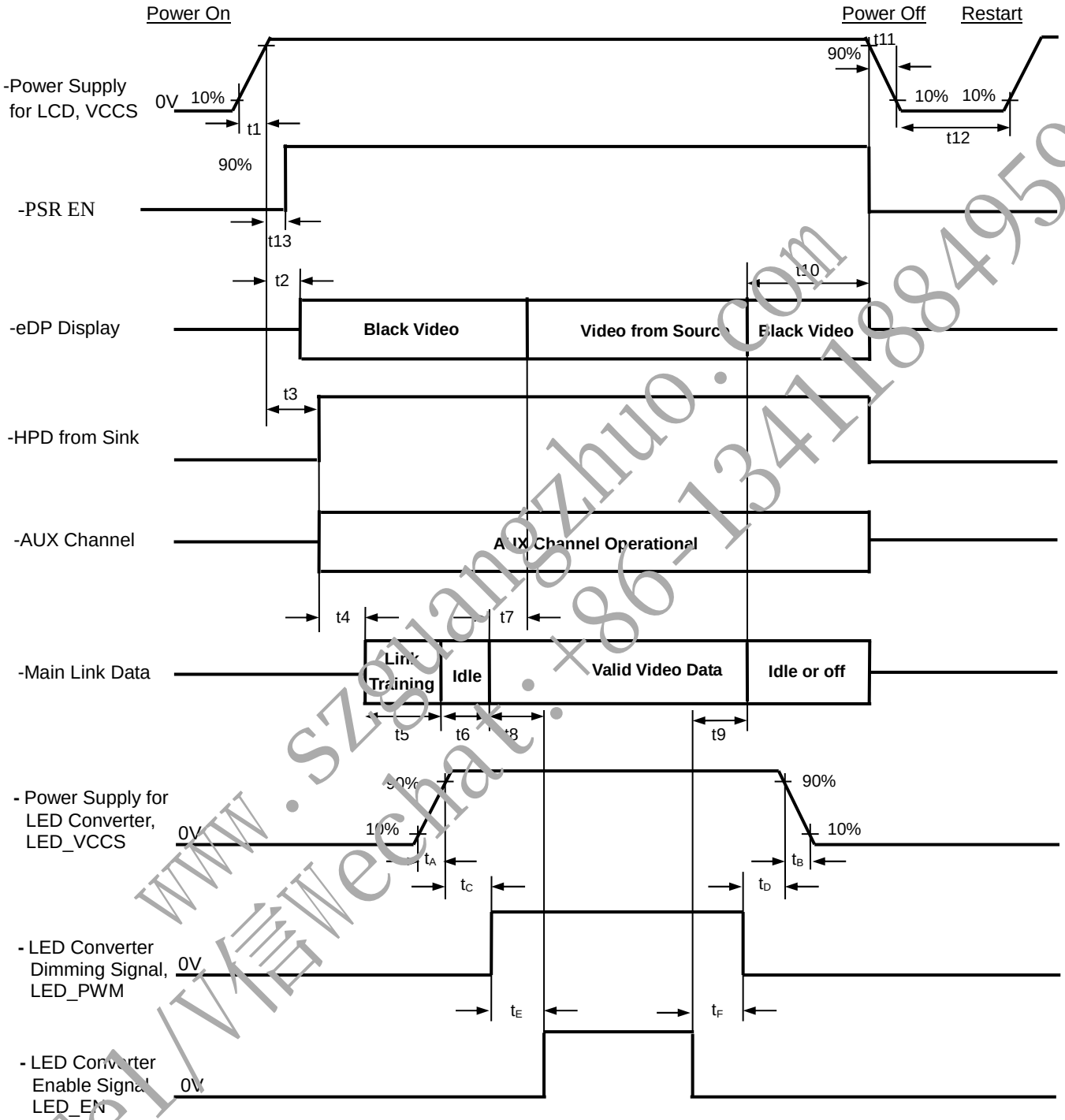
Note (1) The panel can operate at 480Hz normal mode and power saving mode, respectively. All reliability tests are based on specific timing of 480Hz refresh rate. We can only assure the panel's electrical function at power saving mode.

INPUT SIGNAL TIMING DIAGRAM



4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.



Timing Specifications

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	Power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t2	Delay from LCD,VCCS to black video generation	Sink	0	200	ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source (see Notes:2 and 3 below)
t3	Delay from LCD,VCCS to HPD high	Sink	0	200	ms	Sink AUX Channel must be operational upon HPD high (see Note:4 below)
t4	Delay from HPD high to link training initialization	Source	0	-	ms	Allows for Source to read Link capability and initialize
t5	Link training duration	Source	0		ms	Dependant on Source link training protocol
t6	Link idle	Source	0	-	ms	Min Accounts for required BS-Idle pattern. Max allows for Source frame synchronization
t7	Delay from valid video data from Source to video on display	Sink	0	50	ms	Max value allows for Sink to validate video data and timing. At the end of T7, Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and Sink will no longer generate automatic Black Video
t8	Delay from valid video data from Source to backlight on	Source	80	-	ms	Source must assure display video is stable *: Recommended by INX. To avoid garbage image.
t9	Delay from backlight off to end of valid video data	Source	50	-	ms	Source must assure backlight is no longer illuminated. At the end of T9, Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and Sink will automatically display Black Video. (See Notes: 2 and 3 below) *: Recommended by INX. To avoid garbage image.
t10	Delay from end of valid video data from Source to power off	Source	0	500	ms	Black video will be displayed after receiving idle or off signals from Source
t11	VCCS power rail fall time, 90% to 10%	Source	0.5	10	ms	-

t12	VCCS Power off time	Source	500	-	ms	-
t13	Delay from LCD,VCCS to PSR_EN high	Source	(0)	(5)	ms	PSR function select time
t_A	LED power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t_B	LED power rail fall time, 90% to 10%	Source	0	10	ms	-
t_C	Delay from LED power rising to LED dimming signal	Source	1	-	ms	-
t_D	Delay from LED dimming signal to LED power falling	Source	1	-	ms	-
t_E	Delay from LED dimming signal to LED enable signal	Source	0	-	ms	-
t_F	Delay from LED enable signal to LED dimming signal	Source	0	-	ms	-

Note (1) Please don't plug or unplug the interface cable when system is turned on.Before LCD_VCCS and LED_VCCS are ready, it is recommended to pull down the backlight control signals.

Note (2) The Sink must include the ability to automatically generate Black Video autonomously. The Sink must automatically enable Black Video under the following conditions:

- Upon LCDVCC power-on (within T2 max)
- When the "NoVideoStream_Flag" (VB-ID Bit 3) is received from the Source (at the end of T9)

Note (3) The Sink may implement the ability to disable the automatic Black Video function, as described in Note (2), above, for system development and debugging purposes.

Note (4) The Sink must support AUX Channel polling by the Source immediately following LCDVCC power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to response to an AUX Channel transaction with the time specified within T3 max.

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

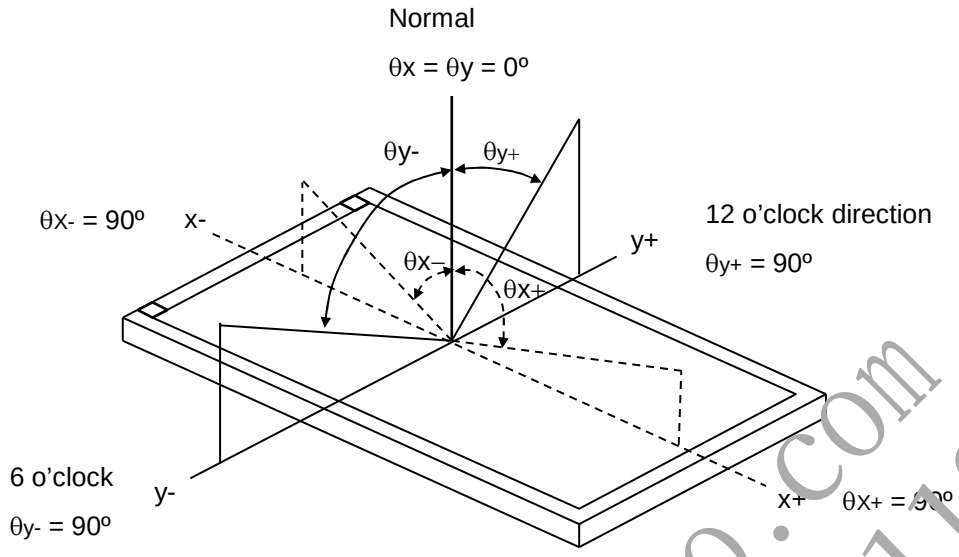
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	94.4	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	800	1000	-	-	(2), (5) ,(7)
Response Time		T_R		-	5	7	ms	(3) ,(7)
		T_F		-	4	5	ms	
		TGtG (OD OFF)			3	5		
		TGtG (OD ON)		-	7	9	ms	
Average Luminance of White		LAVE		255	300	-	cd/m²	(4), (6) ,(7)
Color Chromaticity	Red	Rx		Typ – 0.03	0.640	Typ + 0.03	-	(1) ,(7)
		Ry			0.330		-	
	Green	Gx			0.300		-	
		Gy			0.600		-	
	Blue	Bx			0.150		-	
		By			0.060		-	
	White	Wx			0.313		-	
		Wy			0.329			
Viewing Angle	Horizontal	θ_x+	CR≥10	80	89	-	Deg.	(1),(5) , (7)
		θ_x-		80	89	-		
	Vertical	θ_Y+		80	89	-		
		θ_Y-		80	89	-		
White Variation		δW_{5p}	θ_x=0°, θ_Y =0°	80	90		-	(5),(6) , (7)
		δW_{13p}	θ_x=0°, θ_Y =0°	65	75		-	
Low Blue Light		BLR	θ_x=0°, θ_Y =0°	-	-	50	%	1), (5), (7), (8) (9)
		CCT		5500	6500	7000	K	
		BLTF				0.085		

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

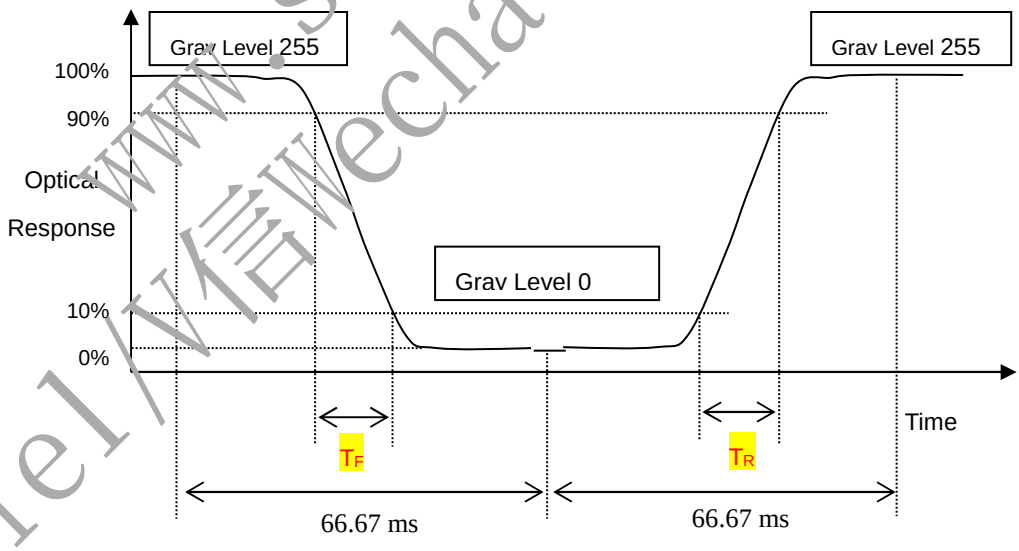
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note(6).

Note (3) Definition of Response Time (T_R, T_F):



-The TGtG is the response time means the transition time from "Gray N" to "Gray M" (N,M=0~255).

- T_{GtG_AVE} is the total average of the T_{GtG} data (Measured by INX GTG instrument)

- The gray (N,M) stands for the (0,32,64,~255) as the following table.

* It depends on Overshoot rate

Gray to gray		M								
		0	32	64	96	128	160	192	224	255
N	0									
	32									
	64									
	96									
	128									
	160									
	192									
	224									
	255									

Note (4) Definition of Average Luminance of White (L_{AVE}):

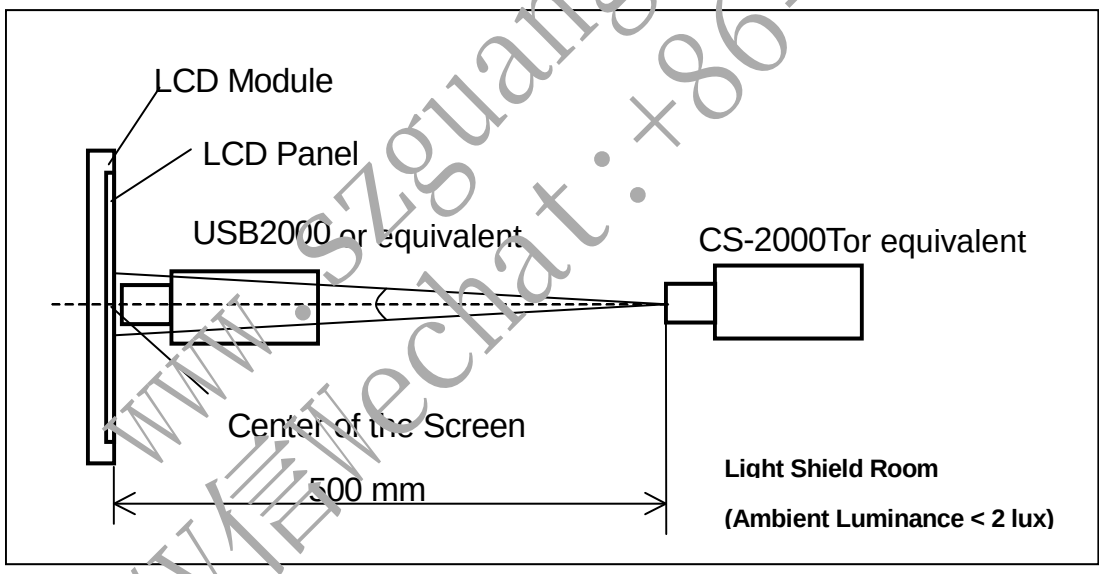
Measure the luminance of White at 5 points

L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note(6)

Note (5) MeasurementSetup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring.In order to stabilize the luminance, the measurement should be executed after lighting Backlight for20 minutes in a windless room.

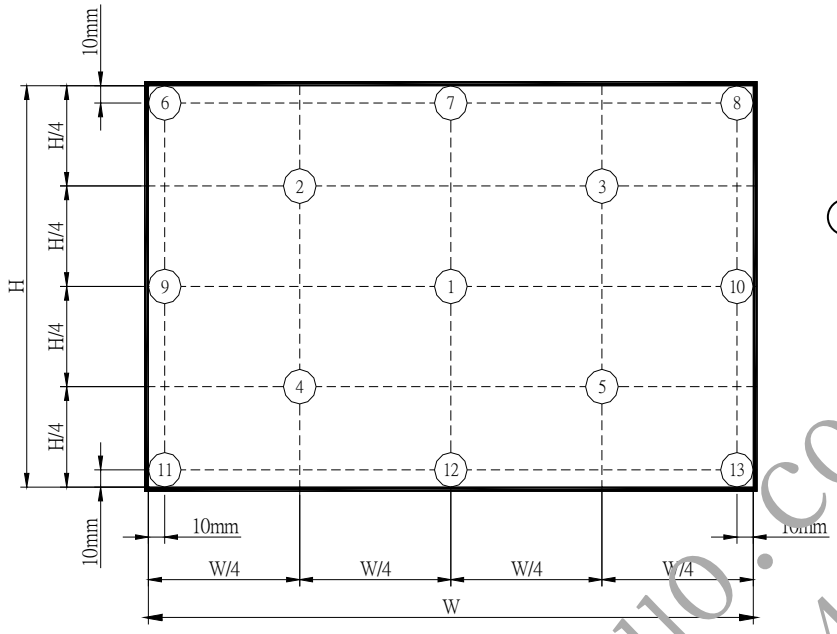


Note (6) Definition of White Variation(δW):

Measure theluminance of gray level 255 at 5 points / 13 points

δW_{5p}={Minimum [L (1) ~ L (5)] / Maximum [L (1) ~ L (5)]}*100%

δW_{13p}={Minimum [L (1) ~ L (13)] / Maximum [L (1) ~ L (13)]}*100%



Ⓧ : Test Point

X=1 to 13

Note(7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted

Note (8) Definition of Blue Light Ratio (BLR)

Measure the luminance of gray level 255 at center points

$$Blue\ Light\ Ratio(BLR) = \left[\frac{Range\ (415\sim455\ nm)}{Range\ (400\sim500\ nm)}\right] x\ 100\%$$

Range (415~455 nm): Light intensity between 415 nm and 455 nm

Range (400~500 nm): Light intensity between 400 nm and 500 nm

BLR = BLR (1)

BLR (X) is corresponding to the Blue Light Ratio of the point X at Figure in Note (6)

Note (9) Definition of Blue light toxicity

Measure the luminance of gray level 255 at center points

$$BLTF = \frac{100}{683} x \int_{380}^{780} L(\lambda) x B(\lambda) x \Delta\lambda \Big/ \int_{380}^{780} L(\lambda) x g(\lambda) x \Delta\lambda$$

in which:

Δ λ = 1

L(λ): spectral irradiance in μW·cm-2·nm-1

B(λ): Blue-Light Hazard Function

g(λ): CIE 1931 RGB luminosity function

683 - maximum spectral luminous efficacy constant (683 lumens per Watt at 555 nm)

6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60ºC, 240 hours	(1) (2)
Low Temperature Storage Test	-20ºC, 240 hours	
Thermal Shock Storage Test	-20ºC, 0.5hour←→60℃, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	50ºC, 240 hours	
Low Temperature Operation Test	0ºC, 240 hours	
High Temperature & High Humidity Operation Test	50℃, 80% RH, 240 hours	
ESD Test (Operation)	150pF, 330Ω, 1sec/cycle Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±15KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave, 1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect.

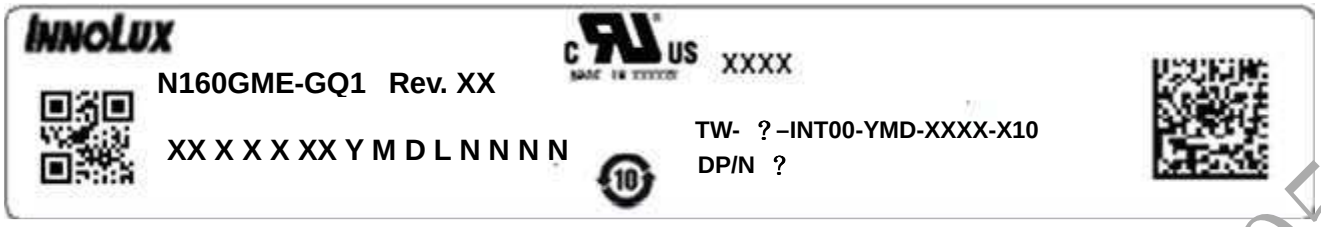
Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

7. PACKING

7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: N160GME-GQ1

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X XX XX X XY M DLN N N N

- Serial No.
- Product Line
- Year, Month, Date
- INNOLUX Internal Use
- Revision
- INNOLUX Internal Use

Serial ID includes the information as below:

(a) Manufactured Date: Year:0~9, for 2010~2019

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

(e) UL Logo : XXXX is UL factory ID.

(f) Dell 2D label contains information as below:

(f-1) Serial ID: TW-0SSSSS-INT00-YMD-XXXX-ZZZ

- Serial Numbers
- Production Year, Month, Date
- Manufacturing ID
- Part Number

(f-1-1) Corresponding LCM Fab code XXXXX is as below

-INT00 : Tainan J001 and J003

(f-2) Production location: Made in XXXX.

(f-3) ZZZ:Revision code: X00, X10, X20, A00..etc.

SST (WS)	X00, X01, X02, … X09
PT (ES)	X10, X11, X12, … X19
ST (CS)	X20, X21, X23, … X29
XB (MP)	A00, A01, A02, … A99

7.2 DELL Carton LABEL

Dell carton label contains information as below:

(a) PKG ID: 04688-INT00-YMD-XXXXXX-0SSSSS-ZZ

- Dell P/N
- Serial numbers.
- Production Year, Month, Date
- Manufacturing ID

(b) Production location: Made in XXXX.

(c) Revision code: X00, X10, X20, A00..etc.

(d) BOX Quantity:ZZ

(e) DILoc ID&Mfg ID XXXXX INX LCM Fab Code

(e-1)Corresponding LCM Fab code XXXXX is as below.

7.3 CARTON

(1)Box Dimensions : 540(L)*380(W)*315(H)
(2)20 Module/Carton

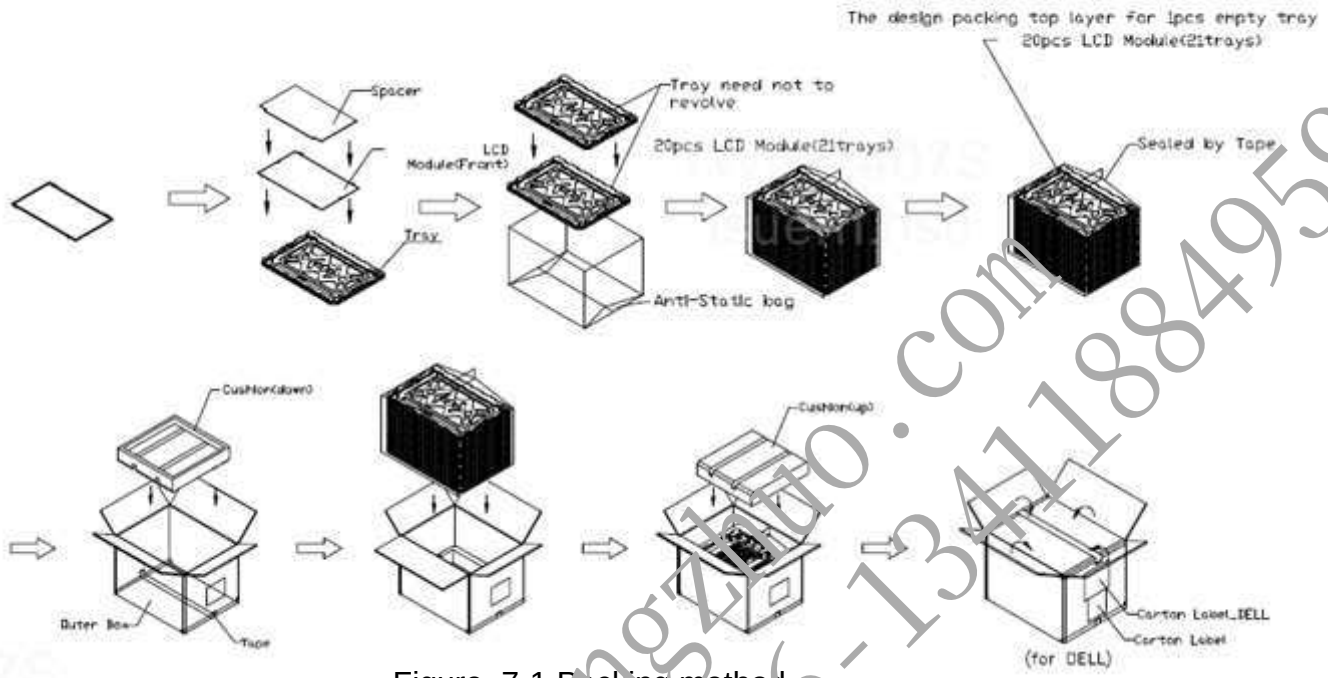


Figure. 7-1 Packing method

7.4 PALLET

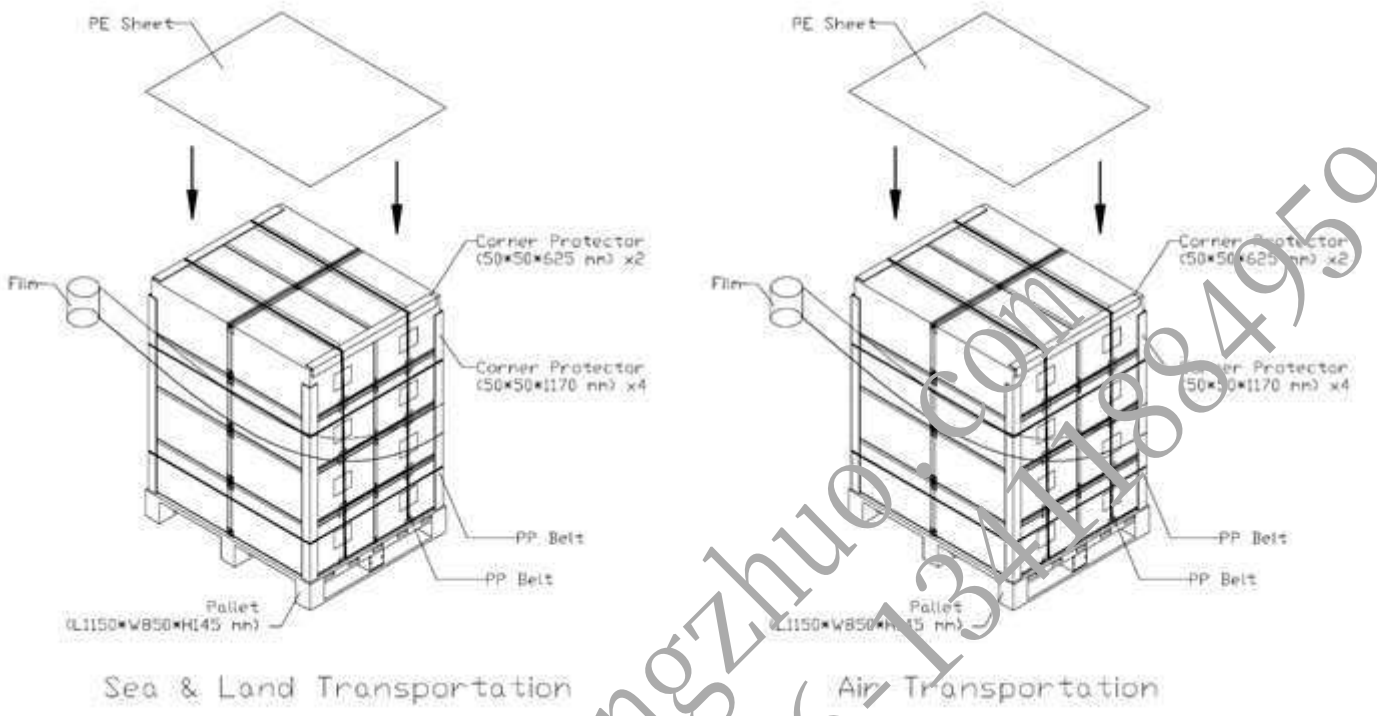


Figure. 7-2 Packing method

7.5 UN-PACKAGING METHOD

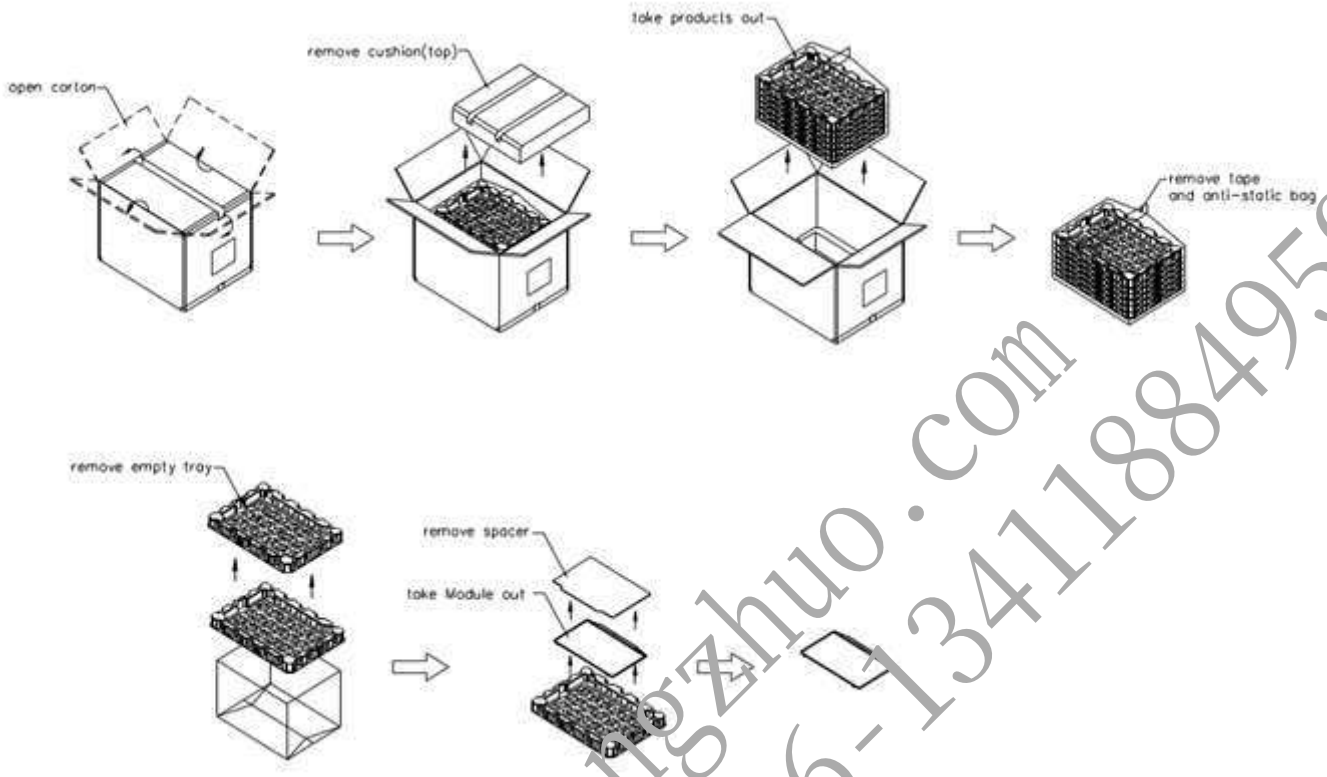


Figure. 7-3 Un-packing method

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

Appendix. EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
1	00	Header	00	00000000
2	01	Header	FF	11111111
3	02	Header	FF	11111111
4	03	Header	FF	11111111
5	04	Header	FF	11111111
6	05	Header	FF	11111111
7	06	Header	FF	11111111
8	07	Header	00	00000000
9	08	EISA ID manufacturer name ("CMN")	0D	00001101
10	09	EISA ID manufacturer name	AE	10101110
11	0A	ID product code (LSB)	1D	00011101
12	0B	ID product code (MSB)	16	00010110
13	0C	ID S/N (fixed "0")	00	00000000
14	0D	ID S/N (fixed "0")	00	00000000
15	0E	ID S/N (fixed "0")	00	00000000
16	0F	ID S/N (fixed "0")	00	00000000
17	10	Week of manufacture ("09")	09	00001001
18	11	Year of manufacture ("2022")	20	00100000
19	12	EDID structure version ("1")	01	00000001
20	13	EDID revision ("4")	04	00000100
21	14	Video I/P definition ("Digital")	A5	10100101
22	15	Active area horizontal ("34.468cm")	22	00100010
23	16	Active area vertical ("21.542cm")	16	00010110
24	17	Display Gamma (Gamma = "2.2")	78	01111000
25	18	Feature support (RGB, Continuous)	03	00000011
26	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	0F	00001111
27	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	95	10010101
28	1B	Rx=0.68	AE	10101110
29	1C	Ry=0.32	52	01010010
30	1D	Gx=0.265	43	01000011
31	1E	Gy=0.69	B0	10110000
32	1F	Bx=0.15	26	00100110
33	20	By=0.06	0F	00001111
34	21	Wx=0.313	50	01010000
35	22	Wy=0.329	54	01010100
36	23	Established timings 1	00	00000000
37	24	Established timings 2	00	00000000
38	25	Manufacturer's reserved timings	00	00000000
39	26	Standard timing ID # 1	01	00000001
40	27	Standard timing ID # 1	01	00000001
41	28	Standard timing ID # 2	01	00000001
42	29	Standard timing ID # 2	01	00000001
43	2A	Standard timing ID # 3	01	00000001
44	2B	Standard timing ID # 3	01	00000001
45	2C	Standard timing ID # 4	01	00000001

46	2D	Standard timing ID # 4	01	00000001
47	2E	Standard timing ID # 5	01	00000001
48	2F	Standard timing ID # 5	01	00000001
49	30	Standard timing ID # 6	01	00000001
50	31	Standard timing ID # 6	01	00000001
51	32	Standard timing ID # 7	01	00000001
52	33	Standard timing ID # 7	01	00000001
53	34	Standard timing ID # 8	01	00000001
54	35	Standard timing ID # 8	01	00000001
55	36	Detailed timing description # 1 Pixel clock ("282.67"MHz, According to VESA CVT Rev1.4)	6B	01101011
56	37	# 1 Pixel clock (hex LSB first)	6E	01101110
57	38	# 1 H active ("2560")	00	00000000
58	39	# 1 H blank ("160")	A0	10100000
59	3A	# 1 H active : H blank ("2560 : 160")	A0	10100000
60	3B	# 1 V active ("1600")	40	01000000
61	3C	# 1 V blank ("132")	84	10000100
62	3D	# 1 V active : V blank ("1600 : 132")	60	01100000
63	3E	# 1 H sync offset ("48")	30	00110000
64	3F	# 1 H sync pulse width ("32")	20	00100000
65	40	# 1 V sync offset : V sync pulse width ("6 : 10")	6A	01101010
66	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width ("48 : 32 : 6 : 10")	00	00000000
67	42	# 1 H image size (“344 mm“)	58	01011000
68	43	# 1 V image size (“215 mm“)	D7	11010111
69	44	# 1 H image size : V image size	10	00010000
70	45	# 1 H boarder ("0")	00	00000000
71	46	# 1 V boarder ("0")	00	00000000
72	47	Non-interlaced, Normal Display, Digital separate, Negative Hsync, Negative Vsync	1A	00011010
73	48	# 2 Dummy Descriptor	00	00000000
74	49	# 2 Dummy Descriptor	00	00000000
75	4A	# 2 Dummy Descriptor	00	00000000
76	4B	# 2 Dummy Descriptor Tag Number	10	00010000
77	4C	# 2 Dummy Descriptor	00	00000000
78	4D	# 2 Dummy	00	00000000
79	4E	# 2 Dummy	00	00000000
80	4F	# 2 Dummy	00	00000000
81	50	# 2 Dummy	00	00000000
82	51	# 2 Dummy	00	00000000
83	52	# 2 Dummy	00	00000000
84	53	# 2 Dummy	00	00000000
85	54	# 2 Dummy	00	00000000
86	55	# 2 Dummy	00	00000000
87	56	# 2 Dummy	00	00000000
88	57	# 2 Dummy	00	00000000
89	58	# 2 Dummy	00	00000000
90	59	# 2 Dummy	00	00000000
91	5A	Flag	00	00000000
92	5B	Flag	00	00000000
93	5C	Flag	00	00000000
94	5D	Data Type Tag: Alphanumeric Data String (ASCII)	FE	11111110

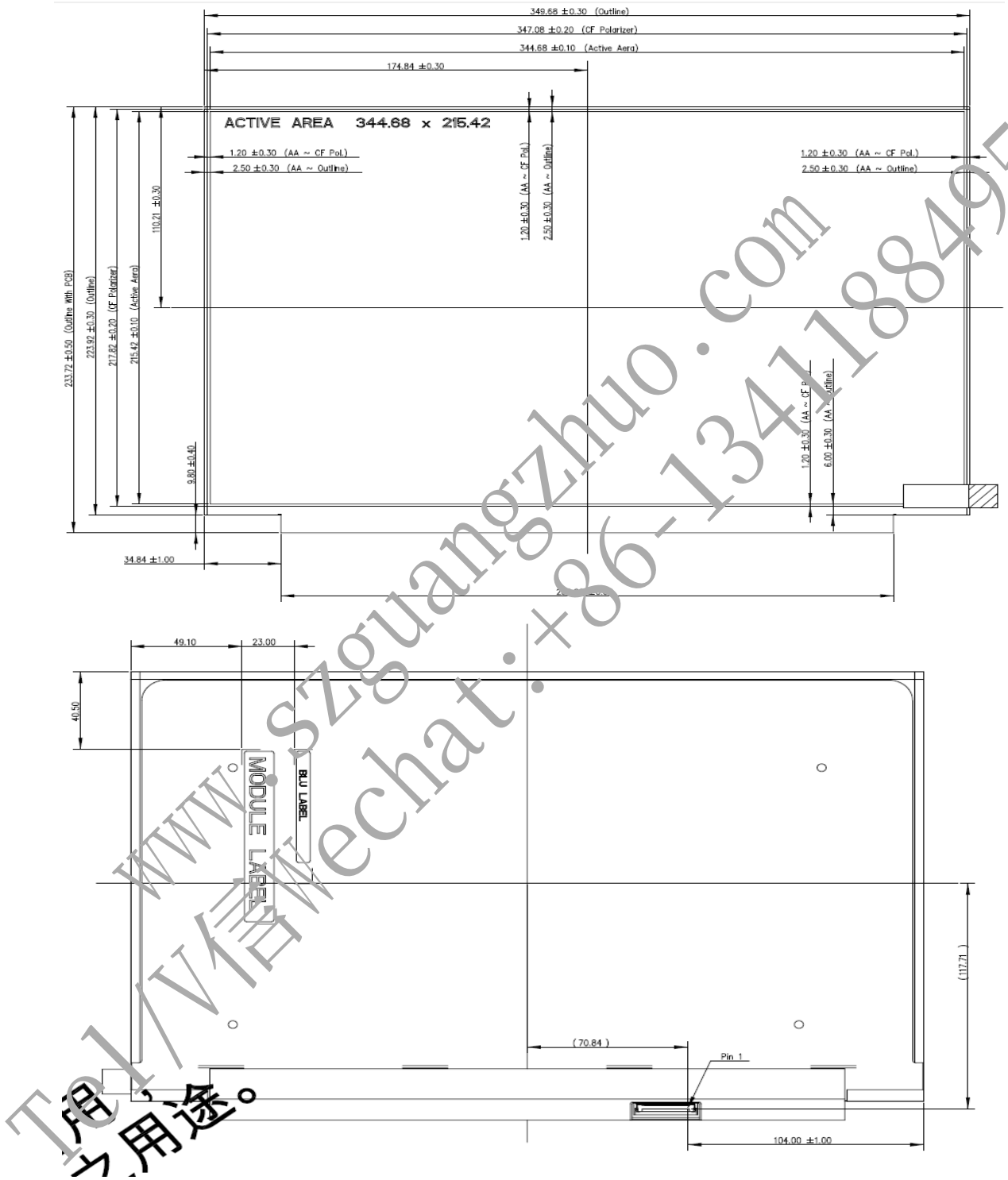
95	5E	Flag	00	00000000
96	5F	Dell P/N 1st Character "4"	34	00110100
97	60	Dell P/N 2nd Character "N"	4E	01001110
98	61	Dell P/N 3rd Character "4"	34	00110100
99	62	Dell P/N 4th Character "5"	35	00110101
100	63	Dell P/N 5th Character "R"	52	01010010
101	64	EDID Revision	00	00000000
102	65	Manufacturer P/N "1"	31	00110001
103	66	Manufacturer P/N "6"	36	00110110
104	67	Manufacturer P/N "0"	30	00110000
105	68	Manufacturer P/N "G"	47	01000111
106	69	Manufacturer P/N "M"	4D	01001101
107	6A	Manufacturer P/N "E"	45	01000101
108	6B	New line character indicates end of ASCII string	0A	00001010
109	6C	Flag	00	00000000
110	6D	Flag	00	00000000
111	6E	Flag	00	00000000
112	6F	Data Type Tag: Manufacturer Specified Data 00	00	00000000
113	70	Flag	00	00000000
114	71	Color Management	02	00000010
115	72	Panel Type and Revision	41	01000001
116	73	Frame Rate	0F	00001111
117	74	Light Controller Interface and Maximum Luminance	9E	10011110
118	75	Front Surface / Polarizer and Pixel Structure	00	00000000
119	76	Multi-Media Features	00	00000000
120	77	Multi-Media Features	00	00000000
121	78	Special Features	00	00000000
122	79	Special Features	0F	00001111
123	7A	Special Features	41	01000001
124	7B	New line character indicates end of ASCII string	0A	00001010
125	7C	Padding with "Blank" character	20	00100000
126	7D	Padding with "Blank" character	20	00100000
127	7E	Extension flag	01	00000001
128	7F	Checksum	72	01110010
129	80	DisplayID EDID extension block tag	70	01110000
130	81	DisplayID version revision	20	00100000
131	82	section size	79	01111001
132	83	product type identifier	02	00000010
133	84	extension count	00	00000000
134	85	data block tag = type 1 timing detailed	22	00100010
135	86	block revision = 00	00	00000000
136	87	Number of payload bytes in block = (N x 20), 1<=N<=12	14	00010100
137	88	Pixel Clk/1000 [low bit]	69	01101001
138	89	Pixel Clk/1000 [middle bit]	DC	11011100
139	8A	Pixel Clk/1000 [high bit]	0B	00001011
140	8B	timing option [prefered 'detailed' timing, No streo, 16:10']	85	10000101
141	8C	Horizontal Active [low bit]	FF	11111111
142	8D	Horizontal Active [high bit]	09	00001001
143	8E	Horizontal blank [low bit]	9F	10011111
144	8F	Horizontal blank [high bit]	00	00000000
145	90	Horizontal offset (front porch) [low bit]	2F	00101111

146	91	Horizontal offset (front porch) [high bit] / Horizontal sync polarity = Positive	00	00000000
147	92	Horizontal Sync width [low bit]	1F	00011111
148	93	Horizontal Sync width [high bit]	00	00000000
149	94	Vertical Active [low bit]	3F	00111111
150	95	Vertical Active [high bit]	06	00000110
151	96	Vertical blank [low bit]	83	10000011
152	97	Vertical blank [high bit]	00	00000000
153	98	Vertical offset (front porch) [low bit]	05	00000101
154	99	Vertical offset (front porch) [high bit] / Vertical sync polarity = Negative	00	00000000
155	9A	Vertical Sync width [low bit]	09	00001001
156	9B	Vertical Sync width [high bit]	00	00000000
157	9C	data block tag = Dynamic Video Timing Range Limits	25	00100101
158	9D	block revision = 01	01	00000001
159	9E	Number of payload bytes in block = 09	09	00001001
160	9F	Minimum Pixel Clk/1,000 [low bit]	69	01101001
161	A0	Minimum Pixel Clk/1,000 [middle bit]	DC	11011100
162	A1	Minimum Pixel Clk/1,000 [high bit]	0B	00001011
163	A2	Maximum Pixel Clk/1,000 [low bit]	69	01101001
164	A3	Maximum Pixel Clk/1,000 [middle bit]	DC	11011100
165	A4	Maximum Pixel Clk/1,000 [high bit]	0B	00001011
166	A5	Minimum Vertical Refresh Rate	3C	00111100
167	A6	Maximum Vertical Refresh Rate:Bits 7:0	A5	10100101
168	A7	Dynamic Video Timing Range Support Flags/Maximum Vertical Refresh Rate s :Bits 9:8	80	10000000
169	A8	CTA [DID Data block tag:81]	81	10000001
170	A9	Block version :00	00	00000000
171	AA	Number of payload bytes	13	00010011
172	AB	AMD VSDB Header	72	01110010
173	AC	AMD IEEE OUI Value	1A	00011010
174	AD	AMD IEEE OUI Value	00	00000000
175	AE	AMD IEEE OUI Value	00	00000000
176	AF	VSDB Version	03	00000011
177	B0	Free sync Capability	01	00000001
178	B1	Min refresh Rate [Hz]	3C	00111100
179	B2	Max refresh Rate [Hz]	A5	10100101
180	B3	Free sync MCCS VCP Code	00	00000000
181	B4	Supported WCG and HDR feature	00	00000000
182	B5	Max Luminance 1	00	00000000
183	B6	Min Luminance 1	00	00000000
184	B7	Max Luminance 2	00	00000000
185	B8	Min Luminance 2	00	00000000
186	B9	Max refresh Rate [Hz]:Bits 7:0	A5	10100101
187	BA	Max refresh Rate [Hz]:Bist 9:8	00	00000000
188	BB	VSDB Block Reserved	00	00000000
189	BC	VSDB Block Reserved	00	00000000
190	BD	VSDB Block Reserved	00	00000000
191	BE	Reserved	00	00000000
192	BF	Reserved	00	00000000
193	C0	Reserved	00	00000000
194	C1	Reserved	00	00000000

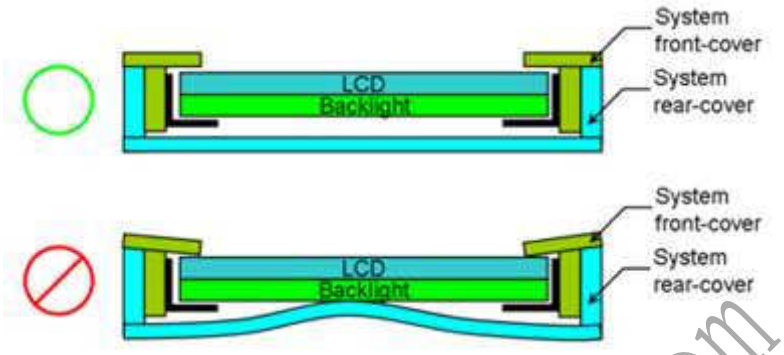
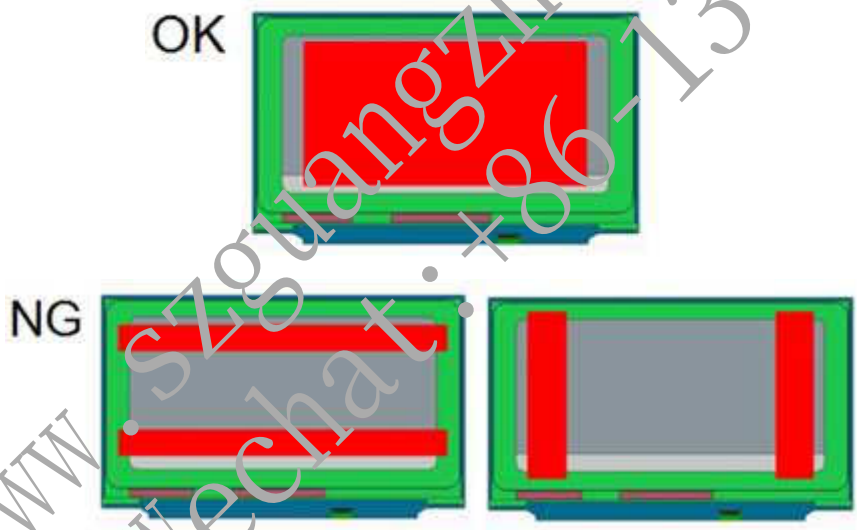
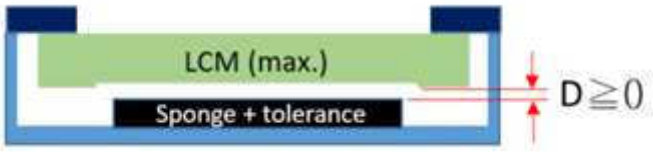
195	C2	Reserved	00	00000000
196	C3	Reserved	00	00000000
197	C4	Reserved	00	00000000
198	C5	Reserved	00	00000000
199	C6	Reserved	00	00000000
200	C7	Reserved	00	00000000
201	C8	Reserved	00	00000000
202	C9	Reserved	00	00000000
203	CA	Reserved	00	00000000
204	CB	Reserved	00	00000000
205	CC	Reserved	00	00000000
206	CD	Reserved	00	00000000
207	CE	Reserved	00	00000000
208	CF	Reserved	00	00000000
209	D0	Reserved	00	00000000
210	D1	Reserved	00	00000000
211	D2	Reserved	00	00000000
212	D3	Reserved	00	00000000
213	D4	Reserved	00	00000000
214	D5	Reserved	00	00000000
215	D6	Reserved	00	00000000
216	D7	Reserved	00	00000000
217	D8	Reserved	00	00000000
218	D9	Reserved	00	00000000
219	DA	Reserved	00	00000000
220	DB	Reserved	00	00000000
221	DC	Reserved	00	00000000
222	DD	Reserved	00	00000000
223	DE	Reserved	00	00000000
224	DF	Reserved	00	00000000
225	E0	Reserved	00	00000000
226	E1	Reserved	00	00000000
227	E2	Reserved	00	00000000
228	E3	Reserved	00	00000000
229	E4	Reserved	00	00000000
230	E5	Reserved	00	00000000
231	E6	Reserved	00	00000000
232	E7	Reserved	00	00000000
233	E8	Reserved	00	00000000
234	E9	Reserved	00	00000000
235	EA	Reserved	00	00000000
236	EB	Reserved	00	00000000
237	EC	Reserved	00	00000000
238	ED	Reserved	00	00000000
239	EE	Reserved	00	00000000
240	EF	Reserved	00	00000000
241	F0	Reserved	00	00000000
242	F1	Reserved	00	00000000
243	F2	Reserved	00	00000000
244	F3	Reserved	00	00000000
245	F4	Reserved	00	00000000

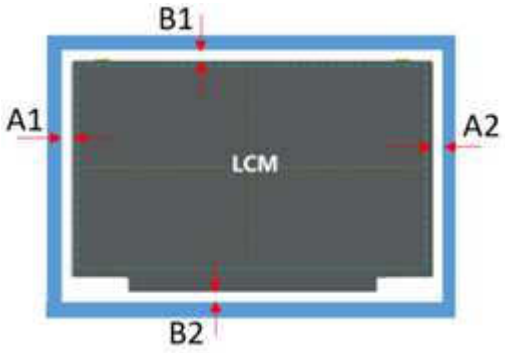
246	F5	Reserved	00	00000000
247	F6	Reserved	00	00000000
248	F7	Reserved	00	00000000
249	F8	Reserved	00	00000000
250	F9	Reserved	00	00000000
251	FA	Reserved	00	00000000
252	FB	Reserved	00	00000000
253	FC	Reserved	00	00000000
254	FD	Reserved	00	00000000
255	FE	Checksum	B5	10110101
256	FF	Checksum	90	10010000

Appendix. OUTLINE DRAWING



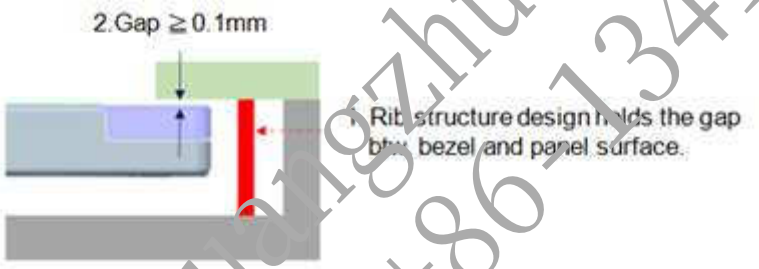
Appendix. SYSTEM COVER DESIGN GUIDANCE

0.	**Permanent deformation of system cover after reliability test**
	
Definition	System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
1	**Sponge area design behind panel**
	
Definition	Sponge area design behind panel can not be across the panel metal rear and the reflector at the same time. It can be on the reflector area only.
2	**Gap between system rear-cover & panel**
	
Definition	The maximum thickness of sponge on the system rear-cover can not interfere to the maximum thickness of panel. Because the interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
3	**Gap Design between panel & around structure**

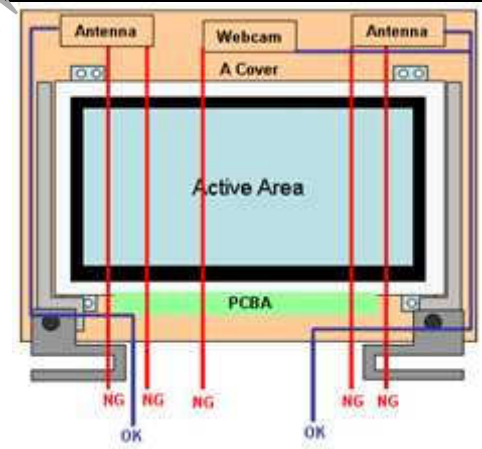


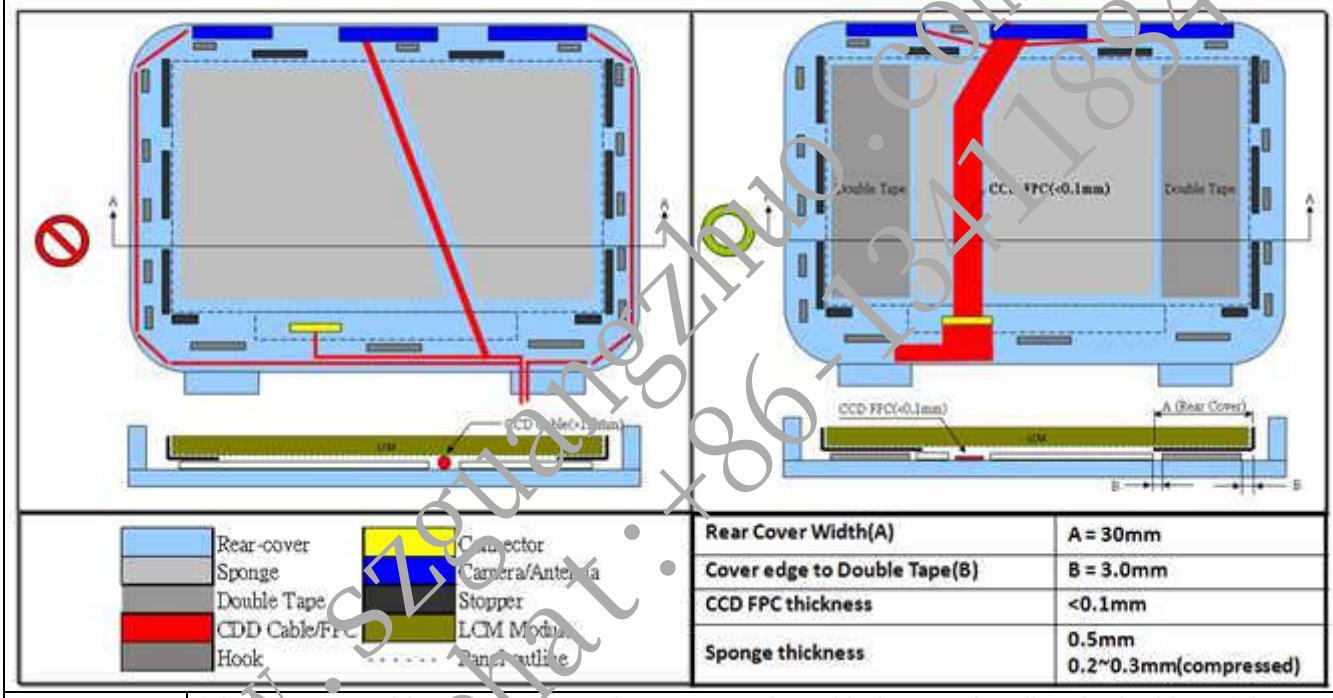
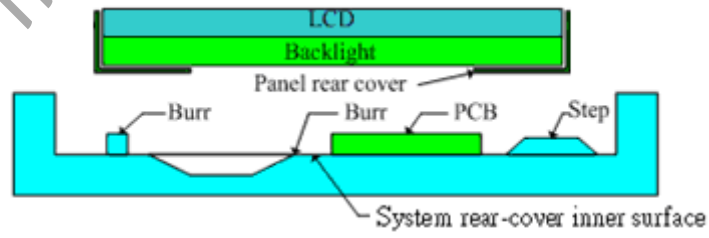
Item	Suggestion	Remark
A1	A1≧0.5	Gap ≧ Panel outline max. tolerance + Assembly max. tolerance
A2	A2≧0.5	
B1	B1≧0.5	
B2	B2≧0.8	

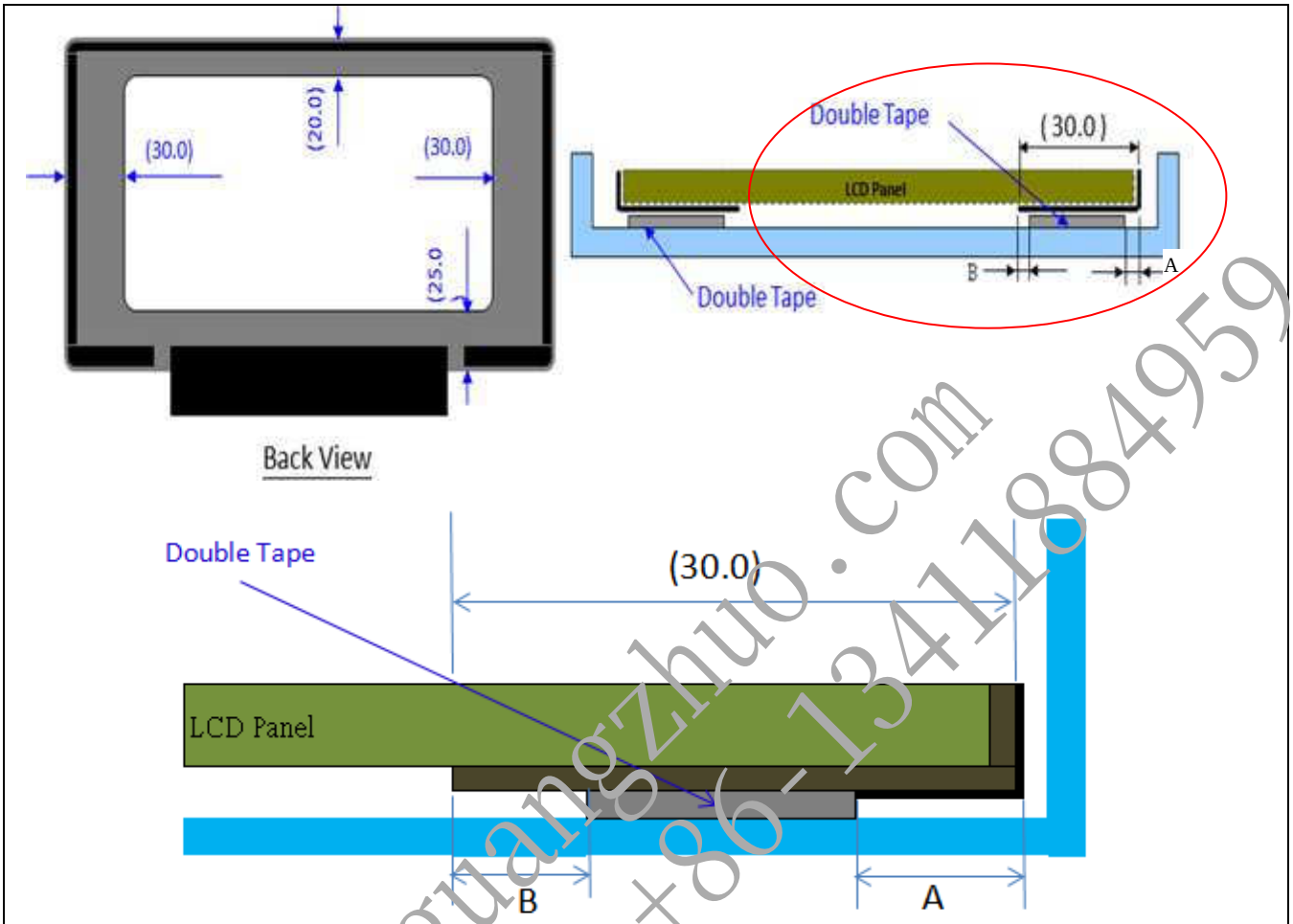
Definition	Gap Design between panel & around structure needs to consider the maximum tolerances of panel outline and assembly at the same time. Gap Design suggestion is shown as A1/A2/B1/B2 on the chart.
4	**Gap between panel & bezel**

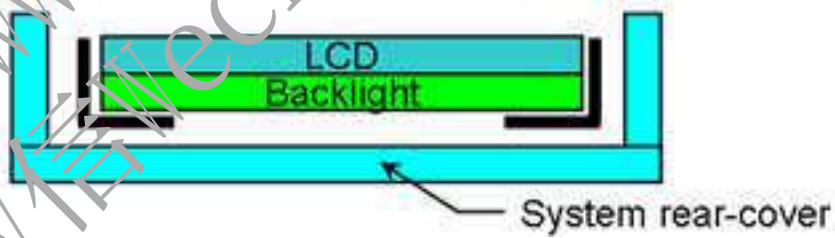


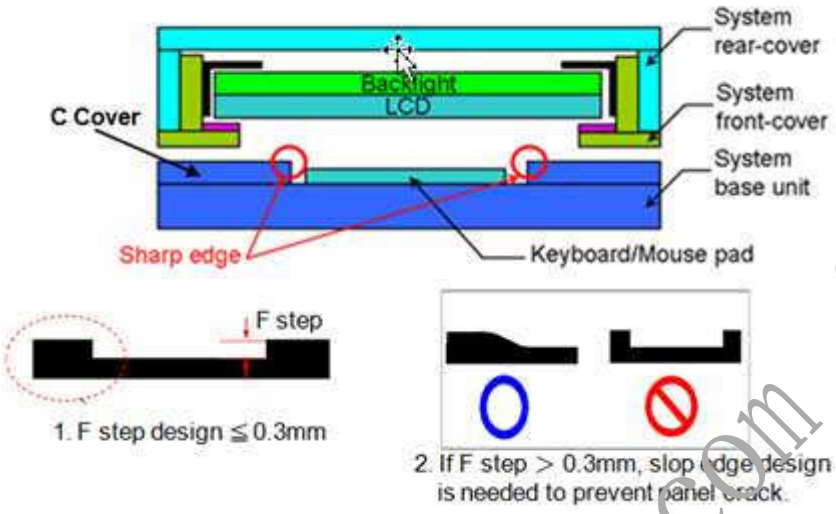
Definition	The gap between system bezel & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system front-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test or during pooling inspection procedure. To remain the sufficient gap, design with system rib higher than maximum panel thickness is recommended. The sufficient gap design is greater or equal to 0.1mm.
5	**Cable routing behind panel**



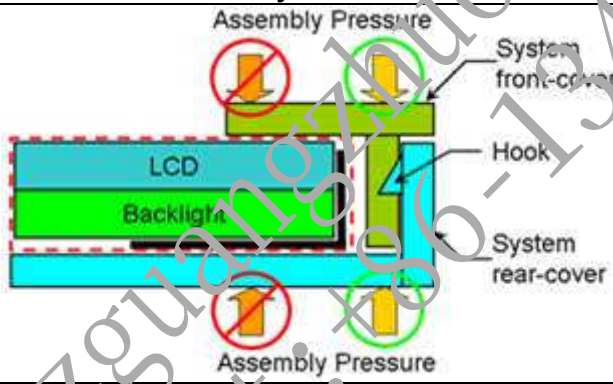
Definition	It is strongly recommended that cables route around the panel outline, not overlap with the panel outline (including PCB). Because issue such as abnormal display & white spot after backpack test, hinge test, twist test or pogo test may occur. If any routings across panel outline are needed, we suggest design as below: -Using FFC/FPC to replace cables. -Routing at the right or left area of panel metal rear. -Avoid any routings at the step of panel or A cover. -No interference to panel. -It should not overlap TCON, COF/FPC, Driver IC
6	**Interference examination of antenna cable and Web Cam wire**
	• To prevent panel damage, we suggest using CCD FPC to replace CCD cable • Using double tape to fix LCM module for no bracket design.  Rear Cover Width(A) A = 30mm Cover edge to Double Tape(B) B = 3.0mm CCD FPC thickness <0.1mm Sponge thickness 0.5mm 0.2~0.3mm(compressed)
	If the antenna cable or Web Cam wire must overlap with the panel outline, both sides of the antenna cable or Web Cam wire must have a sponge(Sponge material can not contain NH3) and sponge require higher antenna cable or Web Cam wire.(Antenna cable or Web Cam wire should not overlap with TCON,COF/FPC,Driver IC) Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
7	**System rear-cover inner surface examination**
	
Definition	Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.
8	**Tape/sponge design on system inner surface**



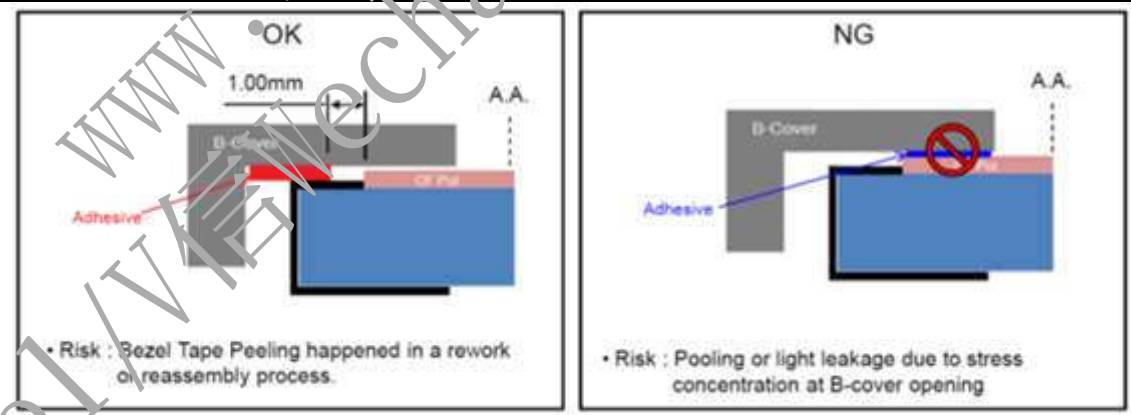
Definition	To prevent peeling the bezel tape in rework process. The length of double tape is 30 – (A+B), A is bezel tape length and B is the double tape attaching tolerance. Ex :A :2mm, B:2mm, the length of double tape is 30-(2+2)=26mm.
9	**Material used for system rear-cover**
	 System rear-cover material: Al-Mg alloy System rear-cover thickness:1.5mm MIN
Definition	System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.
10	**C cover shape design**



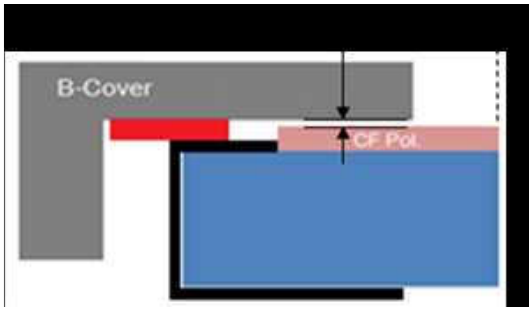
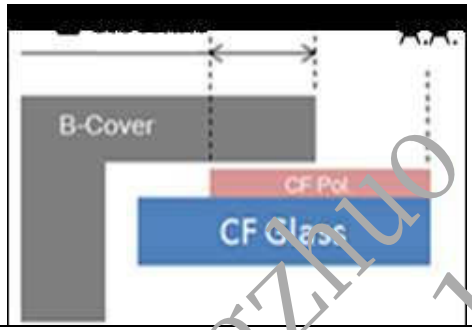
Definition	The F step design on C Cover less than or equal to 0.3mm is recommended. If F step exceeds 0.3mm, the slop edge design is necessary to prevent panel crack.
11	**Assembly SOP examination for system front-cover with Hook design**



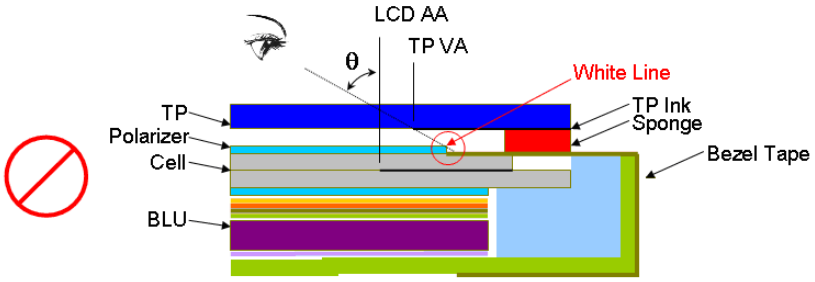
Definition	To prevent panel crack during system front-cover assembly process with hook design, it is not recommended to press panel or any location that related directly to the panel.
12	**Adhesive design between panel & bezel**

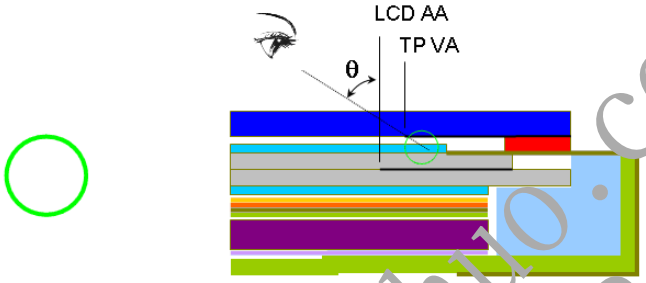


Definition	To prevent panel crack during system front-cover assembly process with double tape design, When system applied adhesive between B-Cover and LCD module, please design a distance 1.00mm between B-Cover's adhesive and CF pol. Do **NOT** put adhesive on CF pol. Adhesive material need be qualified to prevent from doing damage to cell tape after rework. Adhesive material need be qualified to prevent abnormal noise when hinge swinging test.
13	**System front-cover assembly reference with Double tape design**

	
Definition	To prevent system front-cover peeling at double tape contact area, A gap between B-Cover & CF-Pol. Is 0.1mm min.
14	System front-cover opening area reference with TFT-LCD module
	
Definition	To prevent panel the noise of B-cover & CF Pol. Distance from CF Pol. edge to front-cover edge more than 0.65mm.

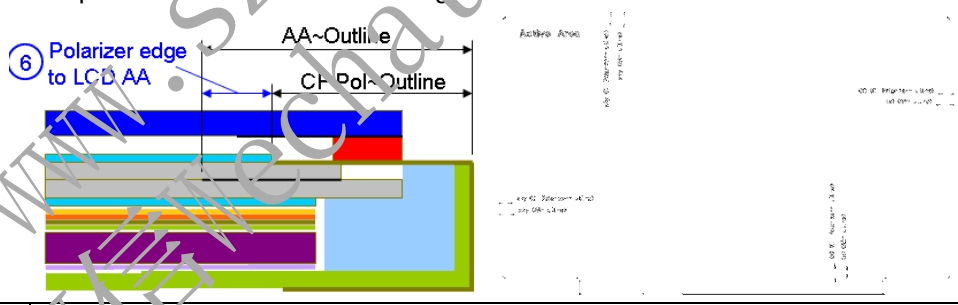
15	Touch Application : TP and LCD Module Combination for White Line Prevention



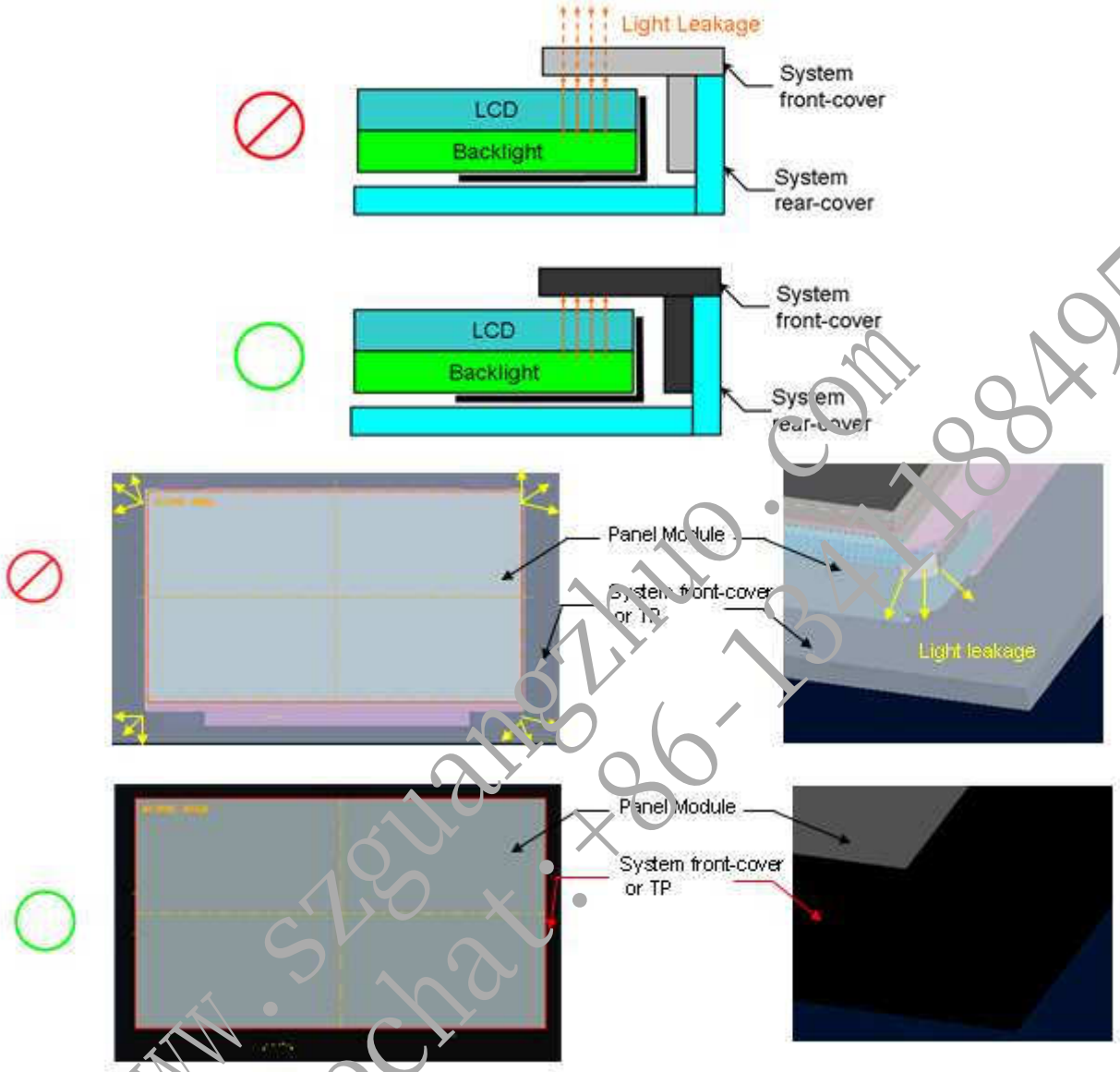


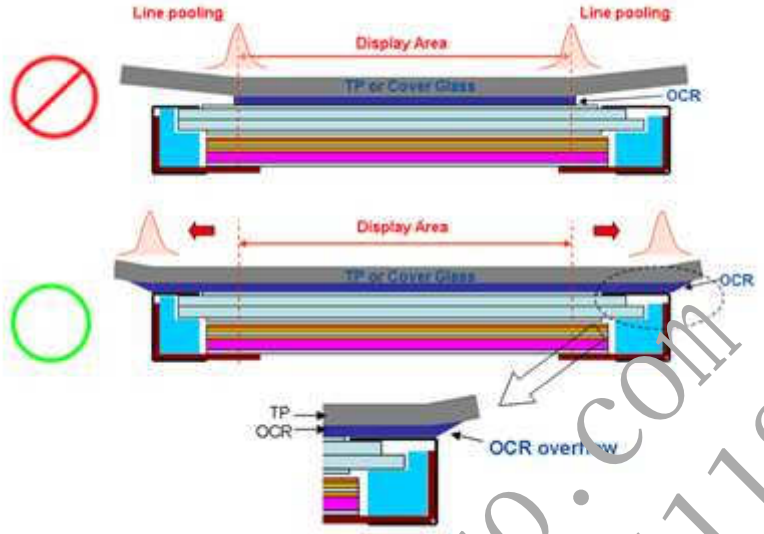
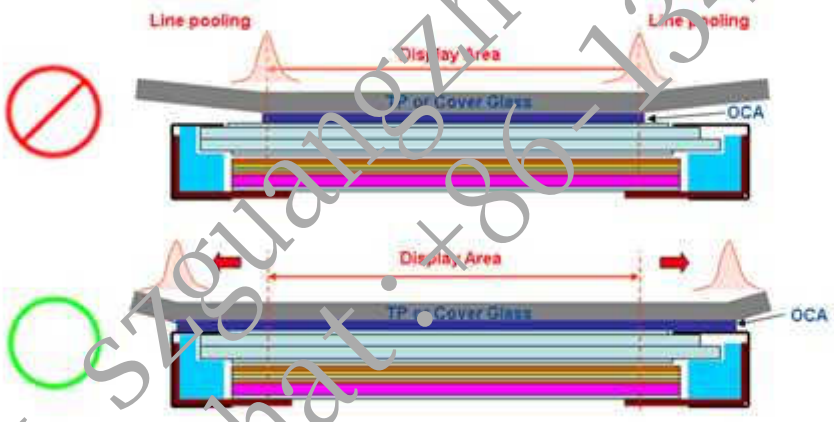
Parameter consideration for White Line Issue :	
1	TP VA to LCD AA distance
2	TP Assembly tolerance
3	TP Ink Printing tolerance
4	Sponge thickness and tolerance
5	Inspection Viewing Angle specification
6	Polarizer edge to LCD AA distance and tolerance

Polarizer edge to LCD AA distance can be derived by “AA~Outline” – “CF Pol~Outline” with respect to INX 2D Outline Drawing on each side.



Definition	For using in Touch Application: to prevent White Line appears between TP and LCD module combination, the maximum inspection angle location must not fall onto LCD polarizer edge, otherwise light line near edge of polarizer will be appear. Parameters such as TP VA to LCD AA distance, TP assembly tolerance, TP Ink printing tolerance, Sponge thickness and tolerance, and Maximum Inspection/Viewing Angle, must be considered with respect to LCD module’s Polarizer edge location and tolerance. This consideration must be taken at all four edges separately. The goal is to find parameters combination that allow maximum inspection angle falls inside polarizer black margin area. Note: Information for Polarizer edge location and its tolerance can be derived from INX 2D Outline Drawing (“AA ~Outline“ - “CF Pol~Outline”). Note: Please feel free to contact INX FAE Engineer. By providing value of parameters above on each side, we can help to verify and pass the white line risk assessment for customer reference.

16	Color of system front-cover material
	
Definition	To prevent light leakage is seen at system front-cover due to material transparency, we suggest using dark color material (black) for system front-cover design.

17	**Use OCR Lamination**
	
Definition	OCR glue as possible beyond module, in order to avoid Line Pooling
18	**Use OCA Lamination**
	
Definition	OCA glue as possible plastered throughout the module, in order to avoid Line Pooling.

Appendix. LCD MODULE HANDLING MANUAL

Purpose	• **This SOP is prepared to prevent panel dysfunction possibility through incorrect handling procedure.** • **This manual provides guide in unpacking and handling steps.** • **Any person which may contact / related with panel, should follow guide stated in this manual to prevent panel loss.**
1.	**Unpacking**

2.	**Panel Lifting**

Use slots at both sides for finger insertion.
Handle panel upward with care.

3.	Do and Don't

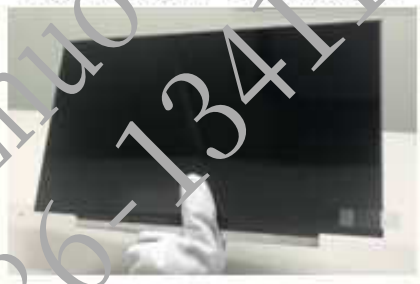
Do :

- Handle with both hands.
- Handle panel at left and right edge.

Don't :

- Lifting with one hand.

- Handle at PCBA side.



Don't :

- Stack panels.

- Press panel.

Don't :

- Put foreign stuff onto panel

- Put foreign stuff under panel

Don't :

- Paste any material unto white reflector sheet

Don't :

- Pull / Push white reflector sheet

Don't :

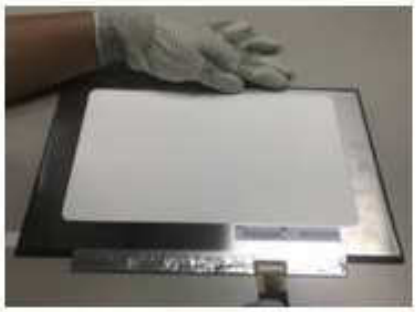
- Hold at panel corner.

Don't :

- Twist panel.

Do :

- Hold panel at top edge while inserting connector.



Don't :

- Press white reflector sheet while inserting connector.

Do :

- Remove panel protector film starts from pull tape

Don't :

- Remove panel protector film From film another side.