Product Specification Sheet

Customer: _____

Model Name: ___MNG007QX2-1___

Date: ___2024/08/13___

Version： ___V03___

Customer's Approval		CSOT	
Signature	Date	Approved By	Date
		Reviewed By	Date
		Prepared By:	Date

Record of Revision

Version	Revise Date	Page	Content
V00	2024/03/12	All	Preliminary Specification
	2024/03/14	P9	PIN 22 32 33 Voltage update
	2024/04/12	P9-P13,P20-P21	
V01	2024/06/07	15	Add LED Light Bar Power Supply Current
		22	Update Optical characteristics
		26	Add Label information
V02	2024/07/11	10	Add circuit of funciton pin
		21	Update power on/off sequence T19
		22	Update Optical characteristics Note7&Note8
		42	Update EDP Link rate capability and setting
V03	2024/08/13	P26 27	Update label
		P40	Update checksum

Contents

1. GENERAL DESCRIPTION

1.1 OVERVIEW

MNG007QX2-1 is a 16" TFT Liquid Crystal Display module with LED Backlight unit and 40 pins eDP 1.4b interface.
This module supports 1920 x 1200 mode and can display 16.7M colors.

1.2 SPECIFICATION SUMMARY

No.	Item	Specification	Unit	Note
1	LCD size	16.0	inch	
2	Resolution	1920 x RGB x 1200		WUXGA
3	Pixel Arrangement	RGB		
4	Model Type	LCM		
5	TFT Technology	Oxide		
6	Display mode	HFS, Normally Black		
7	Active Area	344.6784 (H) × 215.424(V)	mm	
8	pixel pitch	179.52(H)×179.52(V)	um	
9	Display Colors	16.7M		
10	Contrast Ratio	1000:1(Typ)		
11	Color Gamut	45%(Typ) / 42%(min)	CIE1931	
12	LCM Outline Dimension	349.68×224.42×3.05	mm	Typical
13	Luminance	300(Typ)	nits	
14	Low blue light ratio	NA	%	Max
15	Surface treatment(L/P)	Fine AG(Haze 25%)	--	Pol.
16	Interface	eDP 1.4b		4lane@5.4G w/o DSC
17	Refresh Rate	48-144	Hz	
18	Function	PSR2、LRR2.5、SDRRS、DMRRS、VRR		Intel
		PSR-SU、Freesync		AMD
		Gsync、DDS(PSR API)		NV
		OD、ABOT、APOL		Other
19	Method of Inversion	Column Inversion		
20	Power consumption of Panel	1.0(Max)	W	3.3V@Mosaic 144Hz
	Power consumption of Backlight	3.6	W	Max
21	Weight	380	g	Max

Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS =3.3 V, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 ℃, whereas mosaic pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Parameter		Min.	Typ.	Max.	Unit	Note
Unit outline dimensions	Width	349.38	349.68	349.98	mm	
	Height	224.12	224.42	224.72	mm	
	Depth	2.9	3.05	3.2	mm	
Weight		-	-	380	g	

2.1 INTERFACE CONNECTION

Pin40   Pin1
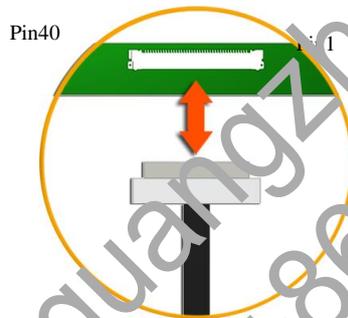
Please refer Appendix Outline Drawing for detail design.

Connector Part No.: **MSAK24025P40M**

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	℃	(1)
Operating Ambient Temperature	T_{OP}	0	+50	℃	(1)

Relative Humidity (% RH)
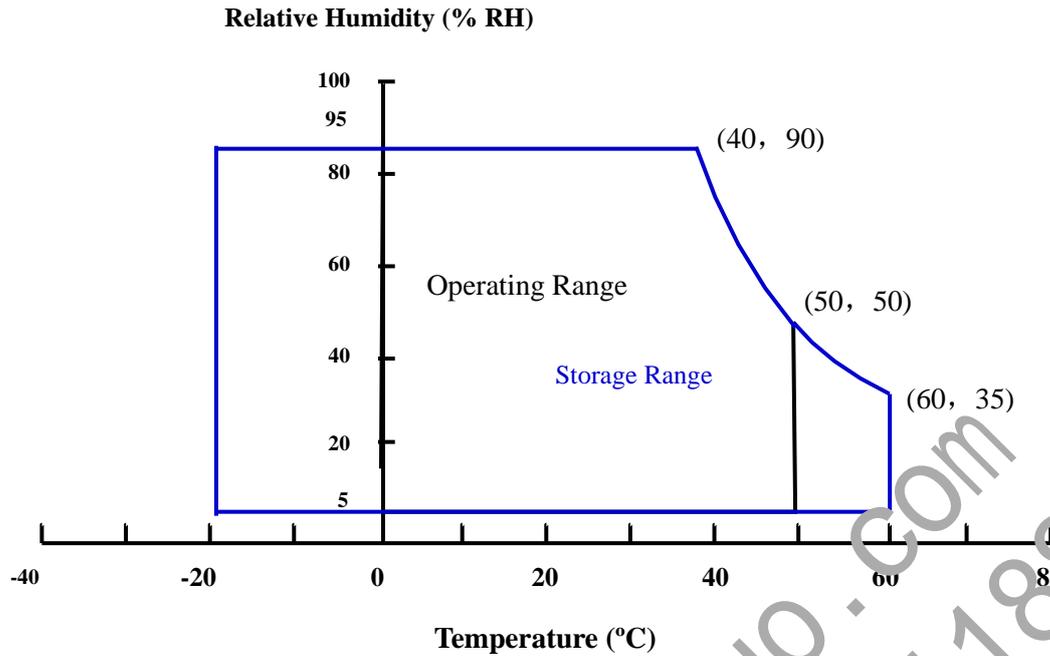
Note (1)

(a) 90% RH Max. (Ta <= 40 ℃).

(b) Wet-bulb temperature should be 39 ℃ Max. (Ta > 40 ℃).

(c) No condensation.

3.2   ELECTRICAL ABSOLUTE RATINGS

3.2.1   TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	+0.3	+4	V	(1)
Logic Input Voltage	VIN	+0.3	+3.6	V	
LCD_Self Test	BIST	-0.3	+5	V	`
Over Driver	OD	-0.3	+2.5	V	(1)
I2C_TCCN_SDA	SDA	-0.3	+2.5	V	(1)
I2C_TCON_SCL	SCL	-0.3	+2.5	V	(1)
Converter Input Voltage	LED_VCCS	-0.3	+26	V	(1)
Converter Control Signal Voltage	LED_PWM,	-0.3	+3.6	V	(1)
Converter Control Signal Voltage	LED_EN	-0.3	+3.6	V	(1)

Note (1) Stresses beyond those listed in above "ELECTRICAL ABSOLUTE RATINGS" may cause permanent damage to the device. Normal operation should be restricted to the conditions described in "ELECTRICAL CHARACTERISTICS".

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM
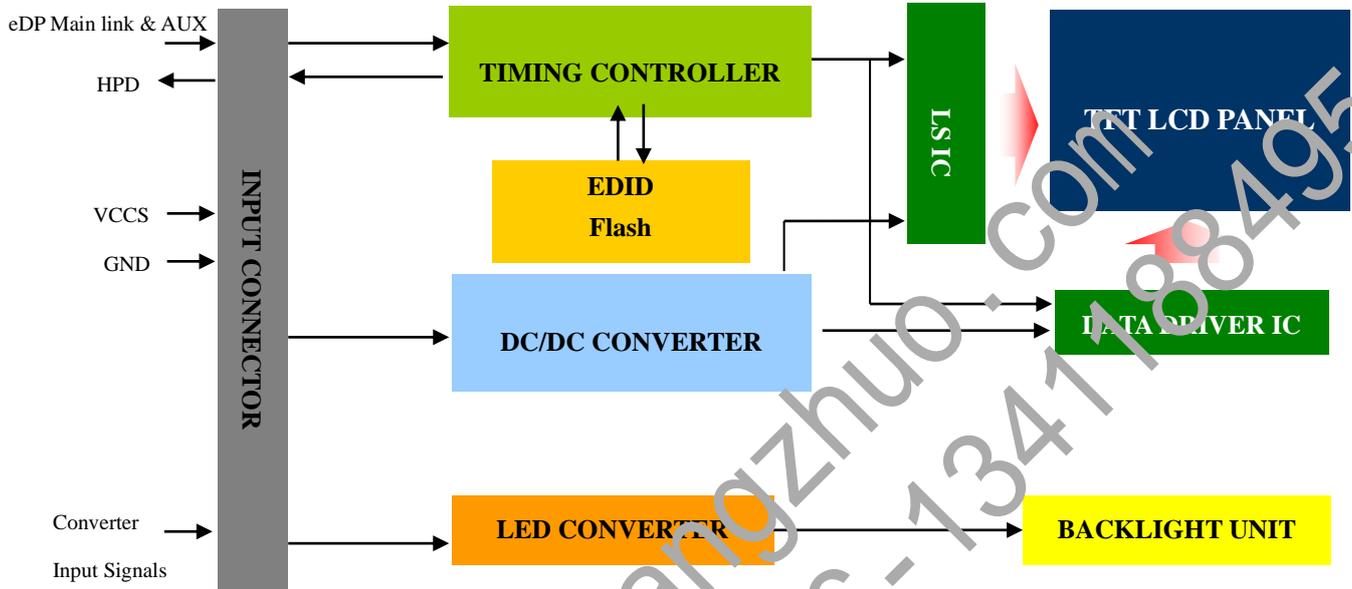
4.2 INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	I/O	Voltage(V)	Note
1	I2C_SCL	I2C SCL or APOL	I/O	1.8	
2	H_GND	High Speed Ground	GND	0	
3	Lane3_N	Comp Signal Link Lane 3	I	0.2	
4	Lane3_P	True Signal Link Lane 3	I	0.2	
5	H_GND	High Speed Ground	GND	0	
6	Lane2_N	Comp Signal Link Lane 2	I	0.2	
7	Lane2_P	True Signal Link Lane 2	I	0.2	
8	H_GND	High Speed Ground	GND	0	
9	Lane1_N	Comp Signal Link Lane 1	I	0.2	
10	Lane1_P	True Signal Link Lane 1	I	0.2	
11	H_GND	High Speed Ground	GND	0	
12	Lane0_N	Comp Signal Link Lane 0	I	0.2	
13	Lane0_P	True Signal Link Lane 0	I	0.2	
14	H_GND	High Speed Ground	GND	0	

15	AUX_CH_P	True Signal Auxiliary Ch.	I/O	0.2	
16	AUX_CH_N	Comp Signal Auxiliary Ch.	I/O	0.2	
17	H_GND	High Speed Ground	GND	0	
18	LCD_VCC	LCD logic and driver	Input Power	3.3	
19	LCD_VCC	LCD logic and driver	Input Power	3.3	
20	LCD_VCC	LCD logic and driver	Input Power	3.3	
21	LCD_VCC	LCD logic and driver	Input Power	3.3	
22	LCD Self Test	LCD Panel Self Test Enable	I	3.3	
23	ABOT	ABOT enable	I	1.8	
24	LCD_GND	LCD logic and driver	GND	0	
25	LCD_GND	LCD logic and driver	GND	0	
26	LCD_GND	LCD logic and driver	GND	0	
27	HPD	HPD signal pin	O	2.7	
28	BL_GND	Backlight_ground	GND	0	
29	BL_GND	Backlight_ground	GND	0	
30	BL_GND	Backlight_ground	GND	0	
31	APOLC	APOL control signal	I/O	1.8	
32	BL_Enable	Backlight On / Off	I	1.8/3.3	
33	BL_PWM_DIM	System PWM signal Input	I/O	1.8/3.3	
34	I2C_SDA	I2C SDA for APOL	I/O	1.8	
35	HW	MOS preventing I2C overwrite	Floating	NC	For CSOT Use
36	BL_PWR	Backlight power	Input Power	5~21V	
37	BL_PWR	Backlight power	Input Power	5~21V	
38	BL_PWR	Backlight power	Input Power	5~21V	
39	BL_PWR	Backlight power	Input Power	5~21V	
40	OD_EN	Over Drive Enable Pull high(1): OD off; Pull low(0): OD on	I	1.8	Disable@high(default),enable@low

Note (1)   The circuit of funciton pin is shown in the following figure.

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CSOT/ MNG007QX2-1		
Pin No.	23	40
Symbol	ABOT	OD_EN
I/O	Input	Input
Input status	High	Disable	Disable
	Floating	Disable	Disable
	Low	Enable	Enable
Circuit		
Pin No.	27	31
Symbol	HPD	APOLC
I/O	Output	Output
Circuit		
Pin No.	1/34	22
Symbol	I2C	BIST
I/O	Input/Output	Input
Circuit		

Pin No.	32	33
Symbol	BL_EN	BL_PWM
I/O	Input	Input
Circuit		

Note (2)   The pixel is shown in the following figure.
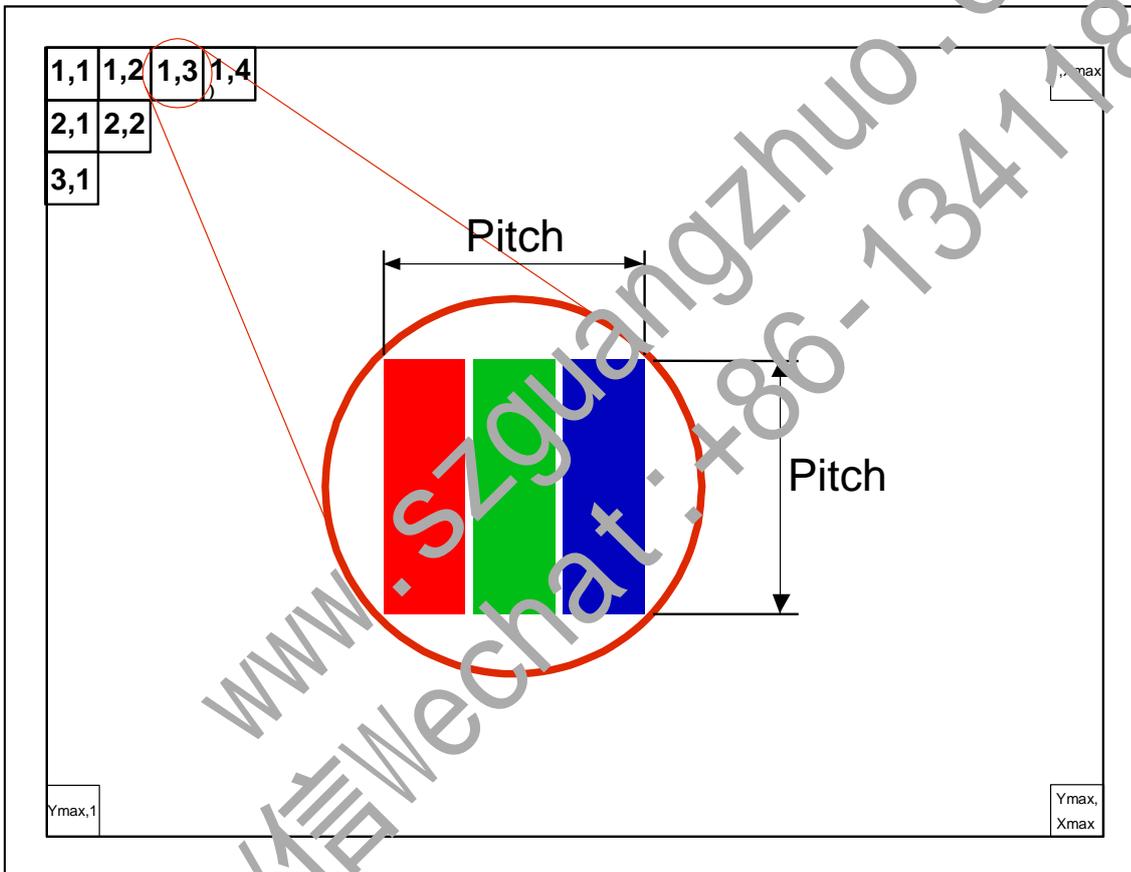
Note (2) I2C using information:

1.TCON I2C(DDS) address: 0xC2(11000010)

2.PMIC address: 0x46 (0100011x)

3.LED Driver: 0x6C(A0=0) (01101000)

4.3   ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)
BIST Control Level		BIST on	1.65	3.3	3.6	V	(1)
		BIST off	0	-	0.5	V	(1)
I2C(SDA/SCL)		on	1.65	1.8	1.98	V	(1)
		off	0	-	0.5	V	(1)
OD(Over Driver)		off	1.65	1.8	1.98	V	(1)
		on	0	-	0.5	V	(1)
Ripple Voltage		V_{RP}	-	-	100	mV	(1)
Inrush Current		I_{RUSH}	-	-	1.5	A	(1)(2)
Power Supply Current	Mosaic	I_{LCD}	-	-	303.03	mA	(3)
Power consumption	Mosaic	P_{LCD}	-	-	1.0	W	(3)
Power Supply Current	Heavy loading	I_{LCD}	-	-	666.67	mA	(4)
Power consumption	Heavy loading	P_{LCD}	-	-	2.2	W	(4)

Note (1) The ambient temperature is Ta = 25 ± 2 ℃.

Note (2) I_{RUSH}: the maximum current when VCCS is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions. Shown as the following figure.

Test pattern: Mosaic

VCCS rising time is 0.5ms
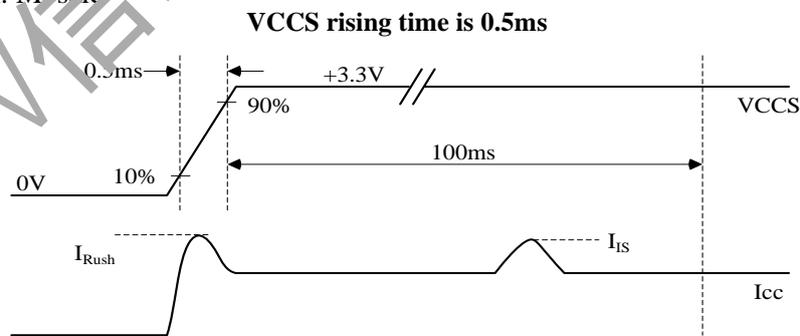
Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ℃, DC Current

and f_v = 144 Hz, whereas a power dissipation check pattern below is displayed.

Mosaic Pattern

Note (4) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 + 2 ℃, DC Current

and f_v = 144 Hz, whereas a power dissipation Heavy loading pattern below is displayed.
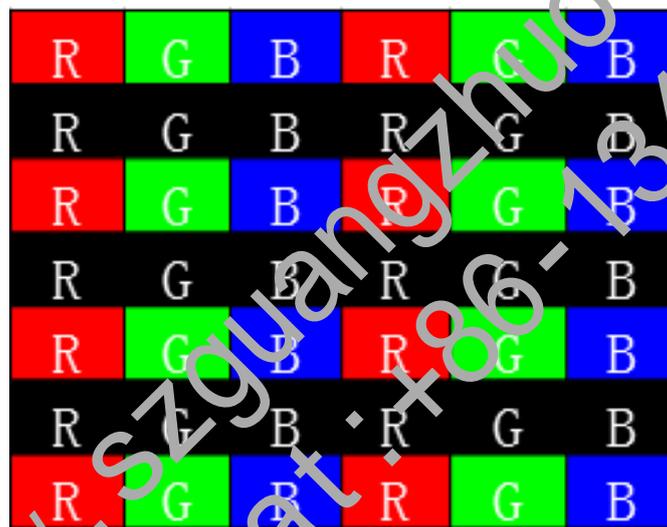
LED CONVERTER SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input power supply voltage		LED_Vccs	5.0	12.0	21.0	V	
Converter Inrush Current		ILED$_{RUSH}$	-	-	1.5	A	(1)
EN Control Level	Backlight On		1.65/2.2	1.8/3.3	2.2/3.6	V	
	Backlight Off		0	-	0.5	V	
PWM Control Level	PWM High Level		1.65/2.2	1.8/3.3	2.2/3.6	V	

	PWM Low Level		0	-	0.5	V	
PWM Control Duty Ratio			1	-	100	%	
PWM Control Permissive Ripple Voltage		V_{PWM_pp}	-	-	100	mV	
PWM Control Frequency		f_{PWM}	200	-	2000	Hz	
LED Power consumption		P_L	-	-	3.6	W	(2)
LED Power Current	LED_VCCS =Typ.	IL-	-	-	300	mA	(3)

Note (1)　　$ILED_{RUSH}$: the maximum current when LED_VCCS is rising,

$ILED_{IS}$: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 ℃, f_{PWM} = 200 Hz, Duty=100%.

VLED rising time is 0.5ms
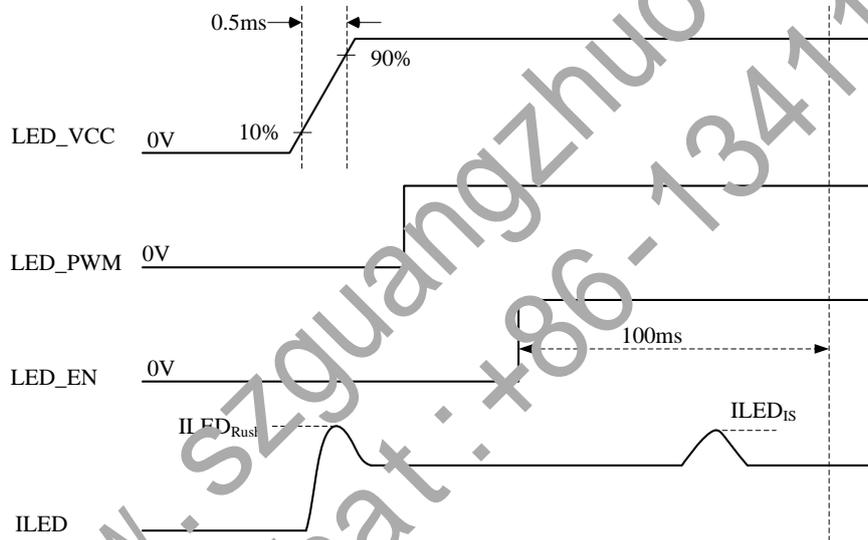
Note(2) $P_L = I_L \times V_L$　(With LED converter transfer efficiency);

Note (3) The specified LED power supply current is under the conditions at "LED_VCCS = Typ.", Ta = 25 ± 2 ℃, fPWM = 200 Hz, Duty=100%.

4.3.1 BACKLIGHT UNIT

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```
                                          1   A1
                                          2   A2
                                          3   NC
                                          4   GND
                                          5   K1
                                          6   K2
                                          7   K3
                                          8   K4
                                          9   K5
                                          10  K6
```
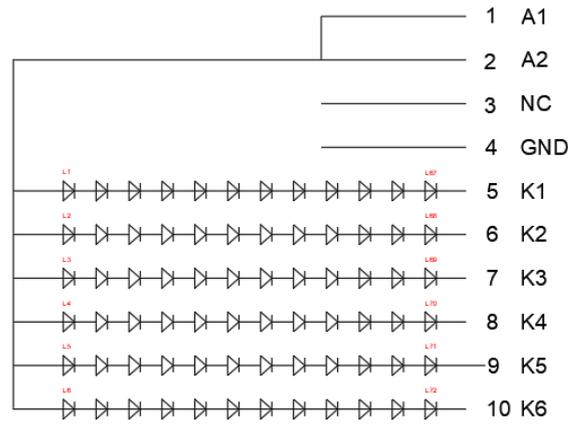
LED: 72ea(6P-12S)

Ta = 25 ± 2 ℃

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	VL	-	33.6	34.3	V	(1)(2)
LED Light Bar Power Supply Current	IL	-	14.5	-	mA	(Duty100%)
Power Consumption	PL	-	-	3.6	W	(3)
LED Life Time	L_{BL}	15000	-	-	Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter :

Note (2) For better LED light bar driving quality it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 ℃ and $I_L = 20$ mA(Per EA) until the brightness becomes ≤ 50% of its original value.

4.4   INPUT SIGNAL TIMING SPECIFICATIONS

4.4.1 eDP AUX Channel Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Unit Interval for AUX channel	UI_{AUX}	0.4	-	0.6	μS	
Peak-to-peak voltage at TP1	$V_{AUX-DIFF-pp}$	0.18	0.2	1.38	V	
AUX DC Common mode Voltage	$V_{AUX-DC-CM}$	0	-	1.2	V	
AUX Short current limit	I_{AUX_SHORT}	-	-	90	mA	
AUX CH termination DC resistor	R_{AUX_TERM}	80	100	120	Ω	Differential input
AUX AC coupling capacitor	C_{AUX}	75	-	200	nF	

| Number of pre-charge pulses | Pre-charge pulses | 10 | - | 16 | | |

4.4.2 eDP Main Link Receiver Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Link clock down spreading	$Down\_Spread\_Amplitude$	0		0.5	%	
Differential Peak-to-peak Input Voltage at Rx package pins	$V_{RX-DIFFp-p}$	120	-	-	mV	
Differential termination resistance	$R_{RX-TERM}$	80	90	100	Ω	
RX short circuit Current Limit	$I_{RX-SHORT}$	-	-	50	mA	
Lane Intra-pair Skew at RX package pins	$T_{RX-SKEW-INTRA-PAIR-High-Bit-Rate}$	-	-	50	ps	

4.4.3 eDP AUX Channel Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Hot plug Detect	V_{HPD}	2.5	-	2.8	V	

Note (1) Display port interface related AC coupled signals are following VESA Display Port Standard V1.4b.
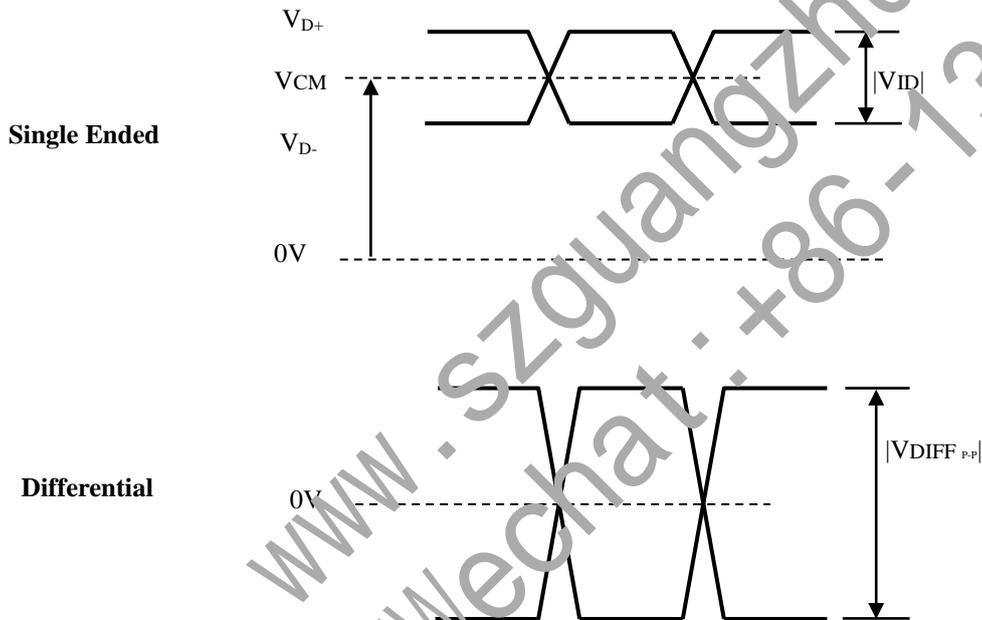
4.4.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color	Data Signal																							
	Red								Green								Blue							
	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0

Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specification is showed as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
	Frame	TV	/	144	/	Hz	
DCLK	Frequency	1/Tc	/	389.38	/	MHz	-
DE	Vertical Total Time	TV	/	1300	/	TH	-
	Vertical Active Display Period	TVD	/	1200	/	TH	-
	Vertical Active Blanking Period	TVB	/	100	/	TH	-
	Horizontal Total Time	TH	/	2080	/	Tc	-
	Horizontal Active Display Period	THD	/	1920	/	Tc	-
	Horizontal Active Blanking Period	THB	/	160	/	Tc	-

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
	Frame	TV	/	60	/	Hz	
DCLK	Frequency	1/Tc	/	162.24	/	MHz	-
DE	Vertical Total Time	TV	/	1300	/	TH	-
	Vertical Active Display Period	TVD	/	1200	/	TH	-
	Vertical Active Blanking Period	TVB	/	100	/	TH	-
	Horizontal Total Time	TH	/	2080	/	Tc	-
	Horizontal Active Display Period	THD	/	1920	/	Tc	-

| Horizontal Active Blanking Period | THB | / | 160 | / | Tc | - |

Note (1) Display timing signal should be contained and transferred by Display Port Main Link stream data packing described in VESA Display Port Standard V1.4b.

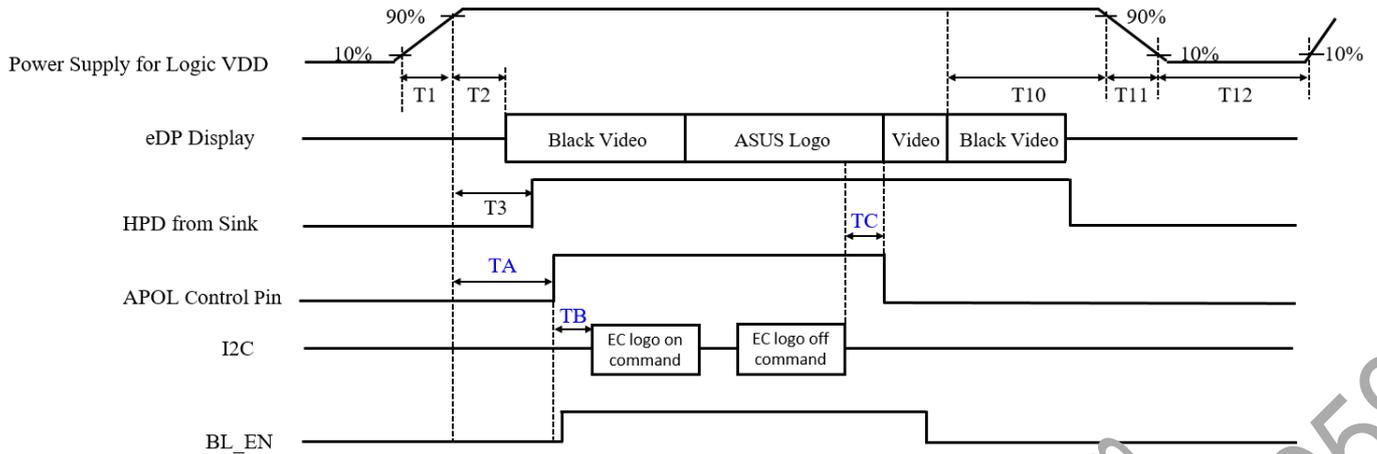### INPUT SIGNAL TIMING DIAGRAM
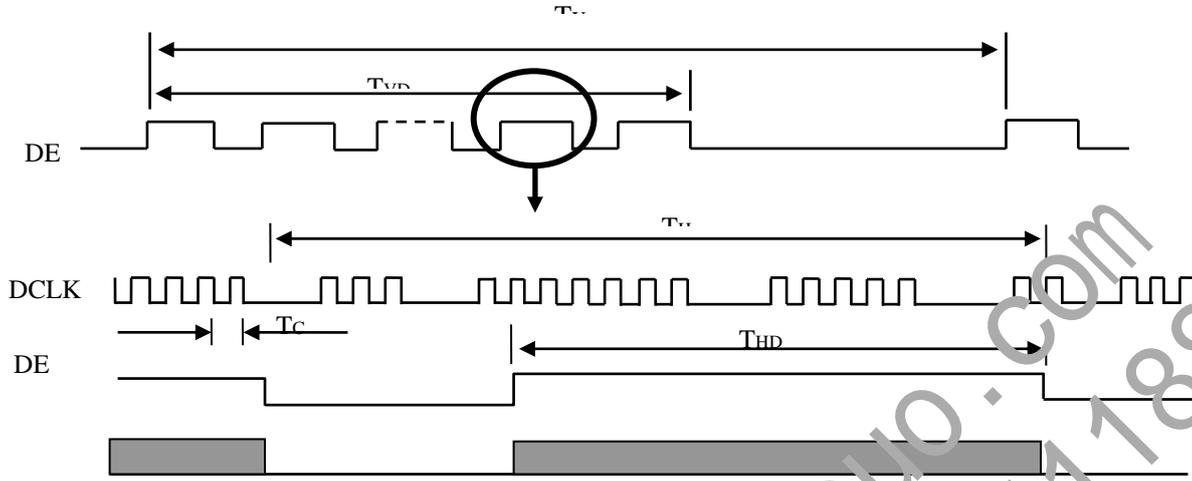
4.6 POWER ON/OFF SEQUENCE
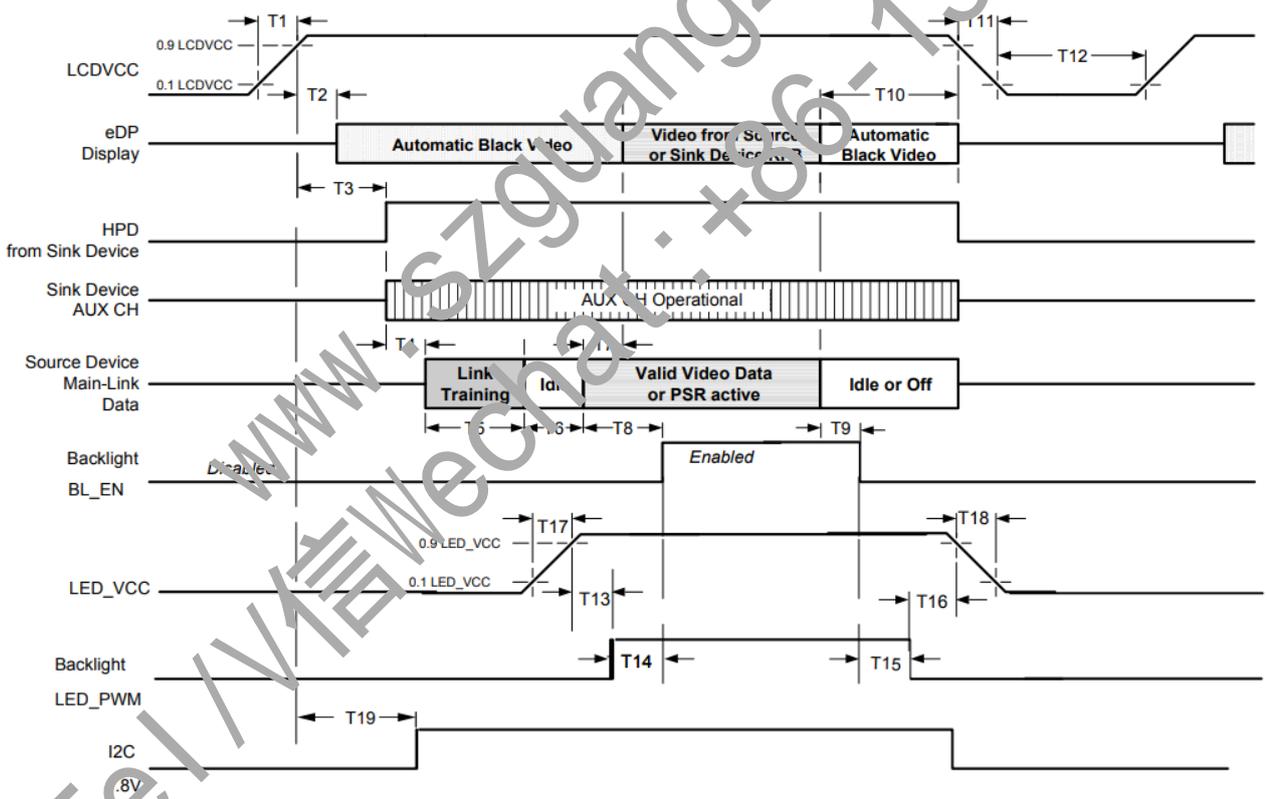
APOL version: V2.3

Guangzhou China Star Optoelectronics Technology Co.,Ltd

| Power Supply for Logic VDD | 90% / 10% ... T1 T2 ... T10 T11 T12 ... 90% 10% 10% |

eDP Display — Black Video | ASUS Logo | Video | Black Video

HPD from Sink — T3

APOL Control Pin — TA ... TC

I2C — TB ... EC logo on command | EC logo off command

BL_EN

Other mode:

Power Supply for Logic VDD — 90% / 10% ... T1 T2 ... T10 T1 T2 ... 90% 10% 10%

eDP Display — Black Video | Video | Black Video

HPD from Sink — T3

APOL Control Pin — TA ... TD

I2C — No EC logo on/off command

BL_EN
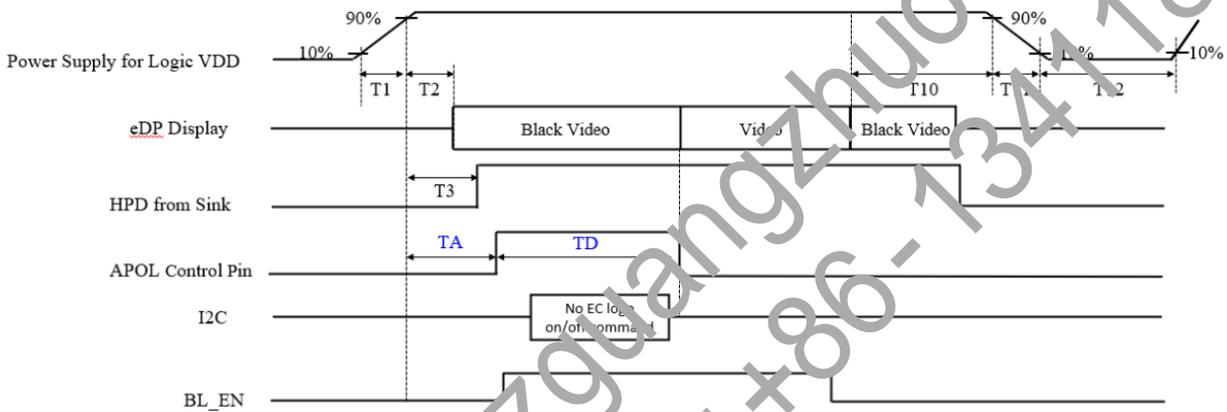
Symbol	Description	Min	Typ.	Max	Unit	Note
T1	Power rail rise time, 10% to 90%	0.5		10	ms	
T2	Delay from LCD,VCCS to eDP Display	0		80	ms	
T3	Delay from LCD,VCCS to HPD high	0		80	ms	
T4	Delay from Sink AUX to link training initialization	-		-	ms	
T5	Link training duration	-		-	ms	
T6	Link idle	-		-	ms	
T7	Delay from valid video data from Source to video on display	0		50	ms	
T8	Delay from valid video data from Source to backlight on	-		-	ms	
T9	Delay from backlight off to end of valid video data	0		T10-50	ms	

		Min.		Max.	Unit	
T10	Delay from end of valid video data from Source to power off	50		500	ms	
T11	VCCS power rail fall time, 90% to 10%	-		10	ms	(1)
T12	VCCS Power off time	500		-	ms	
T13	Delay from VCC to PWM	0		-	ms	
T14	Delay from PWM to LED ENABLE	0		-	ms	
T15	Delay from LED ENABLE to PWM Disable	0		-	ms	
T16	Delay from PWM Disable to VBL 90%	0		-	ms	
T17	Delay from VBL 10% to VBL 90%	0		-	ms	
T18	VBL power rail fall time, 90% to 10%	0		-	ms	
T19	Delay from LCD_VCC to I2C Signal	20	-	-	ms	
TA	Delay from LCD,VCCS to APOL on	0	-	100	ms	
TB	Delay from APOL on to EC logo on command	0	-	25	ms	
TC	Delay from EC logo off command to APOL off	0	-	1	frame	
TD	Delay from APOL on to APOL off (No EC logo)	0	-	50	ms	

Note (1) Please follow the power on/off sequence described above. Otherwise, the LCD module might

abnormal display or be damaged.

Note (2) Please avoid floating state of interface signal at invalid period. When the interface signal is invalid, be sure to pull down the power supply of LCD VCCS to 0 V.

Note (3) The backlight must be turned on after the power supply for the logic and the interface signal is valid.

The backlight must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Please follow the LED backlight power sequence as above. If the customer could not follow, it might cause backlight flash issue during display ON/OFF or damage the LED backlight controller

5. Optical characteristics

	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing angle range	Left/Right	CR>10	80	-	89	Deg.	(1), (3), (4), (6)
	Upper/Lower		80	-	89		
Contrast ratio	CR		800	1000	-	-	(2), (4), (6)
Response time	Tr +Tf	θ=0 deg.	-	-	10		(5)
	GTG ave wi OD		-	-	3.8	ms	
	GTG ave wo OD		-	-	7.5	ms	

Chromaticity of white	x			0.313		-	
	y			0.329		-	
Chromaticity of red	x		Typ.	0.581	Typ.	-	
	y			0.359		-	(2), (6)
Chromaticity of green	x		-0.03	0.356	+0.03	-	Normal operation
	y			0.570		-	
Chromaticity of blue	x			0.161		-	
	y			0.115		-	
Gamut	%		42%	45%.	-	NTSC	
Luminance of White	Y_{LI}	-	255	300	-	cd/m^2	(7)
Gamma	-	-	2.0	2.2	2.4	-	Gray 15~240
Flicker	60hz	Flicker pattern	-	-	-25	dB	/
White uniformity 5pt	δW	θ =0 deg.	-	-	1.25	-	(8)
White uniformity 13pt	δW	θ =0 deg.	-	-	1.5	-	(2), (8)

※The measurement shall be taken 5 minutes after lighting the LCM at the following rating.
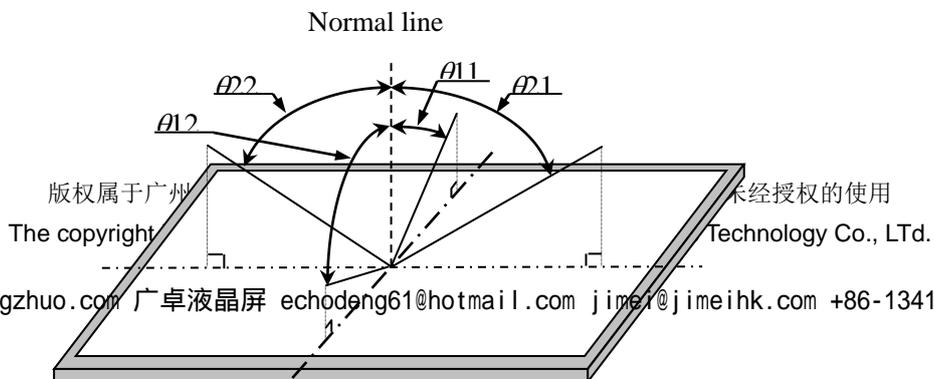
※The optical characteristics shall be measured in a dark room or equivalent.

Note (1) Measurement of viewing angle range

Note (2) Measurement of luminance and Chromaticity and Contrast.
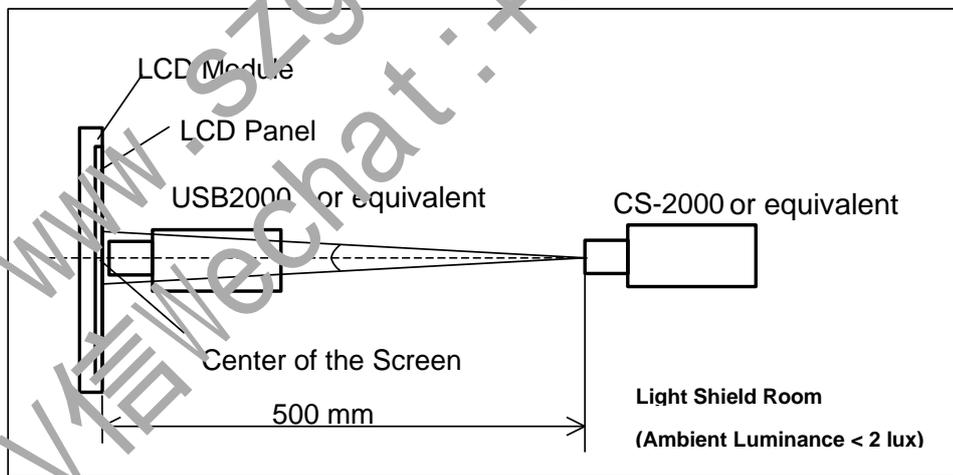
Note (3) Definitions of viewing angle range:
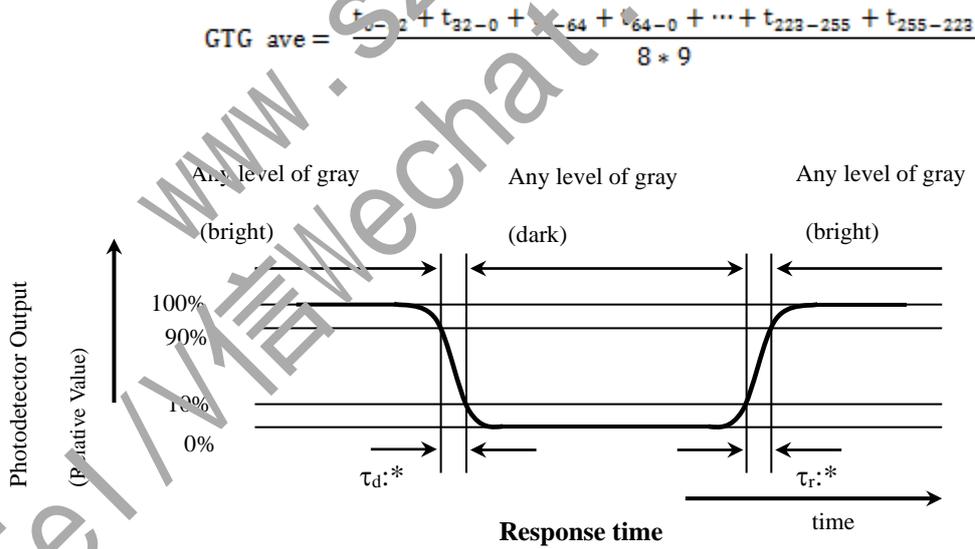
Viewing angle

Note (4)   Definition of contrast ratio:

The contrast ratio is defined as the following.

$$\text{Contrast Ratio} = \frac{\text{Luminance(Brightness) with all pixels white}}{\text{Luminance(Brightness) with all pixels Black}}$$

Note (5) Definition of response time:

The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white" .
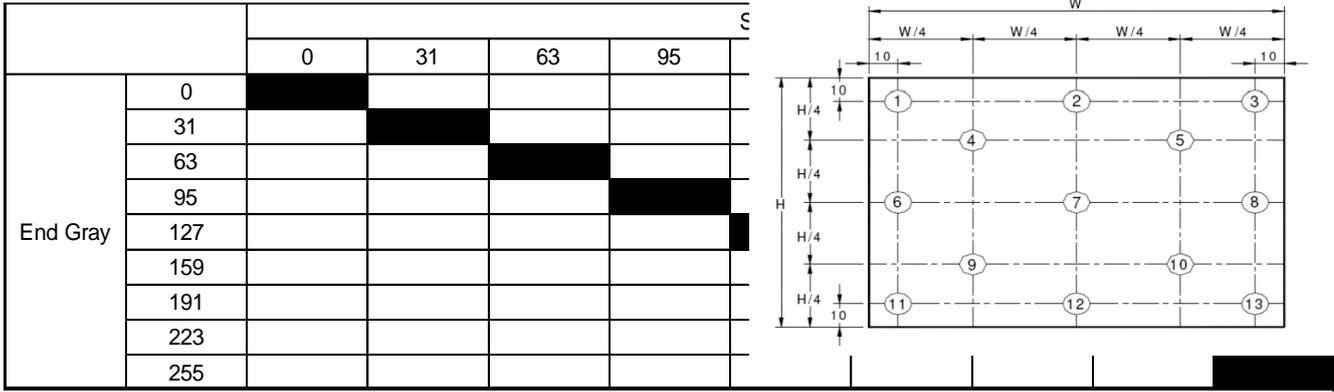
$$\text{GTG ave} = \frac{t_{0-32} + t_{32-0} + t_{0-64} + t_{64-0} + \cdots + t_{223-255} + t_{255-223}}{8*9}$$

Response time

		0	31	63	95	
End Gray	0	■				
	31		■			
	63			■		
	95				■	
	127					■
	159					
	191					
	223					
	255					■

Response time

Note (6) This shall be measured at center of the screen..

Note (7) The Luminance of White is the average of 5 points measurements (4,5,7,9,10) showing in the Fig.9-5

Note (8) Definition of white uniformity:

White uniformity of 5 points is defined as the following with 5 measurements(4,5,7,9,10).

$$\delta_{W1} = \frac{Maximum\ Luminance\ of\ 5\ Points(Brightness)}{Minimum\ Luminance\ of\ 5\ Points(Brightness)}$$

White uniformity of 13 points is defined as the following with 13 measurements(1~13).

$$\delta_{W2} = \frac{Maximum\ Luminance\ of\ 13\ Points(Brightness)}{Minimum\ Luminance\ of\ 13\ Points(Brightness)}$$

Fig.9-5

6. Reliability Test Items

No.	Test Item	Conditions
1	High temperature storage test	60℃, 240 hours
2	Low temperature storage test	-20℃, 240 hours
3	High temperature & high humidity operation test	50℃/80%RH，240hrs
4	Low temperature operation test	0℃，240hrs
5	Thermal shock test	-20℃/30minutes、60℃/30minutes 100cycles
6	ESD	150pF[330Ω]，Contact: ±8KV，Air: ±15KV

[Result Evaluation Criteria] Under the display quality test condition with normal operation state.

Do not change these condition as such changes may affect practical display function.

[Normal operation state] temperature：＋15℃~＋35℃，Humidity：45~75%，Atmospheric pressure：86~106kPa
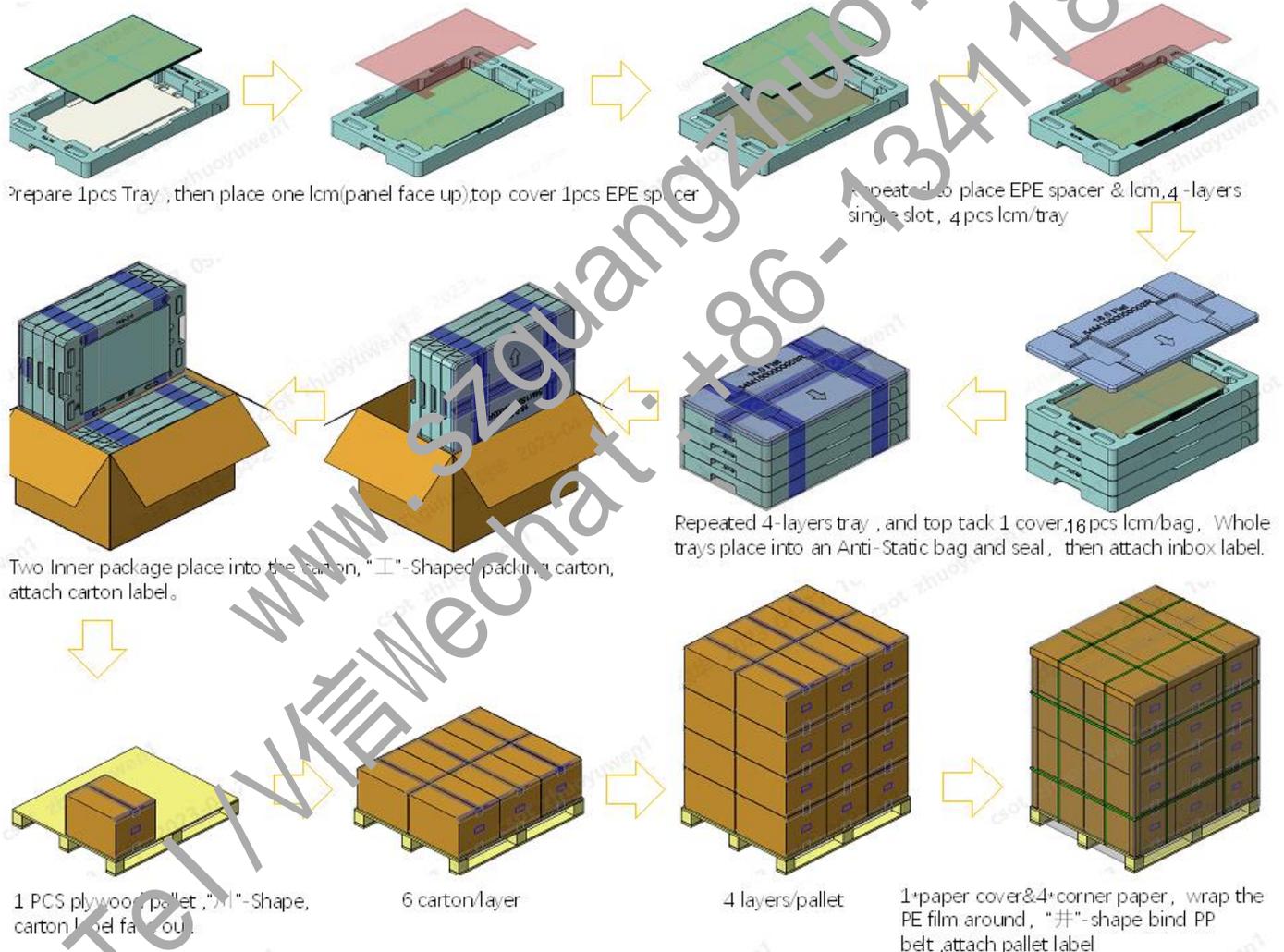
7. Display Quality

The display quality of the color TFT-LCD Module shall be in compliance with the Incoming Inspection Standard.

8. Packaging Condition

8.1 Packing Specifications

Item	Specification	Remark
Carton(Box) Packing	32 PCS/Carton(Box)	4 PCS/Tray,（4+1）*2
Carton(Box) Packing Size	490mm(L)x392mm(W)x310mm(H)	Length x Width x Height
Pallet Packing	24 Carton(Box)/Pallet	6*4
Pallet Packing Size	1200mm(L)x1000mm(W)x1360mm(H)	Length x Width x Height

8.2 Packing Method

Prepare 1pcs Tray , then place one lcm(panel face up),top cover 1pcs EPE spacer.

Repeated to place EPE spacer & lcm,4 -layers single slot , 4 pcs lcm/tray

Repeated 4-layers tray , and top tack 1 cover,16 pcs lcm/bag, Whole trays place into an Anti-Static bag and seal, then attach inbox label.

Two Inner package place into the carton, "工"-Shaped packing carton, attach carton label。

1 PCS plywood pallet ,"井"-Shape, carton label face out

6 carton/layer

4 layers/pallet

1*paper cover&4*corner paper, wrap the PE film around, "井"-shape bind PP belt ,attach pallet label

8.3 Label

Guangzhou China Star Optoelogy Technology Co.,Ltd

RoHS

Model Name:MNG007QX2-1　　Ver.: ##
Part No:11NG007QX21001　　Qty.: 16
Customer No: 18010-16060600　WT: ##.###
　　　　　　　　　　　　　　　KG

华星光电 CSOT

Inbox ID: $Z_1Z_2Z_3Z_4Z_5Z_6Z_7Z_8Z_9Z_{10}Z_{11}Z_{12}Z_{13}Z_{14}Z_{15}Z_{16}Z_{17}Z_{18}Z_{19}Z_{20}$
Note:　　　　　　　　　　　　　　　Made in China

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(1) 华星光电 CSOT

(2) cRUus

(3) RoHS

MADE IN CHINA
(4)

(7)

MNG007QX2-1　(5)

18010-16060600M23

96CAC0001　(6)

ASUSTEK	华硕电脑有限公司	Ver.:##
厂商	华星光电技术有限公司	
厂商料号	MNG007QX2-1 / MNG007QX2-1	
华硕料号	18010-16060600 / 18010-16060600	
品名	LCD 16.0' WUXGA WV EDP BC3 144HZ	
规格	CSOT/MNG007QX2-1	
CSOT PID	11NG007QX21001	
Stage code	MP	
数量	32 / 32	2 / 2
制造周别 (D/C)	2404 / 2404	
Lot No.	500145371240125 / 500145371240125	
原产地	China / China	
Carton No.	$Z_1Z_2Z_3Z_4Z_5Z_6Z_7Z_8Z_9Z_{10}Z_{11}Z_{12}Z_{13}Z_{14}Z_{15}$ $Z_1Z_2Z_3Z_4Z_5Z_6Z_7Z_8Z_9Z_{10}Z_{11}Z_{12}Z_{13}Z_{14}Z_{15}$	
MSL	NA	
净重	## KG	
毛重	## KG	

ASUSTEK	华硕电脑有限公司	Ver.:##
厂商	华星光电技术有限公司	
厂商料号	MNG007QX2-1 / MNG007QX2-1	
华硕料号	18010-16060600 / 18010-16060600	
栈板ID	$Z_1Z_2Z_3Z_4Z_5Z_6Z_7Z_8Z_9Z_{10}Z_{11}Z_{12}Z_{13}Z_{14}Z_{15}Z_{16}$	
栈板总数量	768 / 768	24 / 24
最旧制造周别 (D/C)	2404 / 2404	
原产地	China / China	
交货日期	240125 / 240125	

9. RoHS Directive

This LCD Module is compliant with RoHS Directive.

10. Handling Precautions

a) Be sure to turn off the power supply when inserting or disconnecting the cable .Please insert for too much stress not to join a connector in the case of insertion of a connector.

b) Be sure to design the cabinet so that the Module can be installed without any extra stress such as warp or twist.

c) Since the front polarizer is easily damaged, pay attention not to scratch it.

d) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.

e) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

f) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface. Handle with care.

g) Since CMOS LSI is used in this Module, take care of static electricity and injure the human earth when handling. Observe all other precautionary requirements in handling components.

h) This Open-cell has its circuitry PCBs on the side and should be handled carefully in order not to be stressed.

i) Laminate film is attached to the Module surface to prevent it from being scratched. Peel the laminate film off slowly just before the use with strict attention to electrostatic charges. Ionized air shall be blown over during the action. Blow off the 'dust' on the polarizer by using an ionized nitrogen gun, etc. Working under the following environments is desirable.

   ■ All workers wear conductive shoes, conductive clothes, conductive fingerstalls and grounding belts without fail.

   ■ Use Ionized blower for electrostatic removal, and peel of the laminate film with a constant speed. (Peeling of it at over 2 seconds)

j) The polarizer surface on the panel is treated with Anti Glare . In case of attaching protective board over the LCD, be careful about the optical interface fringe etc. which degrades display quality.

k) Do not expose the LCD Module to direct sunlight, for a long period of time to protect the Module from the ultra violet ray.

l) When handling LCD Modules and assembling them into cabinets, please be noted that long-term storage in the environment of oxidization or deoxidization gas and the use of such materials as reagent, solvent, adhesive, resin, etc. which generate these gasses, may cause corrosion and discoloration of the Modules.

m) Liquid crystal contained in the panel may leak if the LCD is broken. Rinse it as soon as possible if it gets inside your eye or mouth by mistake.

n) Disassembling the Module can cause permanent damage and should be strictly avoided.(Except for protection film of the panel.)

o) Be careful when using it for long time with fixed pattern display as it may cause afterimage.(Please use a screen saver etc., in order to avoid an afterimage.)

p) If a minute particle enters in the Module and adheres to an optical material, it may cause display non-uniformity issue, etc. Therefore, fine-pitch filters have to be installed to cooling and inhalation hole if you intend to install a fan.

q) Epoxy resin (amine series curing agent), silicone adhesive material (dealcoholization series and oxime series), tray forming agent (azo compound) etc, in the cabinet or the packing materials may induce abnormal display with polarizer film deterioration regardless of contact or noncontact to polarizer film.Be sure to confirm the component of them.

r) Do not use polychloroprene. If you use it, there is some possibility of generating Cl2 gas that influences the reliability of the connection between LCD panel and driver IC.

s) Do not put a laminate film on LCD Module, after peeling of the original one. If you put on it, it may cause discoloration or spots because of the occurrence of air gaps between the polarizer and the film.

t) Ground module bezel to stabilize against EMI and external noise.

Appendix. EDID DATA STRUCTURE:

	Address (Dec)	Address (Hex)	Function	Value (Hex)	Value (Dec)	Value (Binary)
Header	0	00	EDID Header	00	0	00000000
	1	01		FF	255	11111111
	2	02		FF	255	11111111
	3	03		FF	255	11111111
	4	04		FF	255	11111111
	5	05		FF	255	11111111
	6	06		FF	255	11111111
	7	07		00	0	00000000
Vendor & Product Identification	8	08	ID Manufacturer Name	0E	14	00001110
	9	09		77	119	01110111
	10	0A	ID Product Code	51	81	01010001
	11	0B		16	22	00010110

	12	0C	ID Serial Number (32-bit serial number)	00	0	00000000
	13	0D		00	0	00000000
	14	0E		00	0	00000000
	15	0F		00	0	00000000
	16	10	Manufacture week (1-53) & Model year Flag (FFh)	00	0	00000000
	17	11	Manufacture year (year -1990) or Model year	22	34	00100010
EDID Version & Revision	18	12	EDID Structure version	01	1	00000001
	19	13	EDID Revision	04	4	00000100
Basic Display Parameters & Features	20	14	Video Input Definition	A5	165	10100101
	21	15	H screen size (cm) or Aspect Ratio	22	34	00100010
	22	16	V screen size (cm) or Aspect Ratio	16	22	00010110
	23	17	Display gamma (gamma x 100)-100	78	120	01111000
	24	18	Feature support(DPMS)	03	3	00000011
Color Characteristics	25	19	Red/Green Low Bits	C4	196	11000100
	26	1A	Blue/White Low Bits	65	101	01100101
	27	1B	Red x	94	148	10010100
	28	1C	Red y	5C	92	01011100
	29	1D	Green x	5B	91	01011011
	30	1E	Green y	92	146	10010010
	31	1F	Blue x	29	41	00101001
	32	20	Blue y	1D	29	00011101
	33	21	White x	50	80	01010000

	34	22	White y	54	84	01010100
Established Timings	35	23	Established Timing 1	00	0	00000000
	36	24	Established Timing 2	00	0	00000000
	37	25	Manufacturer's Reserved Timings	00	0	00000000
Standard Timings: Identification 1 → 8	38	26	Standard Timing Identification #1	01	1	00000001
	39	27		01	1	00000001
	40	28	Standard Timing Identification #2	01	1	00000001
	41	29		01	1	00000001
	42	2A	Standard Timing Identification #3	01	1	00000001
	43	2B		01	1	00000001
	44	2C	Standard Timing Identification #4	01	1	00000001
	45	2D		01	1	00000001
	46	2E	Standard Timing Identification #5	01	1	00000001
	47	2F		01	1	00000001
	48	30	Standard Timing Identification #6	01	1	00000001
	49	31		01	1	00000001
	50	32	Standard Timing Identification #7	01	1	00000001
	51	33		01	1	00000001
	52	34	Standard Timing Identification #8	01	1	00000001
	53	35		01	1	00000001
Preferred Timing Mode	54	36	Pixel Clock/10,000 (LSB)	60	96	01100000
	55	37	Pixel Clock/10,000 (MSB) /	3F	63	00111111
	56	38	Horizontal Active	80	128	10000000
	57	39	Horizontal Blanking	A0	160	10100000
	58	3A	Horizontal Active : Horizontal Blanking	70	112	01110000
	59	3B	Vertical Active	B0	176	10110000
	60	3C	Vertical Blanking	64	100	01100100
	61	3D	Vertical Active : Vertical Blanking	40	64	01000000
	62	3E	Horizontal Sync. Offset	30	48	00110000

	63	3F	Horizontal Sync Pulse Width	20	32	00100000
	64	40	Vertical Sync Offset : Sync Width	26	38	00100110
	65	41	Horizontal Vertical Sync Offset/Width	0C	12	00001100
	66	42	Horizontal Image Size	58	88	01011000
	67	43	Vertical Image Size	D7	215	11010111
	68	44	Horizontal & Vertical Image Size	10	16	00010000
	69	45	Horizontal Border	00	0	00000000
	70	46	Vertical Border	00	0	00000000
	71	47	Signal Interface Type	18	24	00011000
Detailed Timing # 2	72	48	Reserved for definition	00	0	00000000
	73	49	Reserved for definition	00	0	00000000
	74	4A	Reserved for definition	00	0	00000000
	75	4B	ASCII String	FD	253	11111101
	76	4C	Vertical Rate Offsets	00	0	00000000
	77	4D	Minimum Vertical Rate	30	48	00110000
	78	4E	Maximum Vertical Rate:	90	144	10010000
	79	4F	Minimum Horizontal Rate:	BB	187	10111011
	80	50	Maximum Horizontal Rate	BB	187	10111011
	81	51	Maximum Pixel Clock,Binary coded clock rate in MHz ÷ 10,	27	39	00100111
	82	52	Video Timing Support Flags.01h,Range Limits Only	01	1	00000001
	83	53	Line Feed (if Byte 10 = 00h or 01h)	0A	10	00001010
	84	54	Space (if Byte 10 = 00h or	20	32	00100000

			01h)				
	85	55	Space (if Byte 10 = 00h or 01h)	20	32		00100000
	86	56	Space (if Byte 10 = 00h or 01h)	20	32		00100000
	87	57	Space (if Byte 10 = 00h or 01h)	20	32		00100000
	88	58	Space (if Byte 10 = 00h or 01h)	20	32		00100000
	89	59	Space (if Byte 10 = 00h or 01h)	20	32		00100000
Display Descriptor # 3	90	5A	Indicates descriptor #3 is a display Descriptor	00	0		00000000
	91	5B		00	0		00000000
	92	5C	Reserved	00	0		00000000
	93	5D	Tag: ASCII String	FE	254		11111110
	94	5E	Reserved	00	0		00000000
	95	5F	Manufacture name	3D	61		00111101
	96	60		4C	76		01001100
	97	61		32	50		00110010
	98	62		33	51		00110011
	99	63		31	49		00110001
	100	64		31	49		00110001
	101	65		20	32		00100000
	102	66		20	32		00100000
	103	67		20	32		00100000
	104	68		20	32		00100000
	105	69		20	32		00100000
	106	6A		20	32		00100000

	107	6B		FF	255	11111111
Display Descriptor # 4	108	6C	Flag	00	0	00000000
	109	6D	Flag	00	0	00000000
	110	6E	Flag	00	0	00000000
	111	6F	Data Type Tag	FC	252	11111100
	112	70	Flag	00	0	00000000
	113	71	Model Name	4D	77	01001101
	114	72	Model Name	4E	78	01001110
	115	73	Model Name	47	71	01000111
	116	74	Model Name	30	48	00110000
	117	75	Model Name	30	48	00110000
	118	76	Model Name	37	55	00110111
	119	77	Model Name	51	81	01010001
	120	78	Model Name	58	88	01011000
	121	79	Model Name	32	50	00110010
	122	7A	Model Name	2D	45	00101101
	123	7B	Model Name	31	49	00110001
	124	7C	Model Name	0A	10	00001010
	125	7D	Model Name	20	32	00100000
Extension Block Count N	126	7E	Extension flag	01	1	00000001
Checksum	127	7F	Checksum	34	52	00110100
DID 2.0	128	80	EDID Extension Tags	70	112	01110000
	129	81	Display ID version	20	32	00100000
	130	82	section size	79	121	01111001
	131	83	product Type identifier	02	2	00000010
	132	84	extension count	00	0	00000000
Display Parameters	133	85	block tag	21	33	00100001
	134	86	block revision and other data	00	0	00000000

Data Block	135	87	payload	1D	29		00011101
	136	88	Horizontal Image Size	77	119		01110111
	137	89		0D	13		00001101
	138	8A	Vertical Image Size	6A	106		01101010
	139	8B		08	8		00001000
	140	8C	Horizontal Pixel Count	80	128		10000000
	141	8D		07	7		00000111
	142	8E	Vertical Pixel Count	B0	176		10110000
	143	8F		04	4		00000100
	144	90	Feature Support Flags	00	0		00000000
	145	91	Native Color Chromaticity (Red Chromaticity)	4C	76		01001100
	146	92		E9	233		11101001
	147	93		5B	91		01011011
	148	94	Native Color Chromaticity (Green Chromaticity)	9E	158		10011110
	149	95		05	5		00000101
	150	96		95	149		10010101
	151	97	Native Color Chromaticity (Blue Chromaticity)	9C	156		10011100
	152	98		F2	242		11110010
	153	99		1D	29		00011101
	154	9A	Native Color Chromaticity (White Chromaticity)	02	2		00000010
	155	9B		45	69		01000101
	156	9C		54	84		01010100
	157	9D	Native Maximum Luminance (Full Coverage)	B0	176		10110000
	158	9E		5C	92		01011100
	159	9F	Native Maximum Luminance (10% Coverage)	B0	176		10110000
	160	A0		5C	92		01011100

	161	A1	Native Minimum Luminance	00	0	00000000
	162	A2		42	66	01000010
	163	A3	Native Color Depth and Display Device Technology	12	18	00010010
	164	A4	Native Gamma EOTF	78	120	01111000
DID Block #1 Header	165	A5	block tag	22	34	00100010
	166	A6	block rev	00	0	00000000
	167	A7	Payload	14	20	00010100
First Timing	168	A8	Pixel Clock	04	4	00000100
	169	A9		F1	241	11110001
	170	AA		05	5	00000101
	171	AB	timing options	85	133	10000101
	172	AC	H-Active	7F	127	01111111
	14	AD		07	7	00000111
	174	AE	H-Blanking	9F	159	10011111
	175	AF		00	0	00000000
	176	B0	H-offset	2F	47	00101111
	177	B1		00	0	00000000
	178	B2	H-sync pulse width	1F	31	00011111
	179	B3		00	0	00000000
	180	B4	V-Active	AF	175	10101111
	181	B5		04	4	00000100
	182	B6	V-Blanking	63	99	01100011
	183	B7		00	0	00000000
	184	B8	V-offset	31	49	00110001
	185	B9		00	0	00000000
	186	BA	V-sync pulse width	05	5	00000101
	187	BB		00	0	00000000
adaptive sync data block 48-144HZ	188	BC	Adaptive-Sync Data Block	2B	43	00101011
	189	BD	Block revision = 0	00	0	00000000
	190	BE	Number of Payload Bytes in	0C	12	00001100

			block= 12 byte			
	191	BF	FAVT and AVT Supported,Native panel range,successive frame duration Decrease met with in RR Range.	27	39	00100111
	192	C0	00h = Flicker performance is met in any duration increase within the refresh rate range without jitter impact.	00	0	00000000
	193	C1	Minimum Refresh Rate(48/1.001)Hz	30	48	00110000
	194	C2	Maximum Refresh Rate(144x1.00035)Hz	8F	143	10001111
	195	C3		00	0	00000000
	196	C4	00h = Flicker performance is met in any duration decrease within the refresh rate range	00	0	00000000
adaptive sync data block 48-60HZ	197	C5	FAVT and AVT Supported,Native panel range,successive frame duration Decrease met with in RR Range.	27	39	00100111
	198	C6	00h = Flicker performance is met in any duration increase within the refresh rate range without jitter impact.	00	0	00000000
	199	C7	Minimum Refresh Rate(48/1.001)Hz	30	48	00110000
	200	C8	Maximum Refresh Rate(60x1.00035)Hz	3B	59	00111011
	201	C9		00	0	00000000
	202	CA	00h = Flicker performance is met in any duration decrease within the refresh rate range	00	0	00000000

Brightness Luminance Range	203	CB	DID2.0 Data block tag[2Eh]	2E	46	00101110
	204	CC	Block revision	00	0	00000000
	205	CD	Number of Payload Bytes in block=	06	6	00000110
	206	CE	Min SDR Luminance (Full Coverage)	00	0	00000000
	207	CF		42	66	01000010
	208	D0	Max Suggested SDR Luminance (Full Coverage)	B0	176	10110000
	209	D1		5C	92	01011100
	210	D2	Max Boost SDR Luminance	B0	176	10110000
	211	D3		5C	92	01011100
CTA AMD VSDB3 (Freesync range：RR-48)	212	D4	DID2.0 Data block tag[81h] = CTA DisplayID	81	129	10000001
	213	D5	Block revision	00	0	00000000
	214	D6	Number of Payload Bytes in block=	1E	30	00011110
	215	D7	CTA Block1 Tag Code and Block1 Length = Vendor Specific Data Block(03h) +Length of following data block (in bytes)	72	114	01110010
	216	D8	AMD IEEE OUI value (0x00001A)	1A	26	00011010
	217	D9	(Hex. LSB first)	00	0	00000000
	218	DA	(Hex. LSB first)	00	0	00000000
	219	DB	AMD VSDB Version 3	03	3	00000011
	220	DC	Freesync Capability : Seamless Local Dimming Disable Control Not Supported , Seamless Native Color Space & Transfer Switching Curve Not Supported , Seamless Variable Frame Rate	01	1	00000001

		Switching Supported			
221	DD	Min Refresh Rate =	30	48	00110000
222	DE	Max Refresh Rate =	90	144	10010000
223	DF	Freesync MCCS VCP Code	00	0	00000000
224	E0	Support WCG and HDR features : Seamless Gamma 2.2 EOTF Not Supported , Seamless PQ EOTF Not Supported	00	0	00000000
225	E1	Max Luminance 1 (Peak luminance - Maximum luminance (10% white patch))	53	83	01010011
226	E2	Min Luminance 1 (Minimum luminance with 100% full black pattern)	FF	255	11111111
227	E3	Max Luminance 2 (Average luminance (100% full white pattern)	53	83	01010011
228	E4	Min Luminance (Minimum luminance with corner white pattern (2.5% per corner))	FF	255	11111111
229	E5	Freesync Maximum Refresh Rate (LSB) : (Range : 0Hz (000h) ~ 1023Hz (3FFh), for VSDB v3)	90	144	10010000
230	E6	Freesync Maximum Refresh Rate (MSB)	00	0	00000000
231	E7	Maximum Fast Transport Input Pixel Rate [kHz] - bits 7:0	00	0	00000000
232	E8	Maximum Fast Transport Input Pixel Rate [kHz] - bits 15:8	00	0	00000000
233	E9	Maximum Fast Transport Input Pixel Rate [kHz] - bits	00	0	00000000

			23:16			
CTA Colorimetry	234	EA	Tag Code [7:5], Length of data [4:0]	E3	227	11100011
	235	EB	Extended Tag Code	05	5	00000101
	236	EC	Colorimetry Support Flags	04	4	00000100
	237	ED	Colorimetry Metadata Support Flags	00	0	00000000
CTA HDR static metadata	238	EE	Tag Code [7:5], Length of data [4:0]	E6	230	11100110
	239	EF	Extended Tag Code	06	6	00000110
	240	F0	Supported Electro-Optical Transfer Function	01	1	00000001
	241	F1	SM_0 =1: Static Metadata Type 1	01	1	00000001
	242	F2	Desired Content Max Luminance data	53	83	01010011
	243	F3	Desired Content Max Frame-average Luminance data	53	83	01010011
	244	F4	Desired Content Min Luminance data	FF	255	11111111
	245	F5		00	0	00000000
	246	F6		00	0	00000000
	247	F7		00	0	00000000
	248	F8		00	0	00000000
	249	F9		00	0	00000000
	250	FA		00	0	00000000
	251	FB		00	0	00000000
	252	FC		00	0	00000000
	253	FD		00	0	00000000
	254	FE		B1	177	10110001
	255	FF	Checksum	90	144	10010000

Appendix. Checksum of DDS, EDID and FW :TBD（update after code release）

Checksum	
DDS	8FB8
Base EDID(0x7F)	0x34
Extension EDID (0xFE)	0xB1
FW	1DDC

Appendix. OUTLINE DRAWING
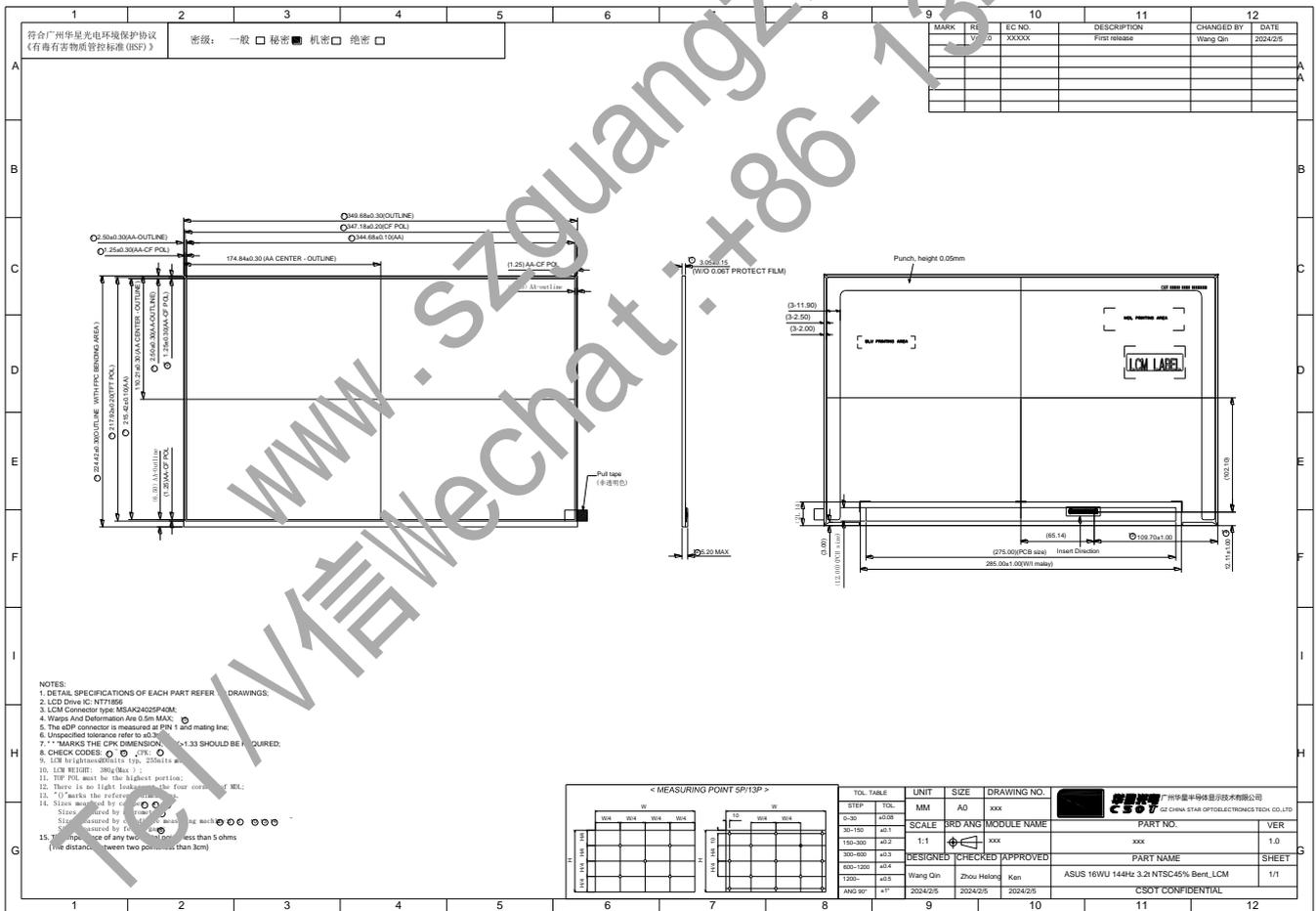
Appendix. EDP Link rate capability and setting

Table 1：

eDP link rate NT71856 TCON link rate capability			
	DSC	Without DSC	Unit
10bpc (HDR/SDR)	Not allowed	5.4G	Gbps/Lane
8bpc (SDR)	Not allowed	5.4G	Gbps/Lane

Table 2：

eDP link rate Actual link rate			
	DSC	Without DSC	Unit
10bpc (HDR/SDR)	N/A	4.32G(N/A)	Gbps/Lane
8bpc (SDR)	N/A	3.24G	Gbps/Lane

Table 3:

Link training condition		
eDP link training **Default link training form**	S0P0	Ex：S0P0
TCON — SOURCE **SSC percentage**	0.5%	Ex：0.5%