

TITLE : NE160QDM-NZB V8.0

Customer: LBG

Product Specification

Rev. 0

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BOE Optoelectronics Technology Co., Ltd

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REVISION HISTORY

()Preliminary Specification
(√)Final Specification

Revision No.	Page	Description of Changes	Date	Prepared
P0	-	Preliminary Release	2023.08.30	Liu Jie
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1.0 GENERAL DESCRIPTION

1.1 Introduction

NE160QDM-NZB V8.0 is a color active matrix TFT LCD module using Oxide TFT's (Thin Film Transistors) as an active switching devices. This module has a 16.0 inch diagonally measured active area with WQXGA resolutions (2560 horizontal by 1600 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 1064.3M(8bit+2FRC) colors and color gamut DCI-P3 100%typ, 96%min . The TFT-LCD panel used for this module is a low reflection and higher color type. Therefore, this module is suitable for Notebook PC. The LED driver for back-light driving is built in this model. All input signals are eDP1.4b interface compatible.

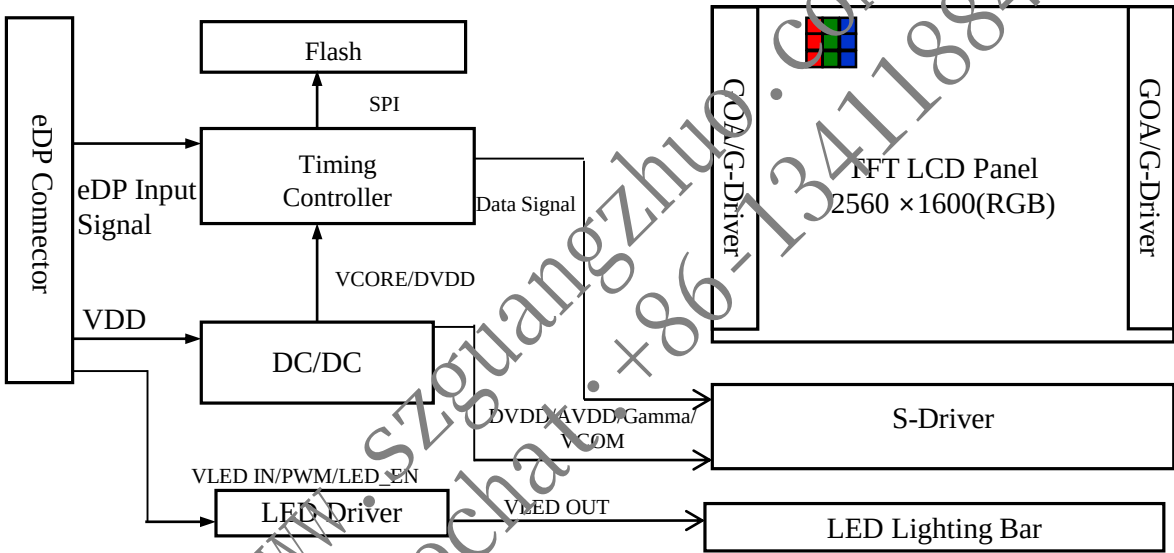


Figure 1. Drive Architecture

1.2 Features

- 4 lane eDP interface with 8.1Gbps link rates
- Thin and light weight, Low Blue Light
- 1064.3M(8bit+2FRC) color depth, color gamut DCI-P3 100%typ, 96%min
- Single LED lighting bar (Bottom side/Horizontal Direction)
- Data enable signal mode
- Green product (RoHS & Halogen free product)
- On board LED driving circuit
- On board EDID chip
- DPCD Version 1.4
- Adjust backlight brightness with DC mode

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1.0 GENERAL DESCRIPTION

1.2 Features

DPCD Ver.	sDRRS	BIST	FRC	PSR	LRR	MBO
1.4	on	on	on	off	off	off
VESA DSC	MSO	AMD Free-sync	HDR	Dimming	OD	DDS
on	off	Freesync premium	HDR400	PWM in DC out	default off, enable by Pin40 pull high	on
G-sync	Esport					
on	on					

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1.3 Application

- Notebook PC (Wide type)

1.4 General Specification

The followings are general specifications at the model NE160QDM-NZB V8.0. (listed in Table 1)

<Table 1. General Specifications>

Parameter	Specification	Unit	Remarks
Active area	344.6784(H) ×215.424(V)	mm	
Number of pixels	2560 (H) ×1600 (V)	pixels	
Pixel pitch	134.64(H) ×134.64(V)	um	
Pixel arrangement	RGB Vertical stripe		
Display colors	1064.3M(8bit+2FRC)		
Color gamut	DCI-P3 100%typ, 96%min		CIE1976
Display mode	Normally Black		
Dimensional outline	349.68±0.3 (H)*224.42±0.3(V)(W/O FPC bending)*2.6 (Max) 349.68±0.3 (H)*224.92(Max) (V)(W/FPC bending)*4.6(Max)	mm	
Weight	325g(max)	g	
Surface treatment	Anti-Glare		
Surface hardness	3H		
Back-light	Bottom edge side, 1-LED lighting bar type		Note 1
Power consumption	P _D : 2.3(Max.)@240Hz W/O OD	W	@Mosaic
	P _{BL} : 5.8(Max.)	W	@VLED =12V
	P _{Total} : 8.1(Max.)	W	@Mosaic

Notes : 1. LED Lighting Bar (88*LED Array)

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2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Absolute Maximum Ratings>

Ta=25+/-2°C

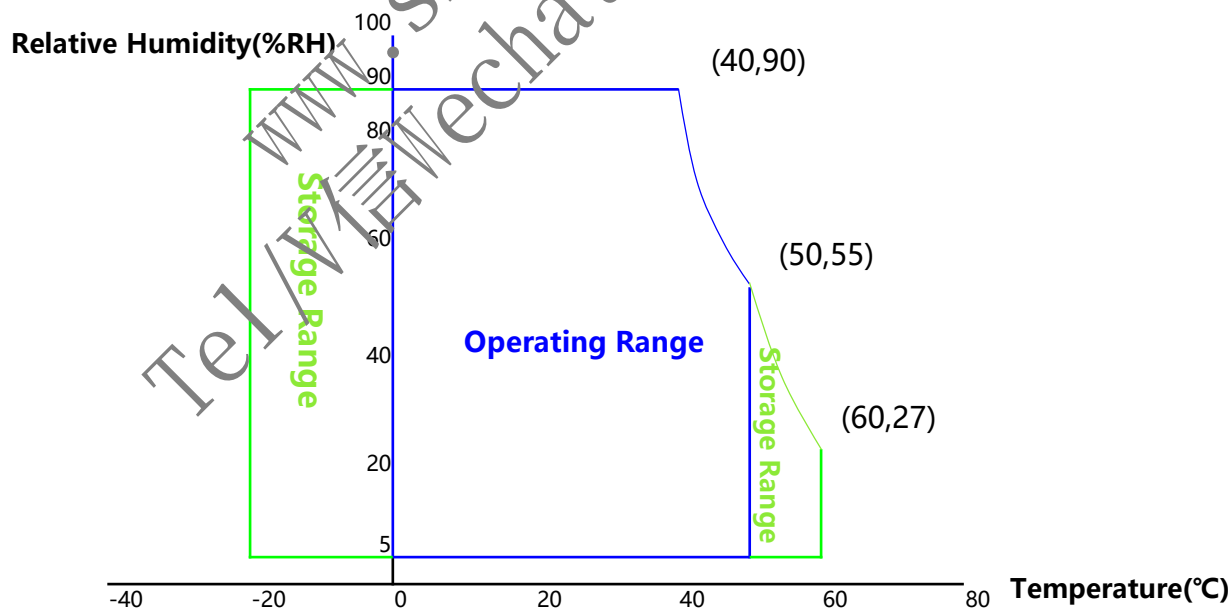
Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V _{DD}	-0.3	4.0	V	Note 1
eDP input Voltage	V _{eDP}	0	2.0	V	
Logic Supply Voltage	V _{IN}	V _{SS} -0.3	V _{DD} +0.3	V	
Operating Temperature	T _{OP}	0	+50	°C	Note 2
Storage Temperature	T _{ST}	-20	+60	°C	

Notes :

1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.

2. Temperature and relative humidity range are shown in the figure below.

90 % RH Max. (40 °C ≥ Ta) Maximum wet- bulb temperature at 39 °C or less. (Ta > 40 °C) No condensation.



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3.0 ELECTRICAL SPECIFICATIONS						
3.1 Electrical Specifications						
< Table 3. Electrical Specifications >					Ta=25+/-2°C	
Parameter		Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V _{DD}	3.0	3.3	3.6	V	Note 1
Permissible Input Ripple Voltage	V _{RF}	-10% VDD	-	+10% VDD	V	@ V _{DD} = 3.3V , note4
BIST Control Level	High Level	0.8 VDDIO	-	3.3	V	@V _{DDIO} =1.8
	Low Level	0	-	0.15 VDDIO	V	
OD Control Level	High Level	1.62	-	1.98	V	@V _{DDIO} =1.8 Note5
	Low Level	0	-	0.6	V	
Power Supply Inrush Current		Inrush	-	2	A	Note3
Power Supply Current	Mosaic	I _{DD}	-	697	mA	Note 1 @240Hz w/o OD
	RGB		-	697	mA	
	Heavy Pattern		-	1.82	A	@240Hz w OD
Power Consumption	Mosaic	P _M	-	2.3	W	@240Hz w/o OD
	RGB	P _{RGB}	-	2.3	W	
	Heavy Pattern	P _{CC}	-	6	W	@240Hz w OD
	BLU	P _{BL}	-	5.8	W	Note 2
	Total	P _{Total}	-	8.1	W	@240Hz Mosaic w/o OD
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3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

Notes :

1. The supply voltage is measured and specified at the interface connector of LCM.

The current draw and power consumption specified is for 3.3V at 25 °C.

- a) Mosaic pattern 8*8
 - b) R/G/B patterns
 - c) Heavy pattern(maximum logic power consumption) : H 1line
- The pattern and Power Consumption is shown for reference only

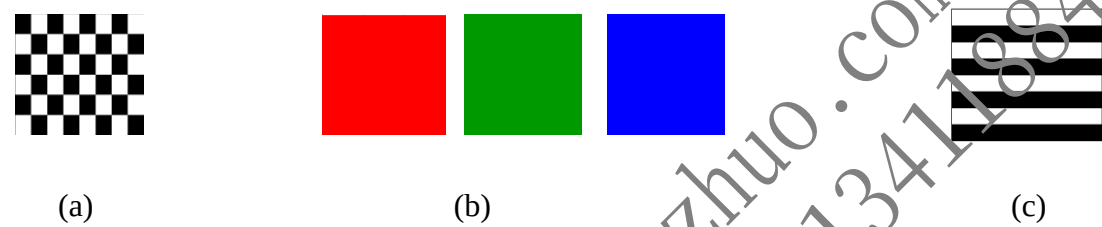


Figure 3. Power Measure Patterns

2. Calculated value for reference ($V_{LED} \times I_{LED}$) , The power consumption with LED Driver are under the $V_{LED} = 12.0V$, 25°C, PWM Duty 100%

3. Measure condition (Figure 4)

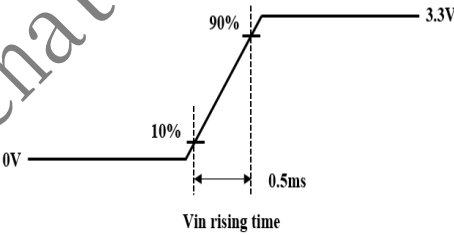
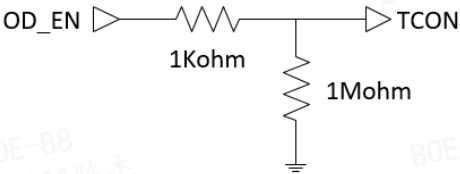


Figure 4. Inrush Measure Condition

4. Input voltage range:3.0~3.6V.Test condition: Oscilloscope bandwidth 20MHz, AC coupling

5.



OD EN#	Over Driver
Hight	Enable
Floating	Disable
Low	Disable

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3.2 Backlight Unit

< Table 4. LED Driving Guideline Specifications > Ta=25+/-2℃

Parameter		Min.	Typ.	Max.	Unit	Remarks	
LED Forward Voltage		V _F	-	-	2.9	V	
LED Forward Current		I _F	-	18.6	-	mA	
LED Power Input Voltage		V _{LED}	5	12	21	V	
LED Power Input Current		I _{LED}	-	-	483.3	mA	Note 1
LED Power Consumption		P _{LED}	-	-	5.8	W	
Power Supply Voltage for LED Driver Inrush		I _{led} inrush	-	-	2	A	Note 3
LED Life-Time		N/A	15,000	-	-	Hour	I _F = 18.6 mA Note 2
EN Control Level	Backlight On	V _{BL_EN}	2.5	-	5.0	V	
	Backlight Off		0	-	0.5	V	
PWM Control Level	High Level	V _{BL_PWM}	2.5	-	5.0	V	
	Low Level		0	-	0.5	V	
PWM Control Frequency		F _{PWM}	200	-	2,000	Hz	
Duty Ratio			1	-	100	%	

Notes :

1. Power supply voltage12V for LED driver.
Calculator value for reference $I_F \times V_F \times 88/\text{driver efficiency} = P_{LED}$
2. The LED life-time define as the estimated time to 50% degradation of initial luminous.
3. Measure condition (Figure 5)

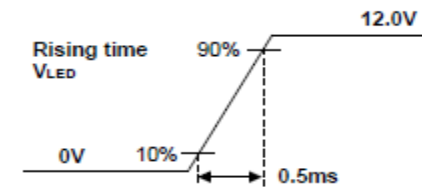


Figure 5. Inrush Measure Condition

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3.3 LED Structure

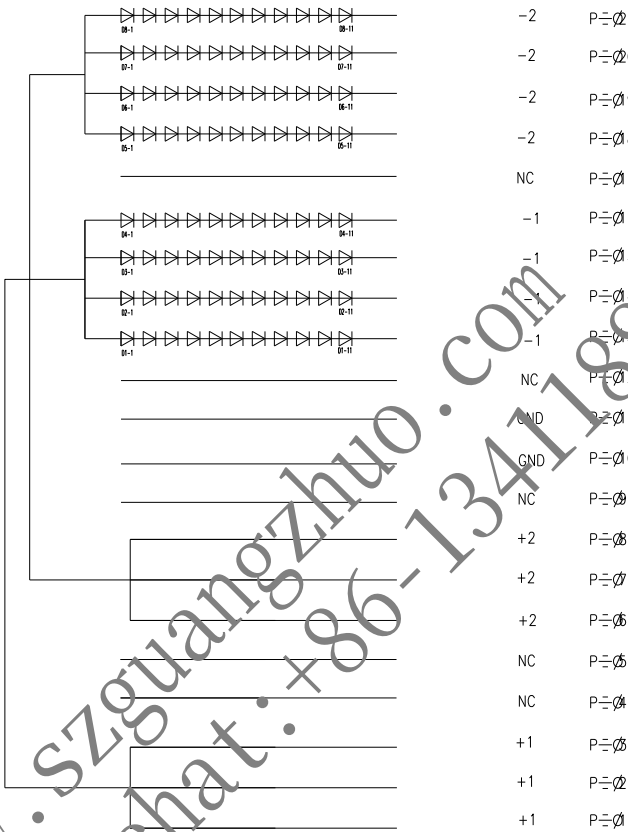


Figure 6. LED Structure

4.0 OPTICAL SPECIFICATION

4.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = $25\pm 2^{\circ}\text{C}$) with the equipment of luminance meter system (PR730&PR810) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0° . We refer to $\theta\theta=0$ ($=\theta 3$) as the 3 o'clock direction (the "right"), $\theta\theta=90$ ($=\theta 12$) as the 12 o'clock direction ("upward"), $\theta\theta=180$ ($=\theta 9$) as the 9 o'clock direction ("left") and $\theta\theta=270$ ($=\theta 6$) as the 6 o'clock direction ("bottom"). While scanning θ and/or Φ , the center of the measuring spot on the display surface shall stay fixed. The backlight should be operating for 30 minutes prior to measurement. VDD shall be $3.3\pm 0.3\text{V}$ at 25°C . Optimum viewing angle direction is 6 o'clock.

4.2 Optical Specifications

<Table 5. Optical Specifications>

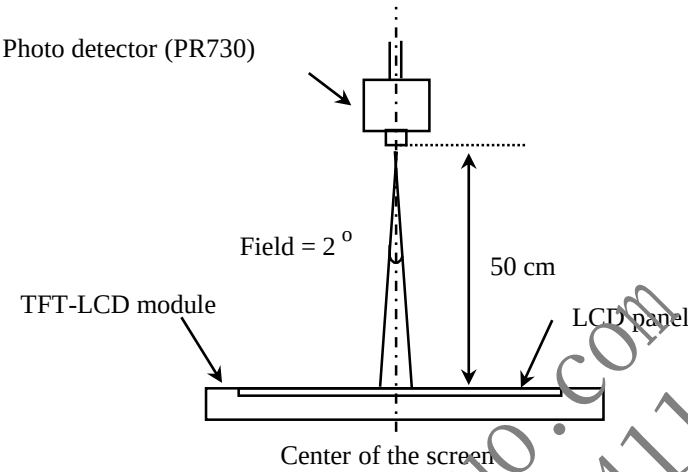
Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ_3	CR > 10	85	89	-	Deg.	Note 1
		Θ_9		85	89	-	Deg.	
	Vertical	Θ_{12}		85	89	-	Deg.	
		Θ_6		85	89	-	Deg.	
Luminance Contrast Ratio		CR	$\Theta = 0^{\circ}$	1000	1200	-		Note 2
Luminance of White	5 Points	Y_w	$\Theta = 0^{\circ}$ ILED = 18.6 mA	425	500	575	cd/m ²	Note 3
White Luminance Uniformity	5 Points	ΔY_5		80	-	-	%	Note 4
	13 Points	ΔY_{13}		66.7	-	-	%	
White Chromaticity		W_x	$\Theta = 0^{\circ}$	0.288	0.313	0.338		Note 5
		W_y		0.304	0.329	0.354		
Reproduction of Color	Red	R_x	$\Theta = 0^{\circ}$	Typ. -0.025	0.682	Typ. +0.025		
		R_y			0.314			
	Green	G_x			0.265			
		G_y			0.692			
	Blue	B_x			0.145			
		B_y			0.058			
CT		-	-	6000		7500		
Color Gamut			DCI-P3	96	100	-	%	CIE 1976
Response Time (Rising + Falling)		T_{RT}	Ta= 25°C $\Theta = 0^{\circ}$	-	9	12	ms	Note 6
GTG		With OD	Ta= 25°C	-	3	4	ms	-
		W/O OD	$\Theta = 0^{\circ}$	-	5	6	ms	-
Cross Talk		CT	$\Theta = 0^{\circ}$	-	-	2.0	%	Note 7
Gamma		-	-	2.0	2.2	2.4	-	

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Notes : 1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 7). 2. Contrast measurements shall be made at viewing angle of $\Theta = 0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see Figure 7) Luminance Contrast Ratio (CR) is defined mathematically. CR = Luminance when displaying a white raster Luminance when displaying a black raster 3. Center Luminance of white is defined as luminance values of 5 point average across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 8 for a total of the measurements per display. 4. The White luminance uniformity on LCD surface is then expressed as : $\Delta Y = \text{Minimum Luminance of 5(or 13) points} / \text{Maximum Luminance of 5(or 13) points.}$(see Figure 8 and Figure 9). 5. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel. 6. The electro-optical response time measurements shall be made as Figure 10 by switching the “data” input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Tf. 7. Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark. (See Figure 11).			
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8. Response time 9*9 matrix

start\end	0	16	32	48	64	80	96	112	128	144	160	176	192	208	224	240	255
0				2.8	2.7	2.7	2.6	2.6	2.6	2.4	2.6	2.3	2.4	2.2	2.2	2.7	3.3
16			3.9	2.7	2.7	2.3	2.7	2.6	2.6	2.6	2.3	2.3	2.2	2.2	2.1	2.7	3.2
32		2.6		2.8	2.6	2.4	2.6	2.3	2.4	2.6	2.3	2.4	2.2	2.2	2.1	2.4	3.2
48	5.2	2.4	2.2		2.8	2.7	2.4	2.4	2.6	2.4	2.4	2.2	2.3	2.1	2.2	2.6	3.2
64	5.5	3.4	2.3	2.7		2.6	2.6	2.3	2.4	2.3	2.4	2.2	2.2	2.1	2.1	2.6	3.3
80	6.1	4.4	3.1	2.3	2.4		2.8	2.3	2.6	2.6	2.2	2.4	2.2	2.2	1.8	2.4	3.2
96	6.1	5.4	2.9	2.6	2.4	2.6		3.2	2.4	2.3	2.4	2.3	2.3	2.2	1.8	2.4	3.3
112	6.7	5.9	3.4	2.6	2.6	2.7	2.6		2.8	2.6	2.6	2.2	2.2	2.2	2.2	2.4	3.3
128	6.7	6.3	4.3	2.8	2.4	2.4	2.3	2.4		3.1	2.6	2.6	2.4	2.3	2.1	2.3	3.5
144	6.7	6.1	5	3.2	2.6	2.4	2.4	2.4	2.8		2.9	2.3	2.3	2.1	2.2	2.2	3.4
160	6.7	6.7	5.2	3.4	2.6	2.4	2.4	2.4	2.6	2.9		2.8	2.7	2.3	2.2	2.2	3.5
176	7	6.7	5.9	3.8	3.1	2.7	2.6	2.7	2.4	2.6	2.8		2.8	2.2	2.2	2.1	3.7
192	7	6.8	6.3	4.5	3.3	2.6	2.4	2.6	2.6	2.4	2.6	2.6		2.6	2.3	2.2	3.8
208	7.3	7.1	6.7	5.5	3.7	2.9	2.7	2.6	2.6	2.7	2.4	2.8	2.7		2.7	2.3	4
224	7.2	7.3	7.1	5.9	4.2	3.3	2.8	2.7	2.4	2.4	2.7	2.4	2.8	3.2		2.7	4.3
240	7.6	7.4	7.3	6.6	5.4	3.5	3.1	2.6	2.7	2.7	2.6	2.4	2.6	2.6	2.6		4.8
255	7.3	7.8	7.7	7.2	6.5	5.1	3.3	2.8	2.4	2.8	2.6	2.6	2.6	2.7	2.6	2.9	

4.3 Optical Measurements



Optical characteristics measurement setup

Figure 7. Measurement Set Up

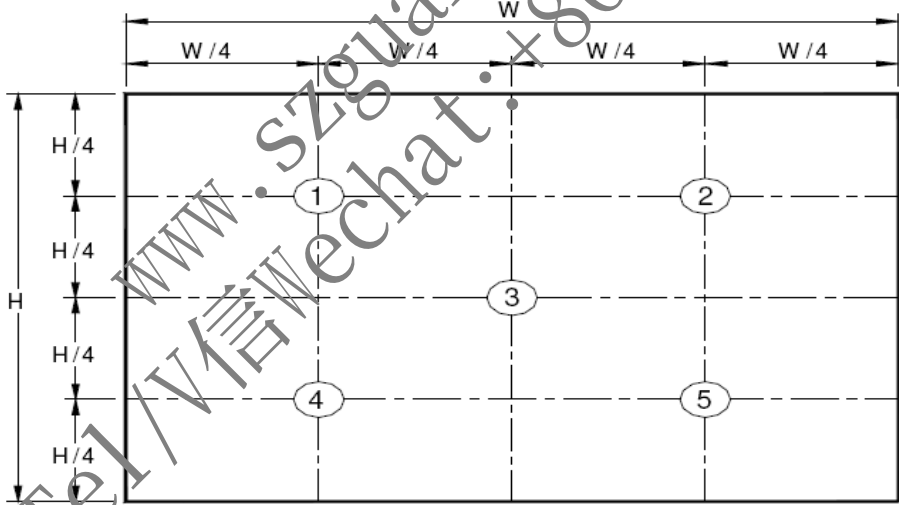


Figure 8. White Luminance and Uniformity Measurement Locations (5 points)

Center Luminance of white is defined as luminance values of center 5 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 7 for a total of the measurements per display.

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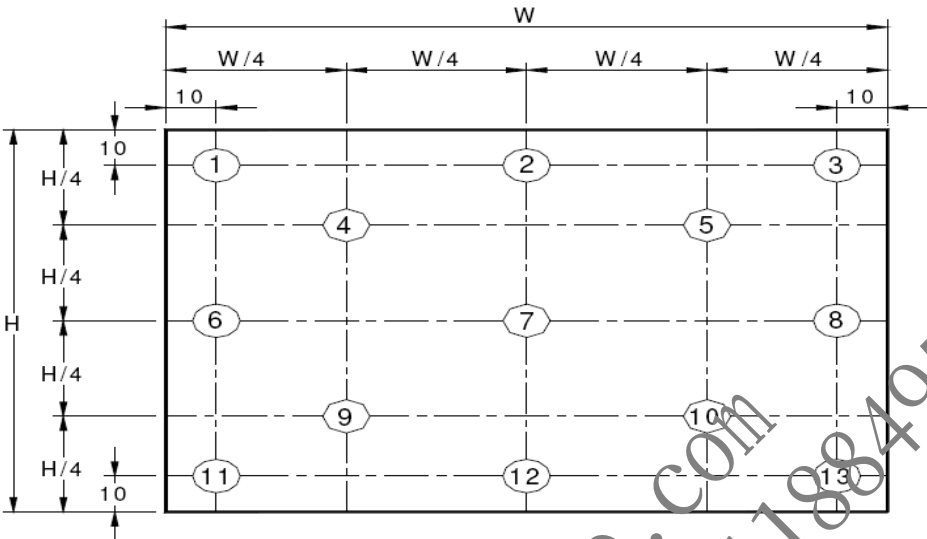


Figure 9. Uniformity Measurement Locations (13 points)

The White luminance uniformity on LCD surface is then expressed as : $\Delta Y5$ = Minimum Luminance of five points / Maximum Luminance of five points (see Figure 8) , $\Delta Y13$ = Minimum Luminance of 13 points /Maximum Luminance of 13 points (see Figure 9).

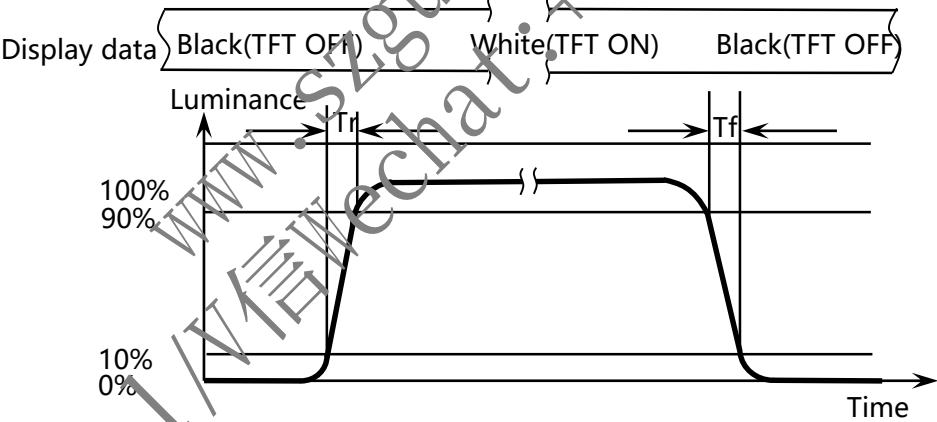
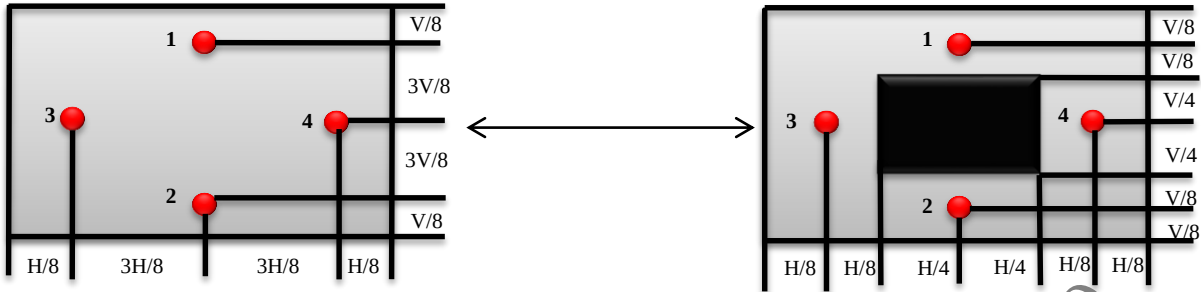


Figure 10. Response Time Testing

The electro-optical response time measurements shall be made as shown in Figure 10 by switching the “data” input signal ON and OFF. Tr: The luminance to change from 10% to 90% ,Tf: The luminance to change from 90% to 10% .

The test system : LMS PR810

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$$\text{Cross Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_A} \right| \times 100$$

Figure 11. Cross Talk Modulation Test Description

Where:

- Y_A = Initial luminance of measured area (cd/m²)
- Y_B = Subsequent luminance of measured area (cd/m²)

The location 1/2/3/4 measured will be exactly the same in both patterns. The test background gray is from L64 to L192.Take the largest data as the result.

Cross Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark.(Refer to Figure 11)

The test system: PR730

5.0 INTERFACE CONNECTION

5.1 Electrical Interface Connection

The electronics interface connector is STM MSAK24025P40G.

The connector interface pin assignments are listed in Table 6.

<Table 6. Pin Assignments for the Interface Connector>

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	I2C_SCL	DDS function	21	LCD_VCC	LCD logic and driver power
2	H_GND	High Speed Ground	22	BIST	BIST function
3	Lane3_N	Comp Signal Link Lane 3	23	LCD_GND	LCD logic and driver ground
4	Lane3_P	True Signal Link Lane 3	24	LCD_GND	LCD logic and driver ground
5	H_GND	High Speed Ground	25	LCD_GND	LCD logic and driver ground
6	Lane2_N	Comp Signal Link Lane 2	26	LCD_GND	LCD logic and driver ground
7	Lane2_P	True Signal Link Lane 2	27	HPD	HPD signal pin
8	H_GND	High Speed Ground	28	BL_GND	Backlight_ground
9	Lane1_N	Comp Signal Link Lane 1	29	BL_GND	Backlight_ground
10	Lane1_P	True Signal Link Lane 1	30	BL_GND	Backlight_ground
11	H_GND	High Speed Ground	31	BL_GND	Backlight_ground
12	Lane0_N	Comp Signal Link Lane 0	32	BL_Enable	Backlight On / Off
13	Lane0_P	True Signal Link Lane 0	33	BL_PWM_DIM	System PWM signal Input
14	H_GND	High Speed Ground	34	I2C_SDA	DDS function
15	AUX_CH_P	True Signal Auxiliary Ch.	35	NC	Need system NC
16	AUX_CH_N	Comp Signal Auxiliary Ch.	36	BL_PWR	Backlight power
17	H_GND	High Speed Ground	37	BL_PWR	Backlight power
18	LCD_VCC	LCD logic and driver power	38	BL_PWR	Backlight power
19	LCD_VCC	LCD logic and driver power	39	BL_PWR	Backlight power
20	LCD_VCC	LCD logic and driver power	40	OD_Enable	OD function default off which can be enable by pull high

Note: I2C using information 1.Tcon I2C(DDS) address: 11000010 2.PMIC Address: 01000110
3.LED driver: 01101100/01101110 ;

5.2 eDP Interface

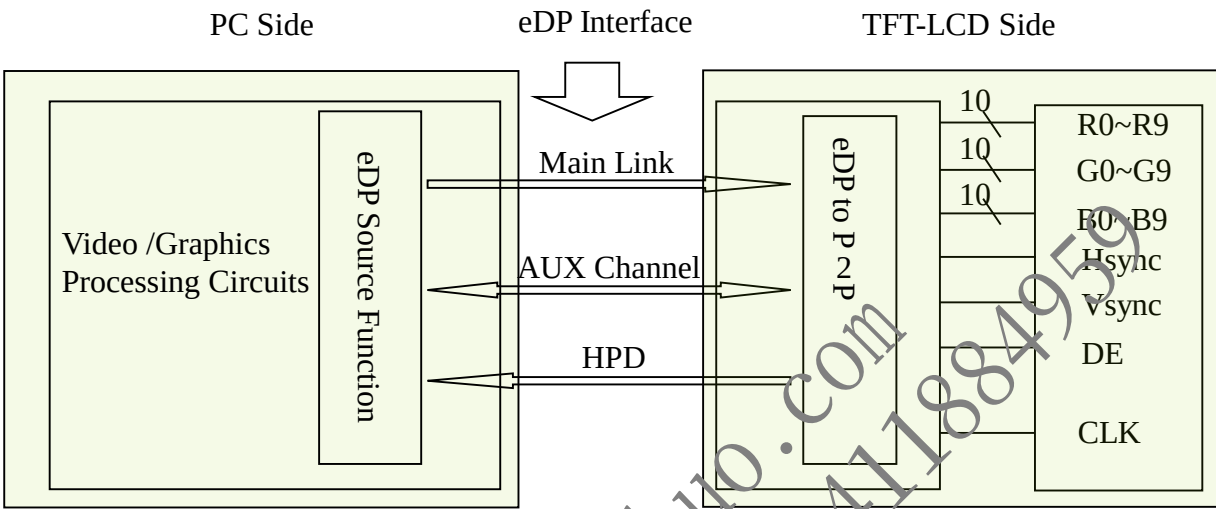


Figure 12. eDP Interface Architecture

Note:
Transmitter : Parade DP501 or equivalent.
Transmitter is not contained in module.

5.3 Data Input Format

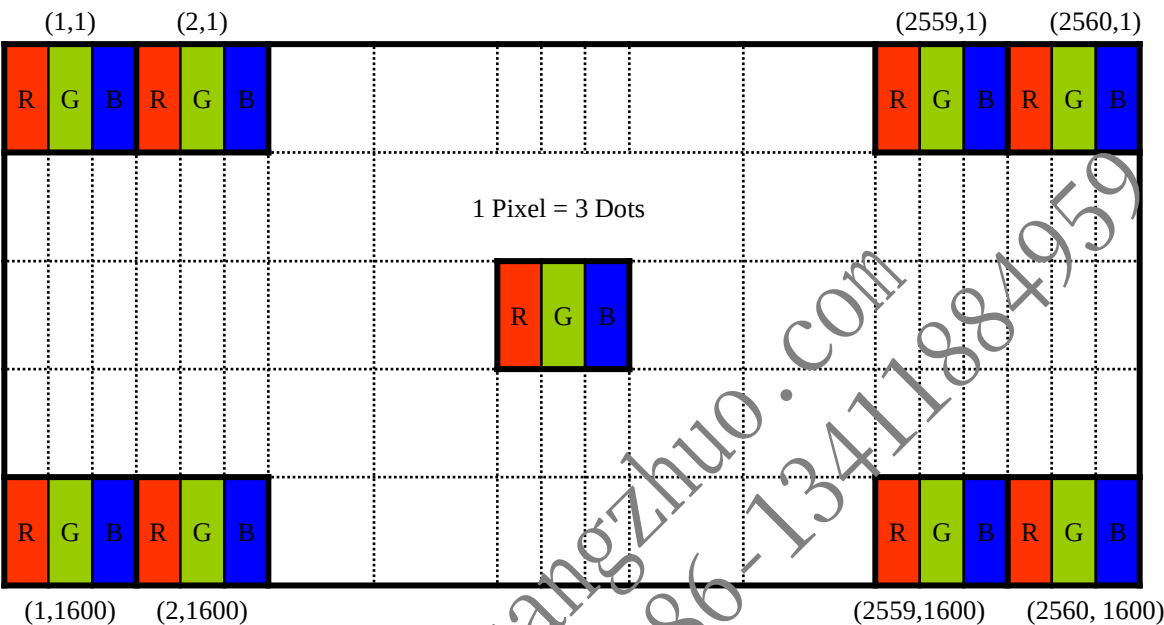


Figure 13. Display Position of Input Data (V-H)

5.4 Back-light & LCM Interface Connection

BLU Interface Connector: I-PEX 20979-021E-01.

<Table 7. Pin Assignments for the BLU Connector>

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vout	LED anode connection	12	NC	No Connection
2	Vout	LED anode connection	13	LED	LED cathode connection
3	Vout	LED anode connection	14	LED	LED cathode connection
4	NC	No Connection	15	LED	LED cathode connection
5	NC	No Connection	16	LED	LED cathode connection
6	Vout	LED anode connection	17	NC	No Connection
7	Vout	LED anode connection	18	LED	LED cathode connection
8	Vout	LED anode connection	19	LED	LED cathode connection
9	NC	No Connection	20	LED	LED cathode connection
10	GND	Ground	21	LED	LED cathode connection
11	GND	Ground			

6.0 SIGNAL TIMING SPECIFICATION

6.1 The NE160QDM-NZB V8.0 Is Operated By The DE Only

< Table 8. Signal Timing Specification >

Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	-	1175.04	-	MHz
Frame Period		Tv	-	1800	-	lines
			-	240	-	Hz
			-	4.16	-	ms
Vertical Display Period		Tvd	-	1600	-	lines
One line Scanning Period		Th	-	2720	-	clocks
Horizontal Display Period		Thd	-	2560	-	clocks

Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	-	293.76	-	MHz
Frame Period		Tv	-	1800	-	lines
			-	60	-	Hz
			-	16.7	-	ms
Vertical Display Period		Tvd	-	1600	-	lines
One line Scanning Period		Th	-	2720	-	clocks
Horizontal Display Period		Thd	-	2560	-	clocks

Note : The above is as optimized setting.

6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 9.

<Table 9. eDP Main-Link RX TP4 Package Pin Parameters>

Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock (Link clock down-spreading)	SSC	-	-	0.5	%	
Differential peak-to-peak input voltage at package pins	VRX-DIFFp-p	120	-	1200	mV	
Rx input DC common mode voltage	VRX_DC_CM	0	-	2	V	
Differential termination resistance	RRX-DIFF	80	100	120	Ω	
Single-ended termination resistance	RRX-SE	40	-	60	Ω	
Rx short circuit current limit	IRX_SHORT	-	-	50	mA	
Intra-pair skew at Rx package pins (HBR) RX intra-pair skew tolerance at HBR	LRX_SKEW_INTRA_PAIR	-	-	60	ps	
AC Coupling Capacitor	CSOURCE_ML	75		200	nF	Source side

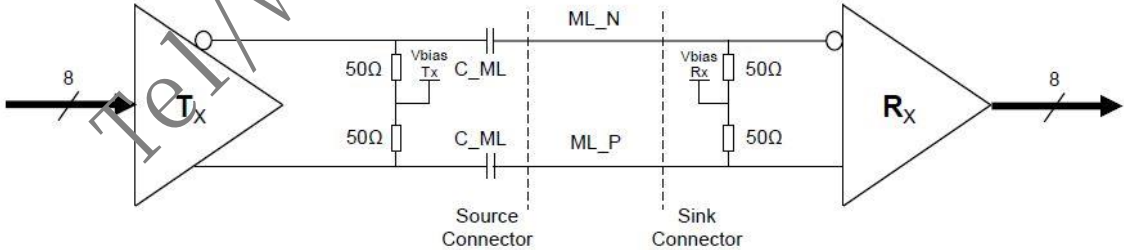


Figure 14. Main link differential pair

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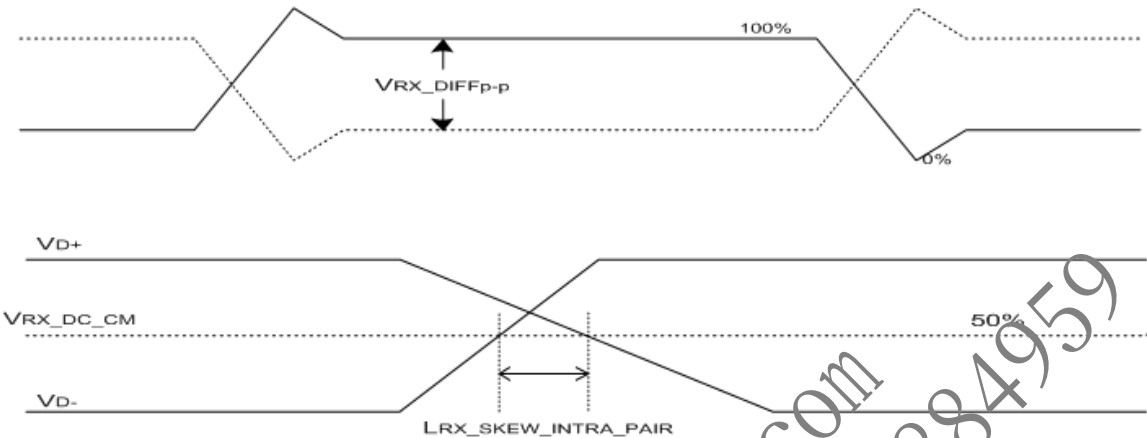


Figure 15. VRX-DIFFp-p & LRX_SKEW_INTRA_PAIR

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<Table 10. HPD Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
HPD voltage	V _{HPD}	2.25	-	3.6	V	
Hot Plug Detection Threshold	-	2.0	-	-	V	Source side Detecting
Hot Unplug Detection Threshold	-	-	-	0.8V	V	
HPD_IRQ Pulse Width	HPD_IRQ	0.5	-	1	ms	
HPD_TimeOut	-	2.0	-	-	ms	

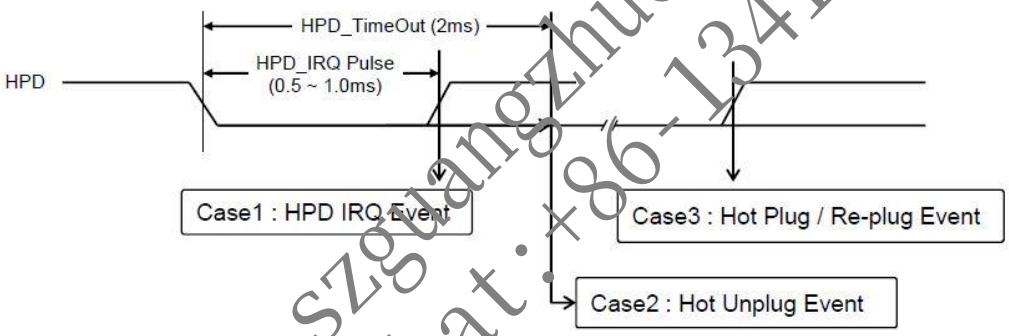


Figure 16. HPD Events

<Table 11. AUX Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
AUX unit interval	UIAUX	0.4	0.5	0.6	Us	
AUX peak-to-peak input differential voltage	VAUX-RX-D IFFp-p	0.29	-	1.38	V	
AUX CH termination DC resistance	RAUX-TER M	80	100	120	Ohm	
AUX DC common mode voltage	VAUX-DC-C M	0	-	2	V	
AUX turn around common mode voltage	VAUX-TUR N-CM	-	-	0.3	V	
AUX short circuit current limit	IAUX-SHOR T	-	-	90	mA	
AUX AC Coupling Capacitor	CSOURCE-A UX	75	-	200	nf	Source side

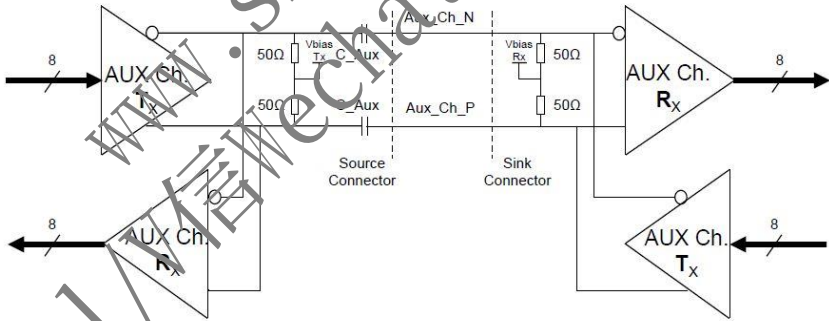


Figure 17. AUX differential pair

7.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

<Table 12. Input Signal & Basic Display Colors & Gray Scale of Colors >

	Colors & Gray scale	Data signal																										
		R0 R1 R2 R3 R4 R5 R6 R7 R8 R9	G0 G1 G2 G3 G4 G5 G6 G7 G8 G9	B0 B1 B2 B3 B4 B5 B6 B7 B8 B9																								
Basic colors	Black	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0																								
	Blue	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1																								
	Green	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0																								
	Light Blue	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1																								
	Red	1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0																								
	Purple	1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1																								
	Yellow	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0																								
	White	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1																								
Gray scale of Red	Black	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0																								
	△	1 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0																								
	Darker	0 1 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0																								
	△	↑									↑																	
	▽	↓									↓																	
	Brighter	1 0 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0																								
	▽	0 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0																								
	Red	1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0																								
Gray scale of Green	Black	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0																								
	△	0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0																								
	Darker	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0																								
	△	↑									↑																	
	▽	↓									↓																	
	Brighter	0 0 0 0 0 0 0 0 0 0	1 0 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0																								
	▽	0 0 0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0																								
	Green	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0																								
Gray scale of Blue	Black	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0																								
	△	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0																								
	Darker	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 1 0 0 0 0 0 0 0 0																								
	△	↑									↑																	
	▽	↓									↓																	
	Brighter	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	1 0 1 1 1 1 1 1 1 1																								
	▽	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1 1 1																								
	Blue	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1																								
Gray scale of White& Black	Black	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0																								
	△	1 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0																								
	Darker	0 1 0 0 0 0 0 0 0 0	0 1 0 0 0 0 0 0 0 0	0 1 0 0 0 0 0 0 0 0																								
	△	↑									↑																	
	▽	↓									↓																	
	Brighter	1 0 1 1 1 1 1 1 1 1	1 0 1 1 1 1 1 1 1 1	1 0 1 1 1 1 1 1 1 1																								
	▽	0 1 1 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1 1 1																								
	White	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1																								

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8.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below.

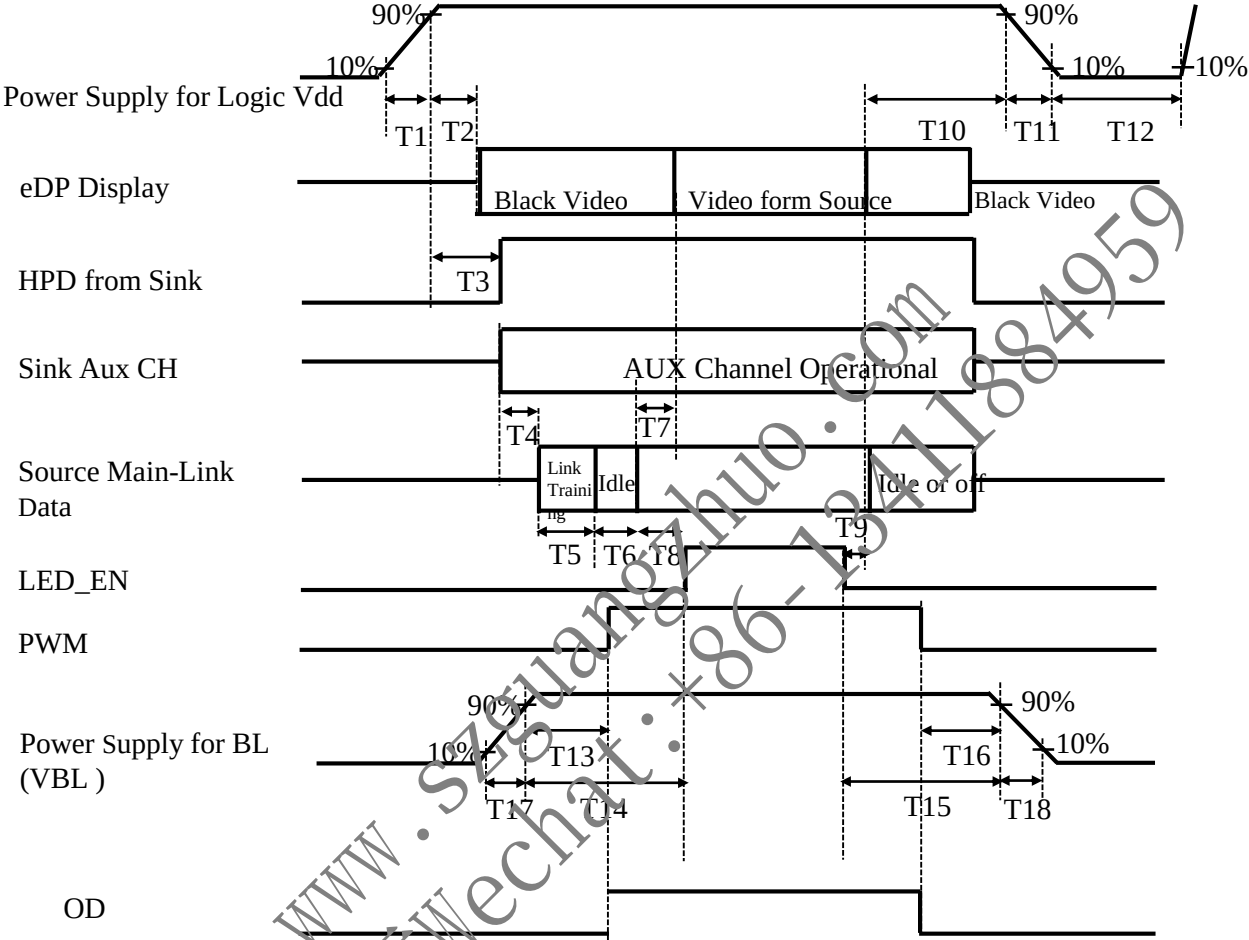


Figure 18. Power Sequence

- 0.5ms ≤ T1 ≤ 10 ms
 - 0ms < T2 ≤ 200 ms
 - 0ms < T3 ≤ 200 ms
 - T4+T5+T6+T8>80ms
 - 0ms < T7 ≤ 50ms
 - 50ms < T8
 - 0ms < T9
- 100ms < T10 < 500 ms
 - 0.5ms ≤ T11 ≤ 10 ms
 - 500ms ≤ T12
 - 0ms < T13
 - 0ms < T14
 - 0ms < T15
 - 0ms < T16
- 0.5ms ≤ T17
 - 0.5ms ≤ T18

Notes:

1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal are valid.

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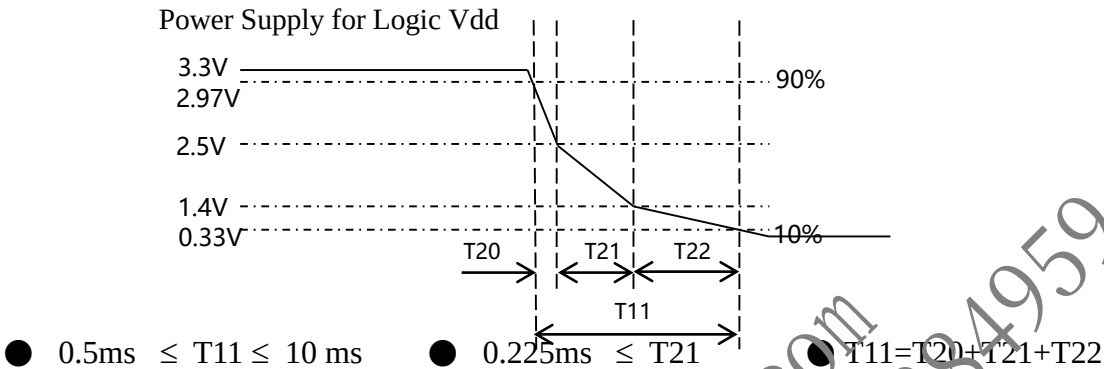


Figure 19. T11 timing requirements

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9.0 Connector Description

Physical interface is described as for the connector on LCM.
 These connectors are capable of accommodating the following signals and will be following components.

9.1 TFT LCD Module

< Table 13. Signal Connector >

Connector Name /Description	For Signal Connector
Manufacturer	STM
Type/ Part Number	MSAK24025P40G
Mating Housing/ Part Number	I-PEX 20454-040T

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10.0 MECHANICAL CHARACTERISTICS

10.1 Dimensional Requirements

Figure 23 shows mechanical outlines for the model NE160QDM-NZB V8.0.
Other parameters are shown in Table 14.

<Table 14. Dimensional Parameters>

Parameter	Specification	Unit
Active Area	344.6784 (H) ×215.424(V)	mm
Number of pixels	2560 (H) X 1600 (V) (1 pixel = R + G + B dots)	pixels
Pixel pitch	134.64 (H) X 134.64 (V)	um
Pixel arrangement	RGB Vertical stripe	
Display colors	1064.3M(8bit+2RFC)	
Display mode	Normally Black	
Dimensional outline	349.68±0.3 (H)*224.42±0.3(V)(W/O FPC bending)*2.6 (Max) 349.68±0.3 (H)*224.92(Max)(V)(W/FPC bending)*4.6(Max)	mm
Weight	325g(max)	g

10.2 Mounting

See Figure 24.

10.3 Anti-Glare and Polarizer Hardness.

The surface of the LCD has an Anti-Glare coating to minimize reflection and a 3H hardness coating to reduce scratching.

10.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 350lux.

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11.0 RELIABILITY TEST

The reliability test items and its conditions are shown in below.
<Table 15. Reliability Test>

No	Test Items	Conditions	Remark
1	High temperature storage test	Ta = 60℃ , 60%RH, 240 hrs	
2	Low temperature storage test	Ta = -20℃ , 240 hrs	
3	High temperature & high humidity operation test	Ta = 50℃ , 80%RH, 240 hrs	
4	High temperature operation test	Ta = 50℃ , 60%RH, 240 hrs	
5	Low temperature operation test	Ta = 0℃ , 240 hrs	
6	Thermal shock	Ta = -20℃ ↔ 60℃ (0.5 hr), 60%±3%RH, 100 cycle	
7	Vibration test (non-operating)	Ta = 25℃ , 60%RH, 1.5G, 10~500Hz, Sine X,Y,Z Sweep rate : 1 hour	Note 1
8	Shock test (non-operating)	Ta = 25℃ , 60%RH, 220G, Half Sine Wave 2msec±X, ±Y, ±Z Once for each direction	Note 1
9	Electro-static discharge test (operating)	Air : 150 pF, 330Ω, ±15 KV Contact : 150 pF, 330Ω, ±8 KV Ta = 25℃ , 60%RH,	Note 2

- Notes :
1. The fixture must be hard enough , so that the module would not be twisted or bent.
 2. Self- recovery and restart recovery is allowed. No hardware failures.

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12.0 HANDLING & CAUTIONS

- (1) Cautions when taking out the module

 - Pick the pouch only, when taking out module from a shipping package.
- (2) Cautions for handling the module

 - As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
 - As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
 - As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
 - Do not pull the interface connector in or out while the LCD module is operating.
 - Put the module display side down on a flat horizontal plane.
 - Handle connectors and cables with care.
- (3) Cautions for the operation

 - When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
 - Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.
- (4) Cautions for the atmosphere

 - Dew drop atmosphere should be avoided.
 - Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.
- (5) Cautions for the module characteristics

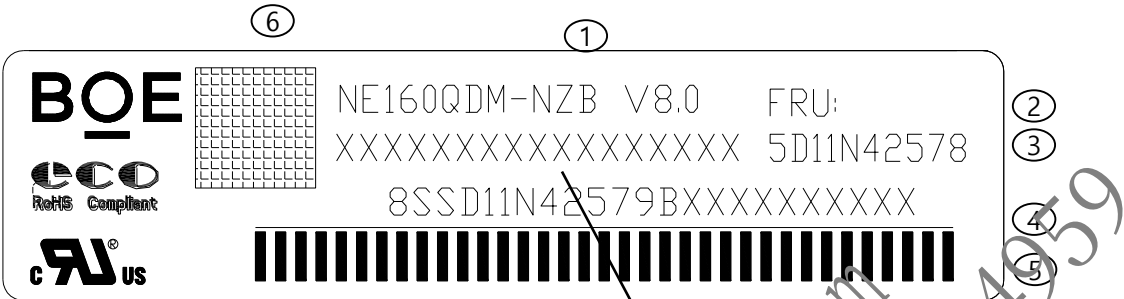
 - Do not apply fixed pattern data signal to the LCD module at product aging.
 - Applying fixed pattern for a long time may cause image sticking.
- (6) Other cautions

 - Do not disassemble and/or re-assemble LCD module.
 - Do not re-adjust variable resistor or switch etc.
 - When returning the module for repair or etc. Please pack the module not to be broken. We recommend to use the original shipping packages.

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13.0 LABEL

(1) Product Label



标签尺寸: 48mm × 12mm, 厚度0.075mm

- 1. FG-CODE: NE160QDM-NZB V8.0
- 2. FRU码: 5D11N42578; PN码: SD11N42579
- 3. MDL ID(厂内信息)
- 4. PPID 8S码: SD11N42579
- 5. MDL ID 条纹码(厂内信息)
- 6. PPID对应二维码(客户端信息)

<Table 16. Module ID Naming Rule>

MDL ID 编码规则

序号号	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
代码	X	X	X	3	X	X	X	3	S	P	0	X	X	X	X	X	X
描述	GBN代码		等级	B3	年	月	日	FG Code后四位				序列号					

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(2) High voltage caution label

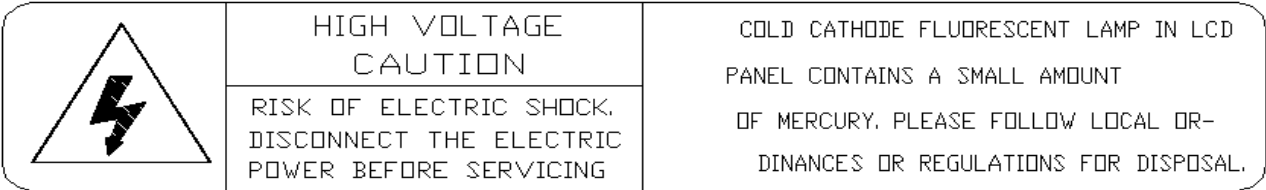


Figure 20. High Voltage Caution Label

(3) Box label

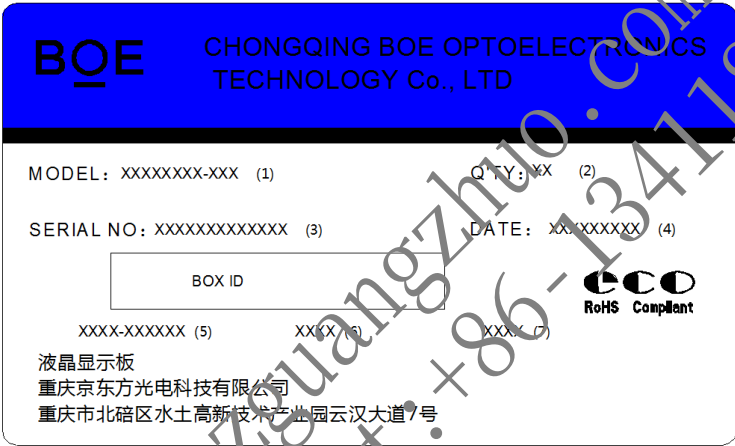


Figure 21. Box Label

Serial number marked part needs to print, show as follows:

1. FG-CODE(Before 12 bit)
2. Product quantity
3. Box ID
4. Date
5. The client section material number(The client)
6. FG-Code After four
7. The supplier code

Total Size:100×60mm

<Table 17. Box Label Naming Rule >

Digit Code	1	2	3	4	5	6	7	8	9	10	11	12	13
Code	X	X	X	X	X	X	X	X	X	X	X	X	X
Description	Product Name		Product Grade	Facility Code	Year		Month	Revision	Box Serial NO.				

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14.0 PACKING INFORMATION

14.1 Packing Order

Spacer×4
MDL×3
Tray

7Tray
+
1Cover

PE Bag

EPE Board

Inner Box

- Put 1 pcs spacer in tray and 1 pcs MDL on spacer.
3 pcs MDL/Tray, 4 pcs Spacer/Tray.
- Put 7 pcs tray and 1 pcs tray cover in PE bag.
- Put PE bag with 2 EPE Cushion in the inner box.
- 21 pcs/Box, 12 Box/Pallet, 252 pcs MDL/Pallet.

Figure 22. Packing Order

14.2 Note

- Box dimension: 522mm*392mm*294mm
- Package quantity in one box: 21pcs
- Total weight: 10.0 kg/Box (Typ)

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Figure 26. TFT-LCD Module Outline Dimensions (Rear view)

Notes:

- ⑮1. Warpage and deformation Spec.: 0.5mm Max..
- The eDP connector is measured at PIN 1 and mating line.
- Unspecified tolerance refer to ± 0.3 mm.
- Top polarizer is the highest portion.
- Critical dimension: ①~⑮ cpk:① ②⑨⑩
- Do not have light leakage on four corners of module.
- Measurement method refer to Appendix A
- System matching refer to Appendix B
- “() ”marks the reference dimensions.
- Cell tape and polarizer step tolerance is 0.057 ± 0.026 mm for L/R/U portion.

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16.0 EDID Table

Address (HEX)	Function	Hex	Dec	crc	Input values.	Notes
00	Header	00	0		0	EDID Header
01		FF	255		255	
02		FF	255		255	
03		FF	255		255	
04		FF	255		255	
05		FF	255		255	
06		FF	255		255	
07		00	0		0	
08	ID Manufacturer Name	09	9		BOE	ID = BOE
09		E5	229			
0A	ID Product Code	8B	139		3211	ID = 3211
0B		0C	12			
0C	Family ID	68	104		104	Family ID for LBG
0D		00	0			
0E	Reserved	00	0		0	
0F		00	0		0	
10	Week of manufacture	24	36		36	
11	Year of Manufacture	21	33		2023	Manufactured in 2023
12	EDID Structure Ver.	01	1		1	EDID Ver 1.0
13	EDID revision #	04	4		4	EDID Rev. 0.4
14	Video input definition	B5	181		-	Refer to right table
15	Max H image size	22	34		34	34.468 cm (Approx)
16	Max V image size	16	22		22	21.542 cm (Approx)
17	Display Gamma	78	120		2.2	Gamma curve = 2.2
18	Feature support	03	3		-	Refer to right table
19	Red/Green low bits	AD	173		-	Red / Green Low Bits
1A	Blue/White low bits	35	53		-	Blue / White Low Bits
1B	Red x high bits	AE	174	698	0.682	Red (x) = 10101110 (0.682)
1C	Red y high bits	50	80	322	0.314	Red (y) = 01010000 (0.314)
1D	Green x high bits	43	67	271	0.265	Green (x) = 01000011 (0.265)
1E	Green y high bits	B1	177	709	0.692	Green (y) = 10110001 (0.692)
1F	Blue x high bits	25	37	148	0.145	Blue (x) = 00100101 (0.145)
20	BLue y high bits	0E	14	59	0.058	Blue (y) = 00001110 (0.058)
21	White x high bits	50	80	321	0.313	White (x) = 01010000 (0.313)
22	White y high bits	54	84	337	0.329	White (y) = 01010100 (0.329)
23	Established timing 1	00	0		-	-
24	Established timing 2	00	0		-	
25	Established timing 3	00	0		-	

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26	Standard timing #1	01	1			Not Used	
27		01	1				
28	Standard timing #2	01	1			Not Used	
29		01	1				
2A	Standard timing #3	01	1			Not Used	
2B		01	1				
2C	Standard timing #4	01	1			Not Used	
2D		01	1				
2E	Standard timing #5	01	1			Not Used	
2F		01	1				
30	Standard timing #6	01	1			Not Used	
31		01	1				
32	Standard timing #7	01	1			Not Used	
33		01	1				
34	Standard timing #8	01	1			Not Used	
35		01	1				
36	Detailed timing/monitor descriptor #1	C0	192		293.7600	293.76MHz Main clock	
37		72	114				
38		00	0		2560	Hor Active = 2560	
39		A0	160		160	Hor Blanking = 160	
3A		A0	160		-	4 bits of Hor. Active + 4 bits of Hor. Blanking	
3B		40	64		1600	Ver Active = 1600	
3C		C8	200		200	Ver Blanking = 200	
3D		60	96		-	4 bits of Ver. Active + 4 bits of Ver. Blanking	
3E		30	48		48	Hor Sync Offset = 48	
3F		20	32		32	H Sync Pulse Width = 32	
40		36	54		3	V sync Offset = 3 line	
41		00	0		6	V Sync Pulse width : 6 line	
42		59	89		345	Horizontal Image Size = 344.68 mm (Low 8 bits)	
43		D7	215		215	Vertical Image Size = 215.42 mm (Low 8 bits)	
44		10	16		-	4 bits of Hor Image Size + 4 bits of Ver Image Size	
45		00	0		0	Hor Border (pixels)	
46		00	0		0	Vertical Border (Lines)	
47	1A	26		-	-		
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		Customer Spec			0	2023.11.10
48	Detailed timing/monitor descriptor #2	00	0		-	Indicates descriptor is a display Descriptor
49		00	0		-	
4A		00	0		-	
4B		FD	253		-	Tag Number for Display Range Limits Descriptor
4C		0C	12		12	Vertical/Horizontal Rate Offset are zero
4D		3C	60		60	Minimum Vertical Rate:60 Hz
4E		F0	240		240	Maximum Vertical Rate:240 Hz
4F		B1	177		432	Minimum Horizontal Rate:432 kHz
50		B1	177		432	Maximum Horizontal Rate:432 kHz
51		76	118		1175.0400	Maximum Pixel Clock:1175.04 MHz
52		01	1		-	Range Limits Only
53		0A	10		-	Display Range Limits & CVT Support Definition
54		20	32		-	
55		20	32		-	
56		20	32		-	
57		20	32		-	
58		20	32		-	
59		20	32		-	
5A	Detailed timing/monitor descriptor #3	00	0			Indicates descriptor #3 is a display Descriptor
5B		00	0			Reserved
5C		00	0			
5D		FE	254			Tag: ASCII String
5E		00	0			Reserved
5F		42	66		B	Manufacture name : BOECQ
60		4E	79		O	
61		45	69		E	
62		20	32			
63		43	67		C	
64		51	81		Q	
65		0A	10			
66		20	32			
67		20	32			
68	20	32				
69	20	32				
6A	20	32				
6B	20	32				
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6C	Detailed timing/monitor descriptor #4	00	0			Indicates descriptor #4 is a display Descriptor
6D		00	0			
6E		00	0			Reserved
6F		FE	254			Tag: ASCII String
70		00	0			Reserved
71		4E	78		N	Model name : NE160QDM-NZB
72		45	69		E	
73		31	49		1	
74		36	54		6	
75		30	48		0	
76		51	81		Q	
77		44	68		D	
78		4D	77		M	
79		2D	45		-	
7A		4E	78		N	
7B		5A	90		Z	
7C		42	66		B	
7D		0A	10			
7E	Extension flag	02	2			-
7F	Checksum	9B	155	155		

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80	Tag	02	2	2	Tag 0x02 assigned by VESA to CTA for this extension
81	Revision Number	03	3	3	indicates revision of CTA-861 used by this device (Ver3)
82	Length of Info Frame	0F	15	15	Byte number offset d where 18-byte descriptors begin (typically Detailed Timing Descriptors)
83	Global Declarations	00	0	0	these bit are utilized as flags in later versions of CTA-861
84	Tag Code [7:5], Length of data [4:0](Start of data block collection(bit7~5: tag code 0x07, bit 4~0:length of following data block is 0x03))	E3	227	227	Colorimetry Data Block , 3 Byte
85	extended Tag Code (0x05)	05	5	5	Colorimetry Data Block
86	Colorimetry Support Flags(BT2020RGB, BT2020YCC, BT2020cYCC, AdobeRGB, AdobeYCC601, sYCC601, xvYCC709, xvYCC601)	80	128	128	support BT2020RGB
87	Colorimetry Metadata Support Flags(DCI-P3, F46=0, F45=0, F44=0, MD3, MD2, MD1, MD0)	80	128	128	0: 非DCI-P3 panel((HDR400); 128: DCI-P3 panel((HDR600))
88	HDR static metadata Tag Code [7:5], Length of data [4:0]	E6	230	230	Colorimetry Data Block , 6 Byte
89	Extended Tag Code(0x06)	06	6	6	HDR Static Metadata Data Block
8A	Supported Electro-Optical Transfer Function	05	5	5	Traditional gamma SDR, SMPTE ST 2084 [2],
8B	SM_0 =1: Static Metadata Type 1	01	1	1	Static Metadata Type 1,
8C	Desired Content Max Luminance data	6A	106	106	panel real max luminance(eg:500)
8D	Desired Content Max Frame-average Luminance data	6A	106	106	panel real max luminance(eg:500)
8E	Desired Content Min Luminance data	48	72	72	panel real min luminance(eg:0.4)
8F		00	0	-	Unused
90		00	0	-	Unused
91		00	0	-	Unused
92		00	0	-	Unused
93		00	0	-	Unused
94		00	0	-	Unused
95		00	0	-	Unused
96		00	0	-	Unused
97		00	0	-	Unused
98		00	0	-	Unused
99		00	0	-	Unused
9A		00	0	-	Unused
9B		00	0	-	Unused
9C		00	0	-	Unused

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9D		00	0		-	Unused
9E		00	0		-	Unused
9F		00	0		-	Unused
A0		00	0		-	Unused
A1		00	0		-	Unused
A2		00	0		-	Unused
A3		00	0		-	Unused
A4		00	0		-	Unused
...		...	...		...	
...		...	...			
...		...	...			
FF	Checksum	F6	246			

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		Customer Spec			0	2023.11.10	
00	DID Extension Header	70	112		112	DisplayID EDID Extension Block tag	
01		20	32		32	DisplayID Version/RevSION = 2.0	
02		79	121		121	Section Size (byte) = 121 bytes	
03		02	2		2	Display Product Primary Use Case	
04		00	0		0	Extension count	
05	DID Block #1 Header	22	34		34	DID2.0 Data block tag[22h] =Detailed Timing Data Block	
06		00	0		0	Block revision = Revision 0	
07		14	20		20	Number of Payload Bytes in block= 20 Bytes	
08	DID DATA Detailed Timing Data Block #1	FF	255		1175.0	Pixel Clock (Low bit, Range = 0.001Mhz (000000h) ~ 16,777.216Mhz (FFFFFFh))	
09		ED	237			Minium Pixel Clock (Middle bit)	
0A		11	17			Minium Pixel Clock (High bit)	
0B		85	133		133	timing options	
0C		FF	255		2560	H-Active	
0D		09	9				
0E		9F	159				
0F		00	0		160	H-Blanking	
10		2F	47		48	H-offset	
11		00	0				
12		1F	31				
13		00	0		32	H-sync pulse width	
14		3F	63		1600	V-Active	
15		06	6				
16		C7	199				
17		00	0		200	V-Blanking	
18		02	2		3	V-offset	
19		00	0				
1A		05	5				
1B		00	0		6	V-sync pulse width	
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		Customer Spec				0	2023.11.10	
1C	DID Block #2 Header	25	37		37	DID2.0 Data block tag[25h] = Dynamic Video Timing Range Limits		
1D		01	1		1	Block revision = Revision 1		
1E		09	9		9	Number of Payload Bytes in block= 9 Bytes		
1F	DID DATA Block #2 Monitor range limited	FF	255		1175.040	Minimum Pixel Clock (Low bit, Range = 0.001Mhz (000000h) ~ 16,777.216Mhz (FFFFFFh))		
20		ED	237			Minium Pixel Clock (Middle bit)		
21		11	17			Minium Pixel Clock (High bit)		
22		FF	255		1175.040	Maximum Pixel Clock (Low bit, Range = 0.001Mhz (000000h) ~ 16,777.216Mhz (FFFFFFh))		
23		ED	237			Maximum Pixel Clock (Middle bit)		
24		11	17			Maximum Pixel Clock (High bit)		
25		3C	60		60	Min. Vertical Rate : 60 Hz (Range : 0Hz (00h) ~ 255Hz (FFh))		
26		F0	240		240	Max. Vertical Rate : 240 Hz (Range : 0Hz (000h) ~ 255Hz (FFh))		
27		80	128		128	Seamless Dynamic Video Timing Support : Seamless Dynamic Video Timing change shall be supported with a fixed horizontal pixel rate and dynamic vertical blanking.		
28		DID Block #3 Header	2B	43		43	DID2.1 Data block tag[2Bh] = Adaptive-Sync Data Block	
29			00	0		0	Block revision = Revision 0	
2A	0C		12		12	Number of Payload Bytes in block= 12 Bytes		
2B	DID DATA Block #3 Adaptive-Sync	27	39		39	Adaptive-Sync Operation and Range Information RR#1		
2C		00	0		0	Flicker performance is met in any duration decrease within the refresh rate range without jitter impact.		
2D		64	100		100	Min. Vertical Rate : 100 Hz		
2E		EF	239		240	Maximum Refresh Rate7:0		
2F		00	0			bit1:0 =01: Maximum Refresh Rate9:8		
30		00	0		0	Flicker performance is met in any duration decrease within the refresh rate range without jitter impact.		
31		27	39		39	Adaptive-Sync Operation and Range Information RR#2		
32		00	0		0	Flicker performance is met in any duration decrease within the refresh rate range without jitter impact.		
33		30	48		48	Min. Vertical Rate : 48 Hz		
34		3B	59		60	Maximum Refresh Rate7:0		
35		00	0			bit1:0 =01: Maximum Refresh Rate9:8		
36		00	0		0	Flicker performance is met in any duration decrease within the refresh rate range without jitter impact.		
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		Customer Spec		0		2023.11.10	
37	DID Block #4 Header	81	129		129	DID2.0 Data block tag[81h] = CTA DisplayID	
38		00	0		0	Block revision = Revision 0	
39		13	19		19	Number of Payload Bytes in block= 19 Bytes	
3A	DID DATA Block #4 AMD VSDB 3	72	114		114	CTA Block1 Tag Code and Block1 Length = Vendor Specific Data Block(03h), Size(byte) = 18 bytes	
3B		1A	26		26	AMD IEEE OUI value (0x00001A)	
3C		00	0			(Hex. LSB first)	
3D		00	0			(Hex. LSB first)	
3E		03	3		3	AMD VSDB Version 3	
3F		03	3		3	Bit 0 = 1 FreeSync supported by panel, Bit 1 = 1 native color space support	
40		3C	60		60	Min Refresh Rate	
41		F0	240		240	Max Refresh Rate	
42		00	0		0	Freesync MCCS VCP Code	
43		20	32		32	Support WCG and HDR features : Gamma 2.2 EOTF Not Supported , PQ EOTF Supported	
44		6A	106		500	Max Luminance 1 (for HDR) = 500nit	
45		48	72		0.4	Max Luminance 2 (for HDR) = 0.4nit	
46		6A	106		500	Max Luminance 2 (for HDR) = 500nit	
47		48	72		0.4	Max Luminance 2 (for HDR) = 0.4nit	
48		F0	240		240	Bits 7:0 -Freesync Maximum Refresh Rate (MSB)	
49		00	0			Bits 9:8 - MSB FreeSync Maximum refresh rate [Hz]	
4A		00	0		0	Maximum Fast Transport Input Pixel Rate [kHz] - bits 7:0	
4B		00	0		0	Maximum Fast Transport Input Pixel Rate [kHz] - bits 15:8	
4C		00	0		0	Maximum Fast Transport Input Pixel Rate [kHz] - bits 23:16	
4D		00	0		-	Unused	
4E		00	0		-	Unused	
4F		00	0		-	Unused	
4D		00	0		-	Unused	
...		...	...		...	...	
...		...	...		...	...	
7D		00	0		-	Unused	
7E	Checksum(00~7E)	C7	199		-		
7F	Checksum(00~7F)	90	144				
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17.0 GENERAL PRECAUTIONS

17.1 HANDLING

- (1) When the module is assembled, It should be attached to the system firmly using every mounting holes.
Be careful not to twist or bend the modules.
- (2) Refrain from strong mechanical shock or any force to the module. Otherwise, it may cause improper operation or damage to the module.
- (3) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than 1 HB pencil lead.
- (4) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.
- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use Ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth .In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static , it may cause damage to the module.
- (9) Use fingerstalls with soft gloves to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Do not pull or fold the LED FPC.
- (12) Do not touch any component which is located on the back side.
- (13) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (14) Pins of connector shall not be touched directly with bare hands.

17.2 STORAGE

- (1) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃ and relative humidity of less than 70%.
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.

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17.3 OPERATION

- (1) Do not connect, disconnect the module in the “ Power On” condition.
- (2) Power supply should always be turned on/off by following item 8.0 “ Power on/off sequence “.
- (3) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
- (4) The standard limited warranty is only applicable when the module is used for general notebook applications. If used for purposes other than as specified, BOE is not to be held reliable for the defective operations. It is strongly recommended to contact BOE to find out fitness for a particular purpose

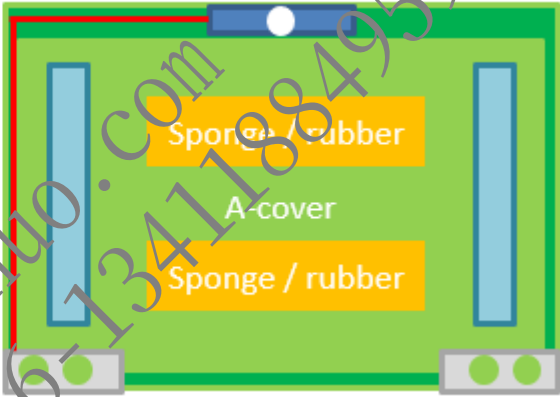
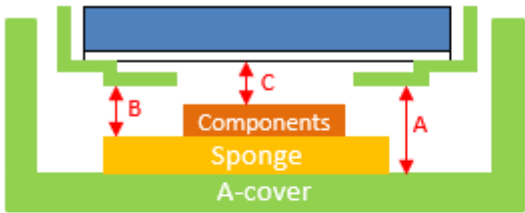
17.4 OTHERS

- (1) Avoid condensation of water. It may result in improper operation or disconnection of electrode.
- (2) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation, Variation in part contents and environmental temperature, so on) Otherwise the module may be damaged.
- (3) If the module displays the same pattern continuously for a long period of time, it can be the situation when The “ image sticks” to the screen.
- (4) This module has its circuitry PCB’s on the rear or bottom side and should be handled carefully to avoid being stressed.

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Appendix B: System design Recommendation

LCM to A-Cover / sponges Z-gap



	Plastic Cover	Metal Cover
A	≥ 1.0mm	≥ 0.8mm
B	≥ 0mm	
C	> 0.5mm	

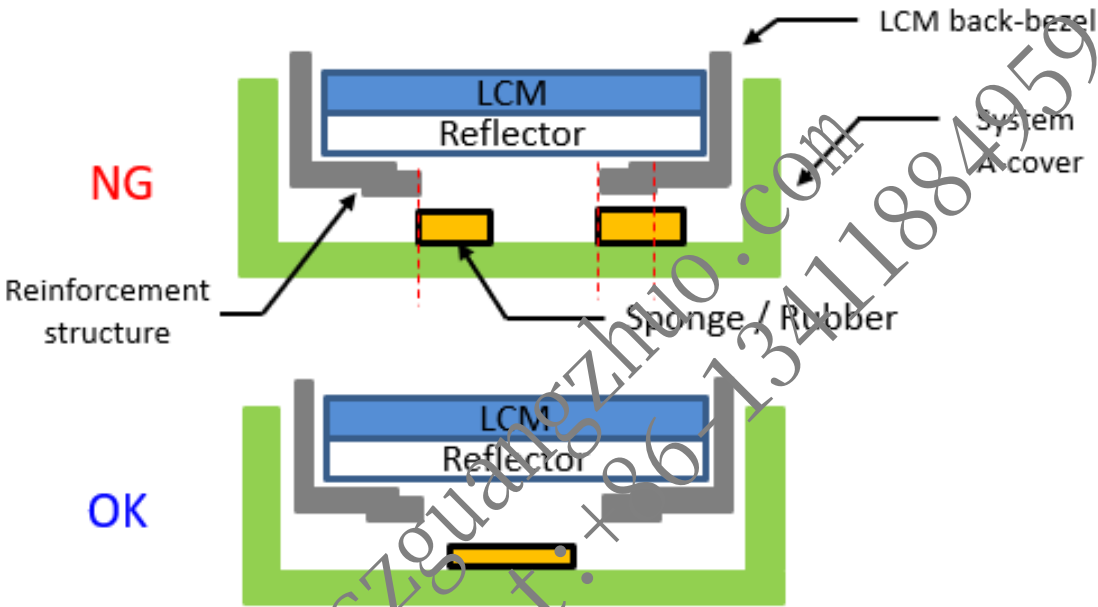
Purpose

The reflector area is very sensitive, BOE would suggest that design enough z-gap to decrease the risk of water ripple, white spots and other abnormal display

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Appendix B: System design Recommendation

LCM to A-Cover / sponges z-gap

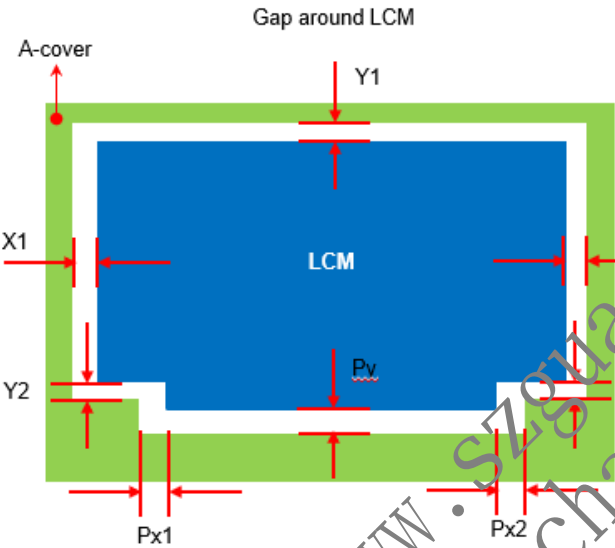


Purpose	If attach sponges or rubbers which correspond to white reflector area, it may cause white spot, pooling or other relative issues. BOE would suggest that attach wide range sponges / rubbers which can cover the LCM back-bezel opening
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Appendix B: System design Recommendation

LCM to side wall / protrusions



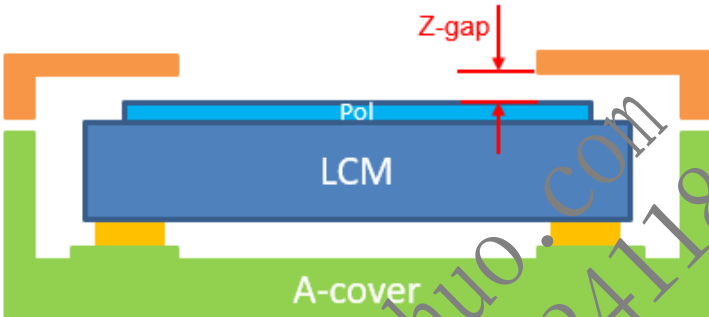
	Normal border (screws)	Narrow border (fix by tapes)
X1 / X2	Min: 0.45mm	Min: 0.35mm
Y1 / Y2	Min: 0.45mm	Min: 0.35mm
Px1 / Px2	Min: 0.55mm	
Py		

Purpose

BOE would suggest that design enough gap around LCM to prevent shock test failure, or interference, cell crack, abnormal display...etc. in the reliability test

Appendix B: System design Recommendation

LCM to B-cover z-gap



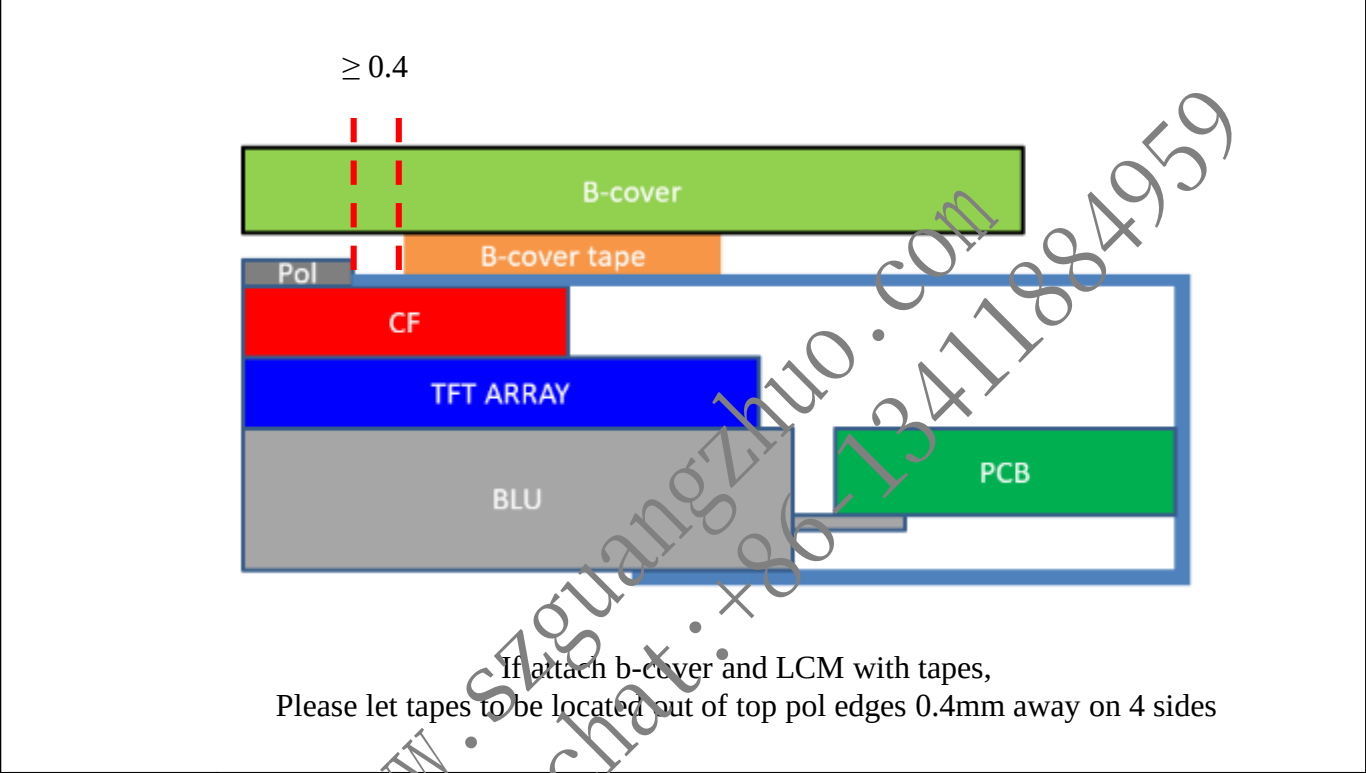
Bezel Tape	Z-Gap
Without	0.15 ~ 0.25mm
With	0.15 ~ 0.20mm

Purpose	Too less z-gap between system B-cover and LCM top pol has high risk that may cause cell crack, pooling, light leakage and other issues
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Appendix B: System design Recommendation

B-cover tape to top pol edge



If attach b-cover and LCM with tapes,
Please let tapes to be located out of top pol edges 0.4mm away on 4 sides

Purpose	To avoid the B-cover tape override top pol then cause pooling or light leakage issue
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Appendix B: System design Recommendation

Antenna Cable & Webcam wire



Purpose

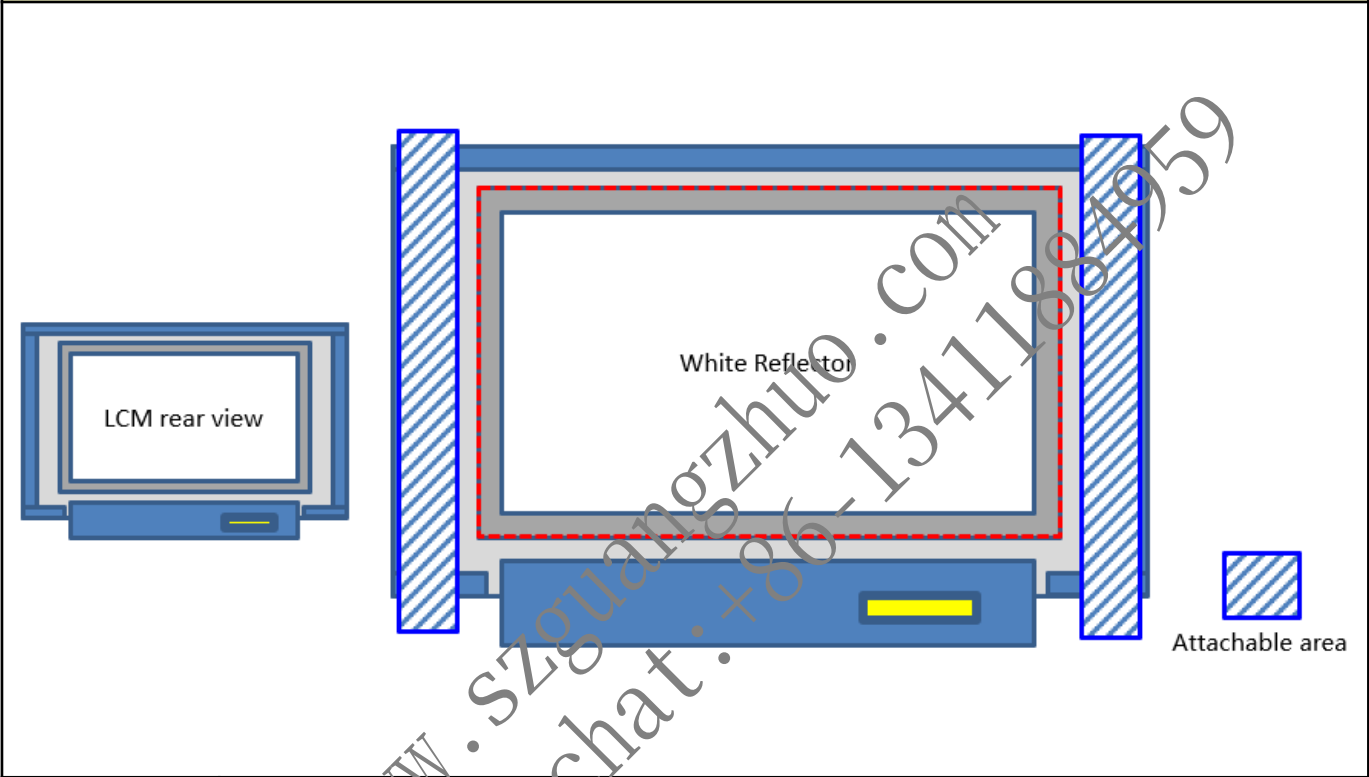
1. BOE would suggest that do not set Antenna or WebCam cable / wire go behind LCM to avoid backpack test, hinge test ,twist test or pogo test with abnormal display
2. If the cable / wire is necessary to go behind LCM, please make a groove with rounds or chamfers to protect the cable / wire, or attach with higher sponges / rubbers adjacent to the cable / wire route
3. Suggest that attach the cable / wire with tapes to A-cover
4. Do not attach anything with LCM reflector area. If attach cable / wire with LCM reflector area, it may cause pooling, white spot, light leakage and other related issues

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Appendix B: System design Recommendation

LCM paste area



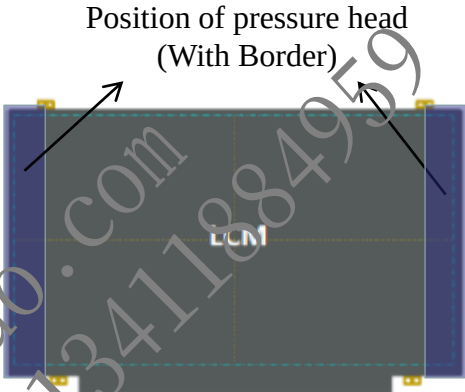
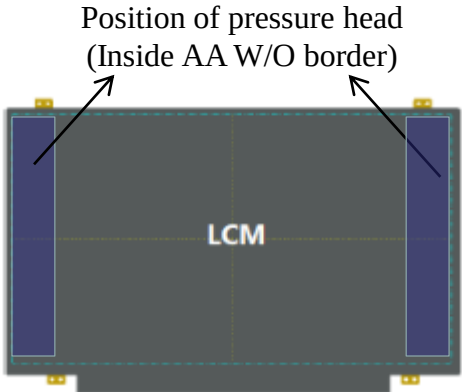
Purpose	If use the stretch remove tapes to fix LCM with A-cover, please set the stretch remove tapes correspond to the LCM back-bezel and do not let the tapes override the back-bezel’s level step of opening
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Appendix B: System design Recommendation

LCM pressable area



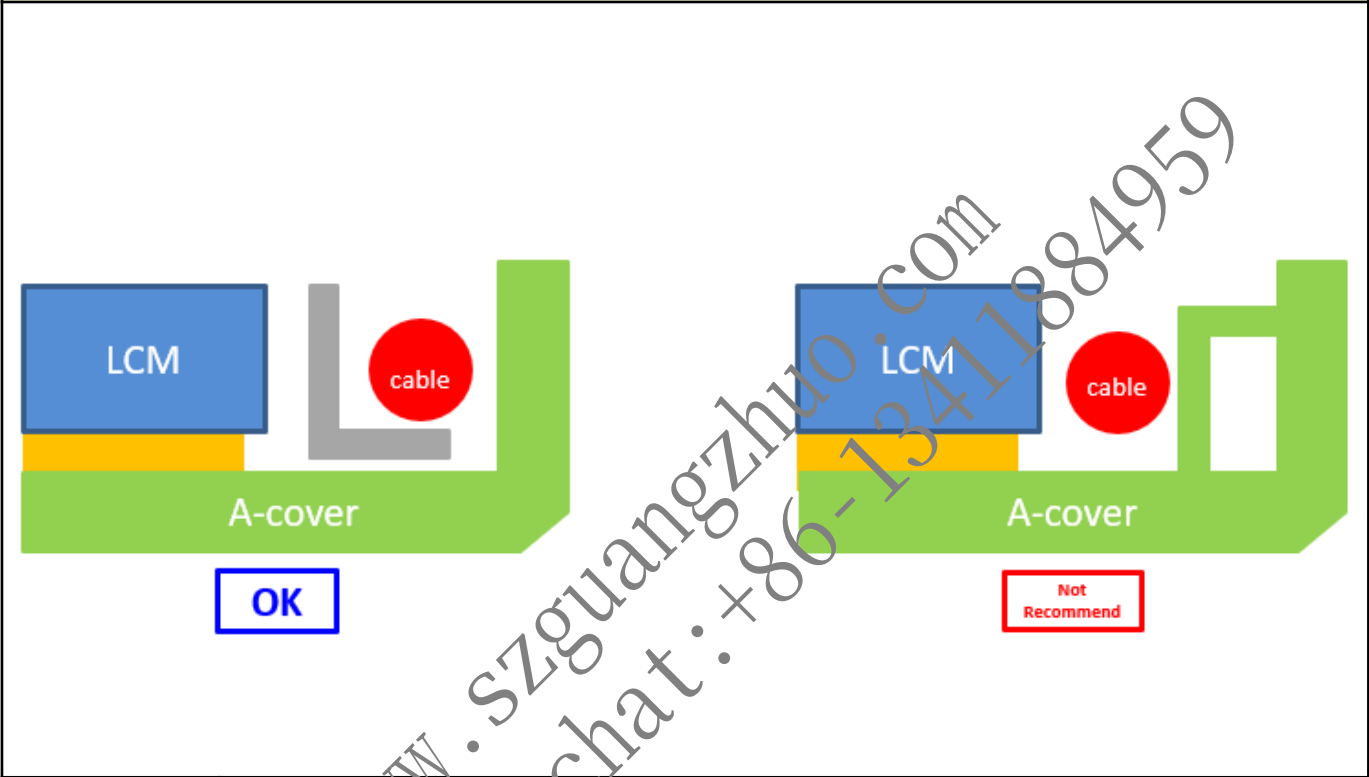
Purpose	1. If LCM is fixed on A-cover by using the press jig during assembling. 2. To avoid panel broken the design of pressure head of press jig can not only pin on cell panel. The pressure head needs to pin on the LCM frame, which the LCM frame can share the pressure of the pressing head.
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Appendix B: System design Recommendation

Wire setting

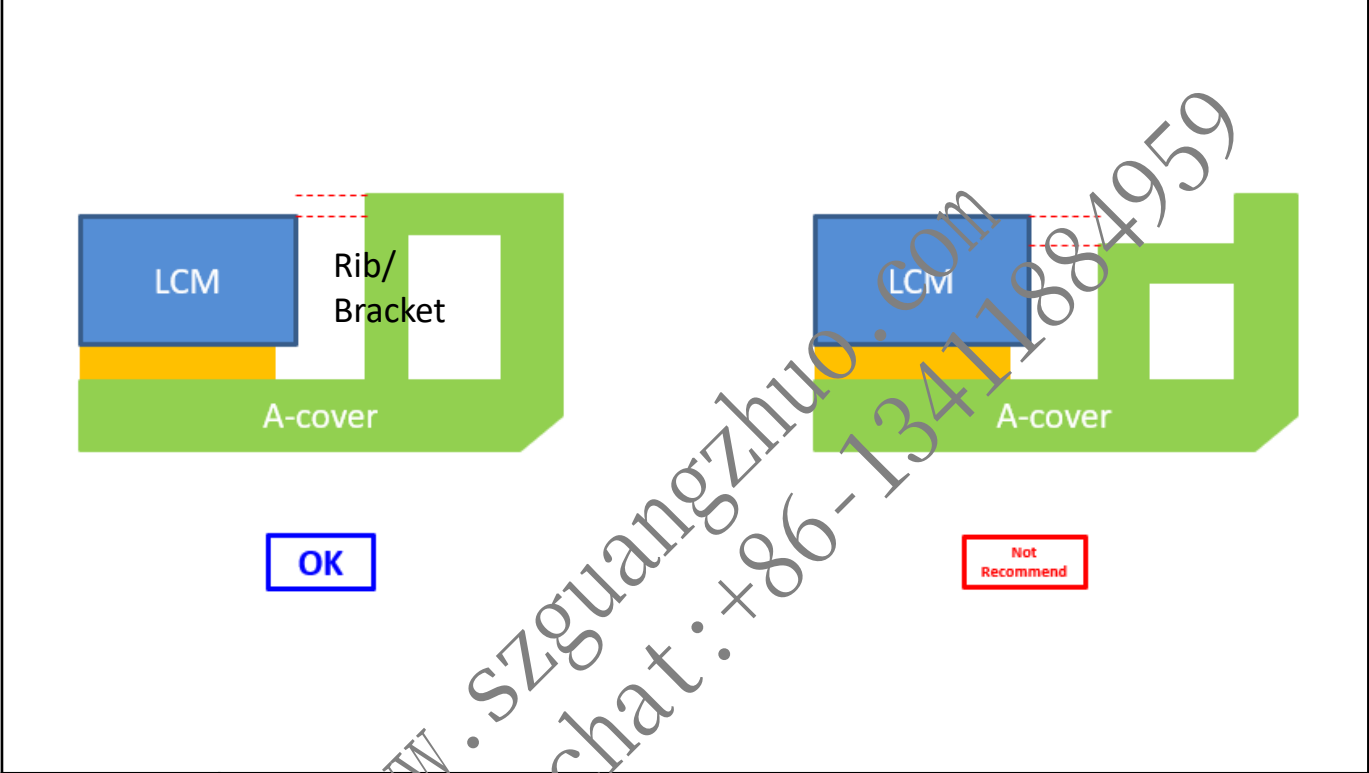


Purpose	Wires should be placed between protrusions/side wall and A-cover. If place the wires between LCM and Protrusions/side wall, it may interfere with LCM when assembling, or even cause LCM broken in reliability test.
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BOE	PRODUCT GROUP	REV	ISSUE DATE
	Customer Spec	0	2023.11.10

Appendix B: System design Recommendation

A-cover strength



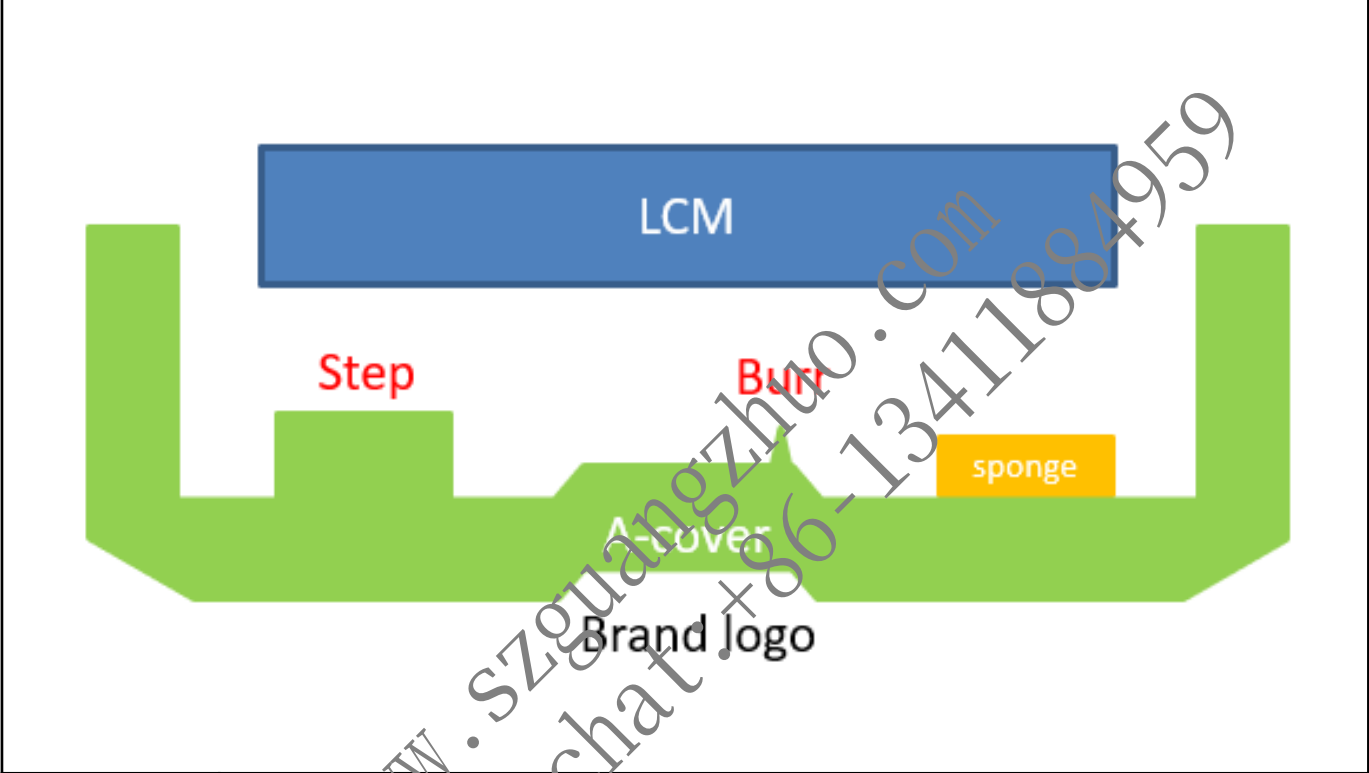
Purpose	- BOE would recommend that structural Rib/Bracket height is higher than LCM, in order to avoiding pressures to LCM. - The L-shape Bracket is recommended.
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BOE	PRODUCT GROUP	REV	ISSUE DATE
	Customer Spec	0	2023.11.10

Appendix B: System design Recommendation

System A-cover Inner Surface

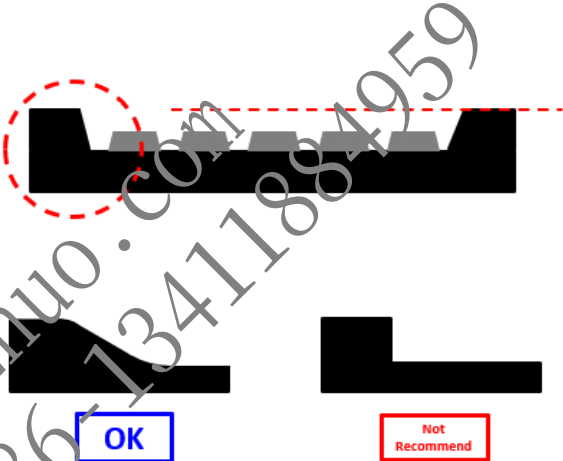
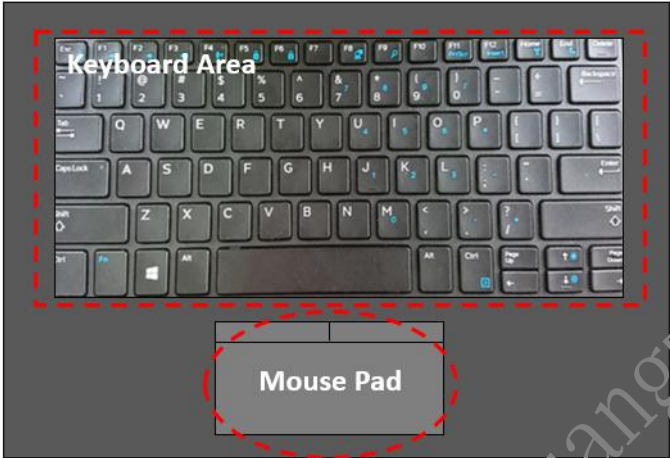


Purpose	There should not exist any burr, segment gap or protrusions beside Logo, which may cause White Spot or Glass Broken by stress concentration.
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BOE	PRODUCT GROUP	REV	ISSUE DATE
	Customer Spec	0	2023.11.10

Appendix B: System design Recommendation

Keyboard area & Mouse pad



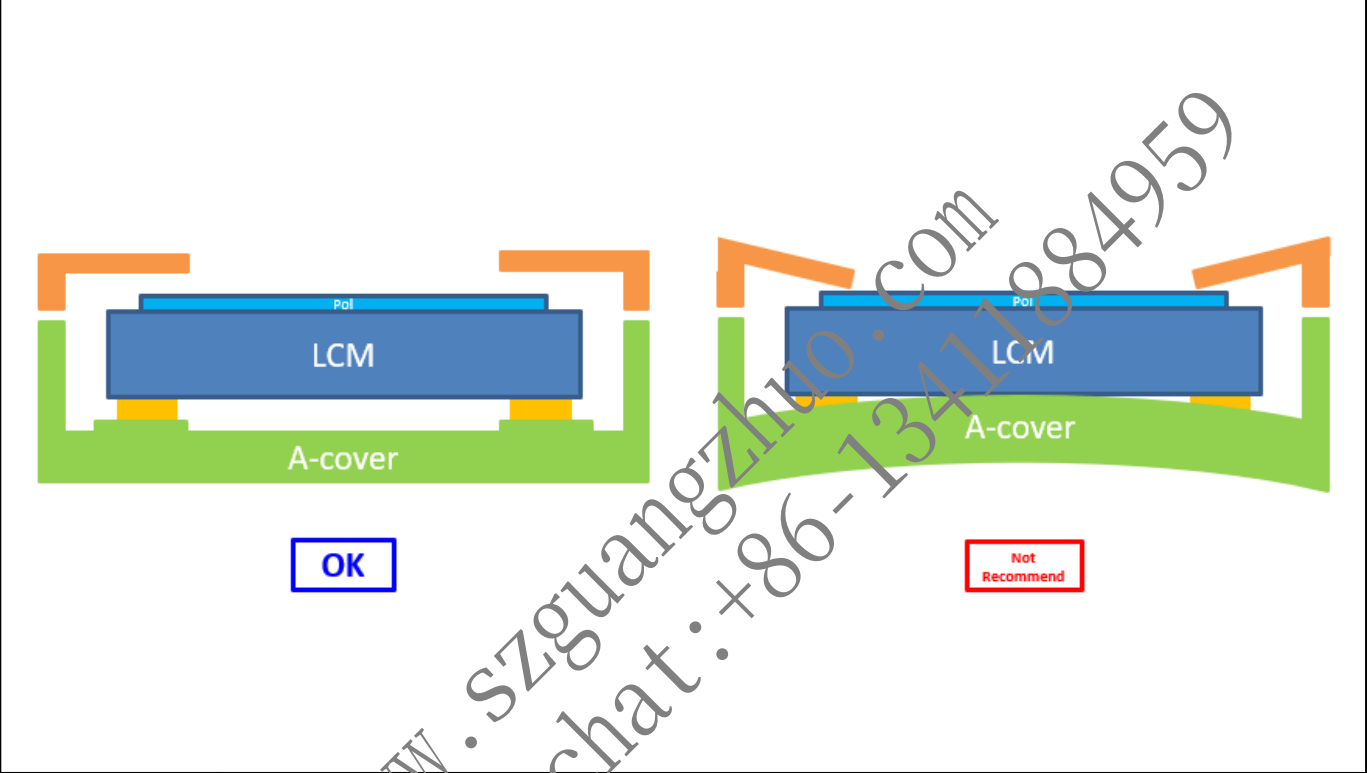
Purpose	The transition surface between keyboard and mouse pad should be smooth and without vertical steps\ too large level steps
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Appendix B: System design Recommendation

System cover reliability

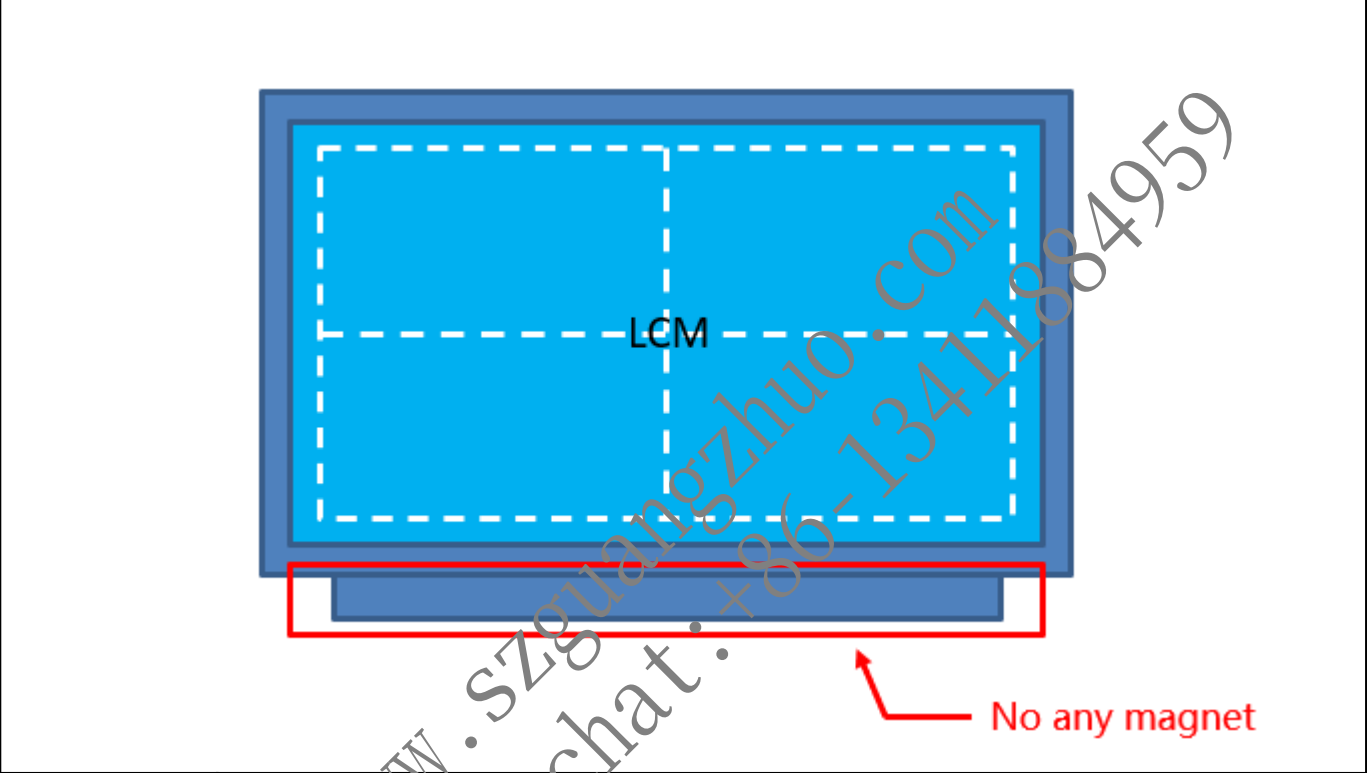


Purpose	1. No interference between system and LCM in assembly process except compressible grounding gaskets 2. The permanent deformation which caused by Reliability test is not allowed to contact LCM
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BOE	PRODUCT GROUP	REV	ISSUE DATE
	Customer Spec	0	2023.11.10

Appendix B: System design Recommendation

A/B-cover near LCD PCBA

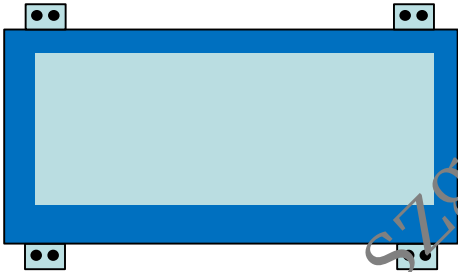


Purpose	There should not been any magnet object close to LCM PCBA, it may cause physical or electricity noise issue
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BOE	PRODUCT GROUP	REV	ISSUE DATE
	Customer Spec	0	2023.11.10

Appendix B: System design Recommendation

A-cover add sponges on Boss side wall



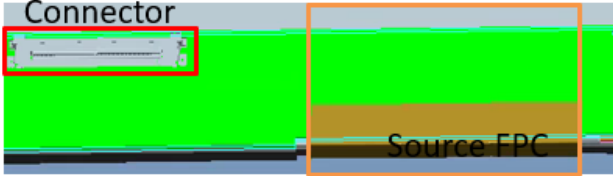
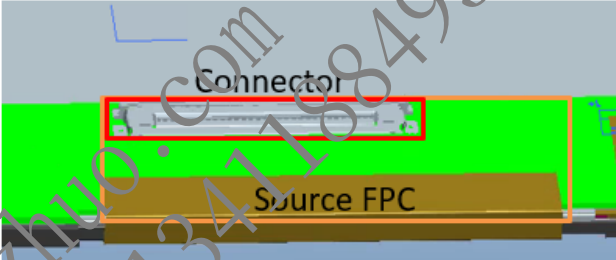
Purpose	BOE would suggest to attach Sponges to the side-wall of the Boss column of A-cover to reduce the risk of panel broken in assembling process.
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Appendix B: System design Recommendation

LCM to A-Cover / sponges z-gap

Y

↑

•

→ X

OK

Not Recommend

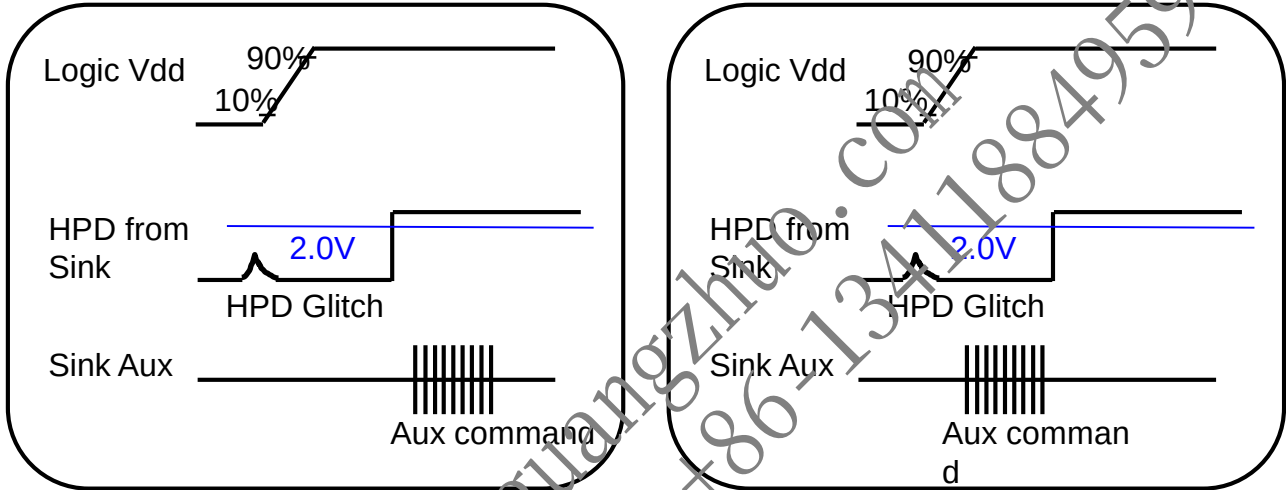
Purpose	Bent type product: The System Connector should not overlap with LCM FPC in X-direction, it may cause FPC lead broken during system connector plug and un-plug process (Panel FPC Bonding location is related to Mask and can not be changed easily)
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SPEC. NUMBER	SPEC. TITLE	PAGE
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BOE	PRODUCT GROUP	REV	ISSUE DATE
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Appendix C : System design Recommendation

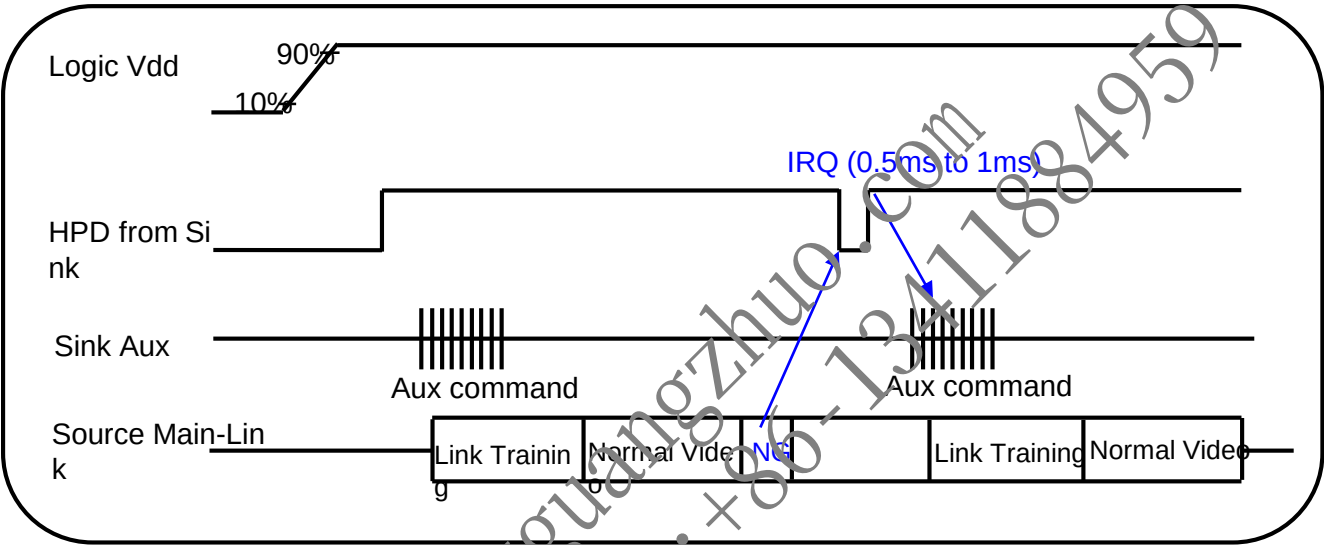
HPD Signal recognition



Purpose	When HPD glitch voltage less than 2.0(V), system signal can't output AUX command data.
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Appendix C : System design Recommendation

HPD Signal Definition IRQ (Interrupt Request)

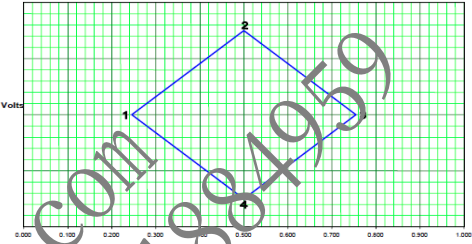
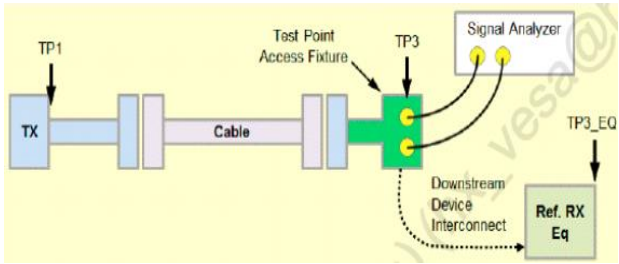


Purpose

When HPD signal low than 0.5ms to 1ms, the source device should check sink status field from the DPCD and take link training again.

Appendix C : System design Recommendation

Main link eye diagram of TP3



Measured TP3 on LCM connector.

Downstream Device Mask at TP3

	UI	Voltage
1	0.246	0
2	0.5	0.075
3	0.755	0
4	0.5	-0.075

	UI	Voltage
1	0.375	0
2	0.5	0.023
3	0.625	0
4	0.5	-0.023

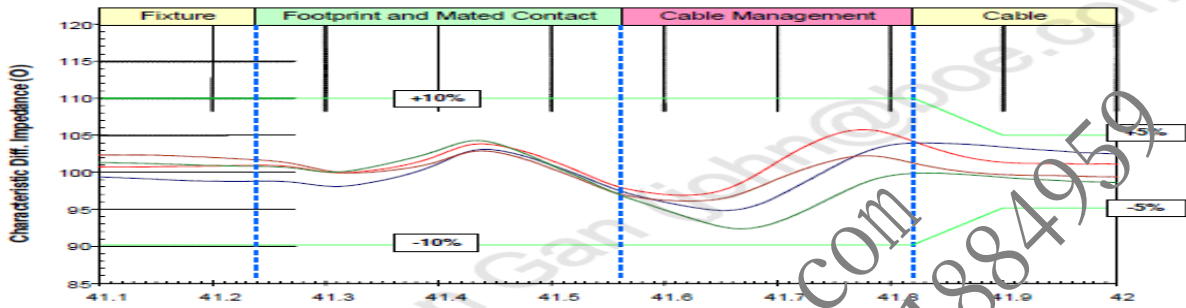
Eye for TP3 at HBR

Eye for TP3 at RBR

Purpose	1. Main Link EYE Diagram should meet TP3 point of VESA. 2. The measure method is through access fixture.
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Appendix C : System design Recommendation

Impedance Profile through a DP Connector



Differential Impedance Profile Measurement Data Example

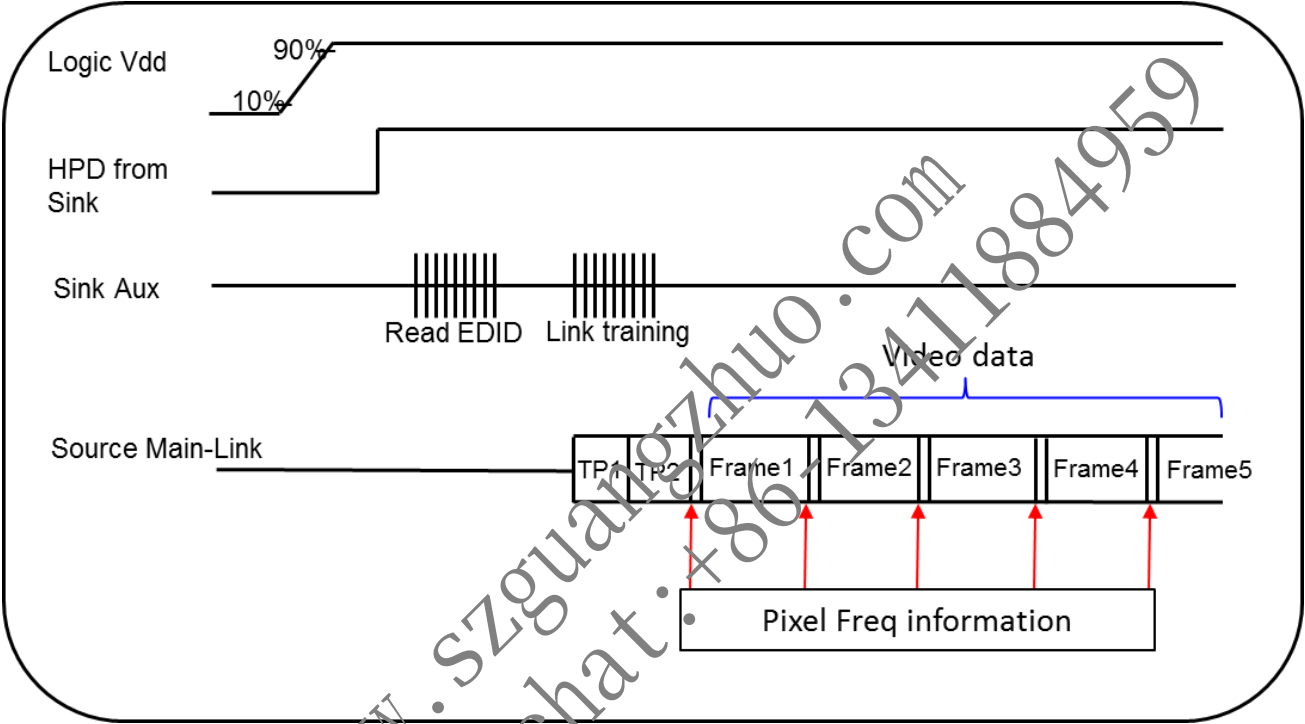
Segment	Differential Impedance Value	Maximum Tolerance
Fixture	100Ω/VESA	±10%
Connector	100Ω/VESA	±10%
Wire management	100Ω/VESA	±10%
Cable	100Ω/VESA	±5%

Impedance Profile Values for Cable Assembly

Purpose	Cable Impedance Profile 100ohm for Cable Assembly
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Appendix C : System design Recommendation

Main Link Pixel Freq information value of MSA data

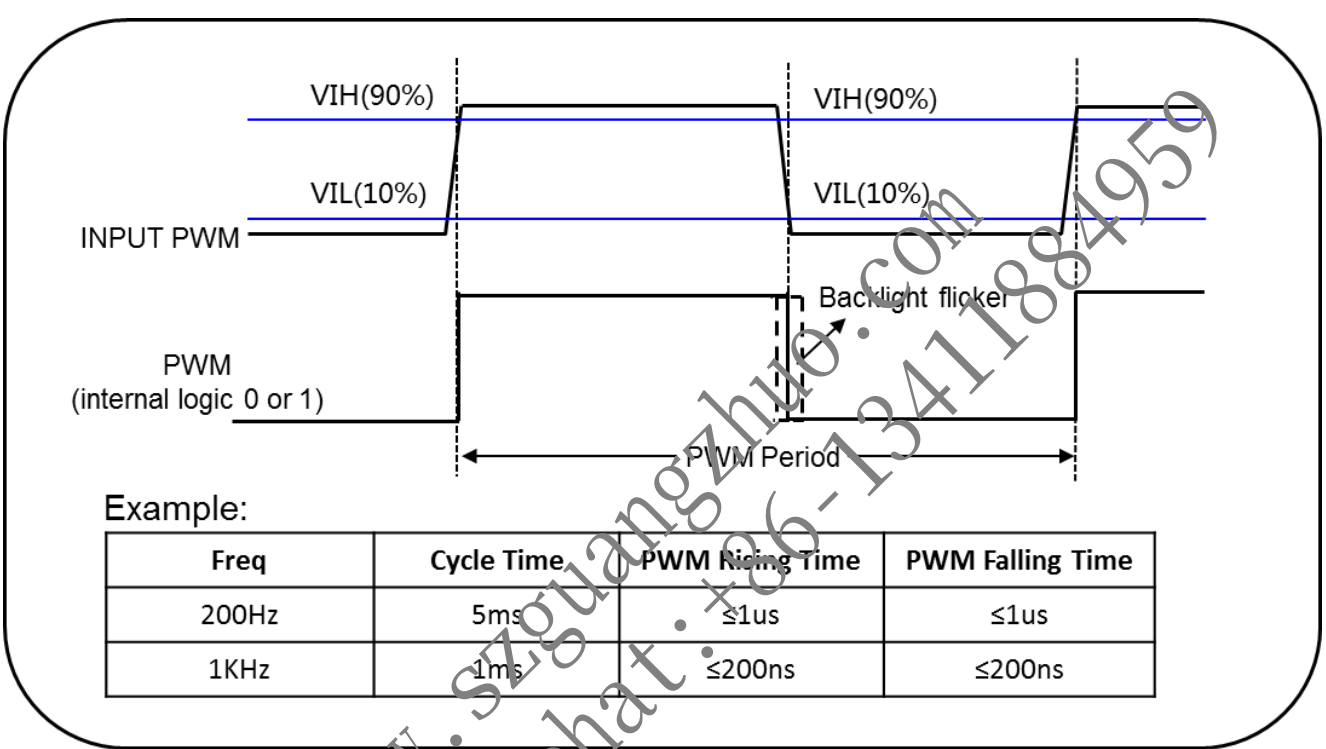


Purpose

- 1. It need to fix pixel freq information value of MSA data output to prevent the initial abnormal pixel freq information value from incoming after power on.
- 2. BOE can read DPCD to check this value. Ex: BIOS is 1.62G , but into windows is 2.7G.

Appendix C : System design Recommendation

System Input PWM Rising/Falling time



Purpose

- LED driver need to calculate the duty cycle of input PWM signal.
- To avoid backlight flicker visible on LCD, system input PWM suggest : PWM rising ≤ 200ppm*cycle time ; PWM falling ≤ 200ppm*cycle time.