Product Specification

AU OPTRONICS CORPORATION

( ) Preliminary Specifications

(✓) Final Specifications

Module	15.6" FHD 16:9 Color TFT-LCD with LED Backlight design
Model Name	B156HAN02.H
H/W	1A
Note ( )	*LED Backlight with driving circuit design*

Customer	**Date**	**Approved by**	**Date**
		Jonken Hsu	*2022/03/28*
Checked & Approved by	**Date**	**Prepared by**	**Date**
		Garfy Lin	2022/03/28
Note: This Specification is subject to change without notice.		**NBBU Marketing Division AU Optronics corporation**	

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
1.0 2022/03/28	All		Final Edition for Customer	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC62368-1 or UL62368-1), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B156HAN02.H is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 FHD, 1920(H) x1080(V) screen and 16.7M colors (RGB 8-bits data driver) with LED backlight driving circuit. All input signals are eDP(Embedded DisplayPort) interface compatible.

B156HAN02.H is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

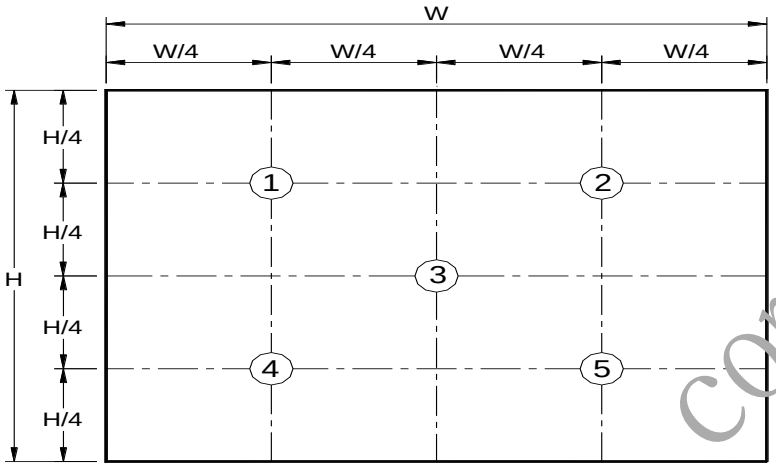
Items	Unit	Specifications			
Screen Diagonal	[mm]	15.6”			
Active Area	[mm]	344.16 X193.59			
Pixels H x V		1920 x 3(RGB) x 1080			
Pixel Pitch	[mm]	0.17925 X 0.17925			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black (AHVA)			
White Luminance (ILED=18mA) **(Note: ILED is LED current)**	[cd/m²]	300 typ. (5 points average) 255 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		1000(typ), 800(min)			
Response Time	[ms]	25 typ / 35 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	4.63 max. (Include Logic and Blu power)			
Weight	[Grams]	310 max.			
Physical Size	[mm]		Min.	Typ.	Max.
		Length	350.36	350.66	350.96
		Width	204.94	205.24	205.54
		Thickness			2.6
Electrical Interface		2 Lane eDP 1.4			
Glass Thickness	[mm]	0.25			
Surface Treatment		Anti-Glare			
Support Color		16.7M colors (RGB 8-bit)			
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	 0 to +50 -20 to +60			
RoHS Compliance		RoHS Compliance			

2.2 Optical Characteristics

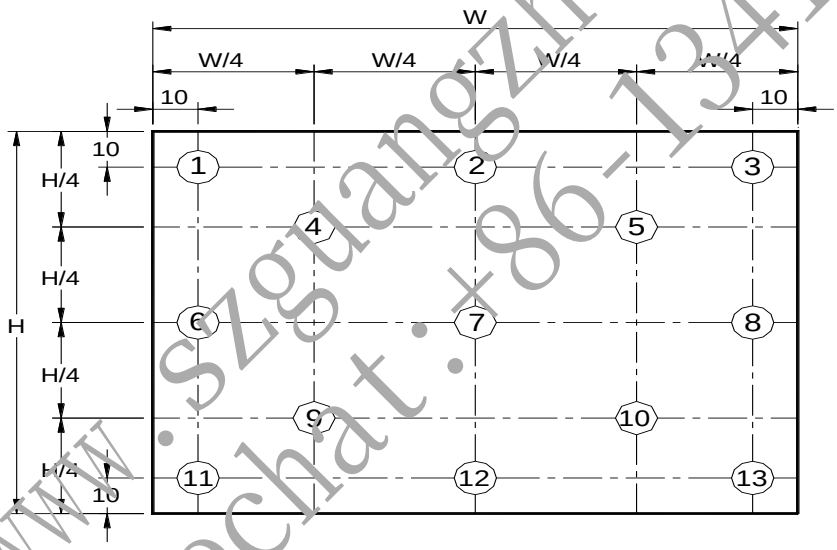
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance ILED=18mA			5 points average	255	300	-	cd/m²	1, 4, 5.
Viewing Angle		θ_R θ_L	Horizontal (Right) CR = 10 (Left)	80 80	89 89	- -	degree	4, 9
		ψ_H ψ_L	Vertical (Upper) CR = 10 (Lower)	80 80	89 89	-		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.4		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.6		2, 3, 4
Contrast Ratio		CR		800	1000	-		4, 6
Cross talk		%			4			4, 7
Response Time		T_{RT}	Rising + Falling	-	25	35	msec	4, 8
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.62	0.653	0.68		4
		Ry		0.30	0.325	0.36		
	Green	Gx		0.26	0.283	0.32		
		Gy		0.59	0.606	0.65		
	Blue	Bx		0.12	0.143	0.18		
		By		0.03	0.058	0.09		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
sRGB		%		95	100	-		
Low Blue Light		K	CCT	5500	-	7000		
		%	TUV	TUV2				10
Gamma Value		-		1.9	2.2	2.5		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



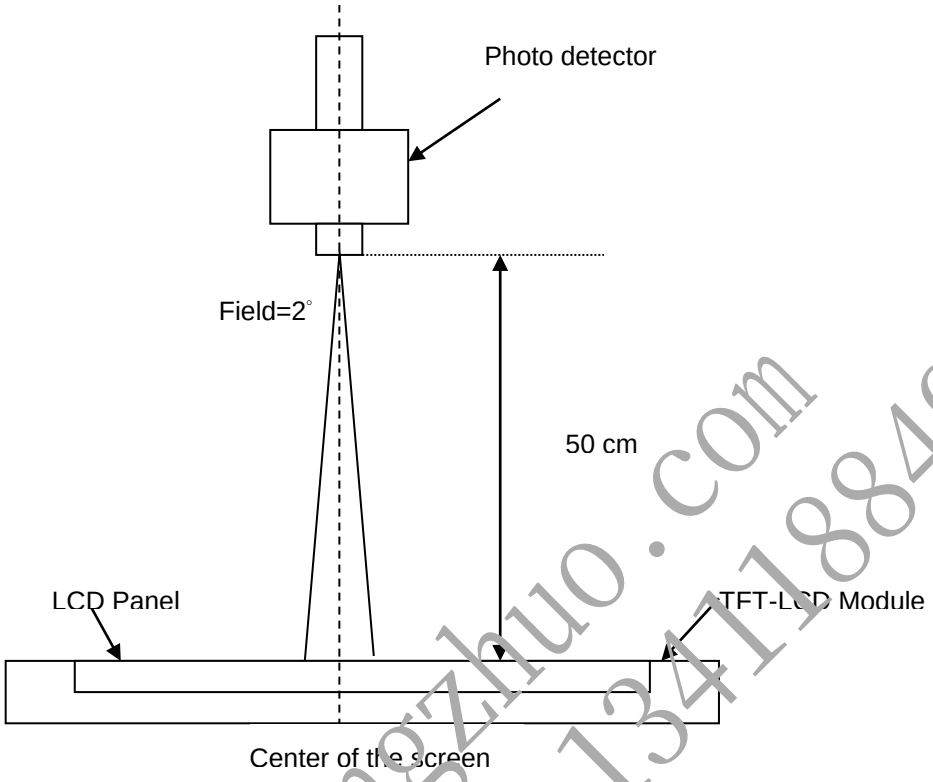
Note 3: The luminance uniformity of 5 and 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

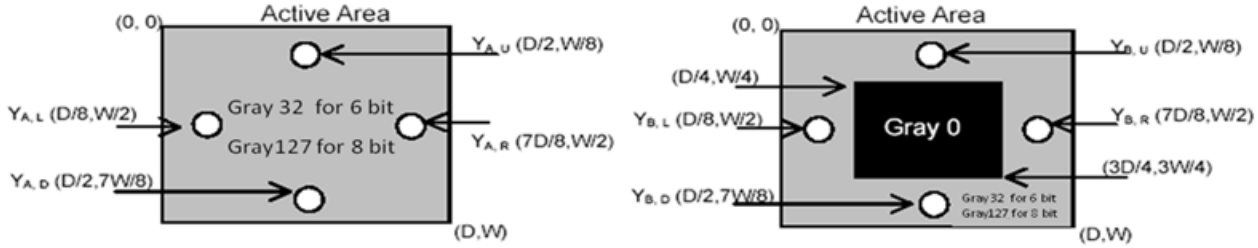
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where

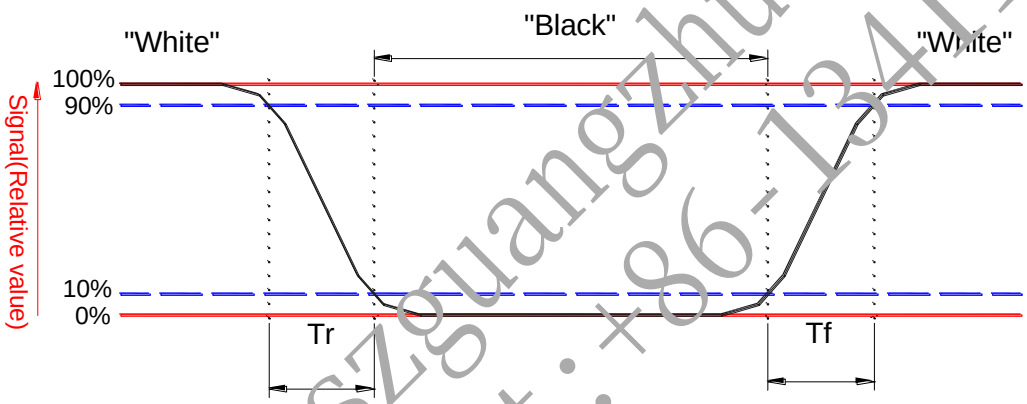
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



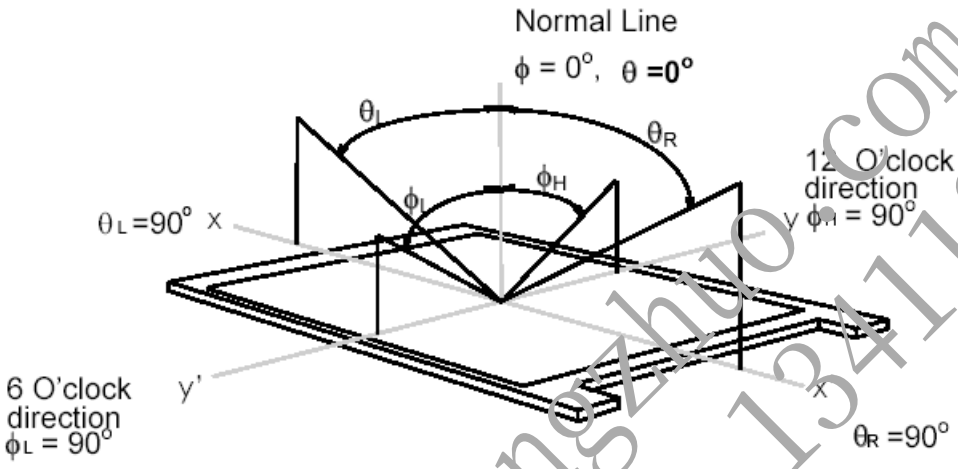
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.

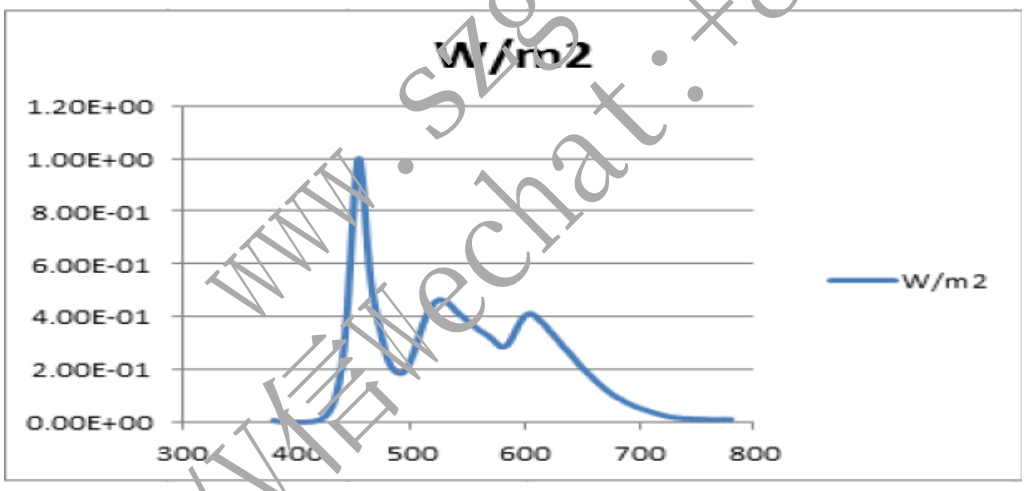


Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.

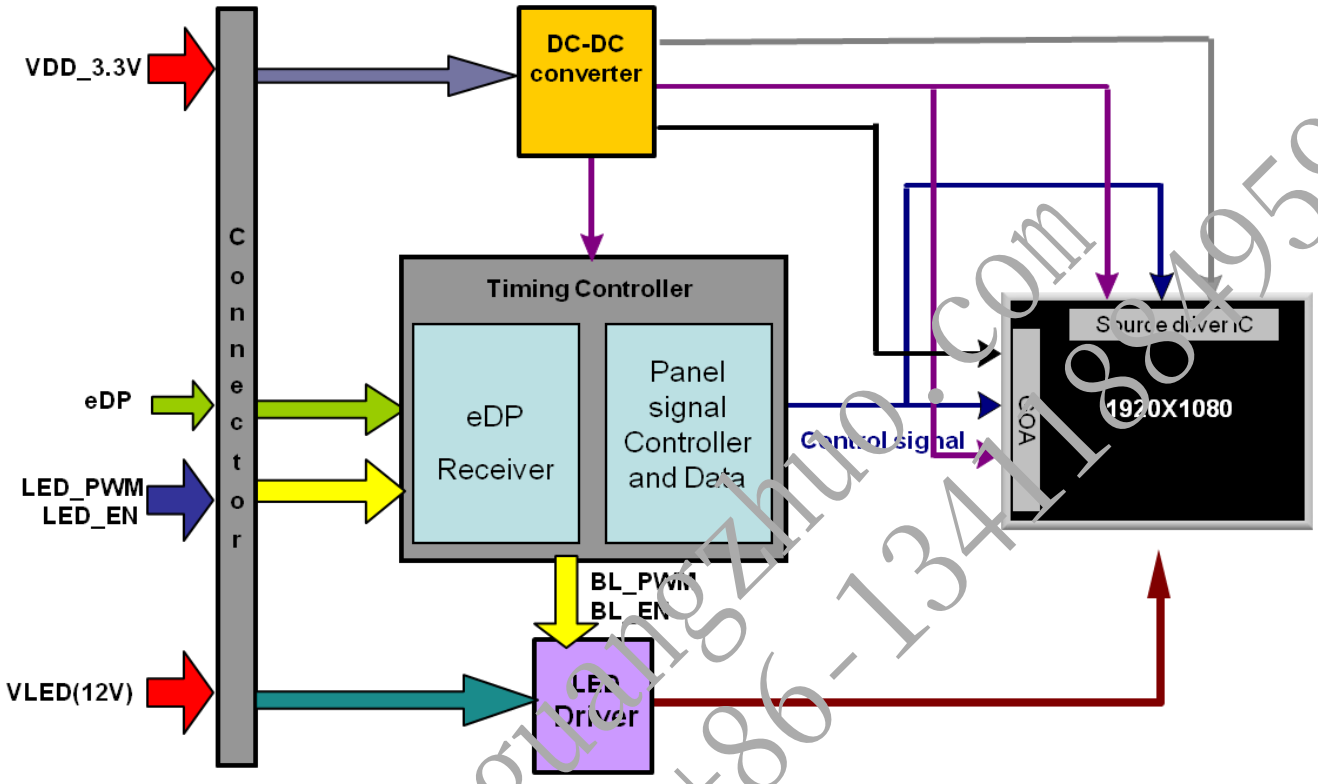


Note 10: Blue Light Ratio: (415nm~455nm)/(400nm~500nm) <50%



3. Functional Block Diagram

The following diagram shows the functional block of the 15.6 inches wide Color TFT/LCD 30 Pin



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operating Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

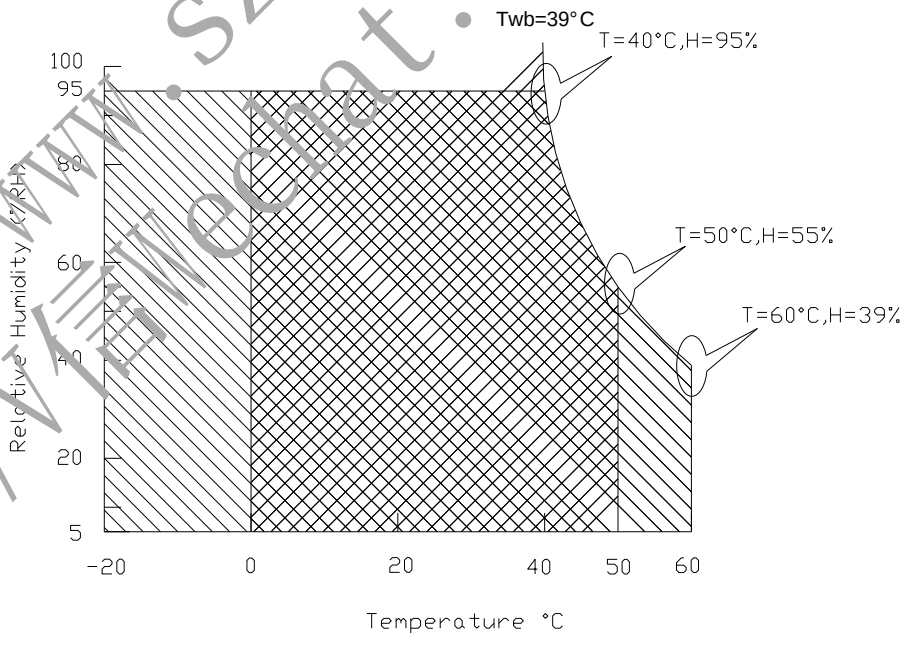
Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).

Note 5: The packing material of system forbid to involve ammonium component

Note 6: The reliability test conditions of system do not exceed the verified conditions of TFT module

Note 7: Be sure the panel test condition do not exceed the component limitation of TFT module(TN Liquid crystal , for example)



Operating Range

Storage Range

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

The power specification are measured under 25℃ and frame frenquency under 60Hz

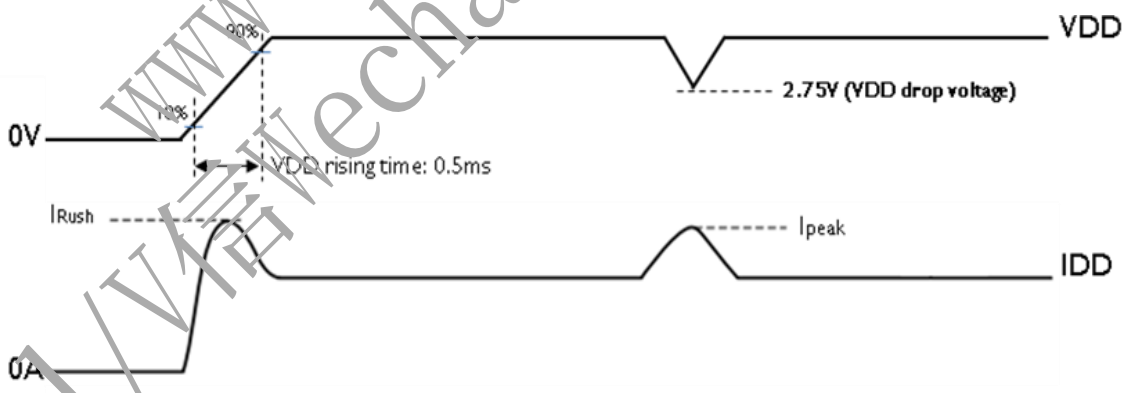
Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	0.75	1.6	[Watt]	Note 1
IDD	IDD Current(RMS)	-	-	533	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
Ipeak	Peak Current			1500	[mA]	Note 2
VDDrp	Allowable Logic/LCD Driver Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : PDD(typ)@ mosaic pattern Maximum Power ; PDD(Max)@ R/G/B pattern Maximum Power

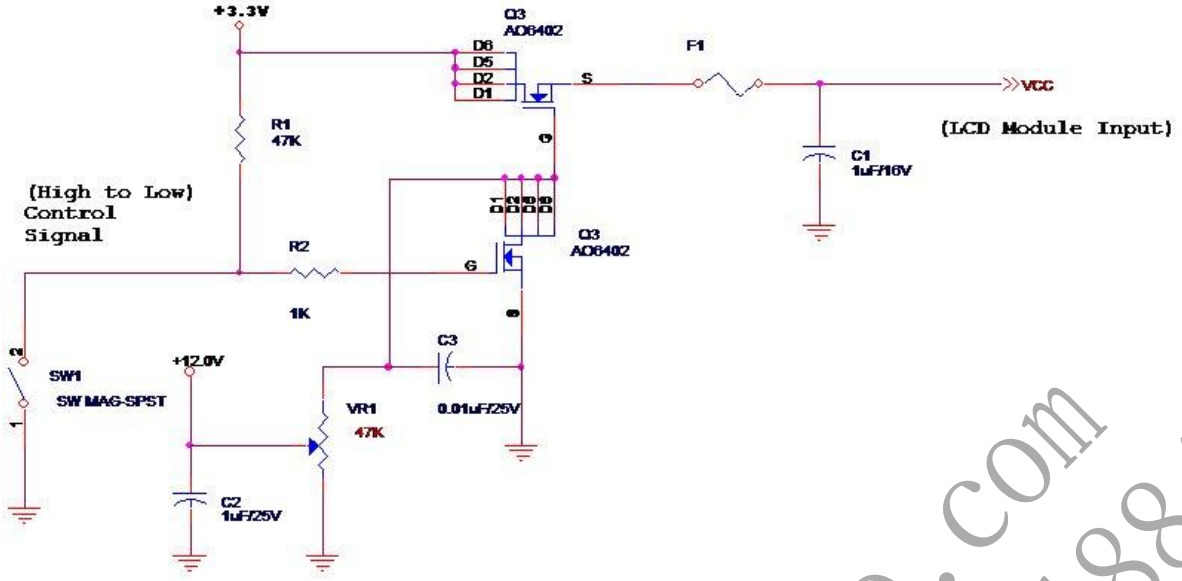
IDD(Max)=PDD(Max) / VDD(Min)

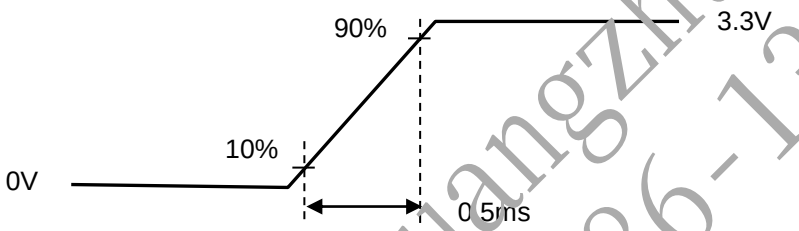
Note 2：
a. IRush: VDD measured rising timing @ 0.5ms

b. IPeak: VDD drop Voltage ≧ 2.75V at this Ipeak current



c. IRush Measure Condition:





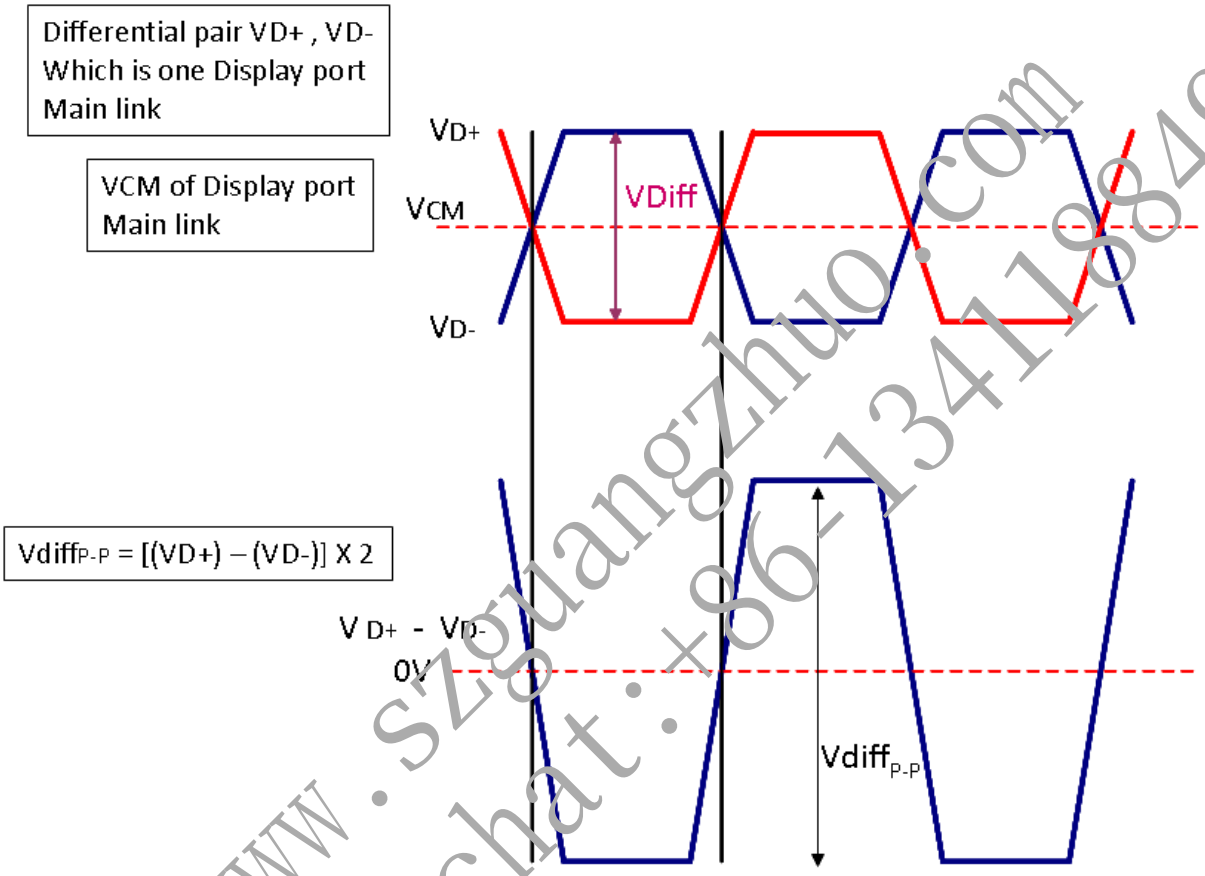
Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

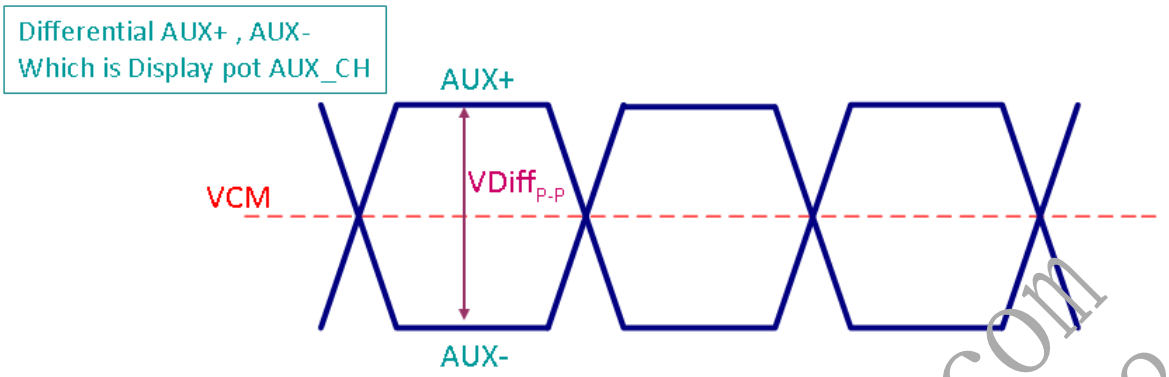
Display Port main link signal:



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	150		1320	mV

Follow as VESA display port standard V1.4

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff P-P	AUX Peak-to-peak Voltage at a receiving Device	270		800	mV

Fallow as VESA display port standard V1.3

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25		3.6	V

Fallow as VESA display port standard V1.3

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	3.88	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25℃), Note 2 IL=20 mA

Note 1: Calculator value for reference P_{LED} = VF (Normal Distribution) * IF (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

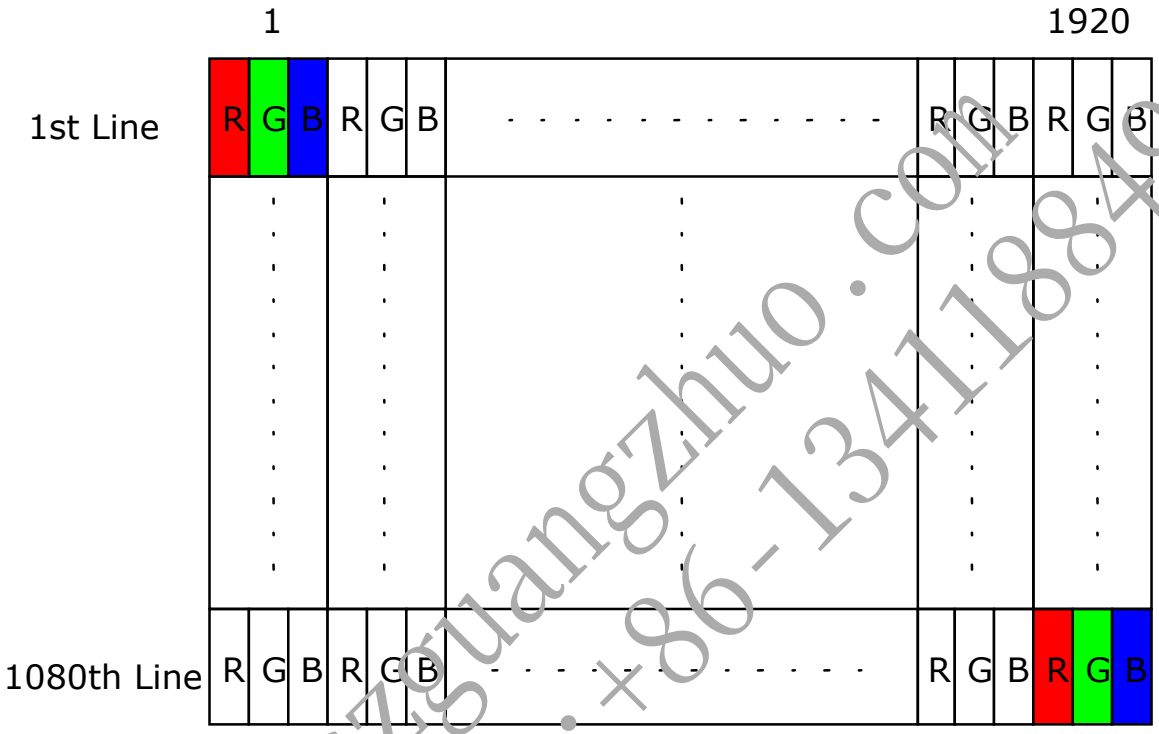
Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	5.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃) Note 3
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

Note 3 : BL Control Mode is DC diming mode.

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

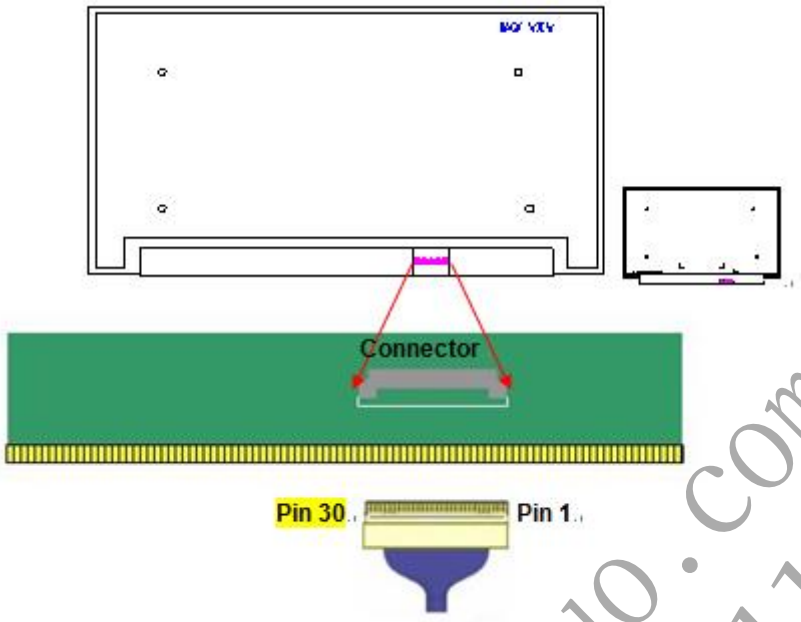
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	IPEX 20765-030E-11A or compatible
Mating Housing/Part Number	IPEX 20704-030T-13 or compatible

6.2.2 Pin Assignment

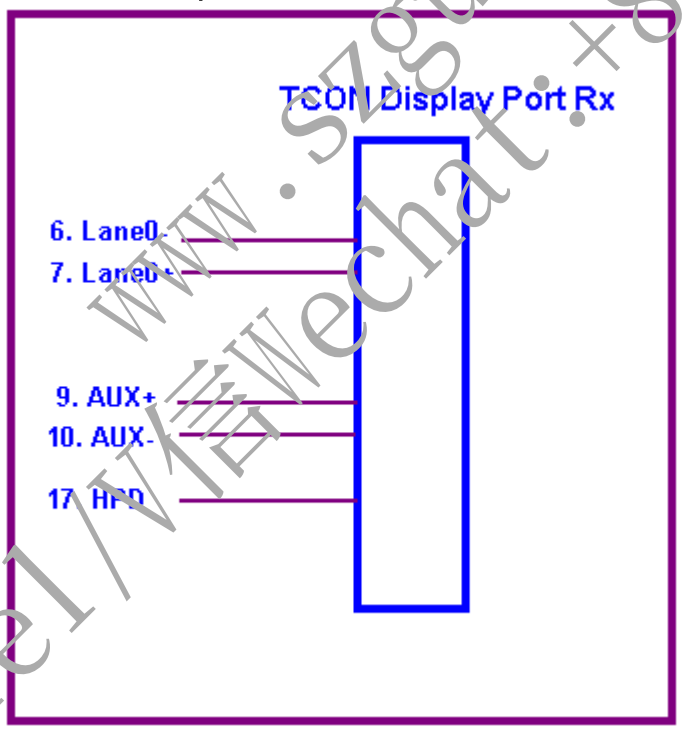
eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO	Symbol	Function
1	NC	No Connect
2	H_GND	High Speed Ground
3	Lane1_N (2 Lane)	Complement Signal Link Lane 1 (2 Lane)
4	Lane1_P (2 Lane)	True Signal Link Lane 1 (2 Lane)
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	LCD_Self_Test	LCD Panel Self Test Enable
15	LCD GND	LCD logic and driver ground
16	LCD GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	BL_GND	Backlight_ground
19	BL_GND	Backlight_ground
20	BL_GND	Backlight_ground
21	BL_GND	Backlight_ground
22	BL_Enable	Backlight On / Off
23	BL PWM DIM	System PWM signal Input
24	NC	Reverse for AUO TEST only
25	NC	Reverse for AUO TEST only
26	BL_PWR	Backlight power (5V~21V)
27	BL_PWR	Backlight power (5V~21V)
28	BL_PWR	Backlight power (5V~21V)
29	BL_PWR	Backlight power (5V~21V)
30	NC	No Connect



Note1: Start from right side.

Note2: Input signals shall be low or High-impedance state when VDD is off.
Internal circuit of **eDP inputs** are as following.



6.3 Interface Timing

6.3.1 Timing Characteristics

For normal display, interface timings should match the 1920x1080 /60Hz manufacturing guide line timing.

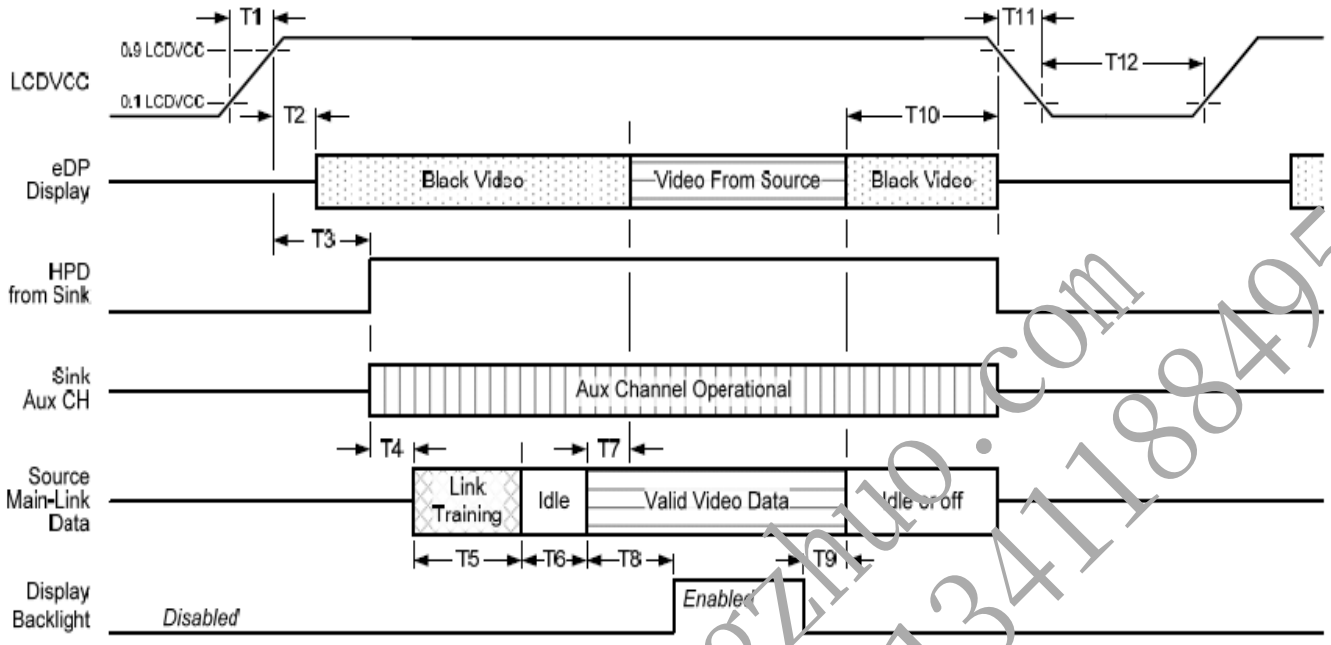
Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		1/ T_{Clock}	94	141	150	MHz
Vertical	Period	T_V	1118	1118	1080+A	T_{Line}
Section	Active	T_{VD}	1080			
	Blanking	T_{VB}	38	38	A	
Horizontal	Period	T_H	2100	2100	1920+B	T_{Clock}
Section	Active	T_{HD}	1920			
	Blanking	T_{HB}	180	180	B	

Note 1 : The above is as optimized setting

Note 2 : The maximum clock frequency = (1920+B)*(1080+A)*60 < 150 MHz

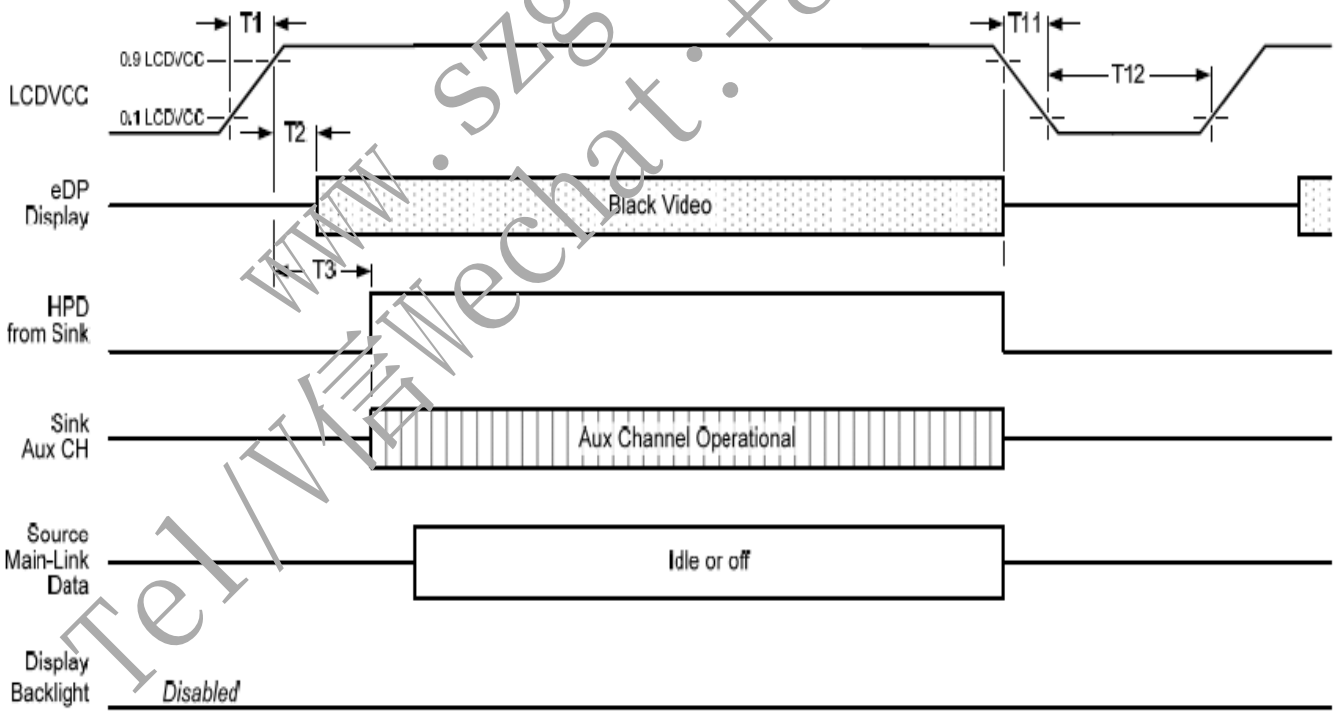
6.4 Power ON/OFF Sequence

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	poser rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		80ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		80ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize
T5	link training duration	source				dependent on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	Max allows for source frame synchronization.
T8	delay from valid video data from source to backlight enable	source				max allows sink validate video data and timing
T9	delay from backlight disable to end of valid video data	source				source must assure display video is stable
T10	delay from end of valid video data from source to power off	source	50ms		500ms	
T11	power rail fail time, 90% to 10%	source			10ms	
T12	power off time	source	500ms			

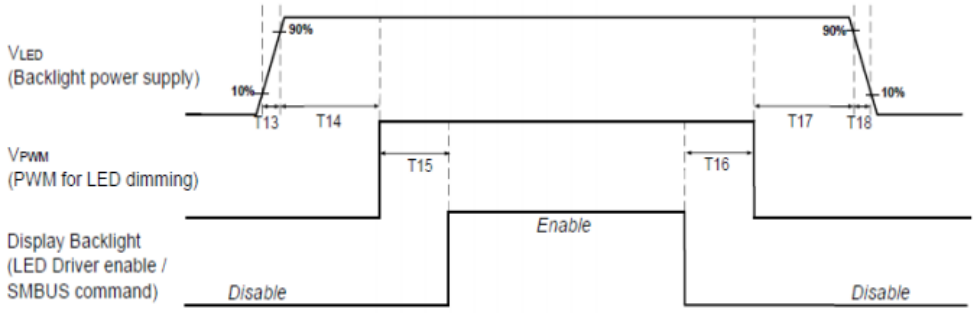
Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max) when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Note 4:T8>T7

Display Port panel B/L power sequence timing parameter:

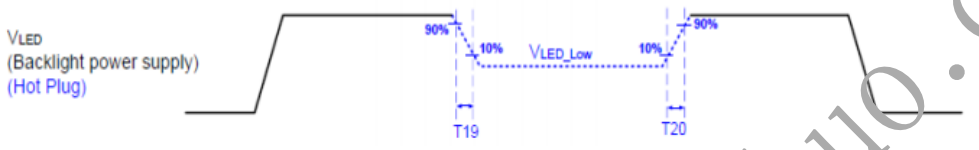


	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	0	-
T16	0	-
T17	10	-
T18	0.5	0
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM} = 1/PWM Frequency

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 35%RH, 300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 150h	
Thermal Shock Test	Ta=-20℃ to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

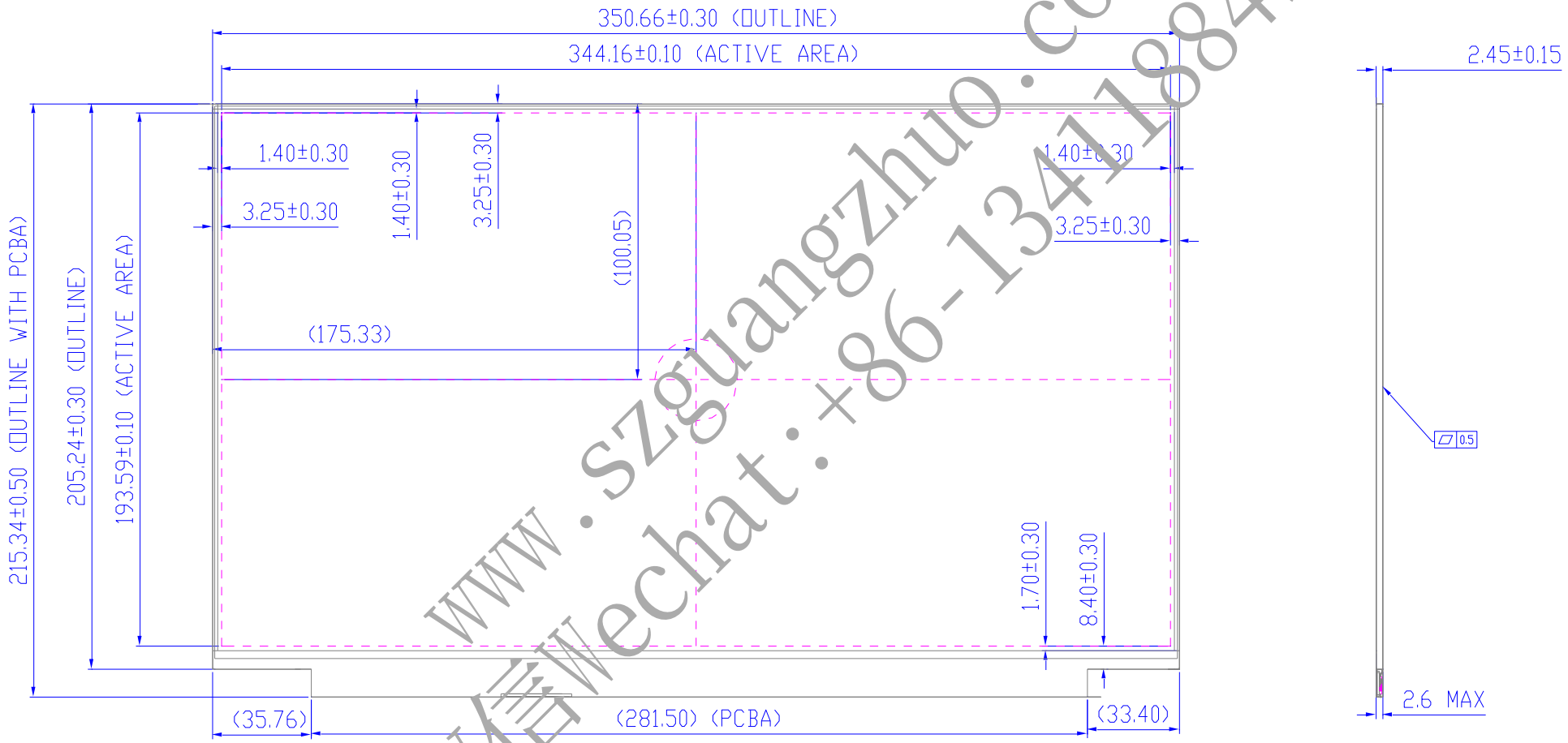
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable. No data lost. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

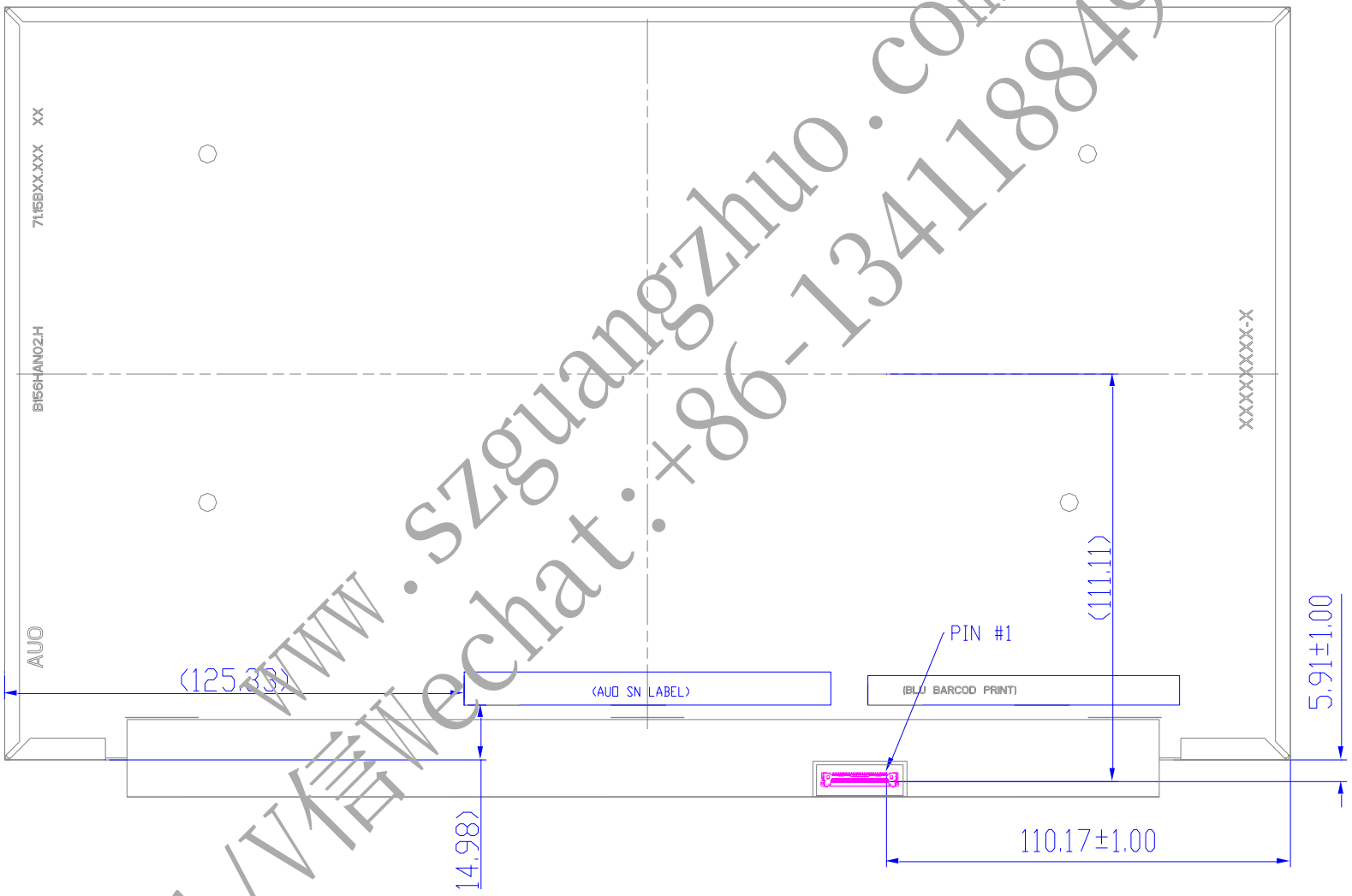
8. Mechanical Characteristics

8.1 LCM Outline Dimension

8.1.1 Standard Front View



8.1.2 Standard Rear View



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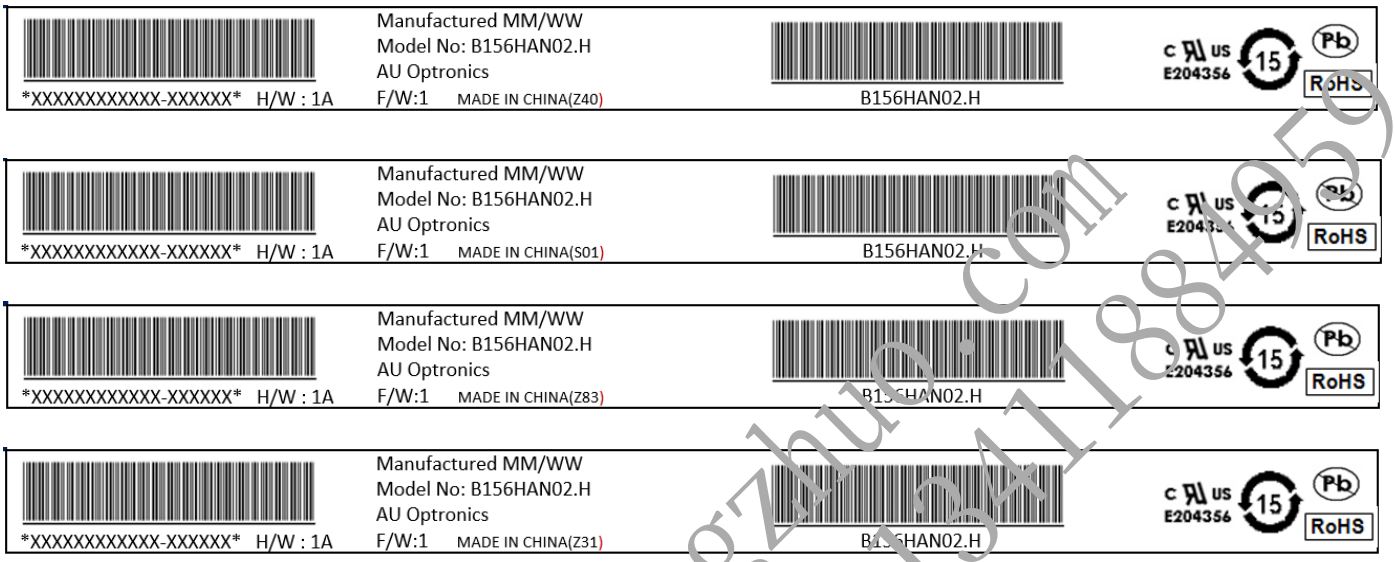
9. Shipping and Package

9.1 Shipping Label Format

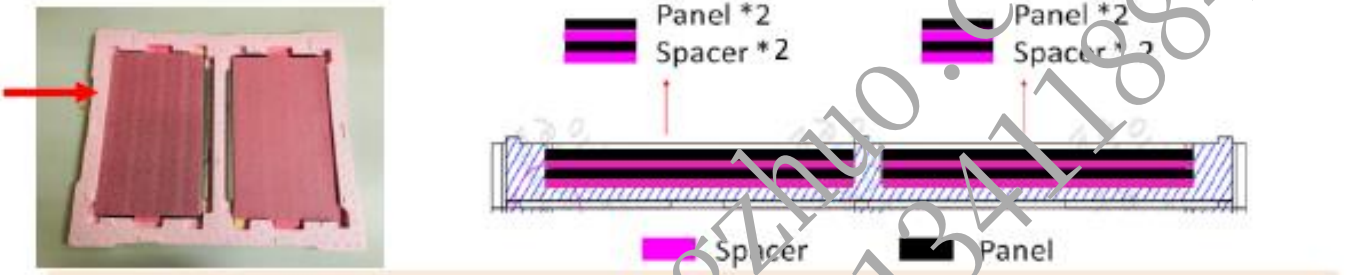


9.2 Carton Package

1. 不撕膜：
將把手貼在 P 板側的右下角

2. 左右底部先放入 1pcs spacer

3. 左右各放入 1pcs panel
(PCBA 側朝向側，可視區朝上)



4. 1 tray 總共放 4pcs panel & 4 pcs spacer (1 穴放 2pcs panel + 2pcs spacer)

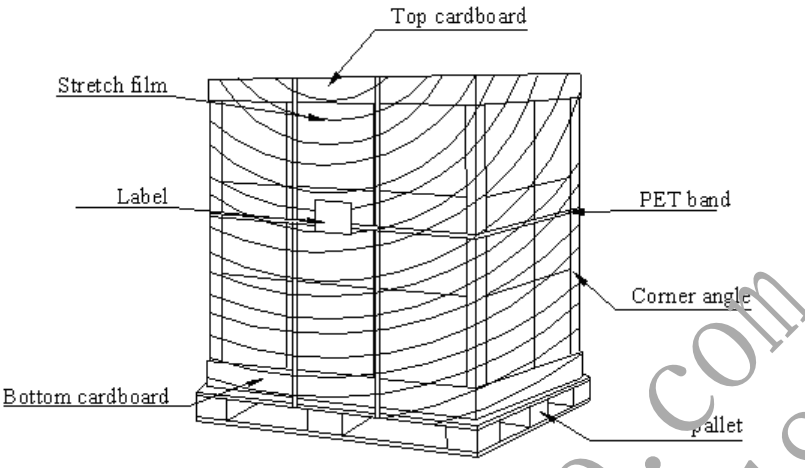
5. Tray 堆疊
- Panel 共 40 片,最上面第 11 個 tray 是空的

6. 打上束帶&裝入靜電袋
(圖面為示意)

7. 以膠帶封袋口&裝入紙箱封口
(圖面為示意)

8. 用透明膠帶以 H 型封箱

9.3 Shipping Package of Palletizing Sequence



10. Appendix:

10.1 EDID Description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01	Header	FF	11111111	255	
02	Header	FF	11111111	255	
03	Header	FF	11111111	255	
04	Header	FF	11111111	255	
05	Header	FF	11111111	255	
06	Header	FF	11111111	255	
07	Header	00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	A3	10100011	163	
0B	Product Code	B0	10110000	176	
0C	32-bit ser #	00	00000000	0	
0D	ID S/N - option	00	00000000	0	
0E	ID S/N - option	00	00000000	0	
0F	ID S/N - option	00	00000000	0	
10	Week of manufacture	00	00000000	0	
11	Year of manufacture	20	00100000	32	
12	EDID Structure Ver.	01	00000001	1	
13	EDID Revision #	04	00000100	4	
14	Video input def. (digital I/P, non-TMDS, CRGB)	A5	10100101	165	
15	Max H image size (rounded to cm)	22	00100010	34	
16	Max V image size (rounded to cm)	13	00010011	19	
17	Display Gamma (=(gamma*100)-100)	78	01111000	120	
18	Feature support (no DPMS, Active OFF, RGB, tmg Blk#1)	02	00000010	2	
19	Red/green low bits (Lower 2:2:2:2 bits)	59	01011001	89	
1A	Blue/white low bits (Lower 2:2:2:2 bits)	B5	10110101	181	
1B	Red x (Upper 8 bits)	A7	10100111	167	
1C	Red y/ highER 8 bits	53	01010011	83	
1D	Green x	48	01001000	72	
1E	Green y	9B	10011011	155	
1F	Blue x	24	00100100	36	
20	Blue y	0E	00001110	14	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	

27	Standard timing #1	01	00000001	1	
28	Standard timing #2	01	00000001	1	
29	Standard timing #2	01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B	Standard timing #3	01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D	Standard timing #4	01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F	Standard timing #5	01	00000001	1	
30	Standard timing #6	01	00000001	1	
31	Standard timing #6	01	00000001	1	
32	Standard timing #7	01	00000001	1	
33	Standard timing #7	01	00000001	1	
34	Standard timing #8	01	00000001	1	
35	Standard timing #8	01	00000001	1	
36	Pixel Clock/10000 LSB	14	00010100	20	
37	Pixel Clock/10000 USB	37	00110111	55	
38	Horz active Lower 8bits	80	10000000	128	
39	Horz blanking Lower 8bits	B4	10110100	180	
3A	HorzAct:HorzBlnk Upper 4:4 bits	70	01110000	112	
3B	Vertical Active Lower 8bits	38	00111000	56	
3C	Vertical Blanking Lower 8bits	26	00100110	38	
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	40	01000000	64	
3E	HorzSync. Offset	6C	01101100	108	
3F	HorzSync.Width	30	00110000	48	
40	VertSync.Offset : VertSync.Width	AA	10101010	170	
41	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0	
42	Horizontal Image Size Lower 8bits	58	01011000	88	
43	Vertical Image Size Lower 8bits	C2	11000010	194	
44	Horizontal & Vertical Image Size (upper 4:4 bits)	10	00010000	16	
45	Horizontal Border (zero for internal LCD)	00	00000000	0	
46	Vertical Border (zero for internal LCD)	00	00000000	0	
47	Signal (non-intr, norm, no stero, sep sync, neg pol)	18	00011000	24	
48	Pixel Clock/10000 LSB	00	00000000	0	
49	Pixel Clock/10000 USB	00	00000000	0	
4A	Horz active Lower 8bits	00	00000000	0	
4B	Horz blanking Lower 8bits	0F	00001111	15	
4C	HorzAct:HorzBlnk Upper 4:4 bits	00	00000000	0	
4D	Vertical Active Lower 8bits	00	00000000	0	
4E	Vertical Blanking Lower 8bits	00	00000000	0	
4F	Vert Act : Vertical Blanking (upper 4:4 bit)	00	00000000	0	
50	HorzSync. Offset	00	00000000	0	
51	HorzSync.Width	00	00000000	0	
52	VertSync.Offset : VertSync.Width	00	00000000	0	

53	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0	
54	Horizontal Image Size Lower 8bits	00	00000000	0	
55	Vertical Image Size Lower 8bits	00	00000000	0	
56	Horizontal & Vertical Image Size (upper 4:4 bits)	00	00000000	0	
57	Horizontal Border (zero for internal LCD)	00	00000000	0	
58	Vertical Border (zero for internal LCD)	00	00000000	0	
59	Signal (non-intr, norm, no stero, sep sync, neg pol)	20	00100000	32	
5A	descriptor #3	00	00000000	0	
5B	Reserved for definition	00	00000000	0	
5C	Reserved for definition	00	00000000	0	
5D	ASCII String	FE	11111110	254	
5E	Reserved for definition	00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62	Reserved for definition	0A	00001010	10	
63	Reserved for definition	20	00100000	32	
64	Reserved for definition	20	00100000	32	
65	Reserved for definition	20	00100000	32	
66	Reserved for definition	20	00100000	32	
67	Reserved for definition	20	00100000	32	
68	Reserved for definition	20	00100000	32	
69	Reserved for definition	20	00100000	32	
6A	Reserved for definition	20	00100000	32	
6B	Reserved for definition	20	00100000	32	
6C	Reserved for definition	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E	Reserved for definition	00	00000000	0	
6F	Reserved for definition	FE	11111110	254	
70	Reserved for definition	00	00000000	0	
71	Manufacture P/N	42	01000010	66	B
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	35	00110101	53	5
74	Manufacture P/N	36	00110110	54	6
75	Manufacture P/N	48	01001000	72	H
76	Manufacture P/N	41	01000001	65	A
77	Manufacture P/N	4E	01001110	78	N
78	Manufacture P/N	30	00110000	48	0
79	Manufacture P/N	32	00110010	50	2
7A	Manufacture P/N	2E	00101110	46	.
7B	Manufacture P/N	48	01001000	72	H
7C	Reserved for definition	20	00100000	32	
7D	Reserved for definition	0A	00001010	10	
7E	Extension Flag	00	00000000	0	

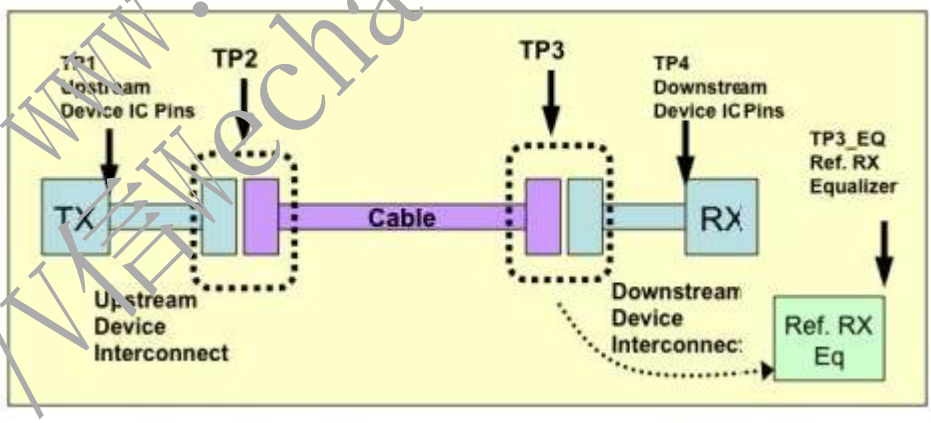
10.2 Notes

DPCD Ver.	sDRRS	DCR	DMRRS	PSR	LRR	LRR Frame rate	MBO	VESA DSC
1.4	Off	Off	Off	off	NA	NA	Off	Off

MSO	G-Sync	Free-Sync	Adaptive Sync	HDR Tier	HDR Ver.	Dimming
Off	Off	Off	Off	NA	NA	PWM

ASSR	Auto ASSR (Tcon support)	VSC/SDP (HDR / eDP 1.4up)	Dream color + Flash lock	WP (Flash lock)
Off	Off	Off	Off	Off

1) The height of cell tape no higher than top polarizer 3.0mm
2) LED Driving Solution: Minimum change scale duty of the PWM is 0.1% @PWM frequency 200Hz.
3) When twisting or pressing LCD module, it may cause unexpected acoustic noises or sounds.
4) Maximum value of "Peak current" is as same as "Inrush current" in Electrical Characteristics (Power Specification)
5) $VDiff_{P-P}$ (Peak-to-peak Voltage at a receiving Device) follow as VESA display port standard (test point, TP3, is on panel's PCBa)



6) Suggest ODMs do not use any parts that contain the ingredient of related Ammonium > 5ppb, and other ingredients, if any.
7) Suggest ODMs do not interfere with panel after system assembly in order to avoid possible mura, yellow spot, light leakage, water ripple or side defects by mechanical stress test.
8) For LCM display (thickness >= 2.6mm), the height of PCBa/FPC floating area 0.5mm max (compressible).
9) For total solution display (thickness >= 2.6mm), the height of PCBa/FPCa/FPC floating area 0.7mm max (compressible).