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NV140FHM-N4T

HW:V8.0

Final Product Specification

Rev. 0

BOE Optoelectronics Technology Co., Ltd

SPEC. NUMBER

S8-65-8C-245

PRODUCT GROUP

TFT-LCD

Rev.

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REVISION HISTORY

() Preliminary Specification

(√) Final Specification

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P0	62	Preliminary Specification	2019.6.17	GaoXueqiang
P1	62	ME outline, Label update, EE value update	2019.7.11	GaoXueqiang
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1.0 GENERAL DESCRIPTION

1.1 Introduction

NV140FHM-N4T V8.0 is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 14.0 inch diagonally measured active area with Full-HD resolutions (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 262k(6bit) colors and color gamut 45%. The TFT-LCD panel used for this module is a low reflection and higher color type. Therefore, this module is suitable for Notebook PC. The LED driver for back-light driving is built in this model.

All input signals are eDP1.2 interface compatible.

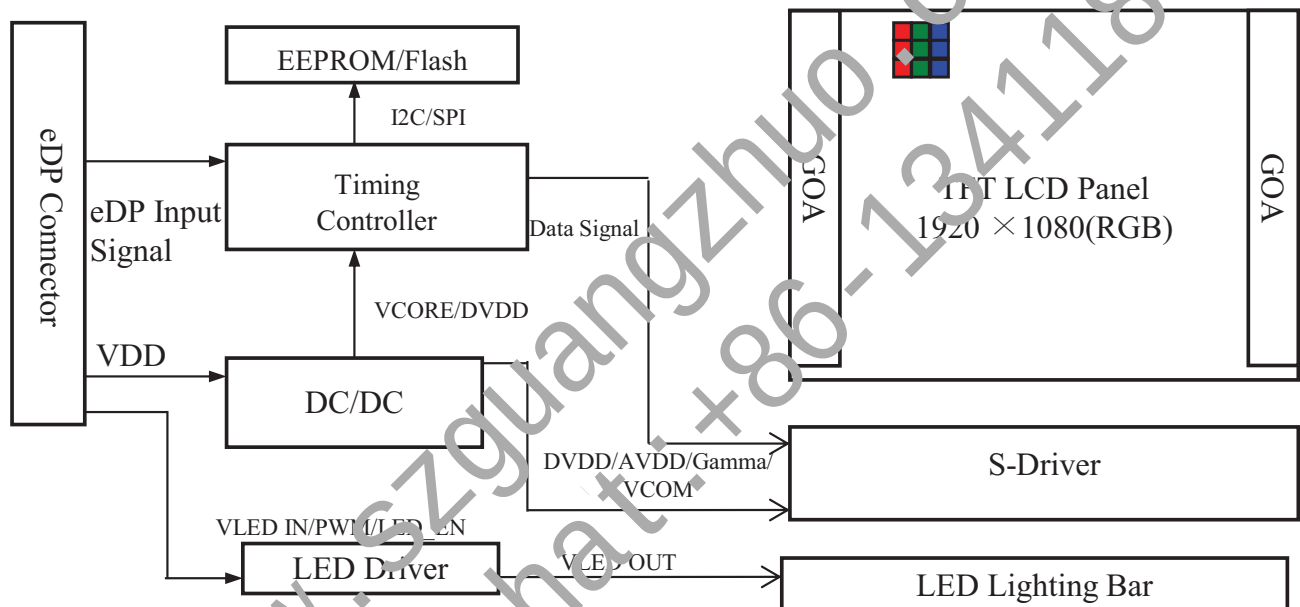


Figure 1. Drive Architecture

1.2 Features

- 2 lane eDP interface with 2.7Gbps link rates
- Thin and light weight
- 262k(6bit) color depth, color gamut 45%
- Single LED lighting bar (Bottom side/Horizontal Direction)
- Data enable signal mode
- Green product (RoHS & Halogen free product)
- On board LED driving circuit
- Low driving voltage and low power consumption
- On board EDID chip
- DPCD Version 1.1
- Function : SDRRS

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1.3 Application

- Notebook PC (Wide type)

1.4 General Specification

The followings are general specifications at the model NV140FHM-N4T V8.0. (listed in Table 1)

<Table 1. General Specifications>

Parameter	Specification	Unit	Remarks
Active area	309.312 (H) × 173.988 (V)	mm	
Number of pixels	1920 (H) × 1080 (V)	pixels	
Pixel pitch	161.1(H) × 161.1(V)	um	
Pixel arrangement	RGB Vertical stripe		
Display colors	262k(6bit)		
Color gamut	45%		
Display mode	Normally Black		
Dimensional outline	315.812 ± 0.3 (H) * 186.068 ± 0.3 (V) (W/O PCB) * 3.0 (Max) 315.812 ± 0.3 (H) * 186.068 ± 0.3 (V) (W/PCB) * 5.0 (Max)	mm	
Weight	300 (max)	g	
Surface treatment	Anti-Glare		
Surface hardness	3H		
Back-light	Bottom edge side, 1-LED lighting bar type		Note 1
Power consumption	P _D : 0.7(Max)	W	@Mosaic
	P _{BL} : 1.85(max)	W	
	P _{Total} : 2.55(Max)	W	@Mosaic

Notes : 1. LED Lighting Bar (36*LED Array)

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2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Absolute Maximum Ratings >

 $T_a = 25 \pm 2^\circ\text{C}$

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-0.3	4.0	V	Note 1
eDP input Voltage	V_{eDP}	0	2.0	V	
Logic Supply Voltage	V_{IN}	$V_{SS}-0.3$	$V_{DD}+0.3$	V	
Operating Temperature	T_{OP}	0	+50	$^\circ\text{C}$	Note 2
Storage Temperature	T_{ST}	-20	+60	$^\circ\text{C}$	

Notes :

1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.

2. Temperature and relative humidity range are shown in the figure below.

95% RH Max. ($40^\circ\text{C} \geq T_a$) Maximum wet - bulb temperature at 39°C or less. ($T_a > 40^\circ\text{C}$) No condensation.

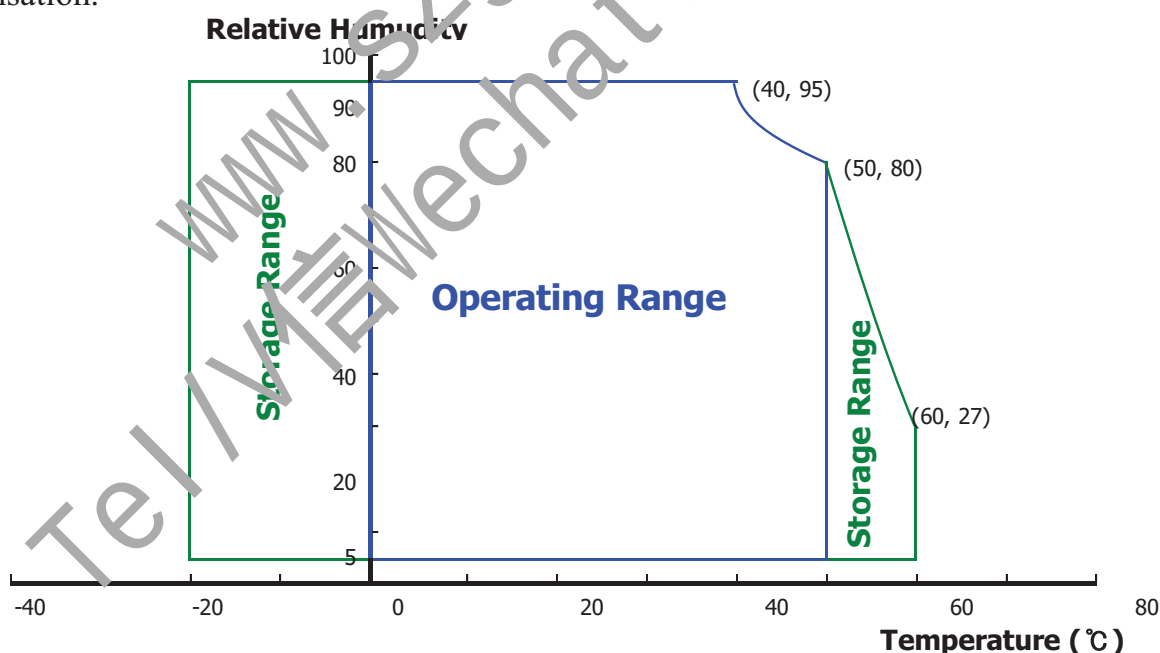


Figure 2. Temperature and Relative Humidity Range

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3.0 ELECTRICAL SPECIFICATIONS**3.1 Electrical Specifications**

< Table 3. Electrical Specifications >

Ta=25+/-2°C

Parameter		Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V _{DD}	3.0	3.3	3.6	V	Note 1
Permissible Input Ripple Voltage	V _{RF}	-10% VDD	-	+10% VDD	V	@ V _{DD} = 3.3V
Power Supply Inrush Current	I _{rush}	-	-	2	A	Note3
Power Supply Current	Mosaic	I _{DD}	-	212	mA	Note 1
	RGB		-	394	mA	
Power Consumption	Mosaic	P _M	-	0.7	W	
	RGB	P _{RGB}	-	1.3	W	
	BLU	P _{BL}	-	1.85	W	Note 2
	Total	P _{Total}	-	2.55	W	@Mosaic

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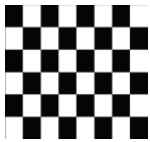
3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

Notes :

- The supply voltage is measured and specified at the interface connector of LCM.
The current draw and power consumption specified is for 3.3V at 25 °C.

- Mosaic pattern 8*8
- R/G/B patterns



(a)



(b)

Figure 3. Power Measure Patterns

- Calculated value for reference ($V_{LED} \times I_{LED}$)
- Measure condition (Figure 4)

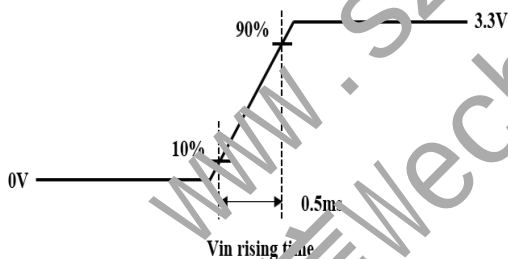


Figure 4. Inrush Measure Condition

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3.2 Backlight Unit

< Table 4. LED Driving Guideline Specifications >

Ta=25+/-2°C

Parameter		Min.	Typ.	Max.	Unit	Remarks
LED Forward Voltage	V _F	-	-	2.9	V	
LED Forward Current	I _F	-	15	-	mA	
LED Power Input Voltage	V _{LED}	5	12	21	V	
LED Power Input Current	I _{LED}	-	-	154.17	mA	Note 1
LED Power Consumption	P _{LED}	-	-	1.35	W	
Power Supply Voltage for LED Driver Inrush	I _{LED} inrush	-	-	2	A	Note 3
LED Life-Time	N/A	15,000	-	-	Hour	I _F = 15 Note 2
EN Control Level	Backlight On	2.5	-	5.0	V	
	Backlight Off	0	-	0.5	V	
PWM Control Level	High Level	2.5	-	5.0	V	
	Low Level	0	-	0.5	V	
PWM Control Frequency	F _{PWM}	200	-	2,000	Hz	
Duty Ratio		5	-	100	%	

Notes :

- Power supply voltage 12V for LED driver.
Calculator value for reference $I_F \times V_F \times 36 / \text{driver efficiency} = P_{LED}$
- The LED life-time define as the estimated time to 50% degradation of initial luminous.
- Measure condition (Figure 5)

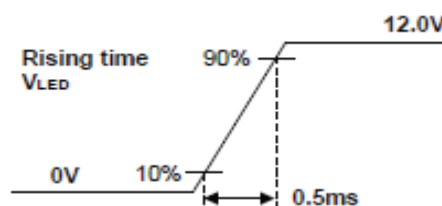


Figure 5. Inrush Measure Condition

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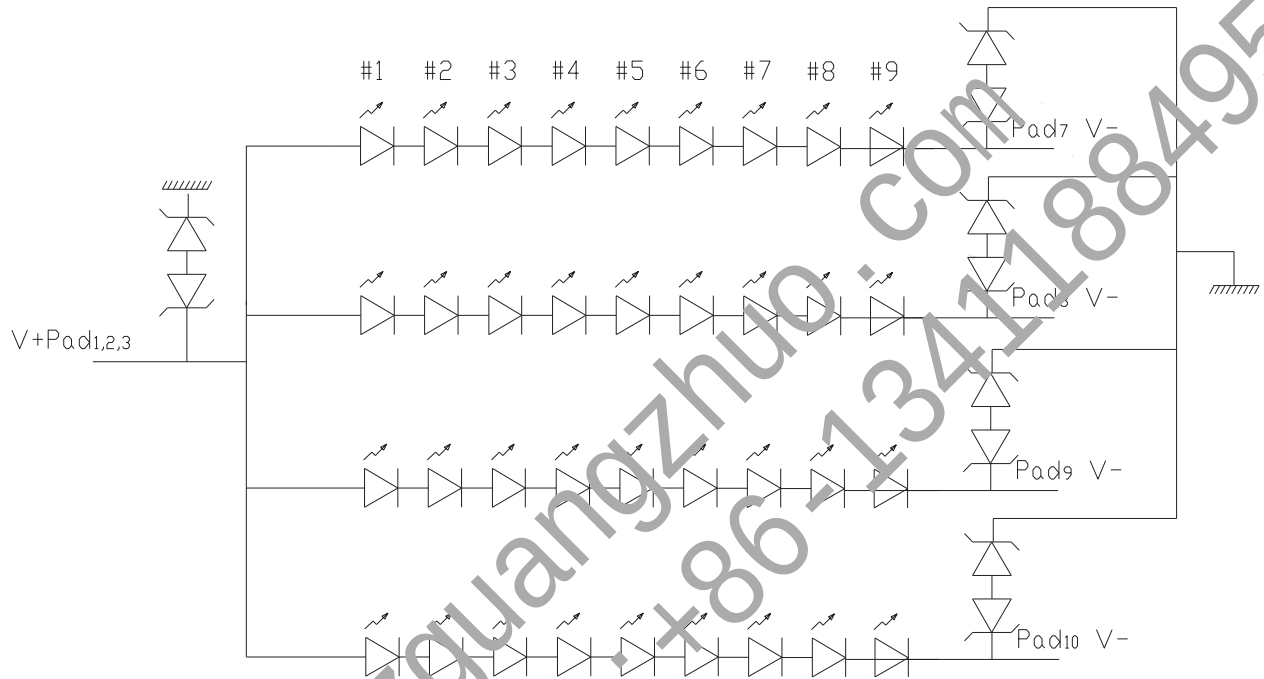
3.3 LED Structure

Figure 6. LED Structure

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4.0 OPTICAL SPECIFICATION

4.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = $25 \pm 2^\circ\text{C}$) with the equipment of luminance meter system (PR730&PR810) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0° . We refer to $\theta=0$ ($=03$) as the 3 o'clock direction (the "right"), $\theta=90$ ($=012$) as the 12 o'clock direction ("upward"), $\theta=180$ ($=09$) as the 9 o'clock direction ("left") and $\theta=270$ ($=06$) as the 6 o'clock direction ("bottom"). While scanning θ and/or Φ , the center of the measuring spot on the display surface shall stay fixed. The backlight should be operating for 30 minutes prior to measurement. VDD shall be $3.3 \pm 0.3\text{V}$ at 25°C . Optimum viewing angle direction is 6 o'clock.

4.2 Optical Specifications

<Table 5. Optical Specifications>

Parameter		Symbol	Condition	Min.	Typ	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ_3	CR ≥ 10	80	85	-	Deg.	Note 1
		Θ_9		80	85	-	Deg.	
	Vertical	Θ_{12}		80	85	-	Deg.	
		Θ_6		80	85	-	Deg.	
Luminance Contrast Ratio		CR	$\Theta = 0^\circ$	600	800	-		Note 2
Luminance of White	5 Points	Y_w	$\Theta = 0^\circ$ LED = 15mA	212.5	250	-	cd/m ²	Note 3
White Luminance Uniformity	5 Points	ΔY_5		-	-	-	%	Note 4
	13 Points	ΔY_{13}		62.5	71.4	-	%	
White Chromaticity		W_x	$\Theta = 0^\circ$	0.283	0.313	0.343		Note 5
		W_y		0.299	0.329	0.359		
Reproduction of Color	Red	R_x	$\Theta = 0^\circ$	Typ.-0.03	0.586	Typ.+0.03		
		R_y			0.364			
	Green	G_x			0.358			
		G_y			0.568			
	Blue	B_x			0.163			
		B_y			0.112			
Color Gamut				Min	45	-	%	
Response Time (Rising + Falling)		T _{RT}	Ta= 25℃ $\Theta = 0^\circ$	-	30	35	ms	Note 6
Cross Talk		CT	$\Theta = 0^\circ$	-	-	2.0	%	Note 7

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Notes :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 7).
2. Contrast measurements shall be made at viewing angle of $\Theta = 0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (see Figure 7) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Center Luminance of white is defined as luminance values of 5 point average across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 8 for a total of the measurements per display.
4. The White luminance uniformity on LCD surface is then expressed as : $\Delta Y = \text{Minimum Luminance of 5(or 13) points} / \text{Maximum Luminance of 5(or 13) points}$. (see Figure 8 and Figure 9).
5. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
6. The electro-optical response time measurements shall be made as Figure 10 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_r , and 90% to 10% is T_r .
7. Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a $10 \pm 1\text{mm}$ diameter area, with all display pixels set to gray 127(of 0 to 255), to the luminance (YB) of that same area when any adjacent area is driven dark. The luminance ratio shall not exceed 1:1.05 (See Figure 11).

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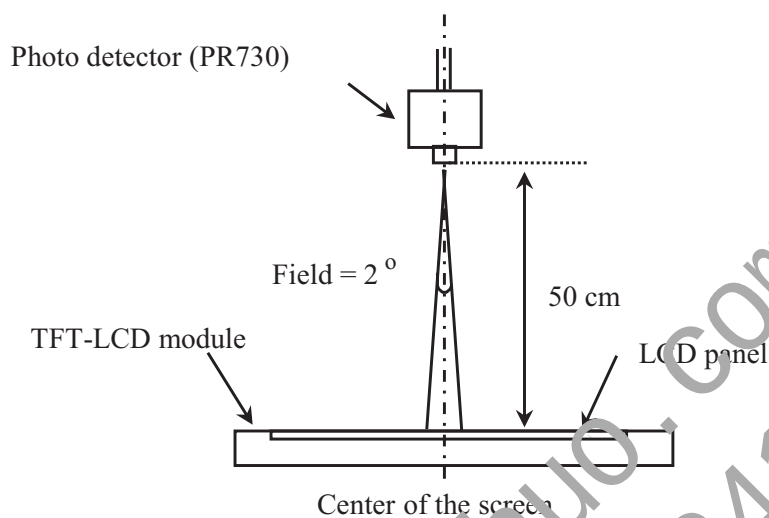
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4.3 Optical Measurements



Optical characteristics measurement setup

Figure 7. Measurement Set Up

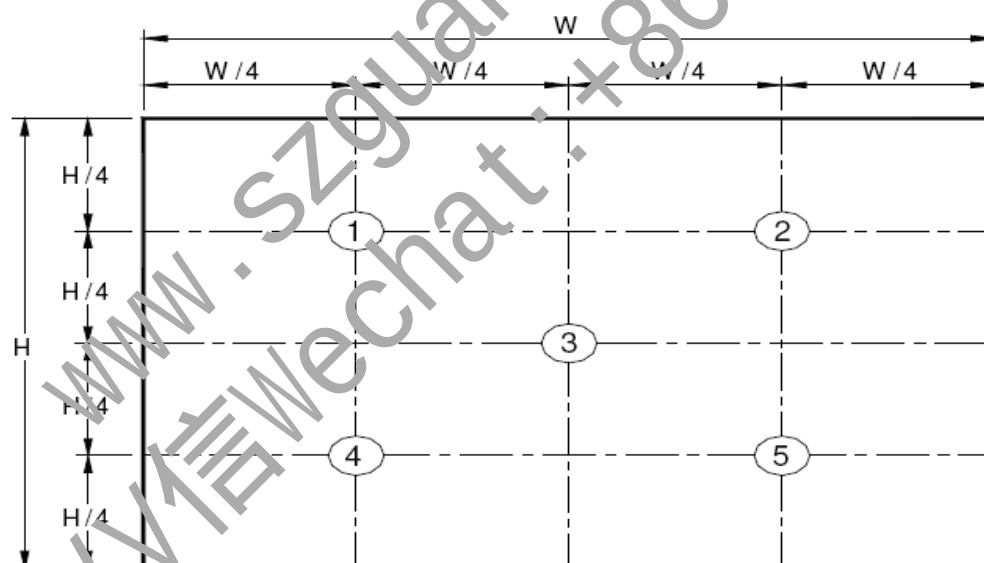


Figure 8. White Luminance and Uniformity Measurement Locations (5 points)

Center Luminance of white is defined as luminance values of center 5 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 7 for a total of the measurements per display.

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The diagram illustrates the timing of data display on a TFT. The top part shows a sequence of data: Black (TFT OFF), White (TFT ON), and Black (TFT OFF). Below this, a graph plots Luminance (0% to 100%) against Time. The rising edge of the luminance curve is marked with T_r (rise time), and the falling edge is marked with T_f (fall time). The curve shows a sharp transition from 0% to 100% luminance during the 'White' period and a sharp transition back to 0% during the next 'Black' period.

The test system : LMS PR810

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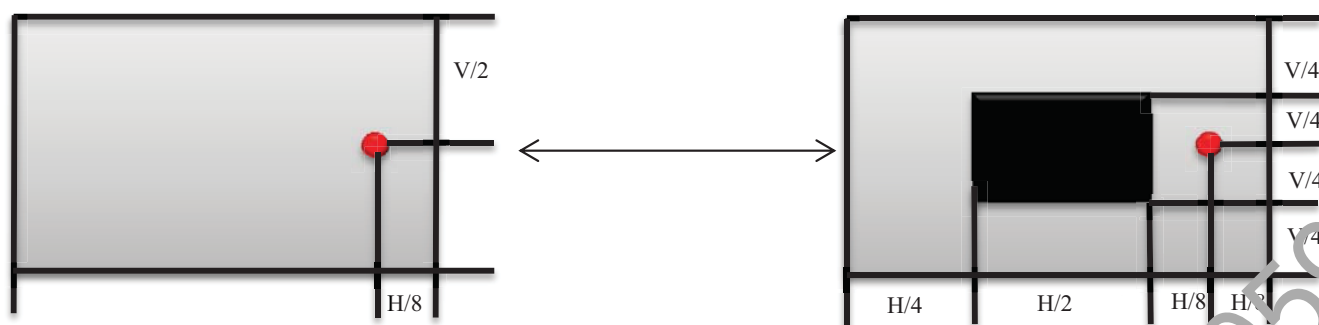
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$$\text{Cross Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_B} \right| \times 100$$

Figure 11. Cross Talk Modulation Test Description

Where:

 Y_A = Initial luminance of measured area (cd/m^2) Y_B = Subsequent luminance of measured area (cd/m^2)

The location measured will be exactly the same in both patterns. The test background gray is L127.

Cross Talk of one area of the LCD surface by another shall be measured by comparing the luminance (Y_A) of a $10 \pm 1\text{mm}$ diameter area, with all display pixels set to a gray level 127, to the luminance (Y_B) of that same area when any adjacent area is driven dark. (Refer to Figure 11)

The test system: PR730

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5.0 INTERFACE CONNECTION

5.1 Electrical Interface Connection

The electronics interface connector is STM MSAK24025P30.

The connector interface pin assignments are listed in Table 6.

<Table 6. Pin Assignments for the Interface Connector>

Terminal	Symbol	Functions
Pin No.	Symbol	Description
1	NC	No Connection
2	H_GND	Ground
3	LANE1_N	eDP RX Channel 1 Negative
4	LANE1_P	eDP RX Channel 1 Positive
5	H_GND	Ground
6	LANE0_N	eDP RX Channel 0 Negative
7	LANE0_P	eDP RX Channel 0 Positive
8	H_GND	Ground
9	AUX_CH_P	eDP AUX CH Positive
10	AUX_CH_N	eDP AUX CH Negative
11	H_GND	Ground
12	LCD_VCC	Power Supply, 3.3V (typ.)
13	LCD_VCC	Power Supply, 3.3V (typ.)
14	NC	No Connection
15	H_GND	Ground
16	H_GND	Ground
17	HPD	Hot Plug Detect Output
18	BL_GND	LED Ground
19	BL_GND	LED Ground
20	BL_GND	LED Ground
21	BL_GND	LED Ground
22	BL_ENABLE	LED Enable Pin(+3.3V Input)
23	BL_PWM	System PWM Signal Input
24	NC	No Connection
25	NC	No Connection
26	BL_POWER	LED Power Supply 5V-21V
27	BL_POWER	LED Power Supply 5V-21V
28	BL_POWER	LED Power Supply 5V-21V
29	BL_POWER	LED Power Supply 5V-21V
30	NC	No Connection

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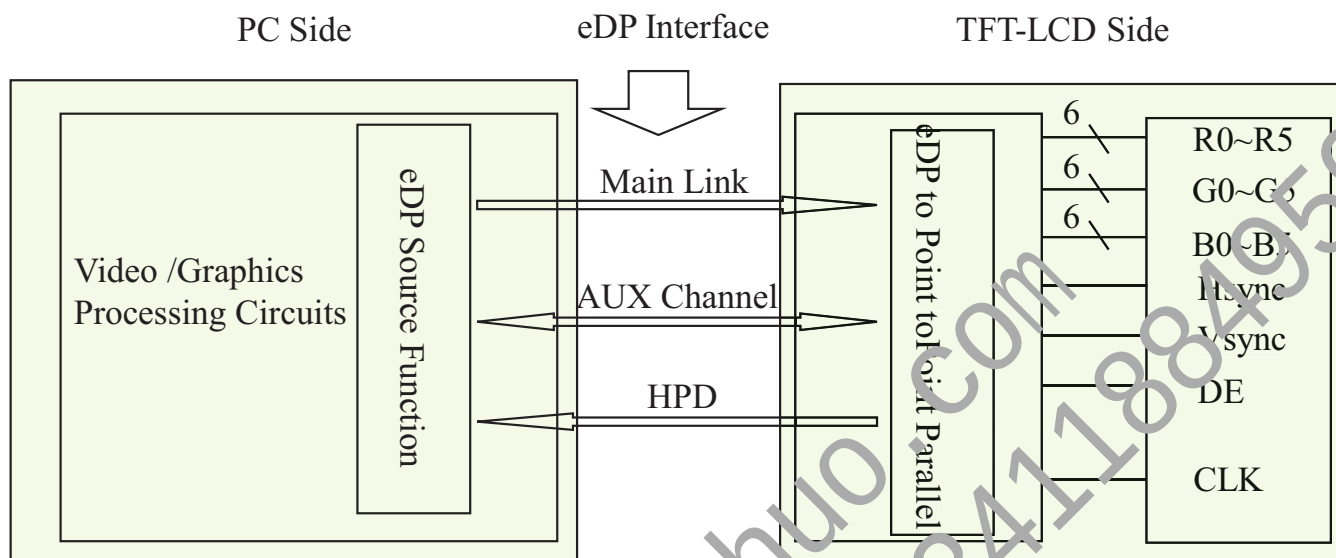
5.2 eDP Interface

Figure 12. eDP Interface Architecture

Note:

Transmitter : Parade DP501 or equivalent.

Transmitter is not contained in module

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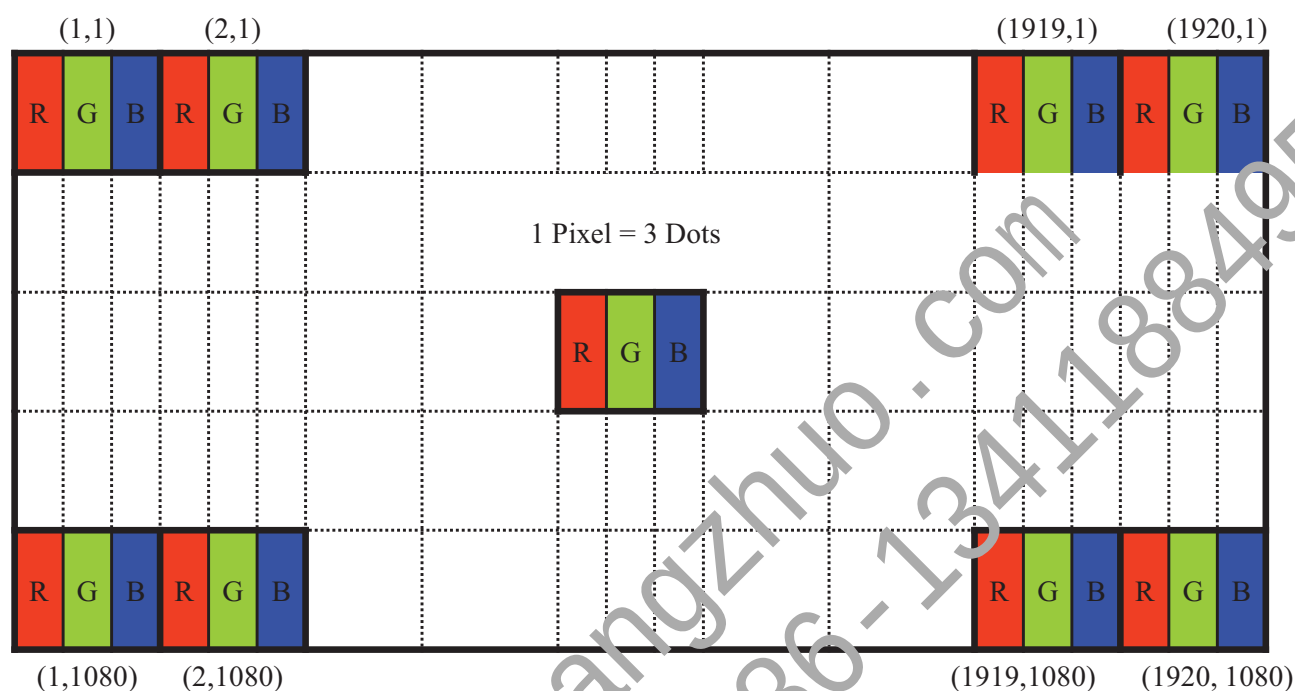
5.3 Data Input Format

Figure 12. Display Position of Input Data (V-H)

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5.4 Back-light & LCM Interface Connection

BLU Interface Connector: STM MSK24022P10 .

<Table 7. Pin Assignments for the BLU Connector>

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	LED	LED cathode connection	6	GND	Ground Connection
2	LED	LED cathode connection	7	NC	No Connection
3	LED	LED cathode connection	8	Vout	LED anode connection
4	LED	LED cathode connection	9	Vout	LED anode connection
5	NC	No Connection	10	vout	LED anode connection

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6.0 SIGNAL TIMING SPECIFICATION**6.1 The NV140FHM-N4T V8.0 Is Operated By The DE Only**

< Table 8. Signal Timing Specification >

Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	146.41	147.06	147.70	MHz
Frame Period		Tv	1135	1140	1145	lines
			-	60	-	Hz
			-	16.67	-	ms
Vertical Display Period		Tvd	-	1080	-	lines
One line Scanning Period		Th	2145	2150	2155	clocks
Horizontal Display Period		Thd	-	1920	-	clocks

Note : The above is as optimized setting.

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6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 9.

<Table 9. eDP Main-Link RX TP4 Package Pin Parameters>

Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock (Link clock down-spreading)	ssc	0	-	0.5	%	
EYE width at package pins	VRX-EYE	0.6			UI	
Differential peak-to-peak input voltage at package pins	VRX-DIFFp-p	120	-	1200	mV	
Rx input DC common mode voltage	VRX_DC_CM	0	-	2	V	
Differential termination resistance	RRX-DIFF	90	-	110	Ω	
Single-ended termination resistance	RRX-SE	40	-	60	Ω	
Rx short circuit current limit	IRX_SHORT	-		50	mA	
Intra-pair skew at Rx package pins (HBR) RX intra-pair skew tolerance at HBR	LRX_SKEW_ INTRA_PAIR	-	-	60	ps	
AC Coupling Capacitor	CSOURCE_ML	75		200	nF	Source side

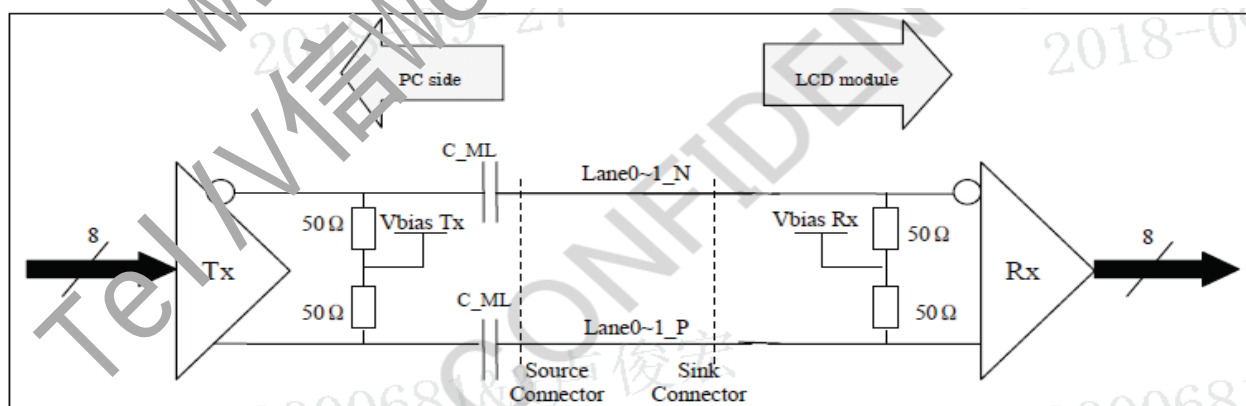


Figure 14. Main link differential pair

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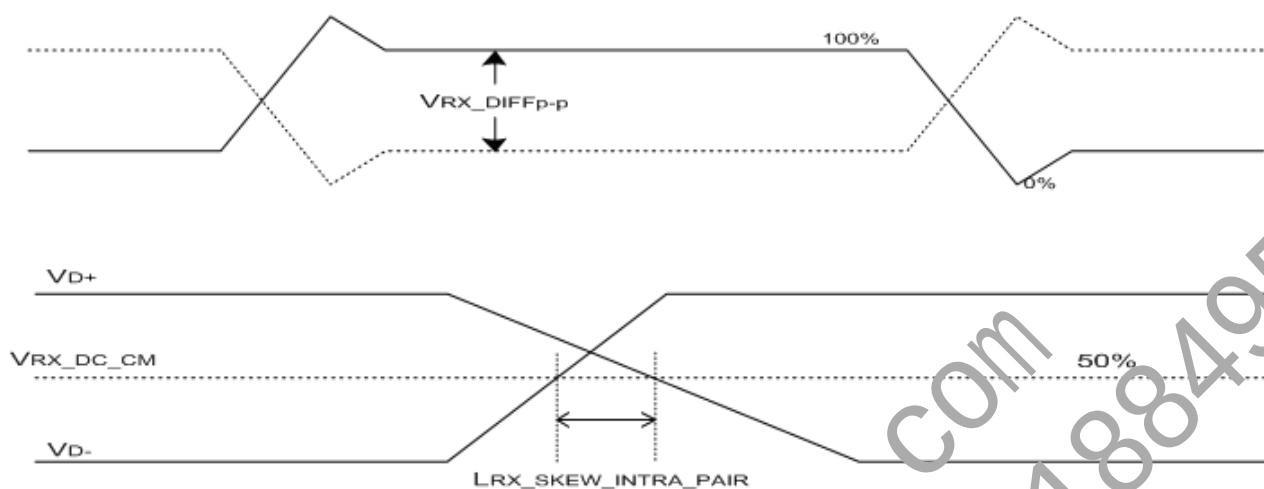


Figure 15. VRX-DIFFp-p & LFX_SKEW_INTRA_PAIR

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<Table 10. HPD Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
HPD voltage	V _{HPD}	2.25	-	3.6	V	
Hot Plug Detection Threshold	-	2.0	-	-	V	Source side Detecting
Hot Unplug Detection Threshold	-	-	-	0.8V	V	
HPD_IRQ Pulse Width	HPD_IRQ	0.5	-	1	ms	
HPD_TimeOut	-	2.0	-	-	ms	

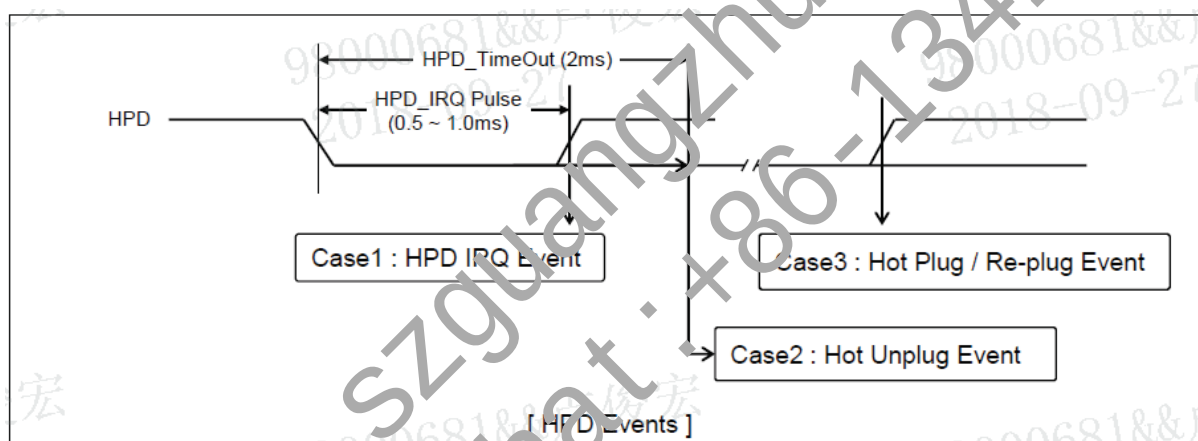


Figure 16. HPD Events

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<Table 11. AUX Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
AUX unit interval	UIAUX	0.4	0.5	0.6	Us	
AUX peak-to-peak input differential voltage	VAUX-RX-D IFFp-p	0.29	-	1.38	V	
AUX CH termination DC resistance	RAUX-TER M	80	100	120	Ω	
AUX DC common mode voltage	VAUX-DC-C M	0	-	2	V	
AUX turn around common mode voltage	VAUX-TUR N-CM	-	-	0.3	V	
AUX short circuit current limit	IAUX-SHOR T	-	-	90	mA	
AUX AC Coupling Capacitor	CSOURCE-A UX	75	-	200	nf	Source side

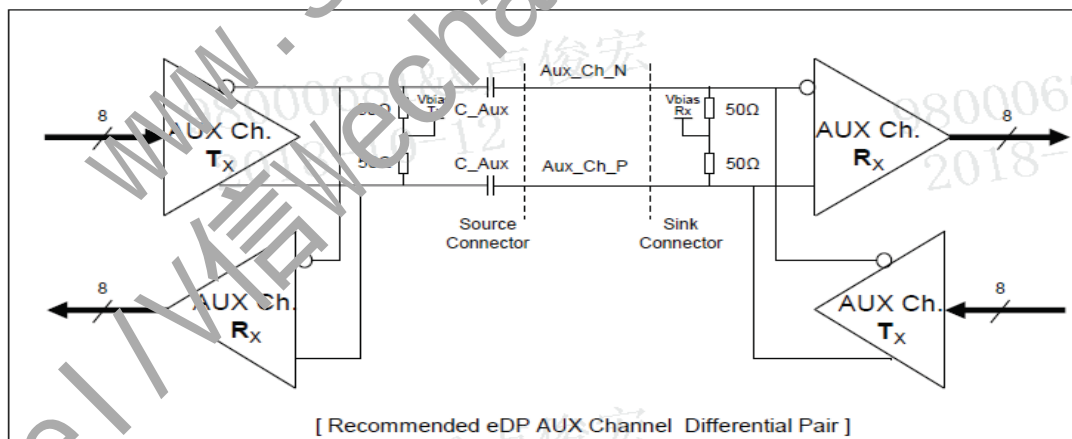


Figure 17. AUX differential pair

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7.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

<Table 12. Input Signal & Basic Display Colors & Gray Scale of Colors >

	Colors & Gray scale	Data signal																	
		R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	B5
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Light Blue	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Purple	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	↑						↑						↑					
	▽	↓						↓						↓					
	Brighter	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	▽	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	△	↑						↑						↑					
	▽	↓						↓						↓					
	Brighter	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0
	▽	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
	△	↑						↓						↑					
	▽	↓						↓						↓					
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Gray scale of White & Black	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0
	Darker	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0
	△	↑						↑						↑					
	▽	↓						↓						↓					
	Brighter	1	0	1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1
	▽	0	1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1	1
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

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8.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below.

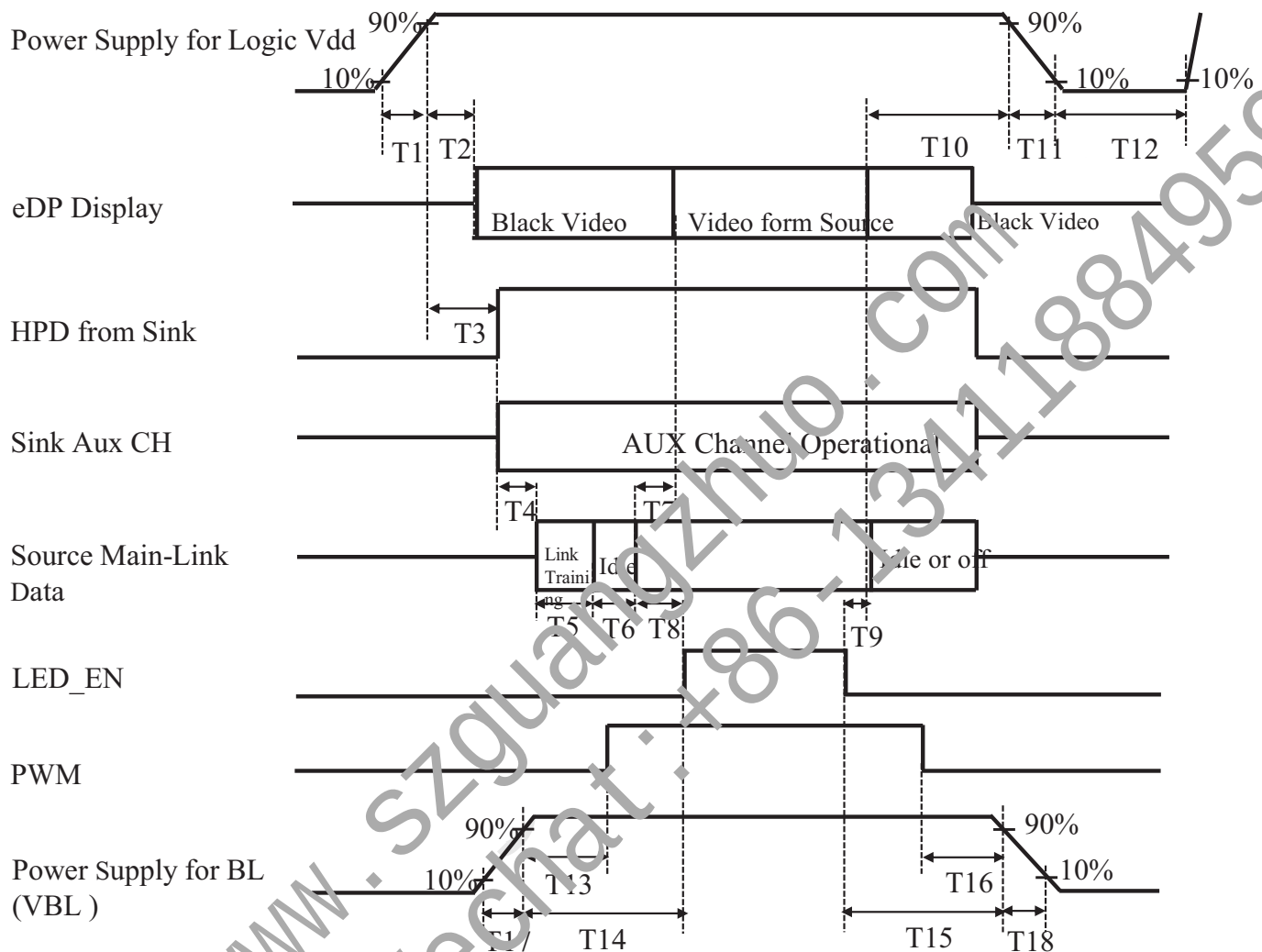


Figure 18. Power Sequence

- $0.5\text{ms} \leq T1 \leq 10\text{ms}$
- $0\text{ms} < T2 \leq 200\text{ms}$
- $0\text{ms} < T3 \leq 200\text{ms}$
- $T4+T5+T6+T8 > 80\text{ms}$
- $0\text{ms} < T7 \leq 50\text{ms}$
- $50\text{ms} < T8$
- $0\text{ms} < T9$
- $0\text{ms} < T10 < 500\text{ms}$
- $0.5\text{ms} \leq T11 \leq 10\text{ms}$
- $500\text{ms} \leq T12$
- $0\text{ms} < T13$
- $0\text{ms} < T14$
- $0\text{ms} < T15$
- $0\text{ms} < T16$
- $0.5\text{ms} \leq T17$
- $0.5\text{ms} \leq T18$

Notes:

1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal are valid.

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9.0 Connector Description

Physical interface is described as for the connector on LCM.

These connectors are capable of accommodating the following signals and will be following components.

9.1 TFT LCD Module

< Table 13. Signal Connector >

Connector Name /Description	For Signal Connector
Manufacturer	STM
Type/ Part Number	MSAK24025P30
Mating Housing/ Part Number	I-PEX 20454-030T

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10.0 MECHANICAL CHARACTERISTICS

10.1 Dimensional Requirements

Figure 23 shows mechanical outlines for the model NV140FHM-N4T V8.0.
Other parameters are shown in Table 14.

<Table 14. Dimensional Parameters>

Parameter	Specification	Unit
Active Area	309.312 (H) × 173.988 (V)	mm
Number of pixels	1920 (H) X 1080 (V) (1 pixel = R + G + B dots)	pixels
Pixel pitch	161.1(H) × 161.1(V)	um
Pixel arrangement	RGB Vertical stripe	
Display colors	262K(6bit)	
Display mode	Normally black	
Dimensional outline	315.812 ± 0.3 (H) * 186.068 ± 0.3 (V) (W/O PCB) * 3.0 (Max) 315.812 ± 0.3 (H) * 186.068 ± 0.3 (V) (W/PCB) * 5.0 (Max)	mm
Weight	300 (max)	g

10.2 Mounting

See Figure 23.

10.3 Anti-Glare and Polarizer Hardness.

The surface of the LCD has an Anti-Glare coating to minimize reflection and a coating to reduce scratching. The Polarizer hardness is 3H.

10.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 350lux.

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11.0 RELIABILITY TEST

The reliability test items and its conditions are shown in below.

<Table 15. Reliability Test>

No	Test Items	Conditions	Remark
1	High temperature storage test	Ta = 60°C , 60%RH, 240 hrs	
2	Low temperature storage test	Ta = -20°C , 240 hrs	
3	High temperature & high humidity operation test	Ta = 50°C , 80%RH, 240 hrs	
4	High temperature operation test	Ta = 50°C , 60%RH, 240 hrs	
5	Low temperature operation test	Ta = 0°C , 240 hrs	
6	Thermal shock	Ta = -20°C ↔ 60°C (0.5 hr), 60% ± 3%RH, 100 cycle	
7	Vibration test (non-operating)	Ta = 25°C , 60%RH, 1.5G, 10~500Hz, Sine X,Y,Z Sweep rate : 1 hour	Note 1
8	Shock test (non-operating)	Ta = 25°C , 60%RH, 220G, Half Sine Wave 2msec ± X, ± Y, ± Z Once for each direction	Note 1
9	Electro-static discharge test (operating)	Air : 150 pF, 330Ω, ± 15 KV Contact : 150 pF, 330Ω, ± 8 KV Ta = 25°C , 60%RH,	Note 2

Notes :

1. The fixture must be hard enough , so that the module would not be twisted or bent.
2. Self- recovery and restart recovery is allowed. No hardware failures.

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12.0 HANDLING & CAUTIONS

(1) Cautions when taking out the module

- Pick the pouch only, when taking out module from a shipping package.

(2) Cautions for handling the module

- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation

- When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

(4) Cautions for the atmosphere

- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics

- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions

- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc. Please pack the module not to be broken. We recommend to use the original shipping packages.

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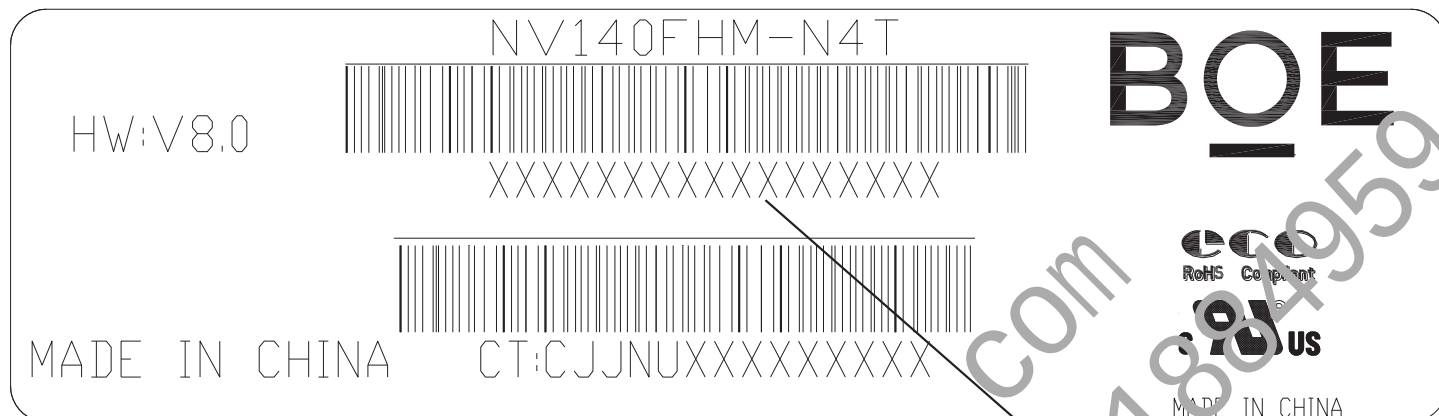
13.0 LABEL**(1) Product Label**

Figure 19. Product Label

Module ID Naming Rule:

<Table 16. Module ID Naming Rule>

Digit Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Code	B	9	A	F	1	7	2	8	D	3	1	0	0	0	0	6	8
Description	Product Name		Product Grade	B8	Year	Month	Model Extension Code (Last 4 Digits of FG CODE)					Serial No. 00001-ZZZZZZ					

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(2) High voltage caution label

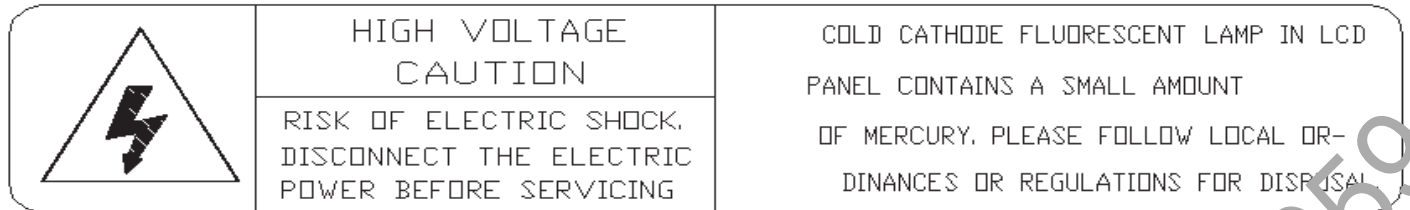


Figure 20. High Voltage Caution Label

(3) Box label

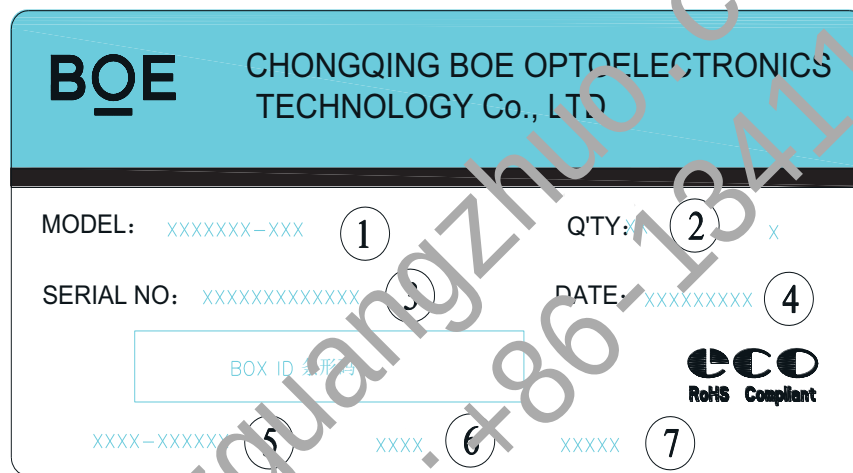


Figure 21. Box Label

Serial number marked part needs to print, show as follows:

1. FG-CODE(Before 12 bit)
2. Product quantity
3. Box ID
4. Date
5. The client section material number(The client)
6. FG-Code After four
7. The supplier code
8. Total Size:100×50mm

<Table 17. Box Label Naming Rule >

Digit Code	1	2	3	4	5	6	7	8	9	10	11	12	13
Code	B	9	A	F	1	7	8	N	0	0	3	2	7
Description	Product Name		Product Grade	B8	Year		Month	Revision	BOX Serial Number				

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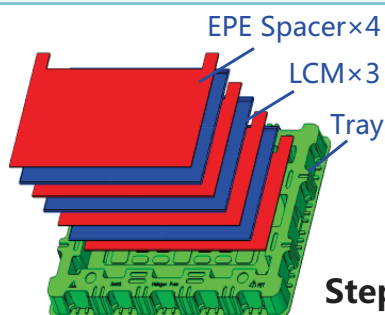
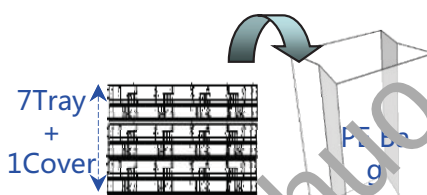
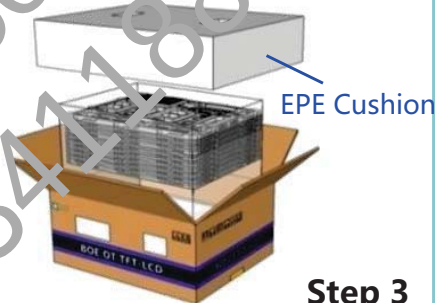
14.0 PACKING INFORMATION**14.1 Packing Order**

1pcs Spacer平放入Tray, 再将 LCM放置Spacer上 (Spacer、LCM放置时注意与Tray中PCB字样对应), 重复上述过程, 最后将 1pcs Spacer 放置在 MDL上。

3 MDL/4 Spacer/Tray

将7层Tray叠码 (不旋转), 顶部放1pcs Cover, 之后将整摞 Tray 放入一个 PE Bag。 21 MDL/7 Tray+1 Cover/Bag

将一包Tray放入Paper Box, 上下放置EPE Cushion。 21 MDL/Paper Box

**Step 1****Step 2****Step 3**

对 Box 进行封箱, 并在标签 Mark框粘贴Box标签。

21 MDL/Paper Box

每层6ea. box码拍, 共3层, 放置纸护角、保护膜后, 横纵两道打包带打包, 5层缠绕膜包裹。

3/8 MDL/18 Box/Pallet

双排双层码放。

18144 MDL/48 Pallet/Track

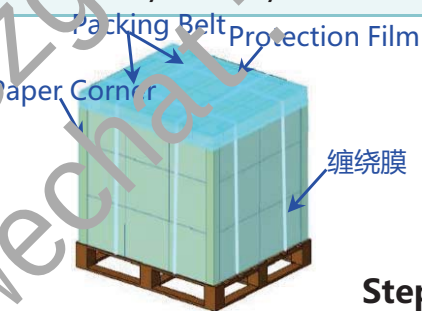
**Step 4****Step 5****Step 6**

Figure 22. Packing Order

14.2 Note

- Box dimension: 480mm*350mm*285mm
- Package quantity in one box: 21pcs
- Total weight: 9.7typ kg/Box

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15.0 MECHANICAL OUTLINE DIMENSION

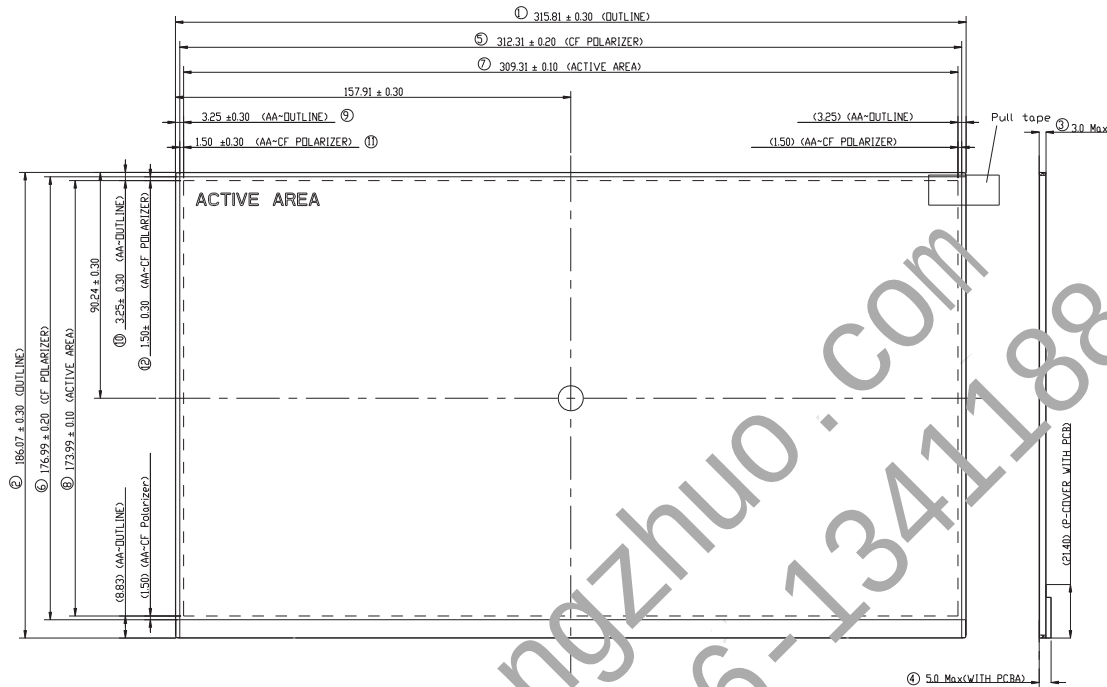


Figure 23. TFT-LCD Module Outline Dimension (Front View)

Notes:

1. Warp and deformation spec.: 0.5mm max.
2. The eDP connector is measured at PIN 1 and mating line.
3. Unspecified tolerance refer to ± 0.3 mm
4. The measurement method for the dimension of module, please refer to product spec..
5. Top polarizer is the highest portion.
6. "()" Means reference dimensions.
7. Critical dimension: ① ~ ⑬ CPK: ① ~ ④

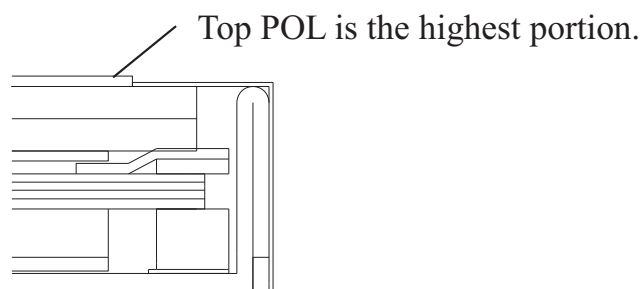


Figure 24. Highest Point Position

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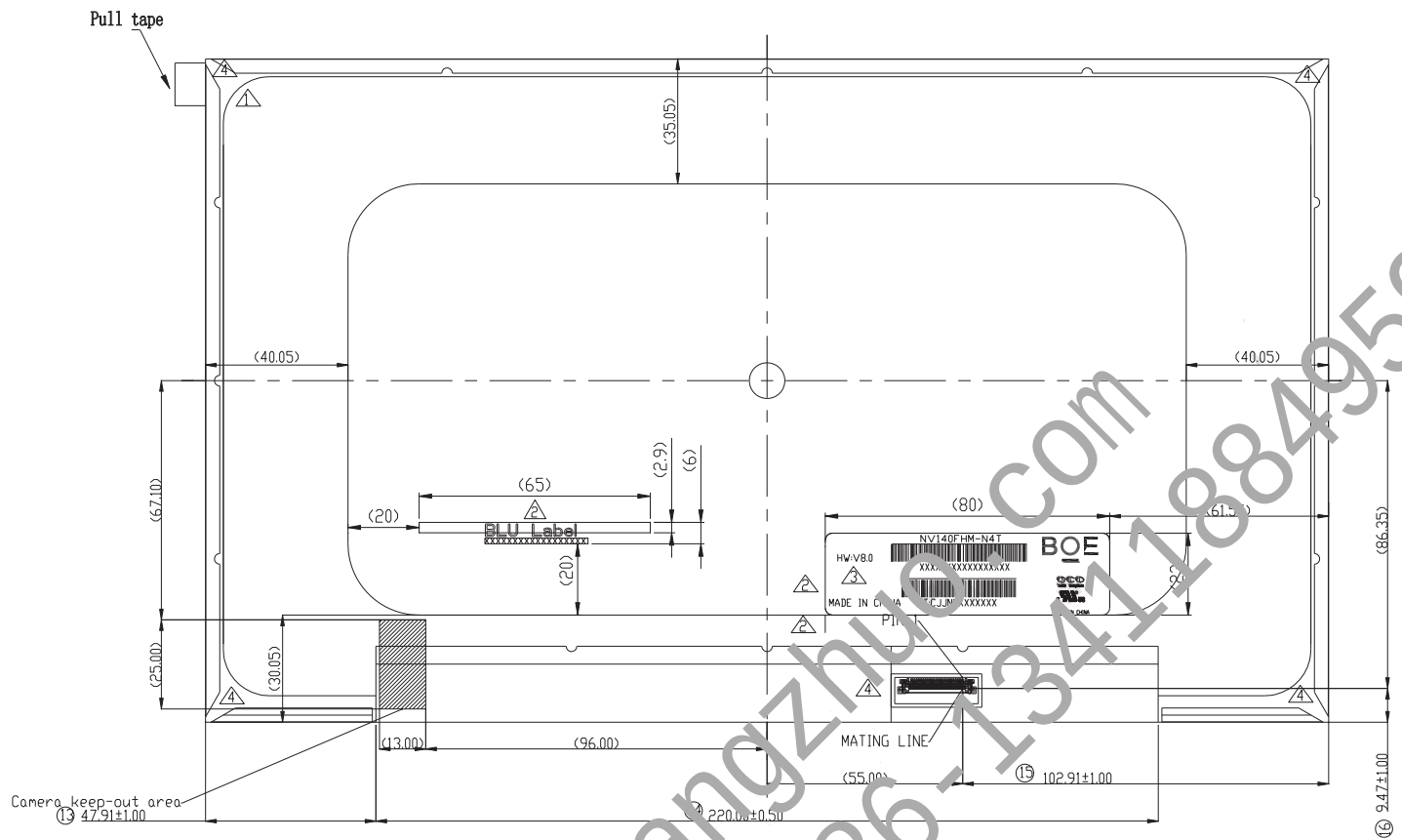


Figure 25. TFT-LCD Module Outline Dimensions (Rear view)

Notes:

1. Warpage and deformation spec : 0.5mm max.
2. The eDP connector is measured at PIN 1 and mating line.
3. Unspecified tolerance refer to ± 0.3 mm.
4. The measurement method for the dimension of module, please refer to product spec..
5. Top polarizer is the highest portion.
6. "()" Means reference dimensions.
7. Critical dimension: ① ~ ⑯ CPK: ① ~ ④

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16.0 EDID Table

Function	Hex	Dec	crc	Input values.	Notes
Header	00	0		0	EDID Header
	FF	255		255	
	FF	255		255	
	FF	255		255	
	FF	255		255	
	FF	255		255	
	FF	255		255	
	00	0		0	
ID Manufacturer Name	09	9		BOE	ID = BOE
	E5	229			
ID Product Code	DA	218		2266	ID = 2266
	08	8			
32-bit serial No.	00	0		0	
	00	0		0	
	00	0		0	
	00	0		0	
Week of manufacture	23	35		35	
Year of Manufacture	1D	29		2019	Manufactured in 2019
EDID Structure Ver.	01	1		1	EDID Ver 1.0
EDID revision #	04	4		4	EDID Rev. 0.4
Video input definition	95	149		-	Refer to right table
Max H image size	1F	31		31	30.9312 cm (Approx)
Max V image size	11	17		17	17.3988 cm (Approx)
Display Gamma	78	120		2.2	Gamma curve = 2.2
Feature support	03	3		-	Refer to right table
Red/Green low bits	1E	30		-	Red / Green Low Bits
Blue/White low bits	F5	245		-	Blue / White Low Bits
Red x high bits	96	150	600	0.586	Red (x) = 10010110 (0.586)
Red y high bits	8D	93	573	0.364	Red (y) = 01011101 (0.364)
Green x high bits	5B	91	367	0.358	Green (x) = 01011011 (0.358)
Green y high bits	41	145	582	0.568	Green (y) = 10010001 (0.568)
Blue x high bits	29	41	167	0.163	Blue (x) = 00101001 (0.163)
Blue y high bits	1C	28	115	0.112	Blue (y) = 00011100 (0.112)
White x high bits	50	80	321	0.313	White (x) = 01010000 (0.313)
White y high bits	54	84	337	0.329	White (y) = 01010100 (0.329)
Established timing 1	00	0		-	Refer to right table
Established timing 2	00	0		-	
Established timing 3	00	0		-	
Standard timing #1	01	1			Not Used
	01	1			
Standard timing #2	01	1			Not Used
	01	1			
Standard timing #3	01	1			Not Used
	01	1			

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Standard timing #4	01	1			Not Used	
	01	1				
Standard timing #5	01	1			Not Used	
	01	1				
Standard timing #6	01	1			Not Used	
	01	1				
Standard timing #7	01	1			Not Used	
	01	1				
Standard timing #8	01	1			Not Used	
	01	1				
Detailed timing/monitor descriptor #1	72	114		147.1	147.06MHz Main clock	
	39	57				
	80	128		1920	Hor Active = 1920	
	E6	230		230	Hor Blanking = 230	
	70	112		-	4 bits of Hor. Active + 4 bits of Hor. Blanking	
	38	56		1080	Ver Active = 1080	
	3C	60		60	Ver Blanking = 60	
	40	64		-	4 bits of Ver. Active + 4 bits of Ver. Blanking	
	30	48		48	Hor Sync Offset = 48	
	20	32		32	H Sync Pulse Width = 32	
	35	54		3	V sync Offset = 3 line	
	00	0		6	V Sync Pulse width : 6 line	
	35	53		309	Horizontal Image Size = 309.312 mm (Low 8 bits)	
	AE	174		174	Vertical Image Size = 173.988 mm (Low 8 bits)	
	10	16		-	4 bits of Hor Image Size + 4 bits of Ver Image Size	
	00	0		0	Hor Border (pixels)	
	00	0		0	Vertical Border (Lines)	
	1A	26		-	Refer to right table	
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Detailed timing/monitor descriptor #2	4C	76		98.0	98.04MHz Main clock	
	26	38				
	80	128		1920	Hor Active = 1920	
	E6	230		230	Hor Blanking = 230	
	70	112		-	4 bits of Hor. Active + 4 bits of Hor. Blanking	
	38	56		1080	Ver Active = 1080	
	3C	60		60	Ver Blanking = 60	
	40	64		-	4 bits of Ver. Active + 4 bits of Ver. Blanking	
	30	48		48	Hor Sync Offset = 48	
	20	32		32	H Sync Pulse Width = 32	
	36	54		3	V sync Offset = 3 line	
	00	0		6	V Sync Pulse width : 6 line	
	35	53		309	Horizontal Image Size = 309.312 mm (Low 8 bits)	
	AE	174		174	Vertical Image Size = 173.988 mm (Low 8 bits)	
	10	16		-	4 bits of Hor. Image Size + 4 bits of Ver Image Size	
	00	0		0	Hor Border (pixels)	
	00	0		0	Vertical Border (Lines)	
	1A	26		-	Refer to right above table	
Detailed timing/monitor descriptor #3	00	0			Nvidia nvDPS (Refer the tab of nvDPS) Lowest refresh rate that does not cause any visual/optical side effect	
	00	0				
	00	0				
	00	0				
	00	0				
	00	0				
	00	0				
	00	0				
	00	0				
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	00	0				
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Detailed timing/monitor descriptor #4	00	0			Detailed Timing Description #4	
	00	0			Flag	
	00	0			Reserved	
	02	2			For Brightness Table and Power consumption	
	00	0			Flag	
	0D	13		-	PWM % [7:0] @ Step 0	
	40	64		-	PWM % [7:0] @ Step 5	
	FF	255		-	PWM % [7:0] @ step 10	
	0A	10		-	Nits [7:0] @ Step 0	
	3C	60		-	Nits [7:0] @ Step 5	
	7D	125		-	Nits [7:0] @ Step 10	
	11	17		-	Panel Electronics Power @ 32x32 Chess Pattern = 700mW	
	0B	11		-	Backlight Power @60 nits = 470.117647058823mW	
	17	23		-	Backlight Power @Step 10 = 1850mW	
	7D	125			Nits @ 100% PWM Duty = 250nit	
	00	0			Format :	
	00	0			terminate with ASCII code 0Ah	
	00	0			and pad field with ASCII code 20h	
Extension flag	00	0		1		
Checksum	AE	174	174	-		

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Appendix A

The Measurement Methods for the Dimensions of Module

Caliper:

- Length of Outline
- Width of Outline (Without/With PCB)
- Thickness of Outline (Without/ With PCB)

Coordinate Measuring Machine:

CF Polarizer Size

Active Area Size

Active Area to Outline (Without Tape Wrinkle or Bulged)

Active Area to CF Polarizer

The Distance of Bracket Holes

P-Cover to Outline (Without Tape Wrinkle or Bulged)

Length of P-Cover

Connector Pin 1 to Outline (Without Tape Wrinkle or Bulged)

Height Gauge: The Different Height of Root and Top on the Bracket
(Need to Calculate From Bracket Angle Spec.)

Feeler Gauge: The Warpage Spec. of Module

Notes:

Except the Critical Dimensions as Above, Other Dimensions are Measured by Coordinate Measuring Machine If Necessary

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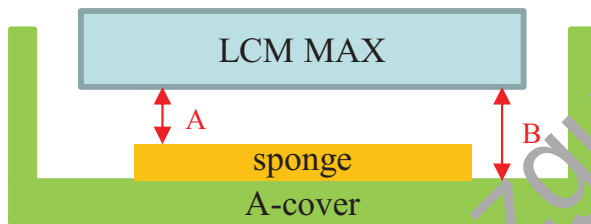
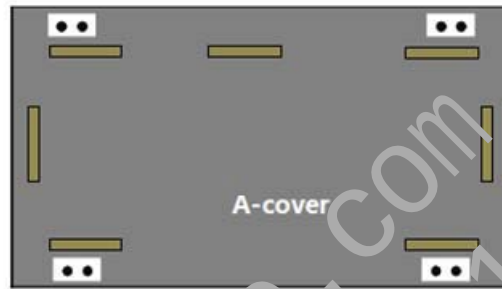
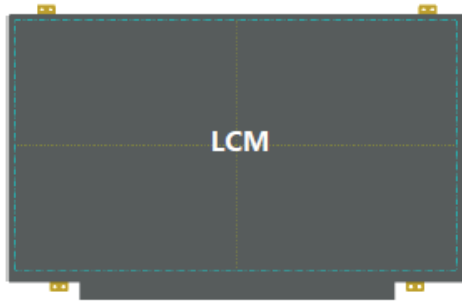
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Appendix B

LCM to A-Cover / sponges z-gap

	Plastic Cover (LCM Thickness: Max)	Metal Cover (LCM Thickness: Max)
A	>0mm	>0mm
B	Min: 1.0mm	Min: 0.8mm
Without the open area of back cover		

Purpose

The reflector area is very sensitive, we suggest that design enough z-gap to decrease the risk of water ripple, white spot and other abnormal display

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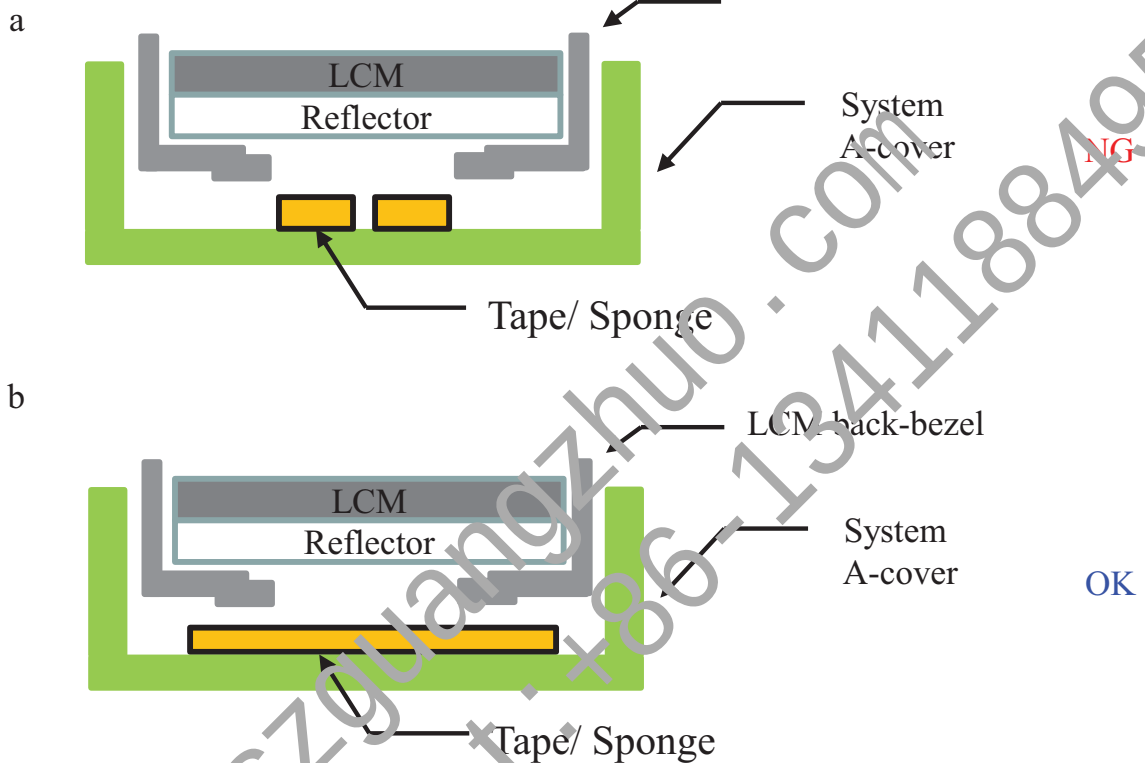
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Appendix B

LCM to A-Cover / sponges z-gap**Purpose**

If attach sponges or rubbers which correspond to white reflector area, it may cause white spot, pooling or other relate issues. We suggest that attach wide range sponges / rubbers which can cover the LCM back-bezel opening

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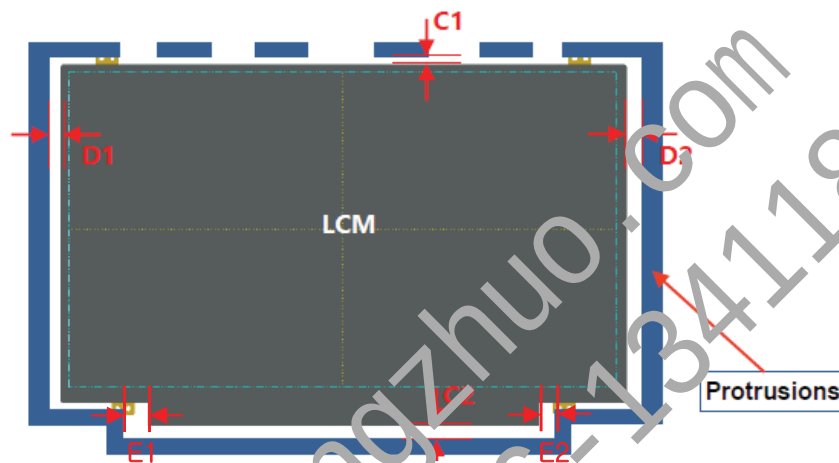
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Appendix B

LCM to side wall / protrusions

	Normal border	Narrow border
D1/D2	Min: 0.45mm	Min: 0.35mm
C1	Min: 0.50mm	
C2	Min: 0.50mm	
E1/E2	Min: 0.55mm	

Purpose

We suggest that design enough gap around LCM to prevent shock test failure, or interference, cell crack, abnormal display...etc. in the reliability test

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Appendix B

LCM to B-cover z-gap

B-cover Tape	Gap
Without	0.15 ~ 0.25mm
With	0.15 ~ 0.20mm

Purpose

Too less z-gap between system B-cover and LCM top pol has high risk to cause cell crack, pooling, light leakage and other issues

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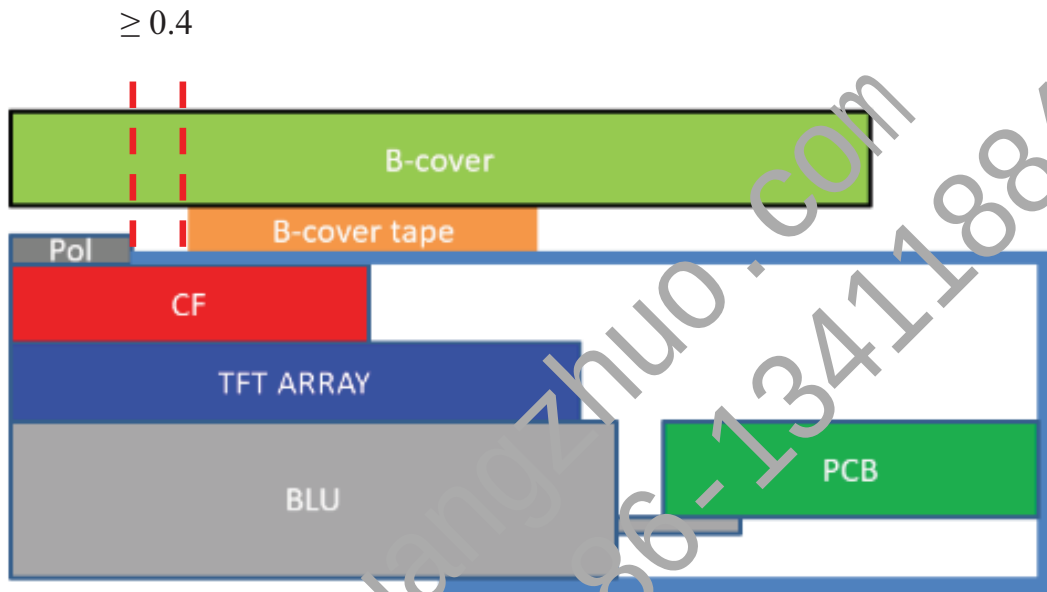
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Appendix B

B-cover tape to top pol edge

If attach b-cover and LCM with tapes,
Please let tapes to be located out of top pol edges 0.4mm away on 4 sides

Purpose

To avoid the B-cover tape override top pol and cause pooling or light leakage issue

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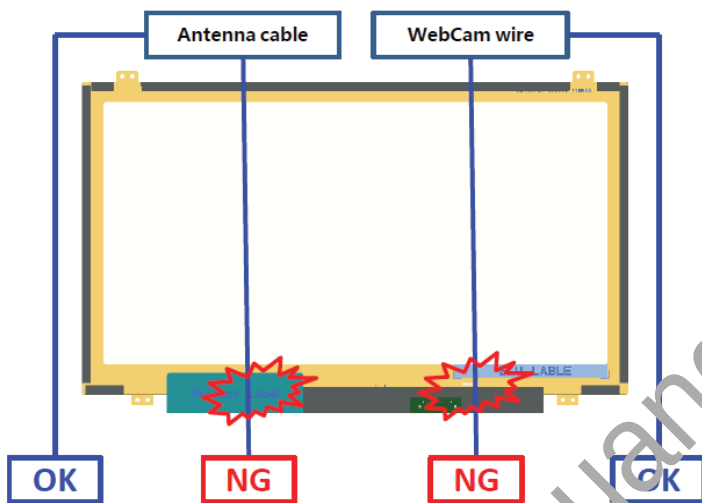
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Appendix B

Antenna Cable & Webcam wire

If sponge within the reflector area is necessary, we suggest that the gap between reflector and sponge is more than 0.5mm

Purpose

1. We suggest that do not set Antenna or WebCam cable / wire go behind LCM to avoid backpack test, hinge test, twist test or pogo test with abnormal display
2. If the cable / wire is necessary to go behind LCM, please make a groove with rounds or chamfers to protect the cable / wire, or attach with higher sponge / rubbers adjacent to the cable / wire route
3. Suggest that attach the cable / wire with tapes to A-cover
4. Do not attach anything with LCM reflector area. If attach cable / wire with LCM reflector area, it may cause pooling, white spot, light leakage and other related issues

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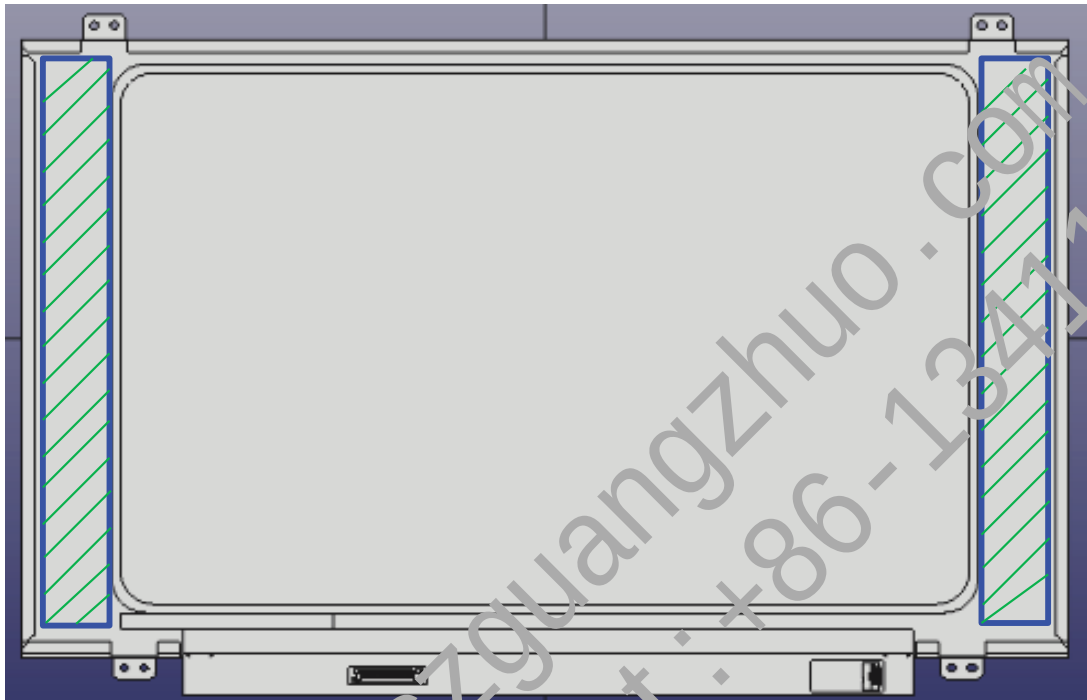
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Appendix B

LCM paste area



Attachment area

Purpose

If use the stretch remove tapes to fix LCM with A-cover, please set the stretch remove tapes correspond to the LCM back-bezel and do not let the tapes override the back-bezel's level step of opening

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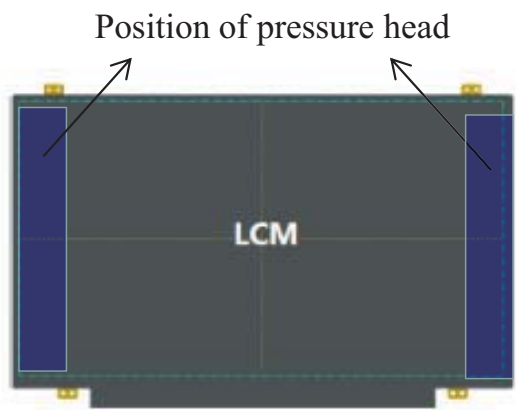
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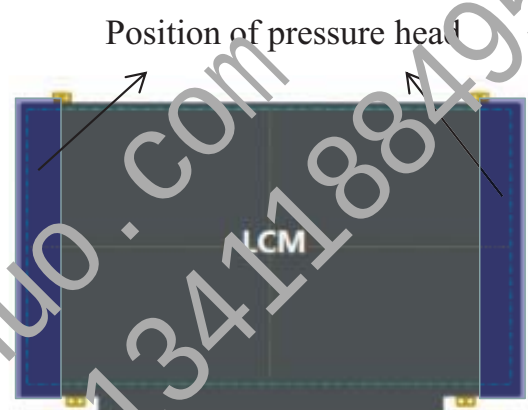
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Appendix B

LCM pressable area

NG



OK

Purpose

1. LCM is fixed on A-cover by double-sided tap which can stick LCM after using the press jig stress LCM during assembling.
2. To avoid panel broken the design of pressure head of press jig can not only pin on cell panel. The pressure head needs to pin on the LCM frame, which the LCM frame can share the pressure of the pressing head.

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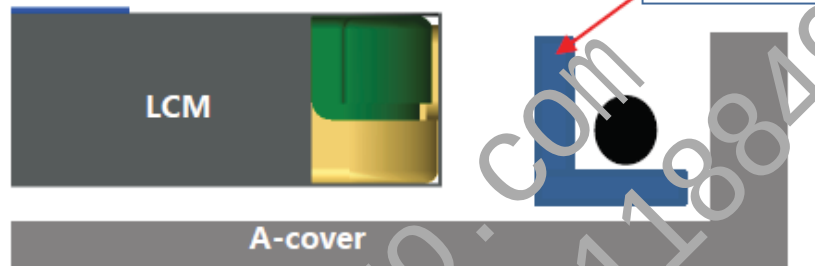
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Wire setting

Purpose

Wire should be placed between Protrusions and A-cover. If place the wire between LCM and Protrusions, it may interfere with LCM when assembling B-covers, or even cause LCM breakage in reliability test.

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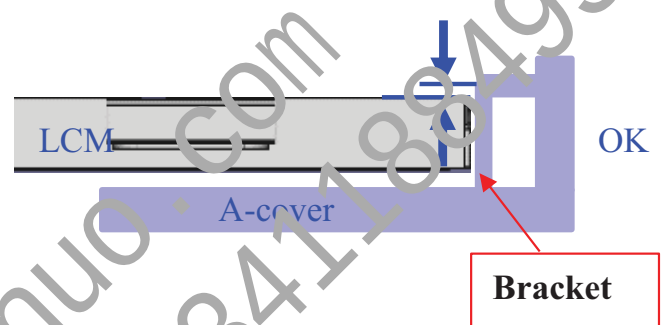
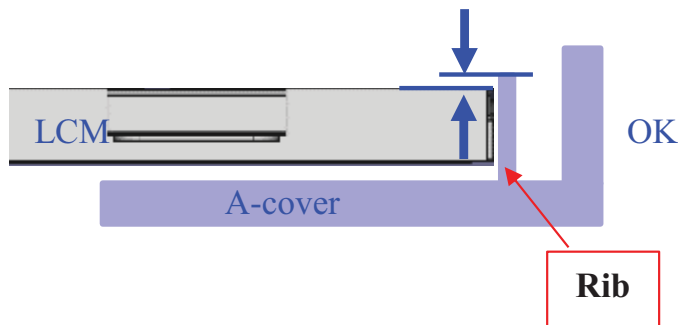
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A-cover strength**Purpose**

1. It is recommended that Rib height is higher than LCM, in order to avoiding press on LCM edge panels.
2. As for LCM is more stronger than Rib, the L Bracket is be recommended.

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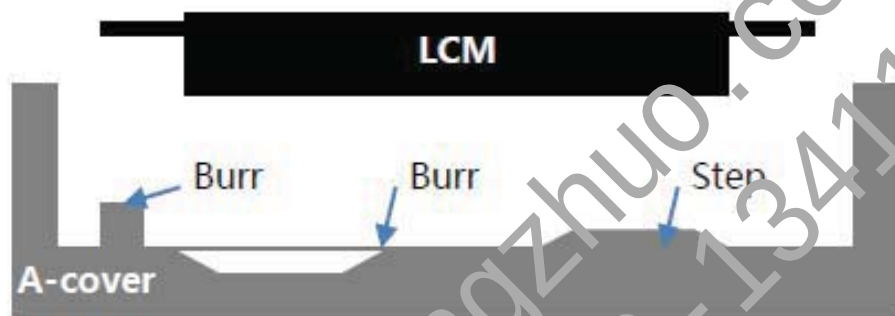
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Appendix B

System A-cover Inner Surface



Purpose

There should not exist any burr, segment gap or protrusions beside Logo, which would cause White Spot or Glass Broken by stress concentration.

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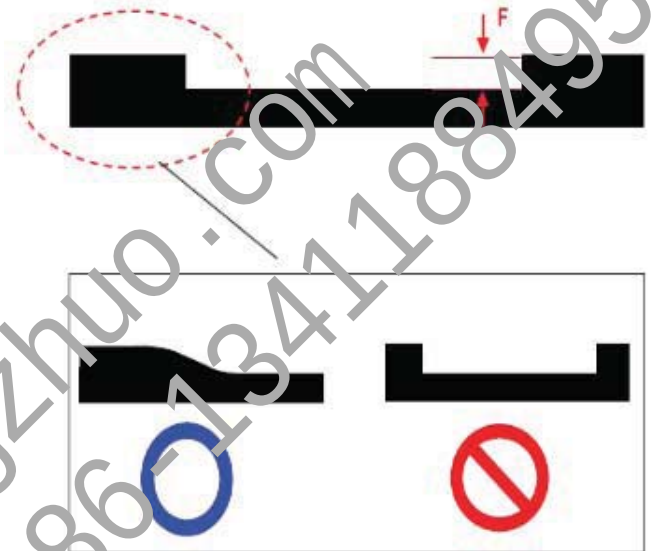
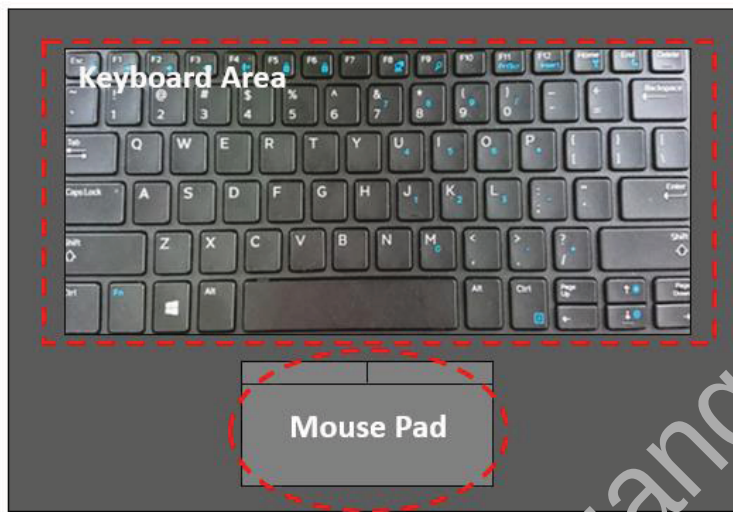
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Appendix B

Keyboard area & Mouse pad

F. max 0.3mm

Purpose

In order to avoiding LCM fragments in reliability test, the step surface of Keyboard and Mouse pad transmits smoothly, and should not be right-angle. For example, when Pogo testing if the broken hole is done in this location, it is easy to produce fragments.

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Appendix B

System cover reliability



Purpose

The permanent deformation part of System cover after the reliability test, including sponge and other structures or components, can not touch LCM.

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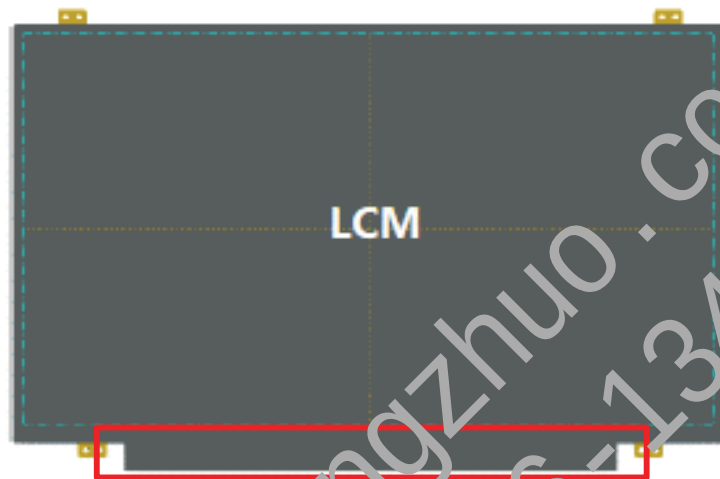
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Appendix B

A/B-cover near LCD PCBA

No magnetic object

Purpose

There should not have magnet object near LCM PCBA, which is prone to cause physical or electricity noise issue

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A-cover add sponges on Boss side wall



Purpose

We suggest to attach Sponges to the side of the Boss column of A-cover to reduce the panel broken possibility in assembly. It is recommended to this design synchronously.

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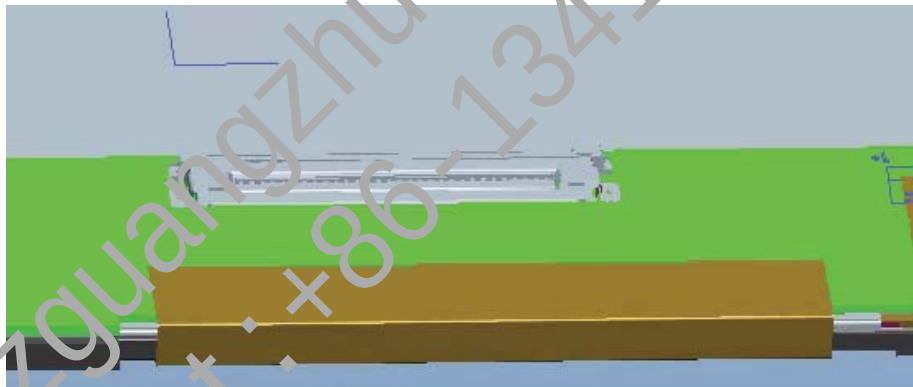
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Appendix B

LCM to A-Cover / sponges z-gap**Purpose**

Bent product: The position of system connector and FPC should be staggered in X direction. Otherwise, when testing, the system Cable line extrudes FPC, leading to FPC Crack. (Panel FPC Bonding location is related to Mask and can not be changed easily)

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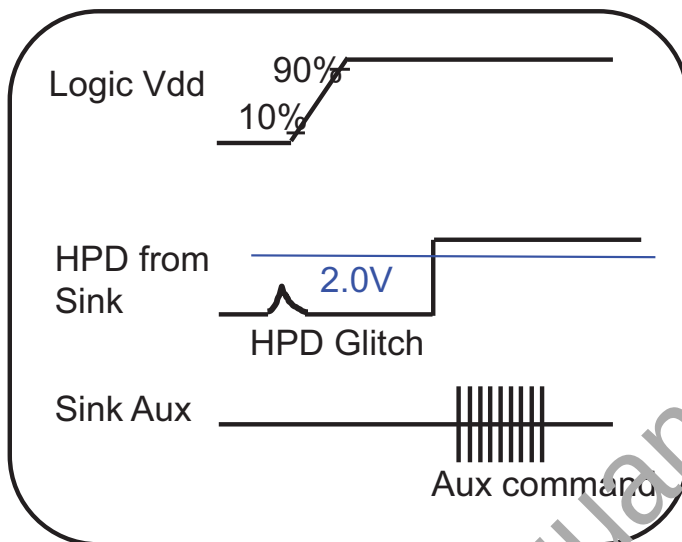
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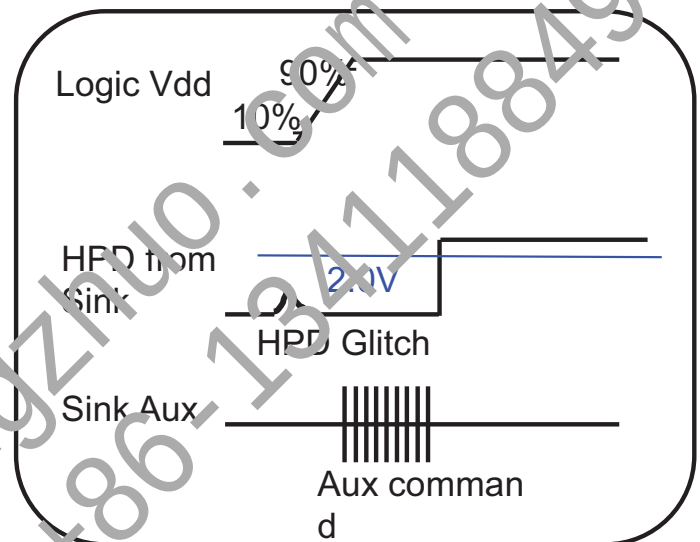
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Appendix C

HPD Signal recognition

Normal Signal (Ignore HPD Glitch)



Abnormal Signal

Purpose

When HPD glitch of source device minimum is 2.0(V).

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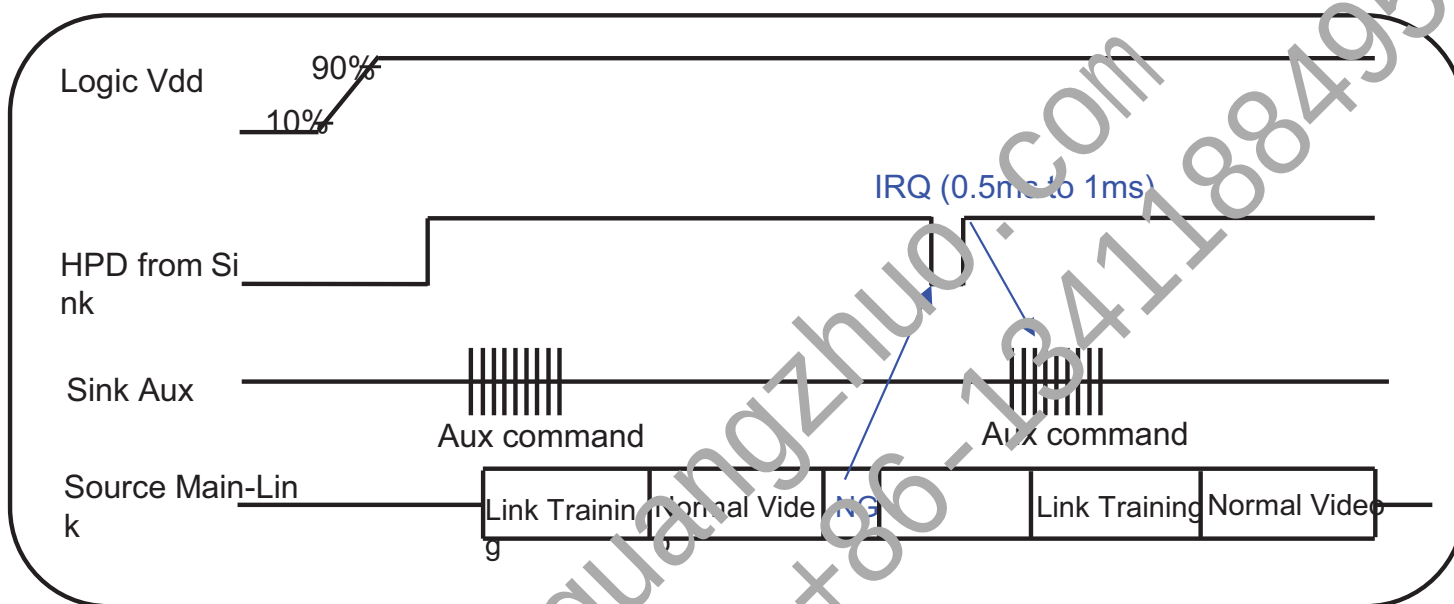
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HPD Signal Definition IRQ (Interrupt Request)**Purpose**

When HPD signal low than 0.5ms to 1ms, the source device should check sink status field from the DPCE and take link training again.

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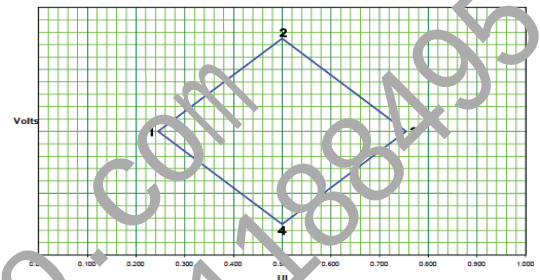
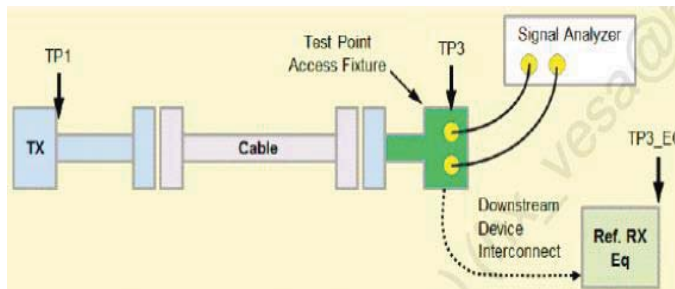
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Appendix C

Main link eye diagram of TP3

Measured TP3 on LCM connector.

Downstream Device Mask at TP3

	UI	Voltage
1	0.246	0
2	0.5	0.075
3	0.755	0
4	0.5	-0.075

Eye for TP3 at FBR

	UI	Voltage
1	0.375	0
2	0.5	0.023
3	0.625	0
4	0.5	-0.023

Eye for TP3 at RBR

Purpose

1. Main Link EYE Diagram should meet TP3 point of VESA.
2. The measure method is through access fixture.

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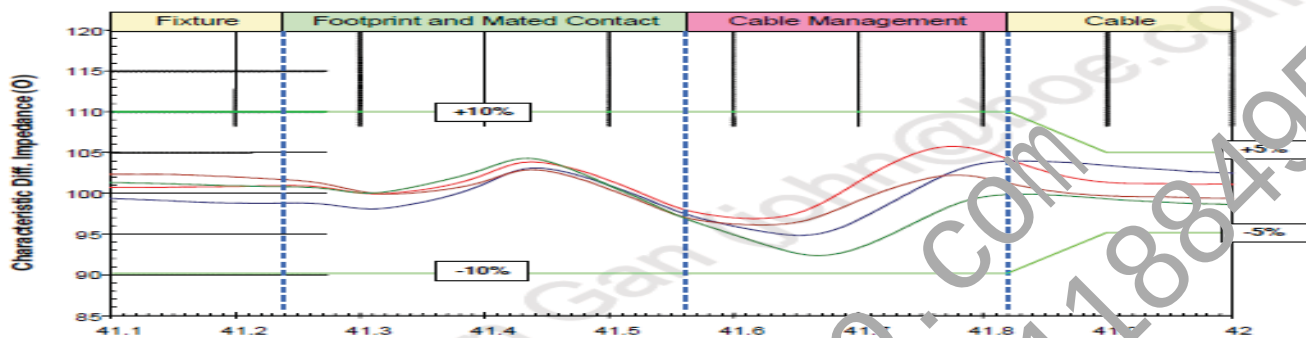
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Appendix C

Impedance Profile through a DP Connector

Differential Impedance Profile Measurement Data Example

Segment	Differential Impedance Value	Maximum Tolerance
Fixture	100Ω/85Ω VESA	±10%
Connector	100Ω/85Ω VESA	±10%
Wire management	100Ω/85Ω VESA	±10%
Cable	100Ω/85Ω VESA	±5%

Impedance Profile Values for Cable Assembly

Purpose

Cable Impedance Profile 100ohm for Cable Assembly

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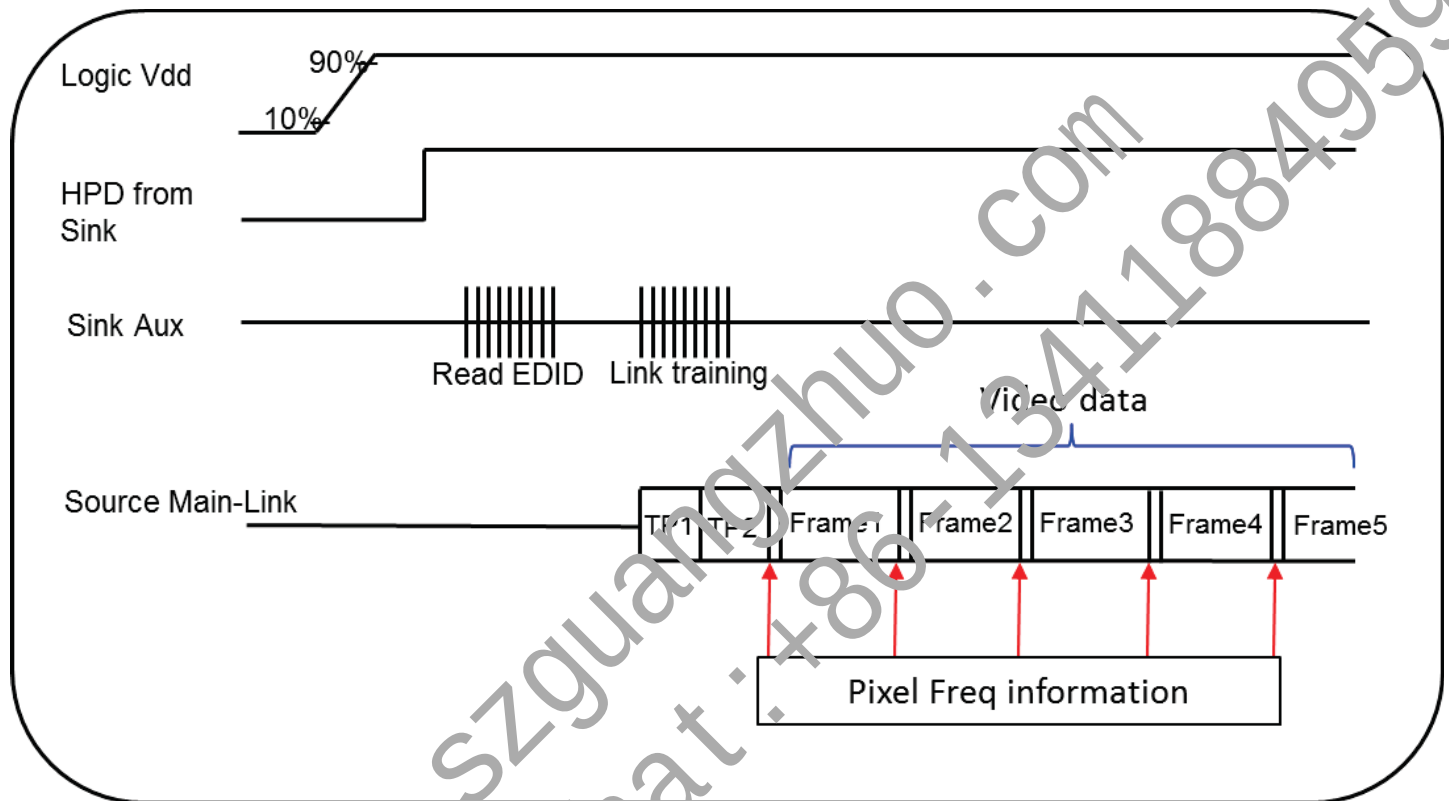
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Appendix C

Main Link Pixel Freq information value of MSA data

Purpose

1. It need to fix pixel freq information value of MSA data output to prevent the initial abnormal pixel freq information value from incoming after power on.
2. BOE can read DPCD to check this value. Ex: BIOS is 1.62G , but into windows is 2.7G.

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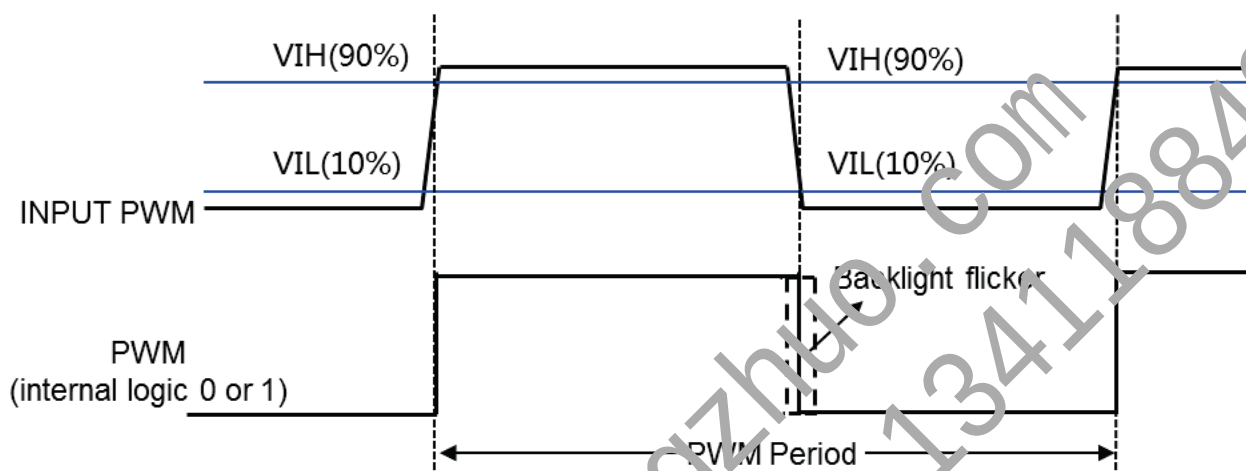
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Appendix C

Main Link Pixel Freq information value of MSA data

Example:

Freq	Cycle Time	PWM Rising Time	PWM Falling Time
200Hz	5ms	$\leq 1\mu s$	$\leq 1\mu s$
1KHz	1ms	$\leq 200ns$	$\leq 200ns$

Purpose

1. LED driver need to calculate the duty cycle of input PWM signal.
2. To avoid backlight flicker visible on LCD, system input PWM suggest :
PWM rising $\leq 200\text{ppm} \times \text{cycle time}$; PWM falling $\leq 200\text{ppm} \times \text{cycle time}$.

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