

PRODUCT SPECIFICATION

- ☐ Tentative Specification
☐ Preliminary Specification
☒ Approval Specification

MODEL NO.: N140JLG

SUFFIX: GT3

DPN: 80M91 Rev.C1

Customer: Dell

APPROVED BY

SIGNATURE

Name / Title

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
許君達	李軒誠	蔡琇仔

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REVISION HISTORY

Version	Date	Page	Description
3.0	Dec 20, 2022	ALL	Approval Spec Ver. 3.0 was first issued.

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1. GENERAL DESCRIPTION

1.1 OVERVIEW

N140JLG-GT3 is a 14.0" (14.0" diagonal) TFT Liquid Crystal Display NB module with LED Backlight unit and 30 pins eDP interface. This module supports 1920 x 1200 WUXGA AAS mode and can display 16,777,216 colors.

1.2 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Screen Size	14.0" diagonal	inch	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1200	pixel	-
Pixel Pitch	0.157 (H) x 0.157 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	Color	-
Interface	eDP 1.4		(2)
LED IC Dimming Mode	DC mode	-	-
Transmissive Mode	Normally Black	-	-
Surface Treatment	Hard coating (3H), Anti-Glare	-	-
Luminance, White	400	Cd/m2	
Color Gamut	100%	sRGB	
Power Consumption	Total 2.75W (max.) @ cell 0.45W (max.), BL 2.30W (max.)		(1)
Special Function	G-sync DD (Not support) G-sync N/SP (Not support) Free-sync (support) PSR (PSR2 support)		

Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, fv = 60 Hz, LED VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 °C, whereas Black pattern is displayed.

Note (2) Display port interface signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.4 (eDP1.4). There are many optional items described in eDP 1.4. If some optional item is requested, please contact us.

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2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	306.29	306.59	306.89	mm	(1)(2)(3)
	Vertical (V) (w PCB)	197.90	198.40	198.90	mm	
	Thickness (T) (w/o PCB)	1.65	1.80	1.95	mm	
	Thickness (T) (w/ PCB)	-	-	3.95	mm	
Active Area	Horizontal	301.49	301.59	301.69	mm	
	Vertical	188.40	188.50	188.60	mm	
Weight		-	160	170	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Dimensions are measured by caliper

Note (3) Panel thickness is measured with calipers clamping mylar or tape tightly



2.1 CONNECTOR TYPE

Please refer appendix outline drawing for detail design.

Connector Part No.: IPEX-20682-030E-02

User's connector Part No: IPEX-20679-030T-0

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

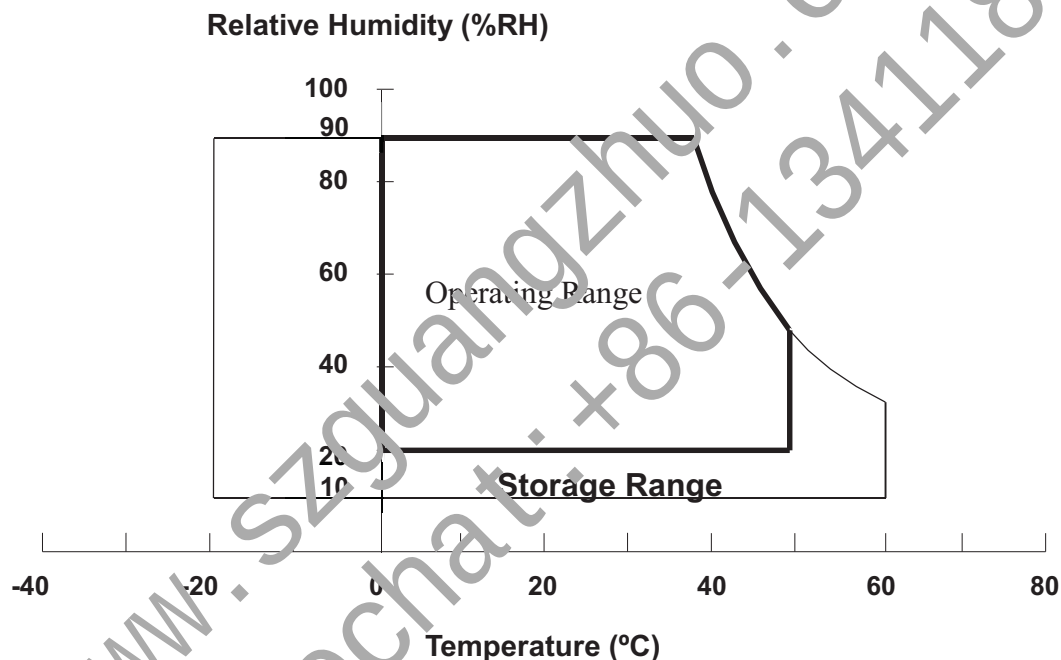
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (2)

Note (1) (a) 90 %RH Max. (Ta < 40 °C).

(b) Wet-bulb temperature should be 39 °C Max.

(c) No condensation.

Note (2) The temperature of panel surface should be 0 °C min. and 60 °C max.



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3.2 ELECTRICAL ABSOLUTE RATINGS

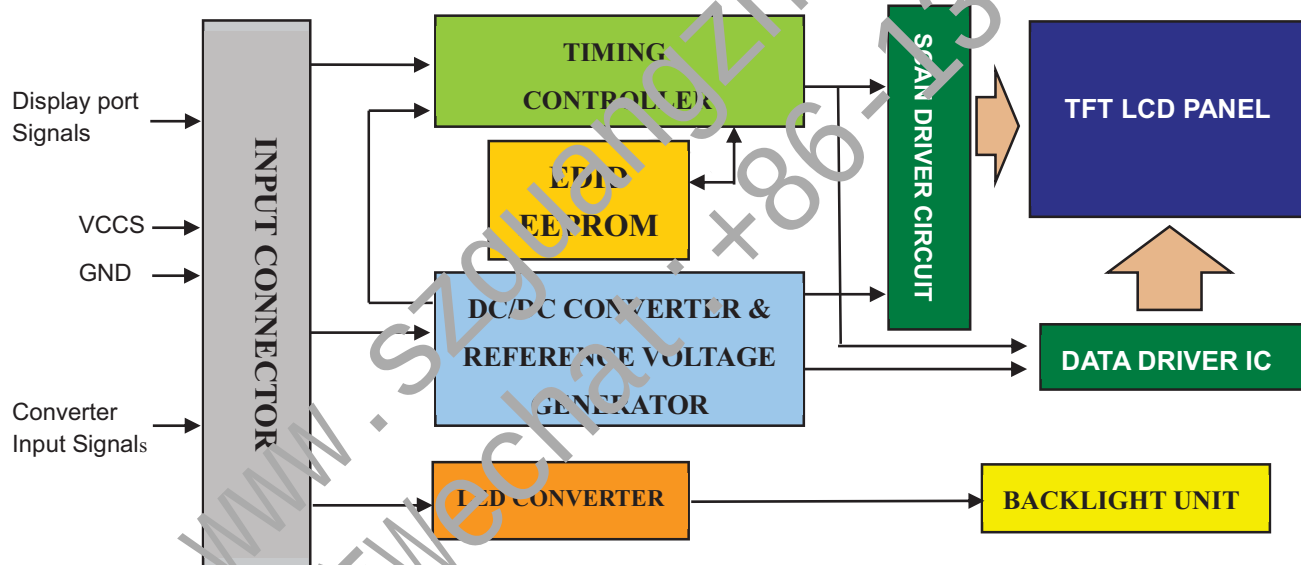
3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V _{IN}	-0.3	VCCS+0.3	V	
Converter Input Voltage	LED_VCCS	-0.3	26	V	(1)
Converter Control Signal Voltage	LED_PWM,	-0.3	3.6	V	(1)
Converter Control Signal Voltage	LED_EN	-0.3	3.6	V	(1)

Note (1) Stresses beyond those listed in above "ELECTRICAL ABSOLUTE RATINGS" may cause permanent damage to the device. Normal operation should be restricted to the conditions described in "ELECTRICAL CHARACTERISTICS".

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



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4.2. INTERFACE CONNECTIONS

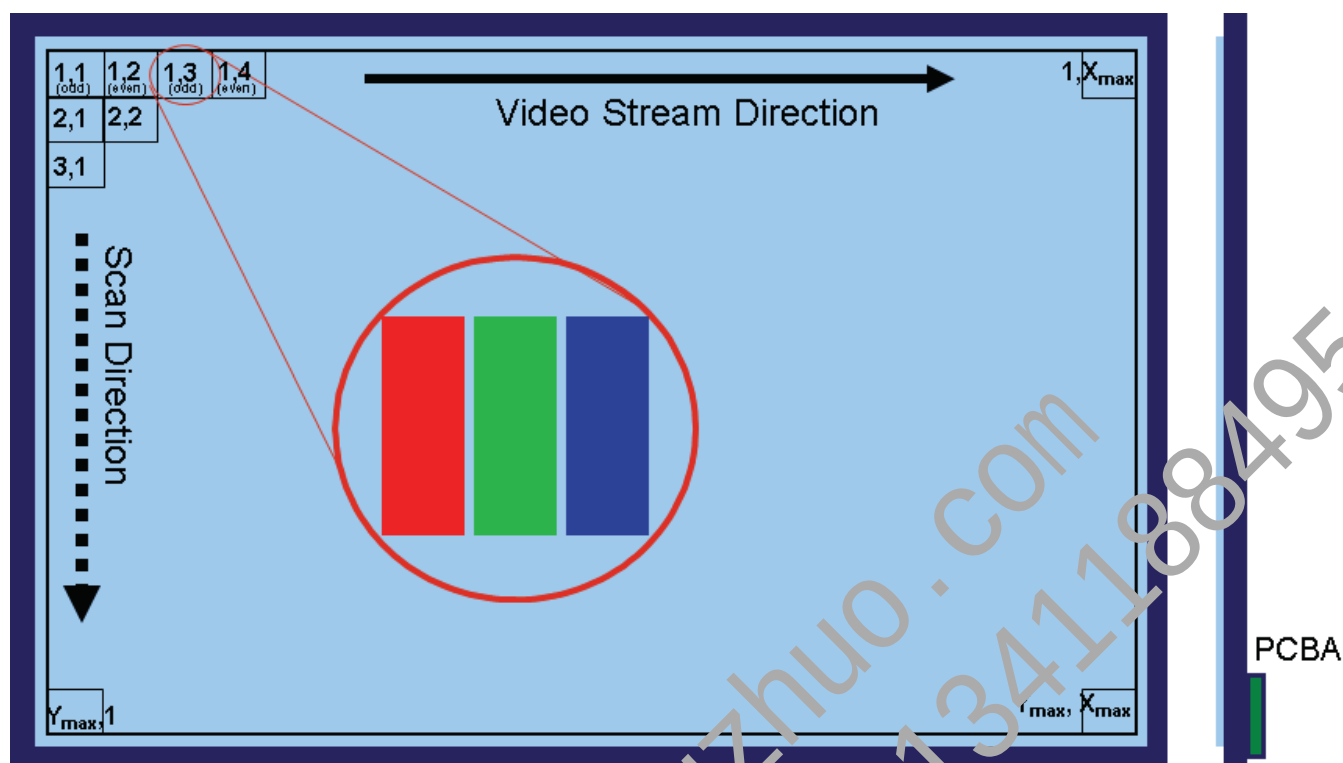
PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	CABC_EN	CABC Enable Input	Note (2)
2	H_GND	High Speed Ground	
3	Lane1_N	Complement Signal Link Lane 1	
4	Lane1_P	True Signal Link Lane 1	
5	H_GND	High Speed Ground	
6	Lane0_N	Complement Signal Link Lane 0	
7	Lane0_P	True Signal Link Lane 0	
8	H_GND	High Speed Ground	
9	AUX_CH_P	True Signal Auxiliary Channel	
10	AUX_CH_N	Complement Signal Auxiliary Channel	
11	H_GND	High Speed Ground	
12	VCCS	LCD logic and driver power	
13	VCCS	LCD logic and driver power	
14	BIST_EN	Panel Built In Self Test Enable	Note (2)
15	GND	LCD logic and driver ground	
16	GND	LCD logic and driver ground	
17	HPD	HPD signal pin	
18	BL_GND	Backlight ground	
19	BL_GND	Backlight ground	
20	BL_GND	Backlight ground	
21	BL_GND	Backlight ground	
22	LED_EN	Backlight on/off	
23	LED_PWM	System PWM signal input for dimming	
24	NC	No Connection (Reserved for LCD test)	
25	NC	No Connection (Reserved for LCD test)	
26	LED_VCCS	Backlight power	(Support 5.0 ~ 21V)
27	LED_VCCS	Backlight power	(Support 5.0 ~ 21V)
28	LED_VCCS	Backlight power	(Support 5.0 ~ 21V)
29	LED_VCCS	Backlight power	(Support 5.0 ~ 21V)
30	CE_EN	Color Engine Enable Input	Note (2)

Note (1) The first pixel is red as shown in the following figure.

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Note (2) The setting of CABC, BIST and Color engine function are as follows.

Pin	Enable	Disable
CABC_EN	Hi	Lo or Open
BIST_EN	Hi	Lo or Open
CE_EN	Hi	Lo or Open

Hi = High level, Lo = Low level.

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

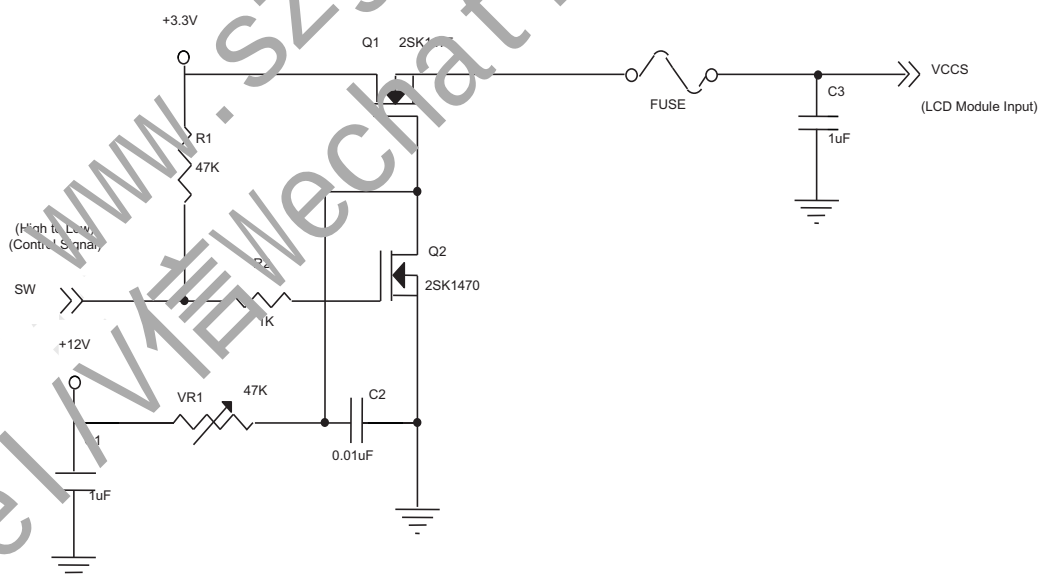
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)(7)
HPD	High Level		2.25	-	2.75	V	(6)
	Low Level		0	-	0.4	V	(6)
HPD Impedance		R _{HPD}	30K			ohm	(5)
Ripple Voltage		V _{RP}	-	-	100	mV	(1)
Inrush Current		I _{RUSH}	-	-	1.5	A	(1)(2)
Power Supply Current	Black	I _{CC}	-	100	120	mA	(3)
	Mosaic		-	105	137	mA	(3)
	Solid Pattern			149	158	mA	(3)
	Mosaic @PSR			105	137	mA	(3)a
	Solid Pattern @ PSR			149	158	mA	(3)a
Power per EBL WG		P _{EBL}		0.66		W	(4)

Note (1) The ambient temperature is $T_a = 25 \pm 2^\circ\text{C}$.

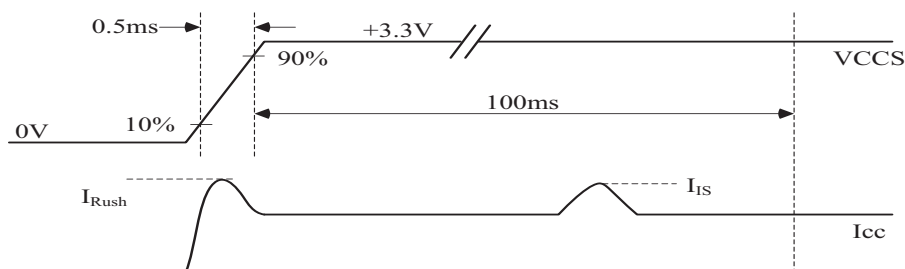
Note (2) I_{RUSH}: the maximum current when VCCS is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: White

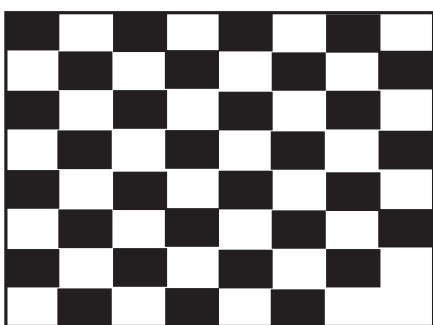


VCCS rising time is 0.5ms



Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, $T_a = 25 \pm 2^\circ\text{C}$, DC Current and $f_v = 60\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

1. Mosaic Pattern



Active Area

2. The solid pattern is the largest one of R/G/B pattern.

Note(3)a The specified power supply current is under the conditions at VCCS = 3.3 V, $T_a = 25 \pm 2^\circ\text{C}$, DC Current and PSR mode enable, whereas a power dissipation check pattern is displayed.

Note (4) The specified power are the sum of LCD panel electronics input power and the converter input power. Test conditions are as follows.

(a) VCCS = 3.3 V, $T_a = 25 \pm 2^\circ\text{C}$, $f_v = 60\text{ Hz}$,

(b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.

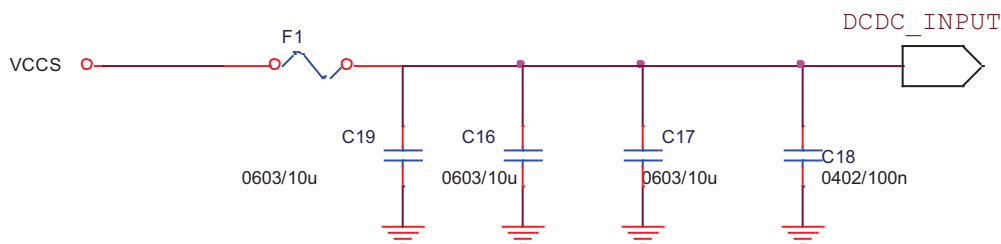
(c) Luminance: 60 nits.

Note (5) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. Please refer to Note (4) of 4.3.2 LED CONVERTER SPECIFICATION to obtain more information.

Note (6) When a source detects a low-going HPD pulse, it must be regarded as a HPD event. Thus, the source must read the link / sink status field or receiver capability field of the DPCD and take corrective action

Note (7) Input VCC Circuit is as below

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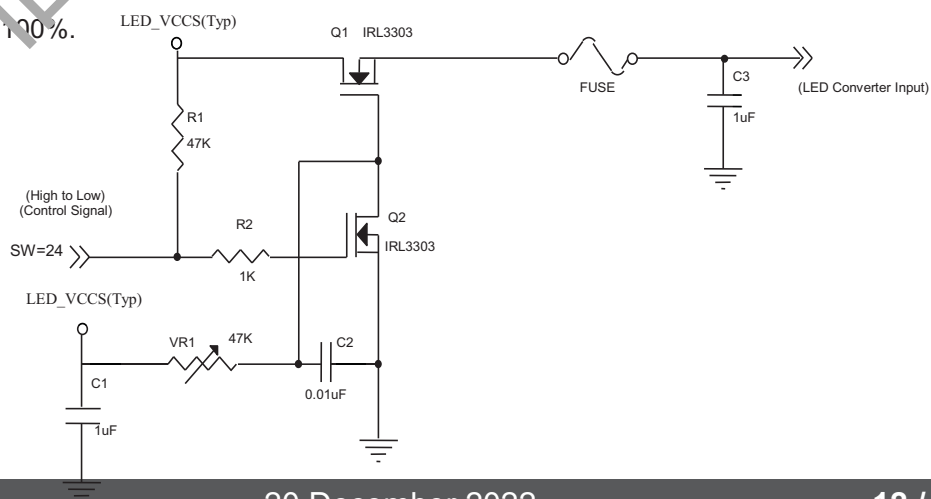
4.3.2 LED CONVERTER SPECIFICATION

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Converter Input Power Supply Voltage	LED_Vccs	5.0	12.0	24.0	V	
Converter Inrush Current	I _{LED_RUSH}	-	-	1.5	A	(1)
LED_EN Control Level	Backlight On	2.2	-	3.6	V	(4)
	Backlight Off	0	-	0.6	V	(4)
LED_EN Impedance	R _{LED_EN}	30K	-	-	ohm	(4)
PWM Control Level	PWM High Level	2.2	-	3.6	V	(4)
	PWM Low Level	0	-	0.6	V	(4)
PWM Impedance	R _{PWM}	30K	-	-	ohm	(4)
PWM Control Duty Ratio		5	-	100	%	(5)
PWM Control Permissible Ripple Voltage	V _{PWM_pp}	-	-	100	mV	
PWM Control Frequency	f _{PWM}	190	-	2K	Hz	(2)
LED Power Current (LED_VCCS = Typ.)	I _{LED}	150	180	192	mA	(3)

Note (1) I_{LED_RUSH}: the maximum current when LED_VCCS is rising,

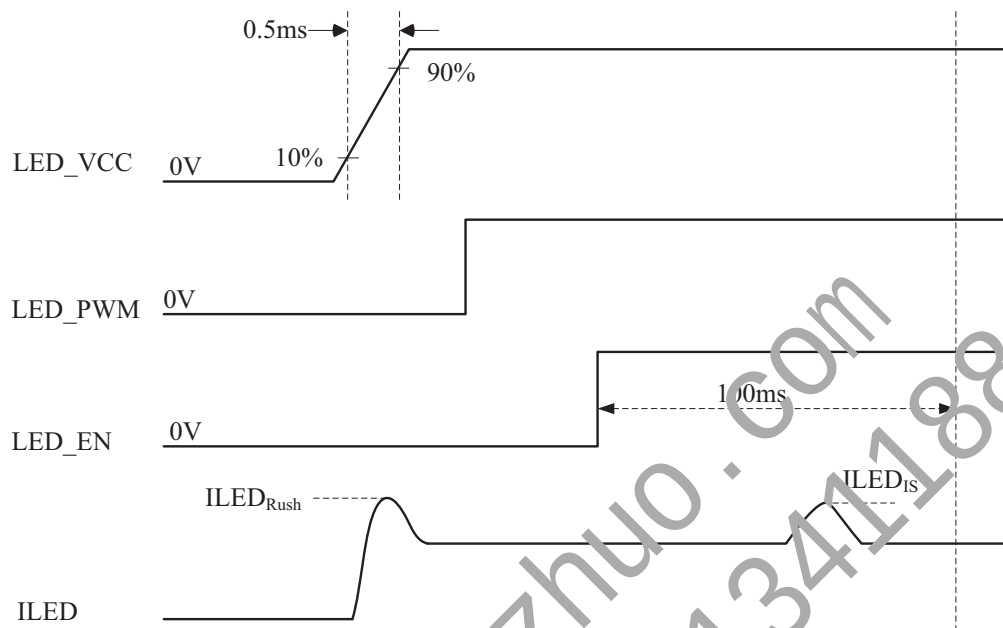
I_{LED}: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 °C, f_{PWM} = 200 Hz, Duty=100%.



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VLED rising time is 0.5ms



Note (2) If PWM control frequency is applied in the range less than 1KHz, the “waterfall” phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

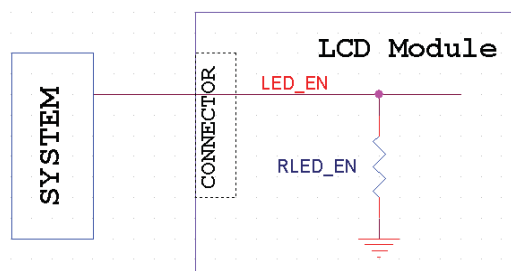
$$(N + 0.33) * f \leq f_{PWM} \leq (N + 0.66) * f$$

N : integer ($N \geq 3$)

f : Frame rate

Note (3) The specified LED power supply current is under the conditions at “LED_VCCS = Typ.”, $T_a = 25 \pm 2^\circ\text{C}$, $f_{PWM} = 200\text{ Hz}$, Duty= 100%.

Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. For example, the figure below describes the equivalent pull down impedance of LED_EN (If it exists, The rest pull down impedances of other signals (eg. HPD, PWM ...) are in the same concept.



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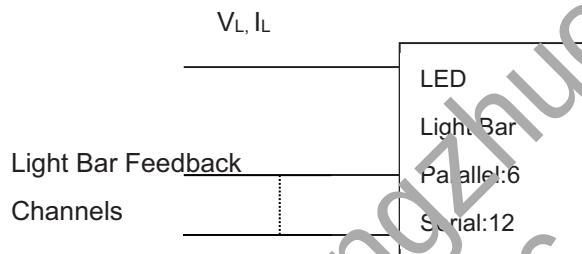
Note (5) If the cycle-to-cycle difference of PWM duty exceeds 0.1%, especially when the PWM duty is low, slight brightness change might be observed.

4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 °C

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	VL	32.4	34.8	36	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	IL	--	54	--	mA	
Power Consumption	PL	-	1.88	1.95	W	(3)
LED Life Time	LBL	15000	--	--	Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below.



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ± 2 °C and IL = 9 mA (Per EA) until the brightness becomes ≤ 50% of its original value.

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4.4 DISPLAY PORT SIGNAL TIMING SPECIFICATION

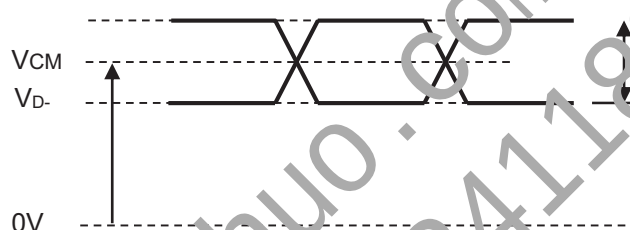
4.4.1 DISPLAY PORT INTERFACE

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Signal Common Mode Voltage(MainLink and AUX)	VCM	0		2	V	(1)(4)
AUX AC Coupling Capacitor	C_Aux_Source	75		200	nF	(2)
Main Link AC Coupling Capacitor	C_ML_Source	75		200	nF	(3)

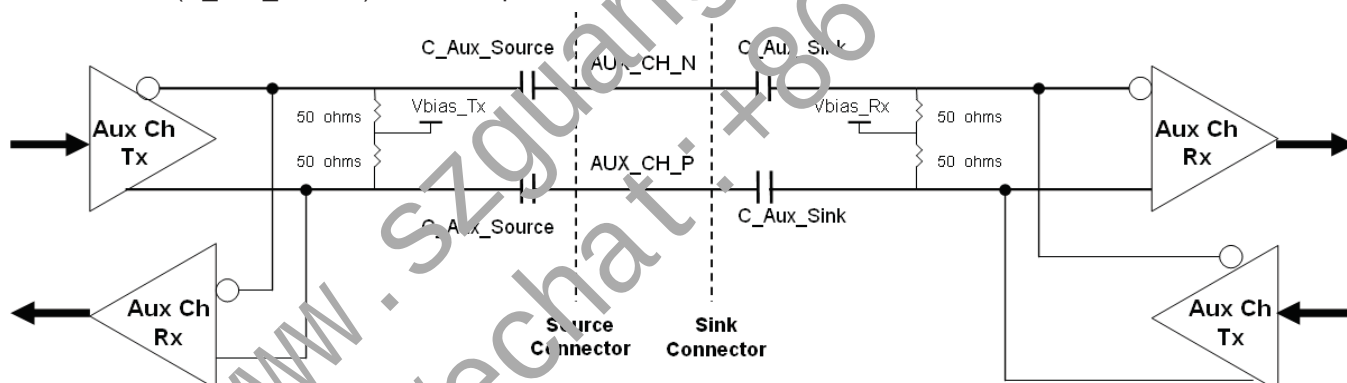
Note (1) Display port interface related AC coupled signals are following VESA DisplayPort Standard

Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2. There are many optional items described in eDP1.2. If some optional item is requested, please contact us.

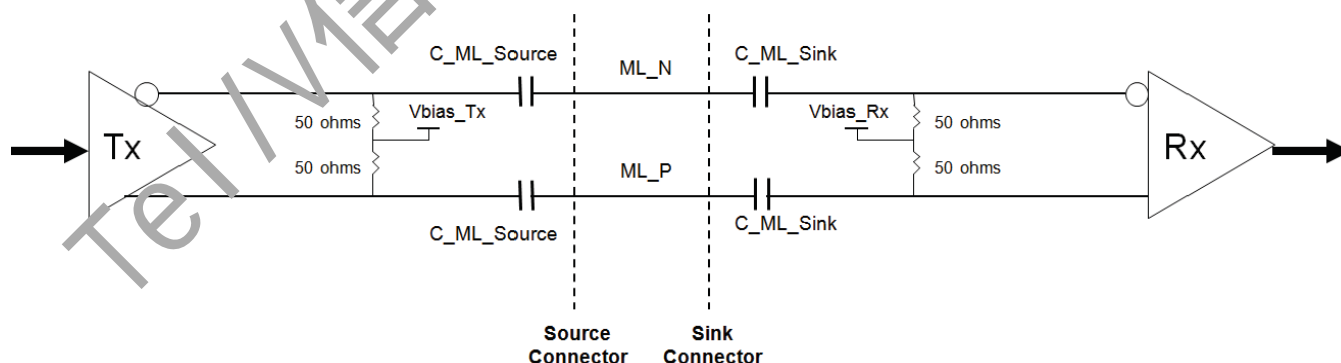
Single Ended



(2) Recommended eDP AUX Channel topology is as below and the AUX AC Coupling Capacitor (C_Aux_Source) should be placed on the source device.



(3) Recommended Main Link Channel topology is as below and the Main Link AC Coupling Capacitor (C_ML_Source) should be placed on the source device.



(4) The source device should pass the test criteria described in DisplayPort Compliance Test Specification (CTS) 1.1

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4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

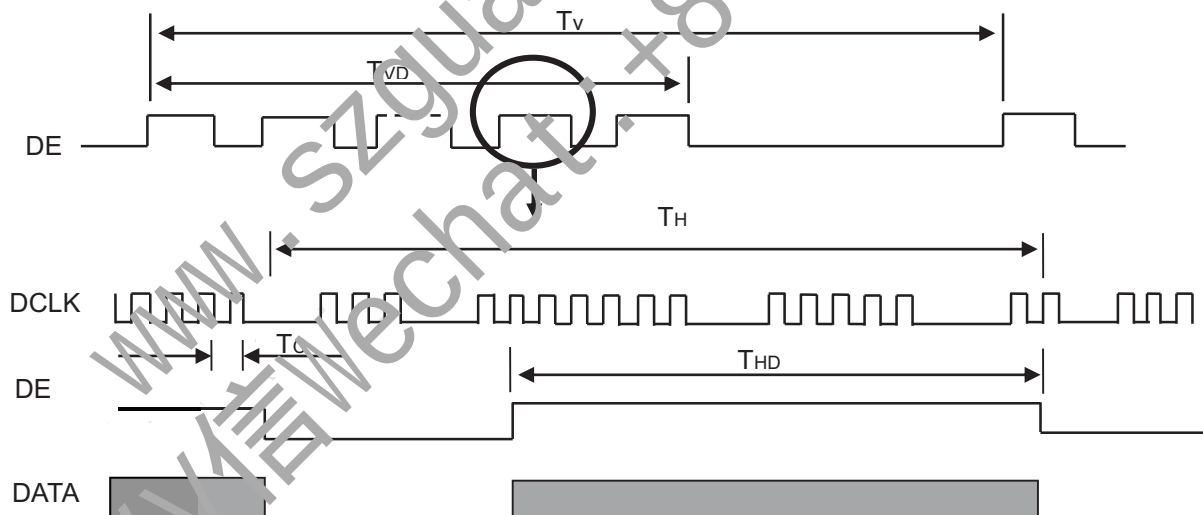
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	153.49	154.26	155.03	MHz	-
DE	Vertical Total Time	TV	1230	1236	1242	TH	-
	Vertical Active Display Period	TVD	1200	1200	1200	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	32	TV-TVD	TH	-
	Horizontal Total Time	TH	2070	2080	2090	Tc	-
	Horizontal Active Display Period	THD	1920	1920	1920	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	160	TH-THD	Tc	-

Refresh rate 48Hz (Power Saving Mode)

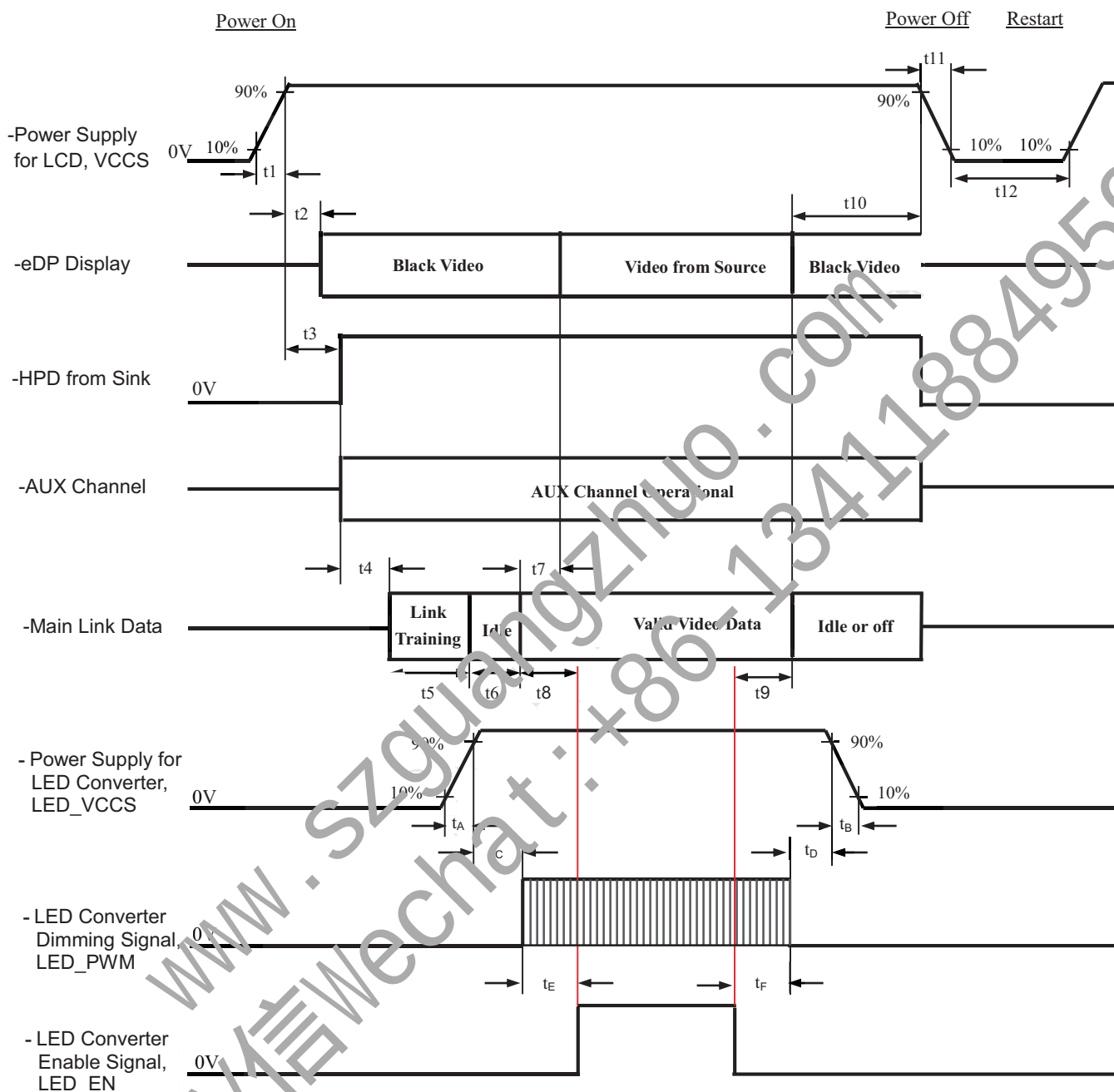
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	153.49	154.26	155.03	MHz	-
DE	Vertical Total Time	TV	1538	1545	1552	TH	-
	Vertical Active Display Period	TVD	1200	1200	1200	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	345	TV-TVD	TH	-
	Horizontal Total Time	TH	2070	2080	2090	Tc	-
	Horizontal Active Display Period	THD	1920	1920	1920	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	160	TH-THD	Tc	-

Note (1) The panel can operate at 60Hz normal mode and power saving mode, respectively. All reliability tests are based on specific timing of 60Hz refresh rate. We can only assure the panel's electrical function at power saving mode.

INPUT SIGNAL TIMING DIAGRAM



4.6 POWER ON/OFF SEQUENCE



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Timing Specifications

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	Power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t2	Delay from LCD,VCCS to black video generation	Sink	0	200	ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source (see Notes:2 and 3 below)
t3	Delay from LCD,VCCS to HPD high	Sink	0	200	ms	Sink AUX Channel must be operational upon HPD high (see Note:4 below)
t4	Delay from HPD high to link training initialization	Source	0	-	ms	Allows for Source to read Link capability and initialize
t5	Link training duration	Source	0	-	ms	Dependent on Source link training protocol
t6	Link idle	Source	0	-	ms	Min Accounts for required BS-Idle pattern. Max allows for Source frame synchronization
t7	Delay from valid video data from Source to video on display	Sink	0	50	ms	Max value allows for Sink to validate video data and timing. At the end of T7, Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and Sink will no longer generate automatic Black Video
t8	Delay from valid video data from Source to backlight on	Source	80	-	ms	Source must assure display video is stable *: Recommended by INX. To avoid garbage image.
t9	Delay from backlight off to end of valid video data	Source	50	-	ms	Source must assure backlight is no longer illuminated. At the end of T9, Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and Sink will automatically display Black Video. (See Notes: 2 and 3 below) *: Recommended by INX. To avoid garbage image.
t10	Delay from end of valid video data from Source to power off	Source	0	500	ms	Black video will be displayed after receiving idle or off signals from Source
t11	VCCS power rail fall time, 90% to 10%	Source	0.5	10	ms	-

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t12	VCCS Power off time	Source	500	-	ms	-
t _A	LED power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t _B	LED power rail fall time, 90% to 10%	Source	0	10	ms	-
t _C	Delay from LED power rising to LED dimming signal	Source	1	-	ms	-
t _D	Delay from LED dimming signal to LED power falling	Source	1	-	ms	-
t _E	Delay from LED dimming signal to LED enable signal	Source	0	-	ms	-
t _F	Delay from LED enable signal to LED dimming signal	Source	0	-	ms	-

Note (1) Please don't plug or unplug the interface cable when system is turned on.

Note (2) The Sink must include the ability to automatically generate Black Video autonomously. The Sink must automatically enable Black Video under the following conditions:

- Upon LCDVCC power-on (within T2 max)
- When the "NoVideoStream_Flag" (VB-ID Bit 3) is received from the Source (at the end of T9)

Note (3) The Sink may implement the ability to disable the automatic Black Video function, as described in Note (2), above, for system development and debugging purposes.

Note (4) The Sink must support AUX Channel polling by the Source immediately following LCDVCC power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to response to an AUX Channel transaction with the time specified within T3 max.

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5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	3.2	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I _L	54	mA

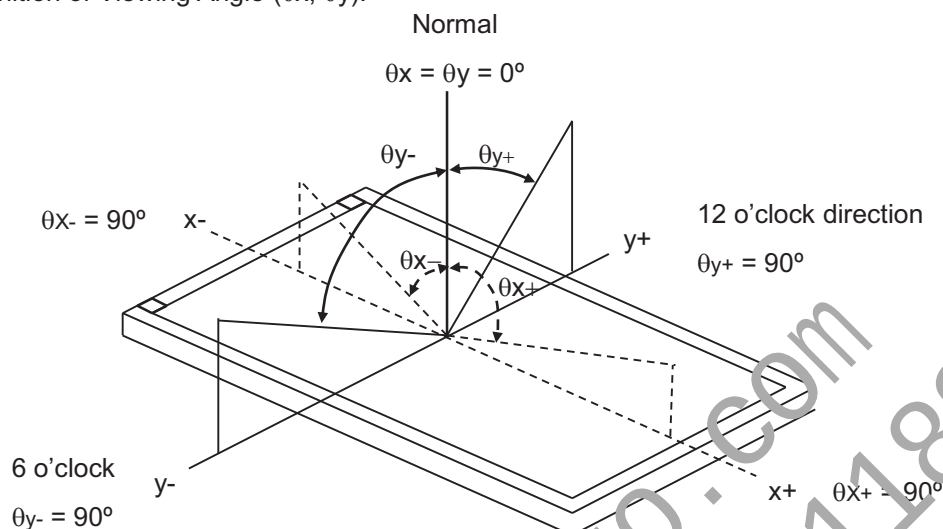
The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing Normal Angle	1000	1200	-	-	(2), (5),(7)
Response Time		T _R		-	16	19	ms	(3),(7)
		T _F		-	14	16	ms	
Average Luminance of White		L _{Ave}		340	400	-	cd/m ²	(4), (6),(7)
Color Chromaticity	Red	R _x	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing Normal Angle CIE1931	Typ - 0.03	0.640	Typ + 0.03	-	(1),(7)
		R _y			0.330		-	
	Green	G _x			0.300		-	
		G _y			0.600		-	
	Blue	B _x			0.150		-	
		B _y			0.060		-	
	White	W _x			0.313		-	
		W _y			0.329		-	
Color Gamut	sRGB	C.G	96	100	--	%	(8)	
Viewing Angle	Horizontal	θ_{x+}	CR≥10	80	89	-	Deg.	(1),(5), (7)
		θ_{x-}		80	89	-		
	Vertical	θ_{y+}		80	89	-		
		θ_{y-}		80	89	-		
White Variation		δW_{50}	$\theta_x=0^\circ, \theta_y=0^\circ$	80	90	-	%	(5),(6), (7)
		δW_{3p}	$\theta_x=0^\circ, \theta_y=0^\circ$	65	75	-	%	
Low Blue Light		BLR	$\theta_x=0^\circ, \theta_y=0^\circ$	-	-	50	%	(1),(5), (9)
		CCT		5500	6500	7000	K	

PRODUCT SPECIFICATION

Note (1) Definition of Viewing Angle (θ_x , θ_y):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{255} / L_0$$

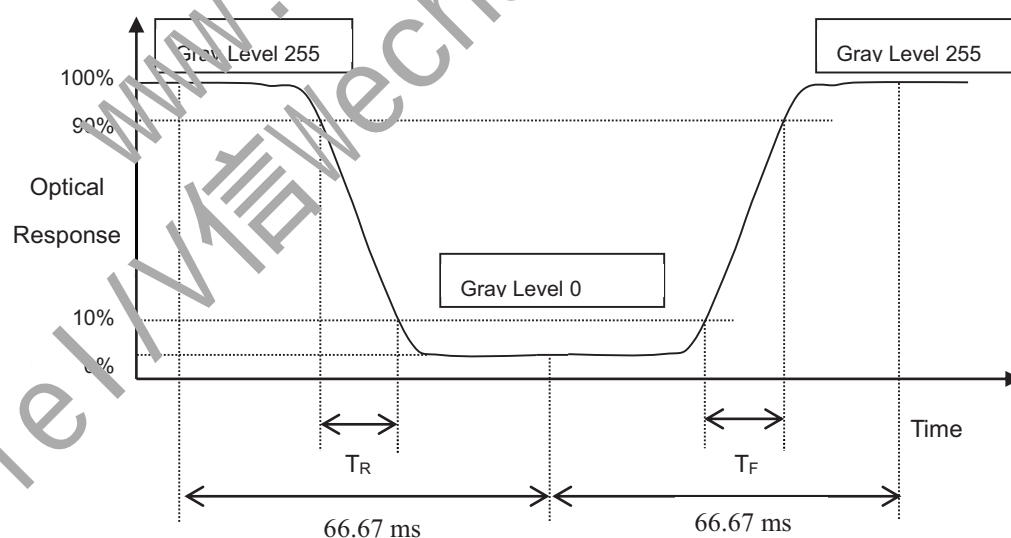
L_{255} : Luminance of gray level 255

L_0 : Luminance of gray level 0

$$CR = CR(1)$$

$CR(X)$ is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R , T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

Measure the luminance of White at 5 points

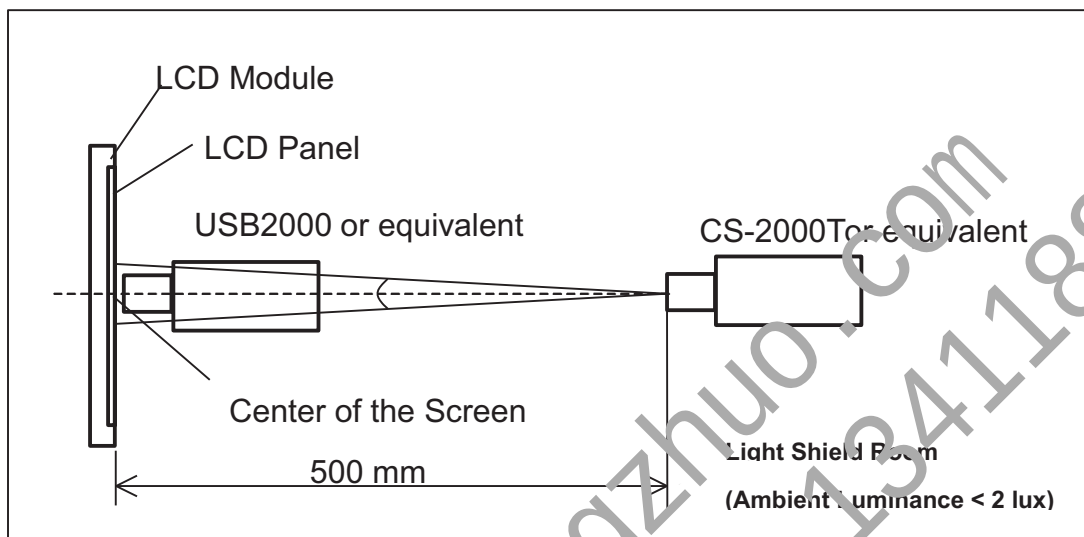
$$L_{AVE} = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$$

PRODUCT SPECIFICATION

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

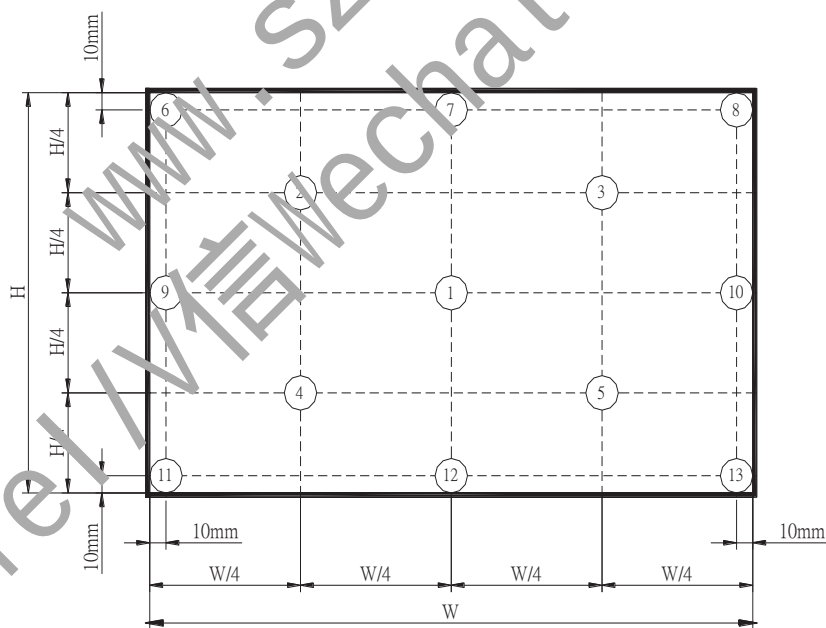


Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

$$\delta W_{5p} = \text{Minimum } [L(1) \sim L(5)] / \text{Maximum } [L(1) \sim L(5)] * 100\%$$

$$\delta W_{13p} = \text{Minimum } [L(1) \sim L(13)] / \text{Maximum } [L(1) \sim L(13)] * 100\%$$



⊗ : Test Point
X=1 to 13

Active area

Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

PRODUCT SPECIFICATION

Note (8) Definition of color gamut (C.G.%):

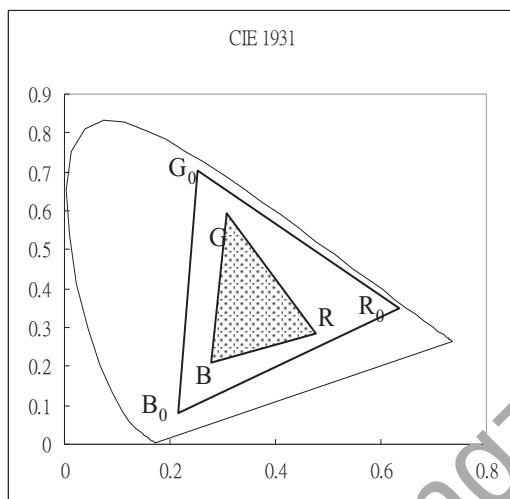
$$C.G.\% = \text{Area}(R, G, B) / \text{Area}(R_0, G_0, B_0) \times 100\%$$

R_0, G_0, B_0 : CIE1931 coordinates of red, green, and blue defined by sRGB.

R, G, B : CIE1931 coordinates of red, green, and blue in module at 255 gray level.

$\text{Area}(R_0, G_0, B_0)$: Area of the triangle defined by coordinate R_0, G_0, B_0 .

$\text{Area}(R, G, B)$: Area of the triangle defined by coordinate R, G, B .



Note (9) Definition of Blue Light Ratio (BLR)

Measure the luminance of gray level 255 at center points

$$\text{Blue Light Ratio (BLR)} = \left[\frac{\text{Range}(415 \sim 455 \text{ nm})}{\text{Range}(400 \sim 500 \text{ nm})} \right] \times 100\%$$

Range (415~455 nm): Light intensity between 415 nm and 455 nm

Range (400~500 nm): Light intensity between 400 nm and 500 nm

$$BLR = BLR(1)$$

BLR (%) is corresponding to the Blue Light Ratio of the point X at Figure in Note (6)

6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60°C, 240 hours	(1) (2)
Low Temperature Storage Test	-20°C, 240 hours	
Thermal Shock Storage Test	-20°C, 0.5hour ↔ 60°C, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	50°C, 240 hours	
Low Temperature Operation Test	0°C, 240 hours	
High Temperature & High Humidity Operation Test	50°C, 80% RH, 240 hours	

PRODUCT SPECIFICATION

ESD Test (Operation)	150pF, 330Ω, 1sec/cycle Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±15KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave, 1 time for each direction of ±X, ±Y, ±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

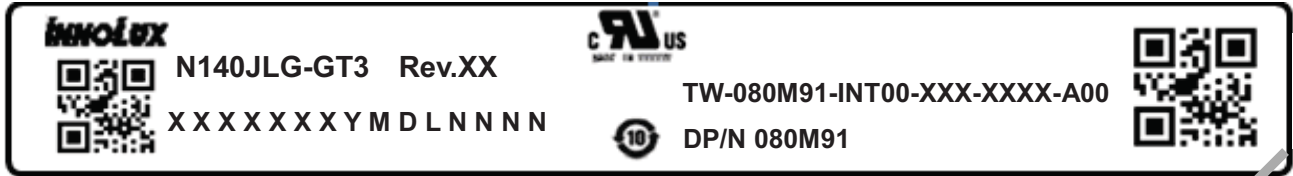
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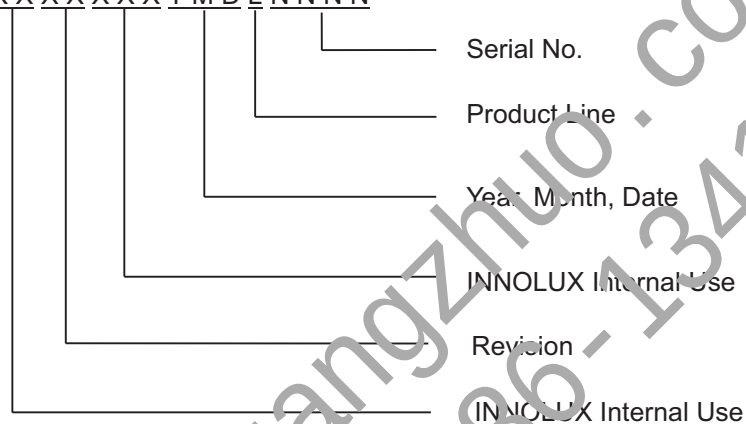
7. PACKING

7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: N140JLG-GT3
- (b) Revision: Rev. XX, for example: C1, C2 ...etc.
- (c) Serial ID: XXXXXYYMDLNNNN



- (d) Production Location: MADE IN XXXX.
- (e) UL logo: XXXX especially stands for panel manufactured by INNOLUX China satisfying UL requirement.

Serial ID includes the information as below:

- (a) Manufactured Date: Year: 0~9, for 2010~2019
 Month: 1~9, A~C, for Jan. ~ Dec.
 Day: 1~9, A~Y, for 1st to 31st, exclude I, O and U
- (b) Revision Code: cover all the change
- (c) Serial No.: Manufacturing sequence of product
- (d) Product Line: 1 -> Line1, 2 -> Line 2, ...etc.

Serial ID includes the information as below:

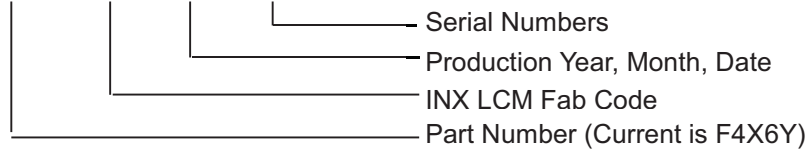
- (a) Manufactured Date: Year: 0~9, for 2010~2019
 Month: 1~9, A~C, for Jan. ~ Dec.
 Day: 1~9, A~Y, for 1st to 31st, exclude I, O and U
- (b) Revision Code: cover all the change
- (c) Serial No.: Manufacturing sequence of product
- (d) Product Line: 1 -> Line1, 2 -> Line 2, ...etc.

PRODUCT SPECIFICATION

(e) UL Logo : XXXX is UL factory ID.

(f) Dell 2D label contains information as below:

(f-1) Serial ID: TW-80M91-XXXXX-YMD-XXXX-ZZZ



(f-1-1) Corresponding LCM Fab code XXXXX is as below

- INZ00: Ningbo F3&F4, No.9, YangZiJiang North Road, Ningbo Bonded Zone, 315806, China

(f-2) Production location: Made in XXXX.

(f-3) ZZZ:Revision code: X00, X10, X20, A00..etc.

BUILD PHASE		REVISION
SST	(WS)	X00, X01, X02, ... X09
PT	(ES)	X10, X11, X12, ... X19
ST	(CS)	X20, X21, X23, ... X29
XB	(MP)	A00, A01, A02, ... A99

PRODUCT SPECIFICATION

7.2 DELL Carton LABEL

Dell carton label contains information as below:

PKG ID (3S) 04688-XXXXX-YMD-XXXXXX-080M91 -ZZ 		 REV A00
DP/N 	080M91 	 Vendor ID Loc ID 04688 XXXXX
BOX Qty ZZ 	MADE IN XXX 	 Mfg Id XXXXX

(a) PKG ID: 04688-XXXXX-YMD-XXXXXX-0SSSSS-ZZ



(b) Production location: Made in XXXX.

(c) Revision code: X00, X10, X20, A00..etc.

(d) BOX Quantity: ZZ

(e) DI/Loc ID & Mfg ID XXXXX INX LCM Fab Code

(e-1) Corresponding LCM Fab code XXXXX is as below

PRODUCT SPECIFICATION

7.2 CARTON

- (1) Box Dimensions : 445(L)*370(W)*275(H)
- (2) 24 modules/Carton

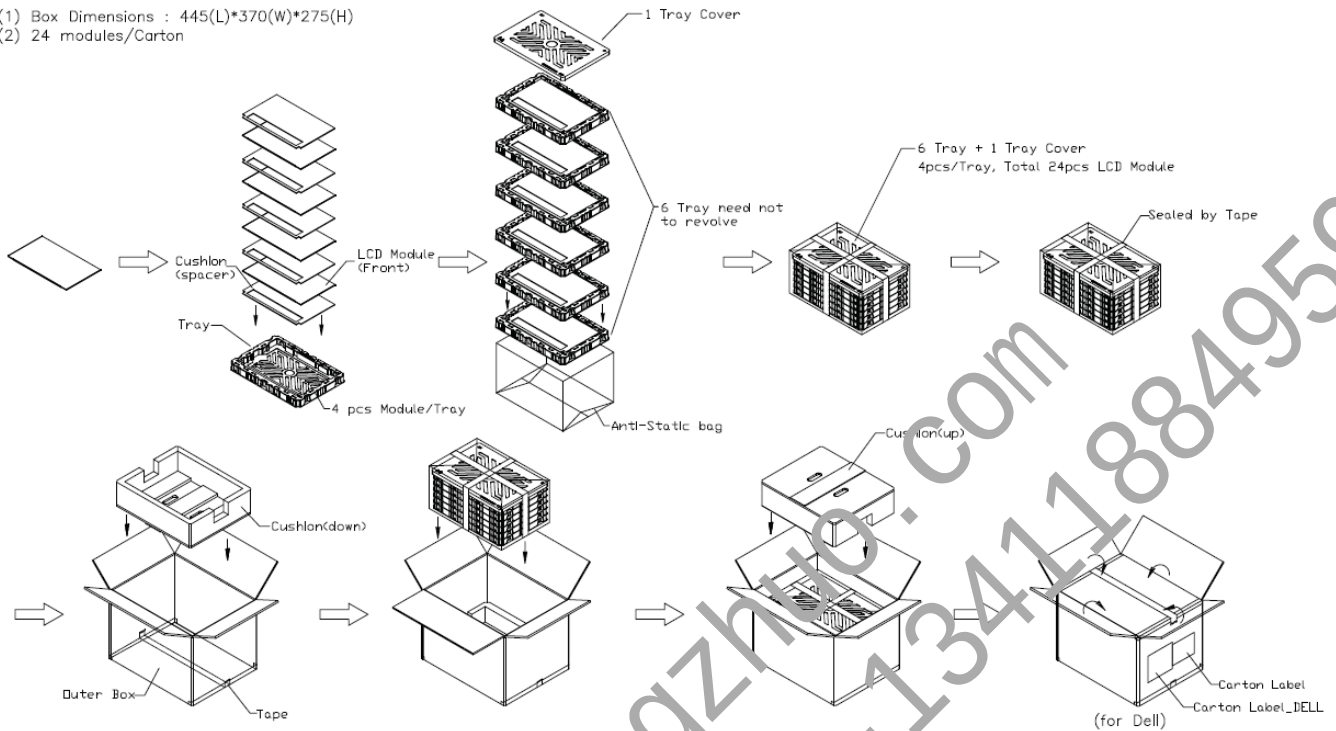


Figure. 7-2 Packing method

PRODUCT SPECIFICATION

7-3 PALLET

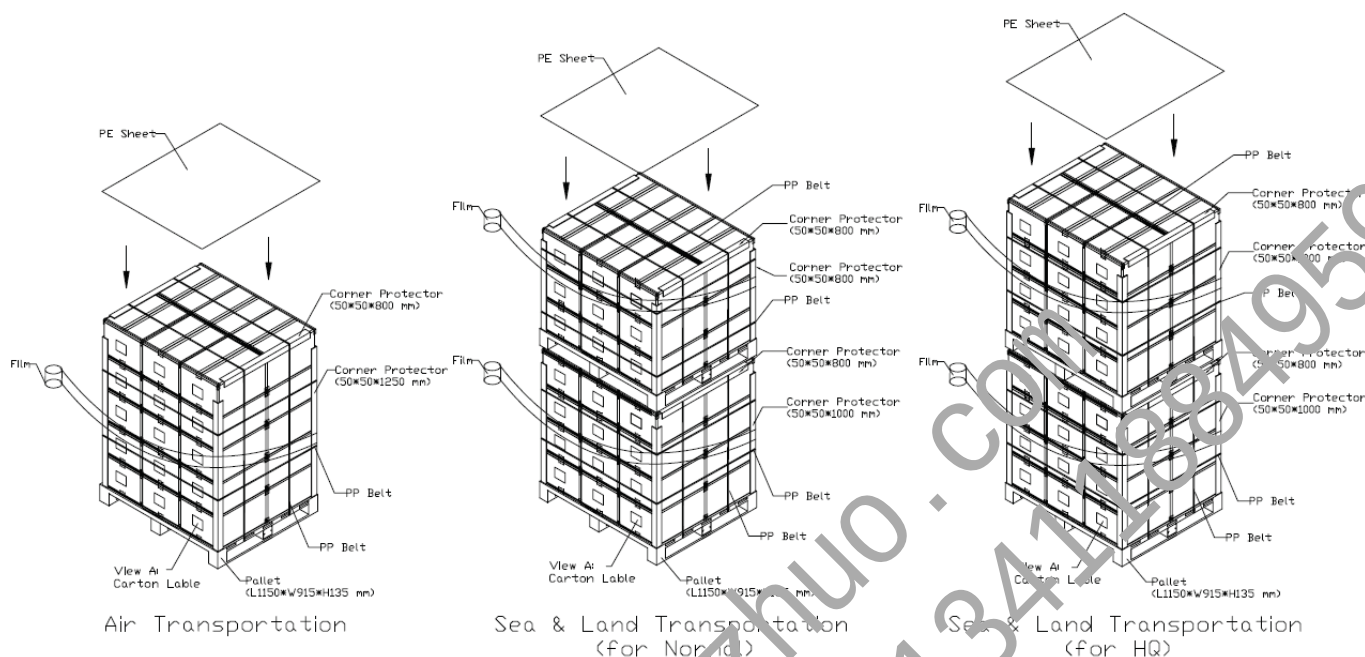


Figure. 7-3 Packing method

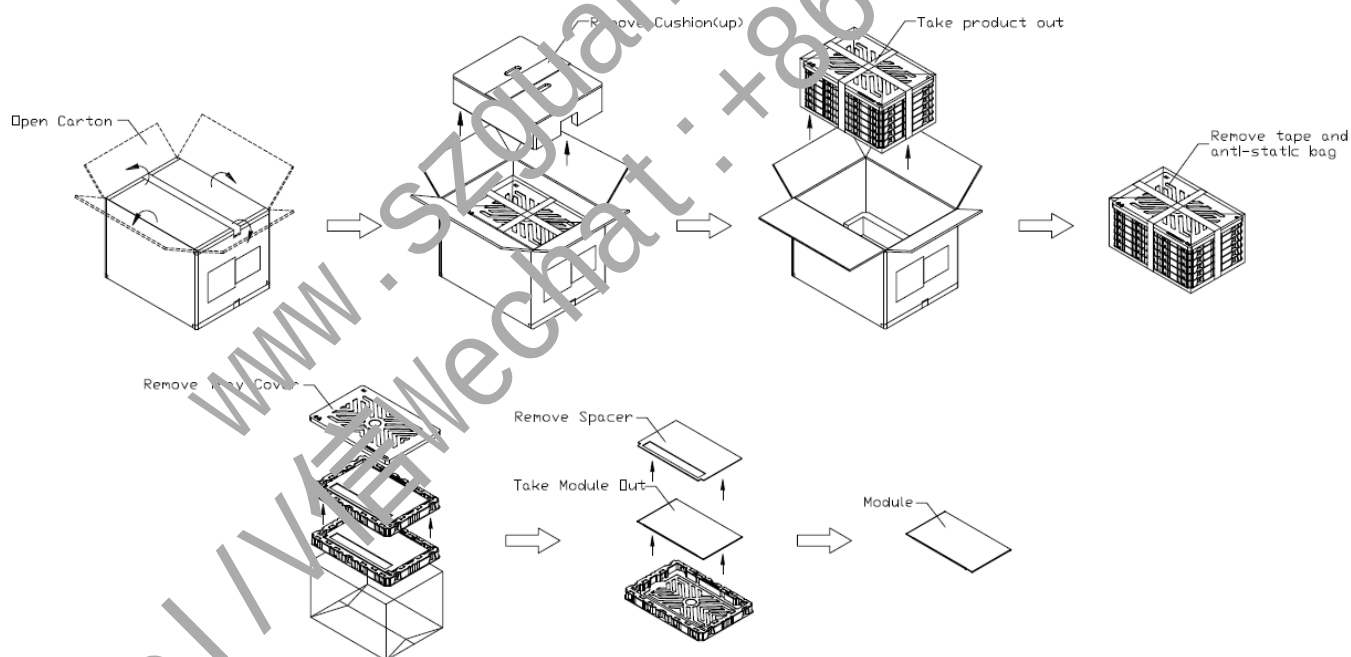


Figure. 7-3 Un-Packing method

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

- (1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.
- (2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
- (3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
- (5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
- (6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.
- (9) Do not disassemble the module.
- (10) Do not pull or fold the LED wire.
- (11) Pins of I/F connector should not be touched directly with bare hands.
- (12) Do not re-attach protective film onto the polarizer because of risk of bubble mura and dust.

8.2 STORAGE PRECAUTIONS

- (1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
- (3) It may reduce the display quality if the ambient temperature is lower than 10 °C. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

- (1) Do not pull the I/F connector in or out while the module is operating.
- (2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMIS LSI chips from damage during latch-up.
- (3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

Appendix. EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPD standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	00	Header	00	00000000
1	01	Header	FF	11111111
2	02	Header	FF	11111111
3	03	Header	FF	11111111
4	04	Header	FF	11111111
5	05	Header	FF	11111111
6	06	Header	FF	11111111
7	07	Header	00	00000000
8	08	ID system manufacturer name ("CMN")	0D	00001101
9	09	ID system manufacturer name	AE	10101110
10	0A	ID system Product Code (LSB)	5A	01011010
11	0B	ID system Product Code (MSB)	14	00010100
12	0C	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
13	0D	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
14	0E	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
15	0F	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
16	10	Week of manufacture (fixed week code)	24	00100100
17	11	Year of manufacture (fixed year code)	20	00100000
18	12	Version=1	01	00000001
19	13	Revision=4	04	00000100
20	14	Vedio Input Definition	A5	10100101
21	15	Active area horizontal ("30.150cm")	1E	00011110
22	16	Active area vertical ("10.85cm")	13	00010011
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("RGB Non-continous")	03	00000011
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	EE	11101110
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	95	10010101
27	1B	Rx=0.640	A3	10100011
28	1C	Ry=0.330	54	01010100
29	1D	Gx=0.300	4C	01001100
30	1E	Gy=0.600	99	10011001
31	1F	Bx=0.150	26	00100110
32	20	By=0.060	0F	00001111
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	No manufacturer's specific timing	01	00000001
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001

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40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("154.26"MHz, According to VESA CVT Rev1.4)	42	01000010
55	37	# 1 Pixel clock (hex LSB first)	3C	00111100
56	38	# 1 H active ("1920")	80	10000000
57	39	# 1 H blank ("160")	A0	10100000
58	3A	# 1 H active : H blank ("1920 : 160")	70	01110000
59	3B	# 1 V active ("1200")	B0	10110000
60	3C	# 1 V blank ("36")	24	00100100
61	3D	# 1 V active : V blank ("1200 : 36")	40	01000000
62	3E	# 1 H sync offset ("48")	30	00110000
63	3F	# 1 H sync pulse width ("32")	20	00100000
64	40	# 1 V sync offset : V sync pulse width ("10 : 6")	A6	10100110
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width	00	00000000
66	42	# 1 H image size ("301 mm")	2D	00101101
67	43	# 1 V image size ("188 mm")	BC	10111100
68	44	# 1 H image size : V image size	10	00010000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder	00	00000000
71	47	Non-interlaced, Normal Display, Digital separate, Positive Hsync, Negative Vsync	1A	00011010
72	48	Indicates that this 18 byte descriptor is a Display Descriptor	00	00000000
73	49	Indicates that this 18 byte descriptor is a Display Descriptor	00	00000000
74	4A	Set to 00h when 18 byte descriptor is used as a Display Descriptor	00	00000000
75	4B	Tag number for Display Range Limits Descriptor	FD	11111101
76	4C	Display Range Limits Offset : FLAGS	00	00000000
77	4D	Minimum Vertical Rate ("48Hz")	30	00110000
78	4E	Maximum Vertical Rate ("60Hz")	3C	00111100
79	4F	Minimum Horizontal Rate ("74KHz")	4A	01001010
80	50	Maximum Horizontal Rate ("74KHz")	4A	01001010
81	51	Maximum Pixel Clock ("154.26MHz")	0F	00001111
82	52	Video Timing Support Flags : Bytes 10 --> 17 indicate support for additional video timings	01	00000001
83	53	Line Feed (0Ah if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	0A	00001010

PRODUCT SPECIFICATION

84	54	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	20	00100000
85	55	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	20	00100000
86	56	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	20	00100000
87	57	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	20	00100000
88	58	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	20	00100000
89	59	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	20	00100000
90	5A	Flag	00	00000000
91	5B	Flag	00	00000000
92	5C	Flag	00	00000000
93	5D	Data Type Tag: Alphanumeric Data String (ASCII)	FF	11111110
94	5E	Flag	00	00000000
95	5F	Dell P/N 1st Character "8"	38	00111000
96	60	Dell P/N 2nd Character "0"	30	00110000
97	61	Dell P/N 3rd Character "M"	4D	01001101
98	62	Dell P/N 4th Character "9"	39	00111001
99	63	Dell P/N 5th Character "1"	31	00110001
100	64	EDID Revision	80	00000000
101	65	Manufacturer P/N "1"	31	00110001
102	66	Manufacturer P/N "4"	34	00110100
103	67	Manufacturer P/N "0"	30	00110000
104	68	Manufacturer P/N "J"	4A	01001010
105	69	Manufacturer P/N "L"	4C	01001100
106	6A	Manufacturer P/N "G"	47	01000111
107	6B	New line character indicates end of ASCII string	0A	00001010
108	6C	Flag	00	00000000
109	6D	Flag	00	00000000
110	6E	Flag	00	00000000
111	6F	Data Type Tag: Manufacturer Specified Data 00	00	00000000
112	70	Flag	00	00000000
113	71	Color Management	02	00000010
114	72	Panel Type and Revision	41	01000001
115	73	Frame Rate	11	00010001
116	74	Light Controller Interface and Maximum Luminance	A8	10101000
117	75	Front Surface / Polarizer and Pixel Structure	00	00000000
118	76	Multi-Media Features	00	00000000
119	77	Multi-Media Features	00	00000000
120	78	Special Features	00	00000000
121	79	Special Features	0A	00001010
122	7A	Special Features	41	01000001
123	7B	New line character indicates end of ASCII string	0A	00001010
124	7C	Padding with "Blank" character	20	00100000
125	7D	Padding with "Blank" character	20	00100000
126	7E	No extension	00	00000000



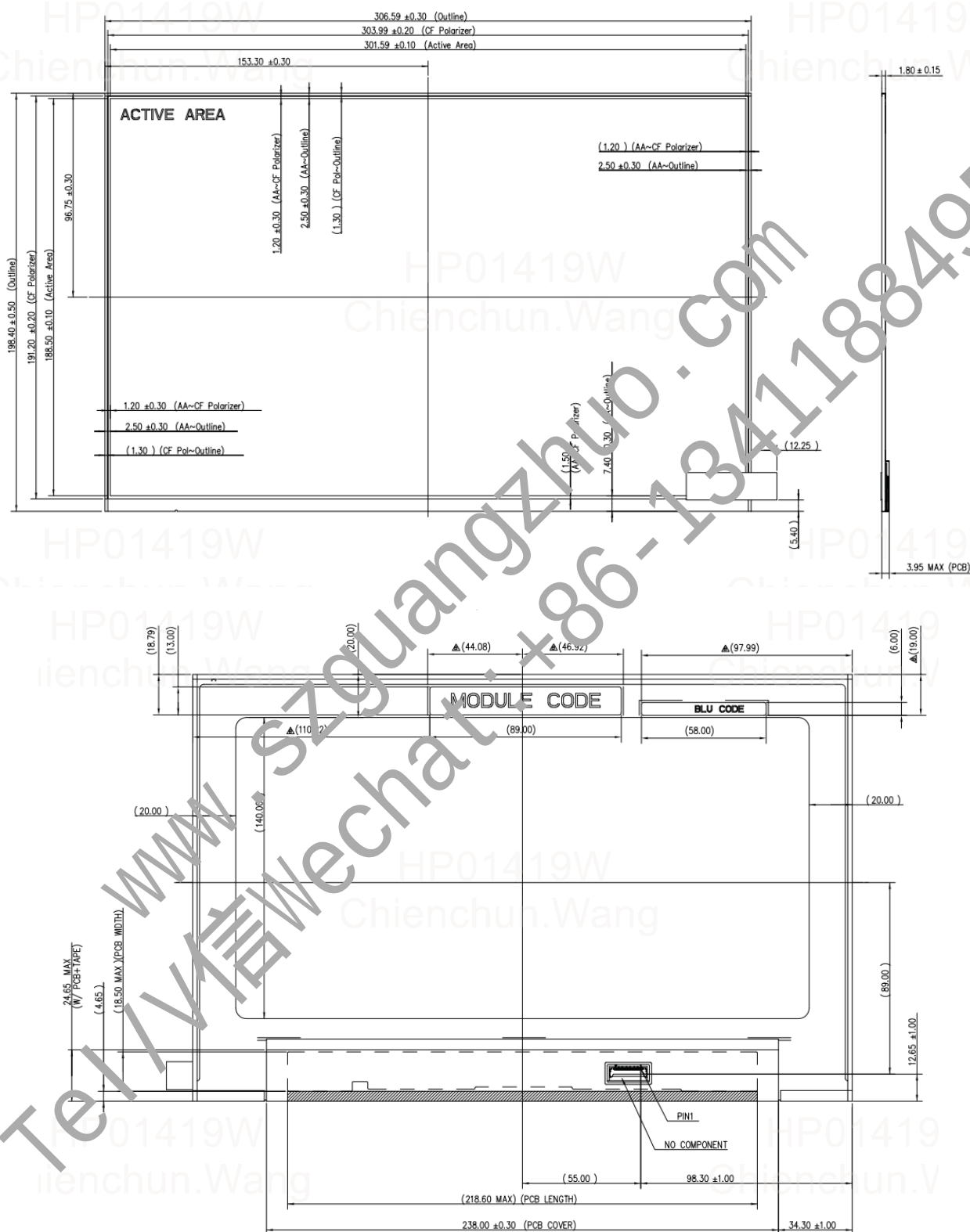
群創光電

PRODUCT SPECIFICATION

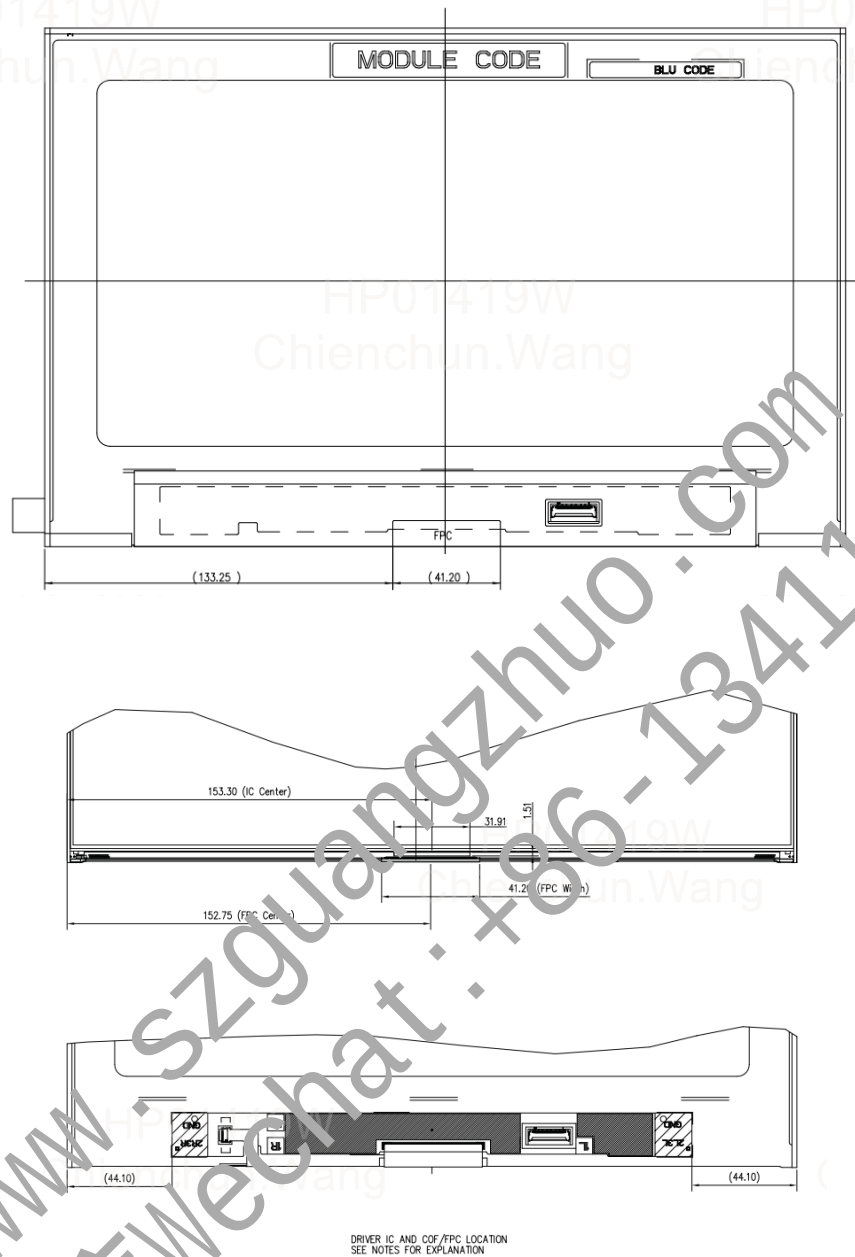
127	7F	Checksum	4E	11001110
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Appendix. OUTLINE DRAWING



PRODUCT SPECIFICATION



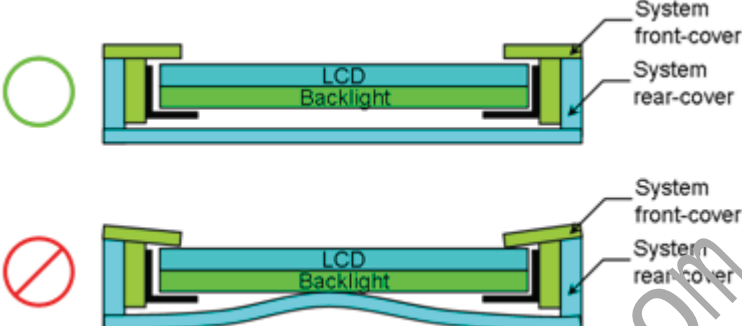
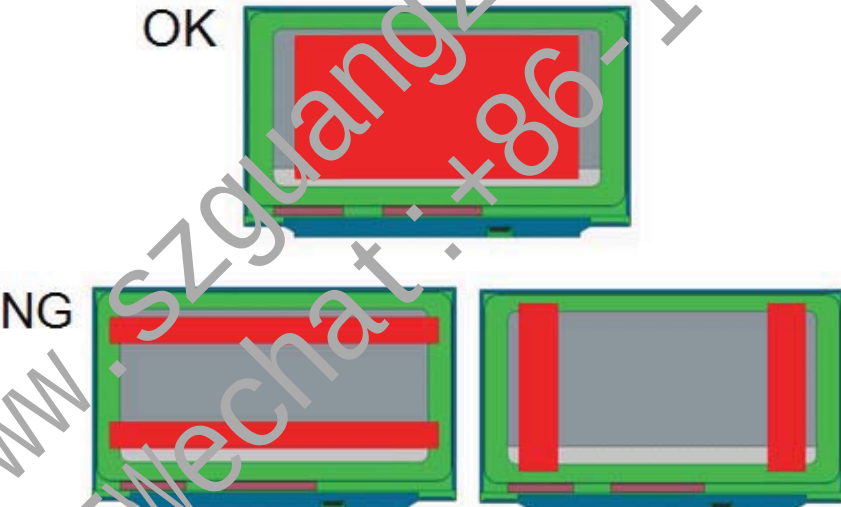
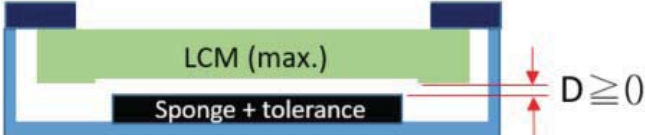
NOTES:

1. IN ORDER TO AVOID ABNORMAL DISPLAY, POOLING AND WHITE SPOT, NO OVERLAPPING IS SUGGESTED AT CABLES, ANTENNAS, CAMERA, WLAN, WAN OR FOREIGN OBJECTS OVER FPC, T-CON AND VR LOCATIONS.
2. ELP CONNECTOR IS MEASURED AT PIN1 AND ITS MATING LINE.
3. MODULE FLATNESS SPEC : 0.5 mm MAX.
4. "()" MARKS THE REFERENCE DIMENSION.
5. MEASUREMENT OF THICKNESS MUST BE MEASURED BY CALIPER OR MICROMETER.

Note. Dimensions measuring instruments as below,

1. Length/ Width/Thickness : Caliper
2. Height : Height gauge

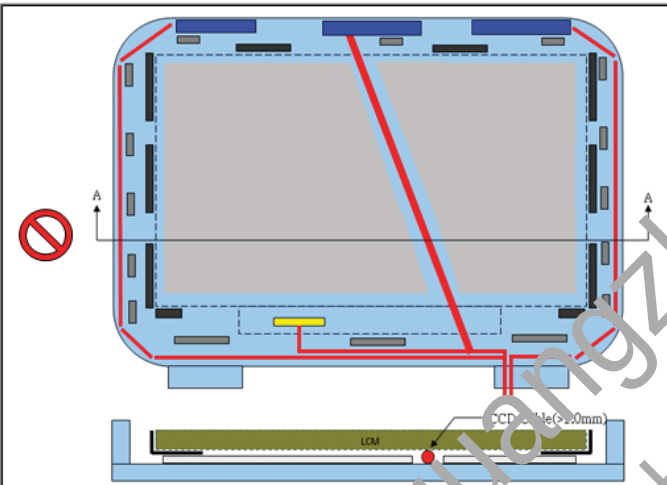
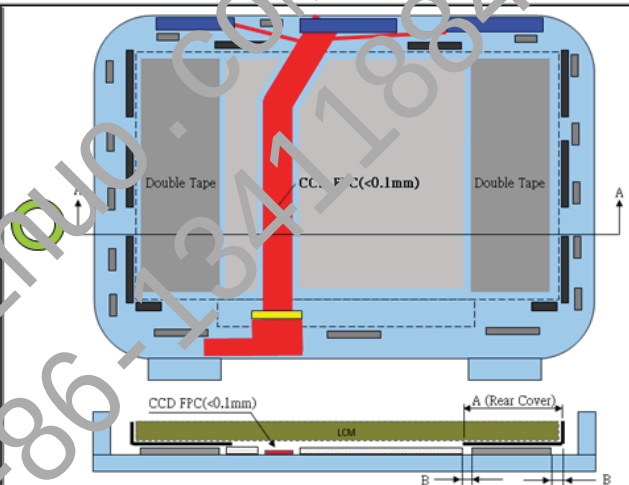
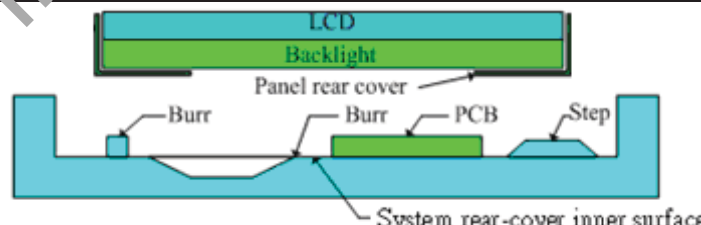
Appendix. SYSTEM COVER DESIGN GUIDANCE

0.	Permanent deformation of system cover after reliability test
	
Definition	System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
1	Sponge area design behind panel
	
Definition	Sponge area design behind panel can not be across the panel metal rear and the reflector at the same time. It can be on the reflector area only.
2	Gap between system rear-cover & panel
	
Definition	The maximum thickness of sponge on the system rear-cover can not interfere to the maximum thickness of panel. Because the interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.

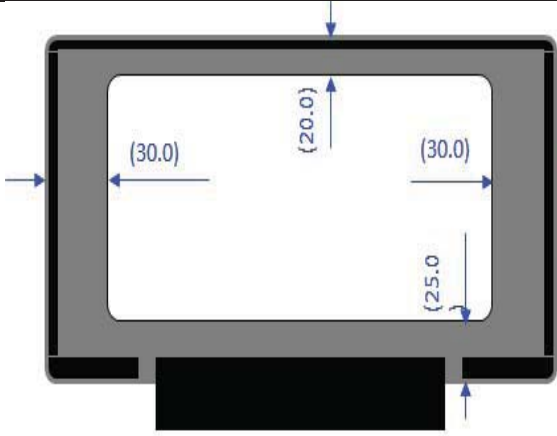
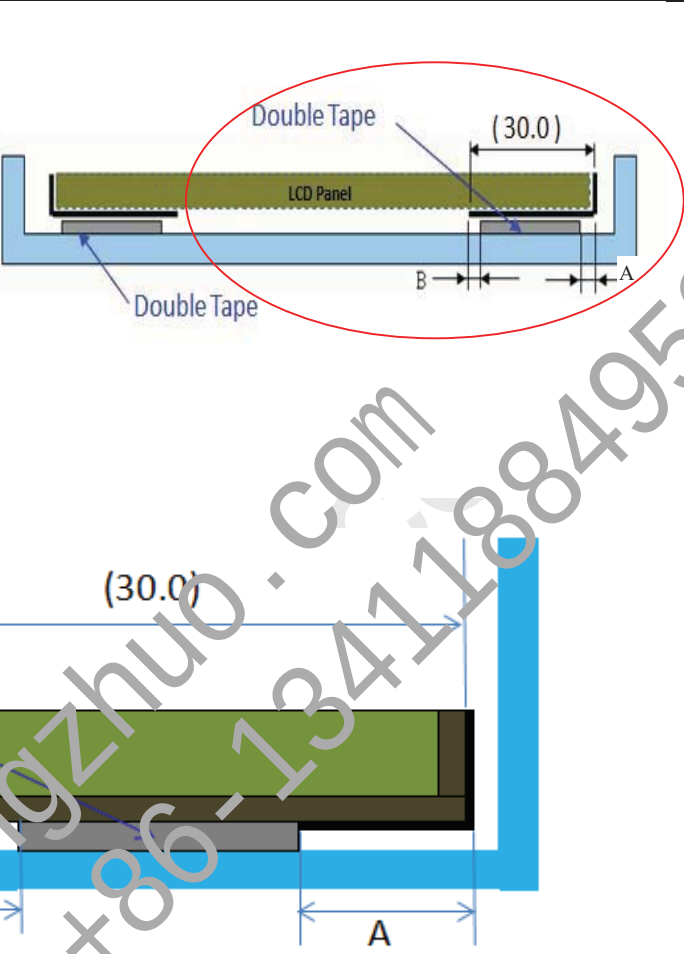
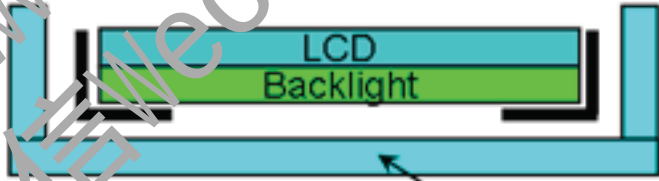
PRODUCT SPECIFICATION

3	Gap Design between panel & around structure												
<table><tr><th>Item</th><th>Suggestion</th><th>Remark</th></tr><tr><td>A1</td><td>$A1 \geq 0.5$</td><td rowspan="4">Gap $\geq$ Panel outline max. tolerance + Assembly max. tolerance</td></tr><tr><td>A2</td><td>$A2 \geq 0.5$</td></tr><tr><td>B1</td><td>$B1 \geq 0.5$</td></tr><tr><td>B2</td><td>$B2 \geq 0.8$</td></tr></table>		Item	Suggestion	Remark	A1	$A1 \geq 0.5$	Gap $\geq$ Panel outline max. tolerance + Assembly max. tolerance	A2	$A2 \geq 0.5$	B1	$B1 \geq 0.5$	B2	$B2 \geq 0.8$
Item	Suggestion	Remark											
A1	$A1 \geq 0.5$	Gap $\geq$ Panel outline max. tolerance + Assembly max. tolerance											
A2	$A2 \geq 0.5$												
B1	$B1 \geq 0.5$												
B2	$B2 \geq 0.8$												
Definition	Gap Design between panel & around structure needs to consider the maximum tolerances of panel outline and assembly at the same time. Gap Design suggestion is shown as A1/A2/B1/B2 on the chart.												
4	Gap between panel & bezel												
Definition	The gap between system bezel & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system front-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test, or during pooling inspection procedure. To remain the sufficient gap, design with system rib higher than maximum panel thickness is recommended. The sufficient gap design is greater or equal to 0.1mm.												
5	Cable routing behind panel												

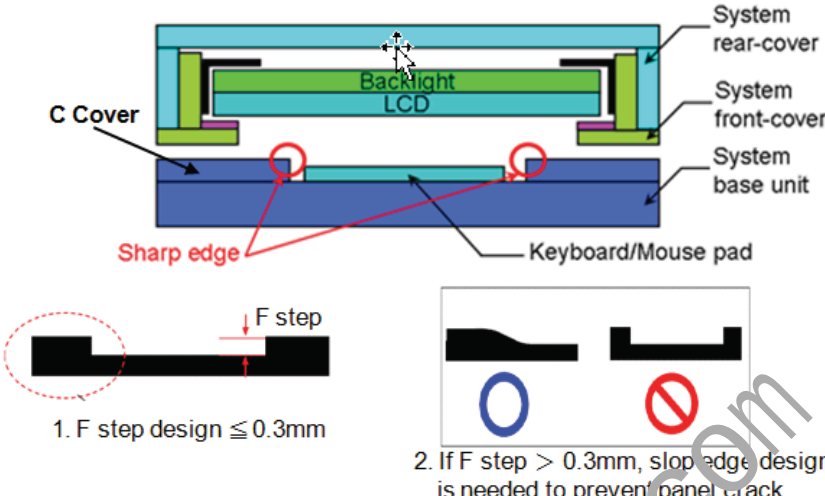
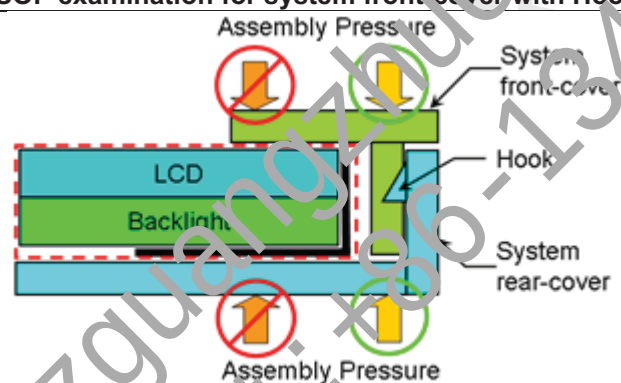
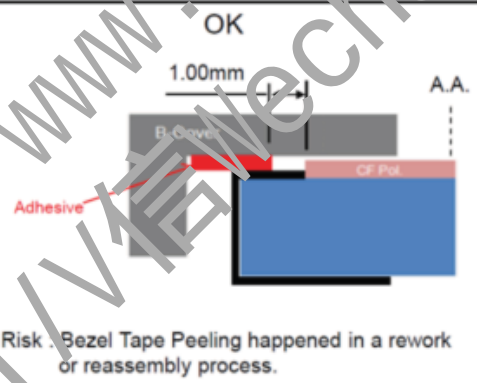
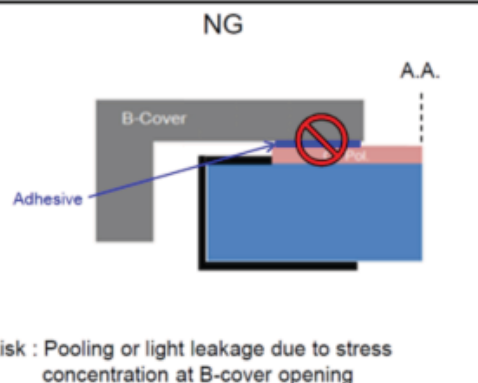
PRODUCT SPECIFICATION

Definition	It is strongly recommended that cables route around the panel outline, not overlap with the panel outline (including PCB). Because issue such as abnormal display & white spot after backpack test, hinge test, twist test or pogo test may occur. If any routings across panel outline are needed, we suggest design as below: -Using FFC/FPC to replace cables. -Routing at the right or left area of panel metal rear. -Avoid any routings at the step of panel or A cover. -No interference to panel. -It should not overlap TCON, COF/FPC, Driver IC												
6	Interference examination of antenna cable and Web Cam wire - To prevent panel damage, we suggest using CCD FPC to replace CCD cable - Using double tape to fix LCM module for no bracket design.   <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;"> Rear-cover Sponge Double Tape CCD Cable/FPC Hook Connector Camera/Antenna Stopper LCM Module Panel outline </td> <td style="width: 70%;"> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td>Rear Cover Width(A)</td><td>A = 30mm</td></tr> <tr> <td>Cover edge to Double Tape(B)</td><td>B = 3.0mm</td></tr> <tr> <td>CCD FPC thickness</td><td><0.1mm</td></tr> <tr> <td>Sponge thickness</td><td>0.5mm</td></tr> <tr> <td></td><td>0.2~0.3mm(compressed)</td></tr> </table> </td> </tr> </table>	Rear-cover Sponge Double Tape CCD Cable/FPC Hook Connector Camera/Antenna Stopper LCM Module Panel outline	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td>Rear Cover Width(A)</td><td>A = 30mm</td></tr> <tr> <td>Cover edge to Double Tape(B)</td><td>B = 3.0mm</td></tr> <tr> <td>CCD FPC thickness</td><td><0.1mm</td></tr> <tr> <td>Sponge thickness</td><td>0.5mm</td></tr> <tr> <td></td><td>0.2~0.3mm(compressed)</td></tr> </table>	Rear Cover Width(A)	A = 30mm	Cover edge to Double Tape(B)	B = 3.0mm	CCD FPC thickness	<0.1mm	Sponge thickness	0.5mm		0.2~0.3mm(compressed)
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	If the antenna cable or Web Cam wire must overlap with the panel outline, both sides of the antenna cable or Web Cam wire must have a sponge(Sponge material can not contain NH3) and sponge require higher antenna cable or Web Cam wire.(Antenna cable or Web Cam wire should not overlap with TCON,COF/FPC,Driver IC) Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.												
7	System rear-cover inner surface examination 												
Definition	Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.												
8	Tape/sponge design on system inner surface												

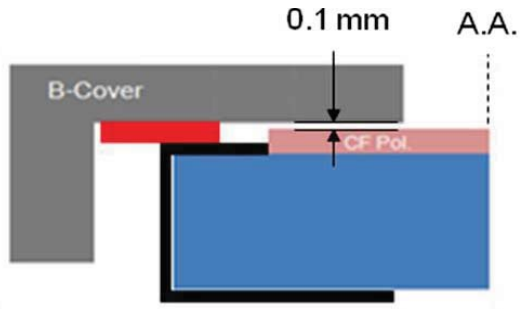
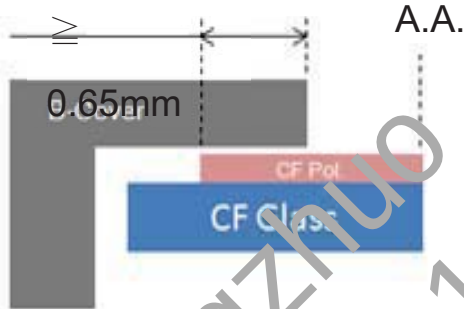
PRODUCT SPECIFICATION

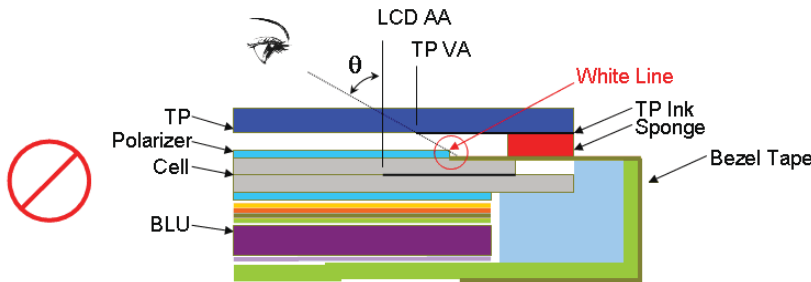
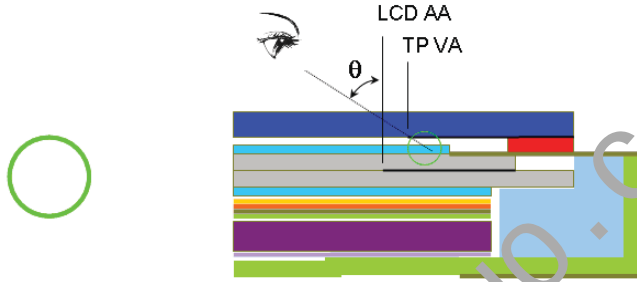
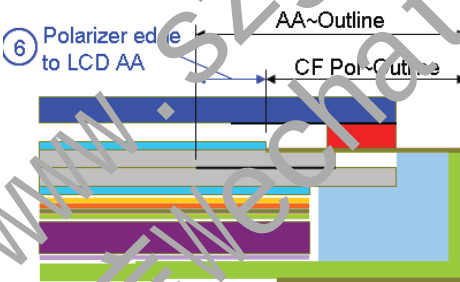
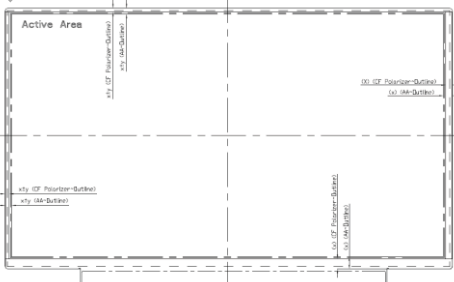
 Back View	 Double Tape LCD Panel Double Tape (30.0) B A
Definition	To prevent peeling the bezel tape in rework process. The length of double tape is $30 - (A+B)$, A is bezel tape length and B is the double tape attaching tolerance. Ex : A :2mm, B:2mm, the length of double tape is $30-(2+2)=26\text{mm}$.
9	Material used for system rear-cover
	 LCD Backlight System rear-cover System rear-cover material: Al-Mg alloy System rear-cover thickness:1.5mm MIN
Definition	System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.
10	C cover shape design

PRODUCT SPECIFICATION

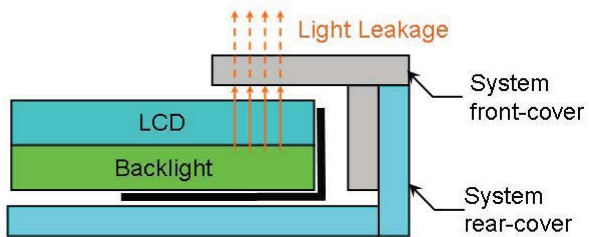
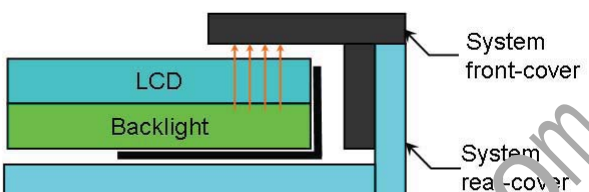
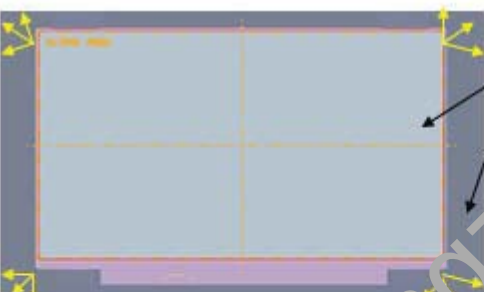
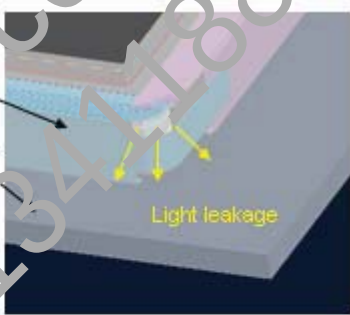
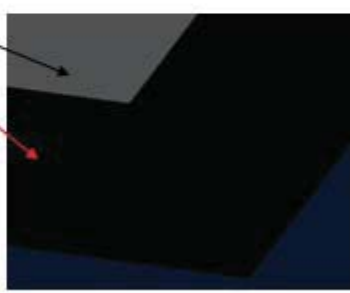
 1. F step design $\leq 0.3\text{mm}$ 2. If F step $> 0.3\text{mm}$, sloped edge design is needed to prevent panel crack.	
Definition	The F step design on C Cover less than or equal to 0.3mm is recommended. If F step exceeds 0.3mm, the sloped edge design is necessary to prevent panel crack.
11	Assembly SOP examination for system front cover with Hook design
	
Definition	To prevent panel crack during system front-cover assembly process with hook design, it is not recommended to press panel on any location that related directly to the panel.
12	Adhesive design between panel & bezel
OK  • Risk : Bezel Tape Peeling happened in a rework or reassembly process. NG  • Risk : Pooling or light leakage due to stress concentration at B-cover opening	
Definition	To prevent panel crack during system front-cover assembly process with double tape design, When system applied adhesive between B-Cover and LCD module, please design a distance 1.00mm between B-Cover's adhesive and CF pol. Do NOT put adhesive on CF pol. Adhesive material need be qualified to prevent from doing damage to cell tape after rework. Adhesive material need be qualified to prevent abnormal noise when hinge swinging test.
13	System front-cover assembly reference with Double tape design

PRODUCT SPECIFICATION

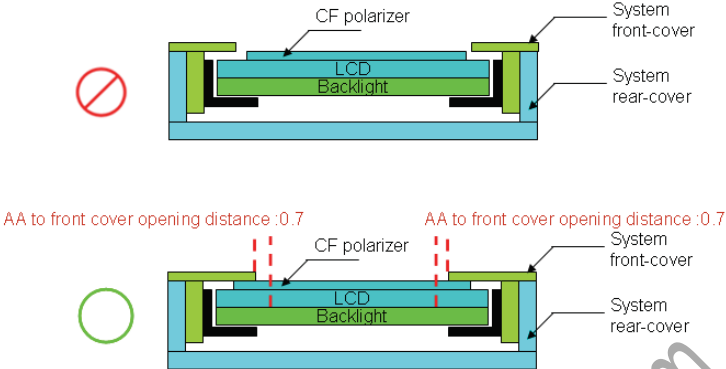
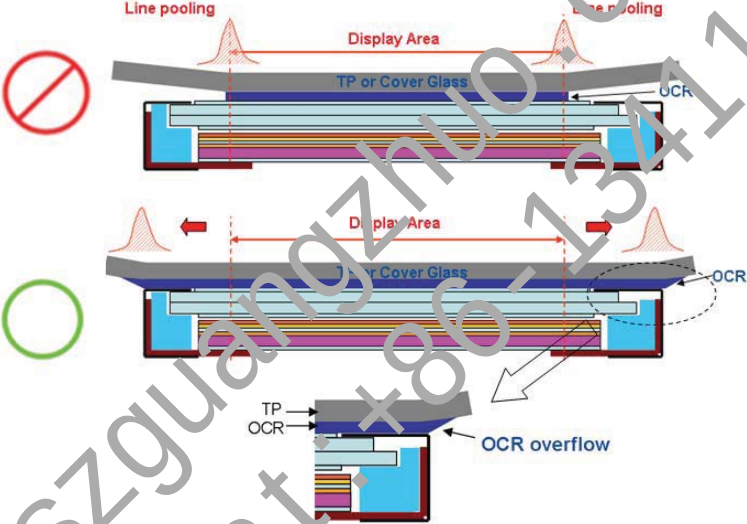
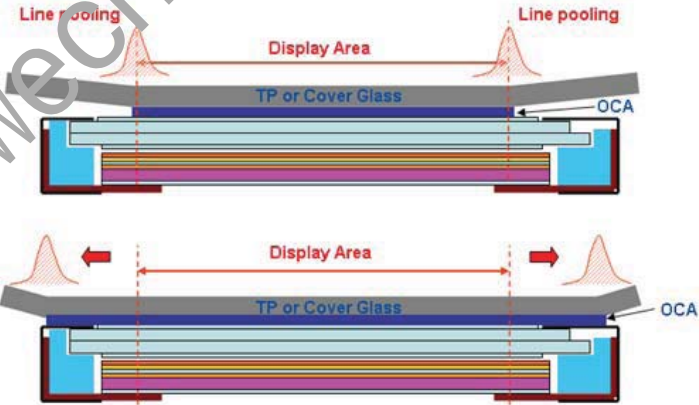
	
Definition	To prevent system front-cover peeling at double tape contact area, A gap between B-Cover & CF-Pol. Is 0.1mm min.
14	System front-cover opening area reference with TFT-LCD module
	
Definition	To prevent panel the noise of B-cover & CF Pol. Distance from CF Pol. edge to front-cover edge more than 0.65mm.

15	Touch Application : TP and LCD Module Combination for White Line Prevention   <table border="1"> <thead> <tr> <th colspan="2">Parameter consideration for White Line Issue</th> </tr> </thead> <tbody> <tr><td>1</td><td>TP VA to LCD AA distance</td></tr> <tr><td>2</td><td>TP Assembly tolerance</td></tr> <tr><td>3</td><td>TP Ink Printing tolerance</td></tr> <tr><td>4</td><td>Sponge thickness and tolerance</td></tr> <tr><td>5</td><td>Inspection/Viewing Angle specification</td></tr> <tr><td>6</td><td>Polarizer edge to LCD AA distance and tolerance</td></tr> </tbody> </table> Polarizer edge to LCD AA distance can be derived by "AA~Outline" – "CF Pol~Outline" with respect to INX 2D Outline Drawing on each side.  	Parameter consideration for White Line Issue		1	TP VA to LCD AA distance	2	TP Assembly tolerance	3	TP Ink Printing tolerance	4	Sponge thickness and tolerance	5	Inspection/Viewing Angle specification	6	Polarizer edge to LCD AA distance and tolerance
Parameter consideration for White Line Issue															
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2	TP Assembly tolerance														
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4	Sponge thickness and tolerance														
5	Inspection/Viewing Angle specification														
6	Polarizer edge to LCD AA distance and tolerance														
Definition	For using in Touch Application: to prevent White Line appears between TP and LCD module combination, the maximum inspection angle location must not fall onto LCD polarizer edge, otherwise light line near edge of polarizer will be appear. Parameters such as TP VA to LCD AA distance, TP assembly tolerance, TP Ink printing tolerance, Sponge thickness and tolerance, and Maximum Inspection/Viewing Angle, must be considered with respect to LCD module's Polarizer edge location and tolerance. This consideration must be taken at all four edges separately. The goal is to find parameters combination that allow maximum inspection angle falls inside polarizer black margin area. Note: Information for Polarizer edge location and its tolerance can be derived from INX 2D Outline Drawing ("AA ~Outline" - "CF Pol~Outline"). Note: Please feel free to contact INX FAE Engineer. By providing value of parameters above on each side, we can help to verify and pass the white line risk assessment for customer reference.														
16	Color of system front-cover material														

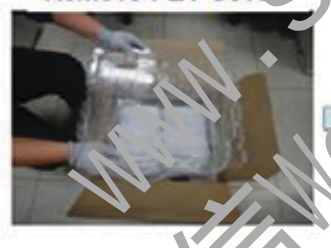
PRODUCT SPECIFICATION

	 Light Leakage LCD Backlight System front-cover System rear-cover
	 System front-cover System rear-cover LCD Backlight
	 Panel Module System front-cover or TP
	 Panel module System front-cover or TP  Light leakage 
Definition	To prevent light leakage is seen at system front-cover due to material transparency, we suggest using dark color material (black) for system front-cover design.

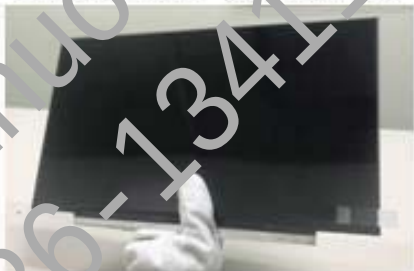
PRODUCT SPECIFICATION

17	AA to front cover opening distance
 AA to front cover opening distance : 0.7	
Definition	To prevent CF polarizer edge leakage .We suggest front cover opening no more than 0.7mm larger than active area on all 4 sides.
18	Use OCR Lamination
 Line pooling Display Area TP or Cover Glass OCR OCR overflow	
Definition	OCR glue as possible beyond module, in order to avoid Line Pooling
19	Use OCA Lamination
 Line pooling Display Area TP or Cover Glass OCA	
Definition	OCA glue as possible plastered throughout the module, in order to avoid Line Pooling.

Appendix. LCD MODULE HANDLING MANUAL

Purpose	- This SOP is prepared to prevent panel dysfunction possibility through incorrect handling procedure. - This manual provides guide in unpacking and handling steps. - Any person which may contact / related with panel, should follow guide stated in this manual to prevent panel loss.
1.	Unpacking
  Open carton  Remove EPE Cushion  Open plastic bag  Cut Adhesive Tape  Remove EPE Cushion	
2.	Panel Lifting
 Remove PET Cover  Remove PE Foam  Handle with care (see next page)  Finger Slot Use slots at both sides for finger insertion. Handle panel upward with care.	

PRODUCT SPECIFICATION

3.	Do and Don't
Do : - Handle with both hands. - Handle panel at left and right edge. 	Don't : - Lifting with one hand.  - Handle at PCBA side. 
Don't : - Stack panels.  - Press panel. 	Don't : - Put foreign stuff onto panel   - Put foreign stuff under panel  

PRODUCT SPECIFICATION

Don't :

- Paste any material unto white reflector sheet



Don't :

- Pull / Push white reflector sheet



Don't :

- Hold at panel corner.



Don't :

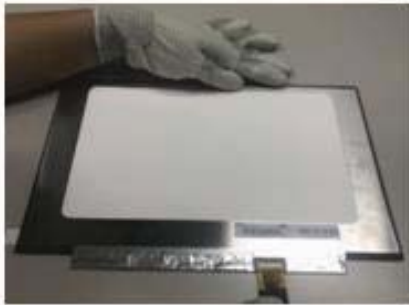
- Twist panel.



PRODUCT SPECIFICATION

Do :

- Hold panel at top edge while inserting connector.



Don't :

- Press white reflector sheet while inserting connector.



Do :

- Remove panel protector film starts from pull tape



Don't :

- Remove panel protector film from another side.



PRODUCT SPECIFICATION

Do:

Remove panel



Don't:

Remove panel



Don't :

- Touch or Press PCB Area.

