Doc. Number:

☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

MODEL NO.: N140JCN
SUFFIX: GE9
DPN: PGCWT Rev.C1

Customer:

APPROVED BY SIGNATURE

Name / Title
Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By

CONTENTS

REVISION HISTORY

Version	Date	Page	Description
1.0	Jul. 14, 2022	ALL	Spec Ver.1.0 was first issued.
1.1	Nov. 4, 2022		
3.0	Doc. 23, 2022	ALL	Spec Ver.3.0 was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N140JCN-GE9 is a 14“ diagonal TFT Liquid Crystal Display module with LED Backlight unit and 40 pins eDP interface. This module supports 1920 x 1200 WUXGA AAS mode and can display 16,777,216 colors.

1.2 GENERAL SPECIFICATIONS

LCD TFT Module + TP Module Combination			
Item	Specification	Unit	Note
Luminance, White	300	Cd/m2	-
Surface Hardness	Hard coating (3H), Anti-Glare	-	-
Color Gamma	72%	NTSC	-
Thickness	3.00 max (W/O PCB), 5.25 max. (With PCB)	mm	-
Driver Element	a-si TFT active matrix	-	-
LCD TFT Module			
Pixel Arrangement	RGB vertical stripe	-	-
Pixel Number	1920 x R.G.B. x 1200	pixel	-
Pixel Pitch	0.15708 (H) x 0.15708 (V)	mm	-
Display Colors	16,777,216	color	-
Interface	eDP 1.3	-	-
Transmissive Mode	Normally Black	-	-
Power Consumption	cell 0.9 W (Max.), BL 3.5 W (Max.)	-	(1)
TP Module			
Number of Channels	42 x 67	-	-
Touch Method	Finger	-	-
Numbers of Touch	10 points	-	-
Accuracy	Meet Windows HLK	mm	-
Linearity	Meet Windows HLK	-	-
Reporting rate	Meet Windows HLK	Hz	-
Interface	HID/I²C	-	-
Power Consumption	Active mode 0.2W(Max), Idle mode 0.1W(Max)	-	(2)

Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, fv = 60 Hz, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 ºC, whereas Black pattern is displayed.

Note (2) The active mode is under the conditions at 10 fingers touch.

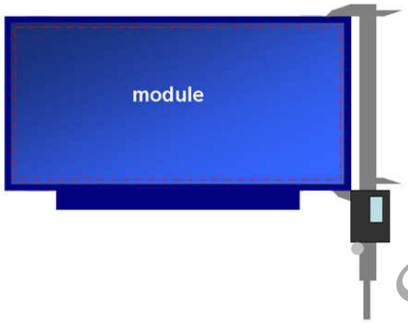
2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	306.29	306.59	306.89	mm	(1)(2)
	Vertical (V)	198.10	198.40	198.70	mm	
	Thickness (T) w/o PCB	-	2.85	3.00	mm	
	Thickness (T) with PCB	-	-	5.25	-	
Bezel Area	Horizontal	-	304.59	-	mm	-
	Vertical	-	191.60	-	mm	-
Active Area	Horizontal	301.49	301.59	301.69	mm	-
	Vertical	188.40	188.50	188.60	mm	-
Glass Thickness	CF	0.35	0.40	0.45	mm	-
	TFT	0.35	0.40	0.45	mm	-
Weight		-	296	310	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Dimensions are measured by caliper

Note (3) Panel thickness is measured with calipers clamping mylar or tape tightly



2.1 CONNECTOR TYPE

Please refer Appendix Outline Drawing for detail design.

Connector Part No.: IPEX-20682-040E-02

User's connector Part No: IPEX-20679-040T-01

3. ABSOLUTE MAXIMUM RATINGS of **ENVIRONMENT**

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

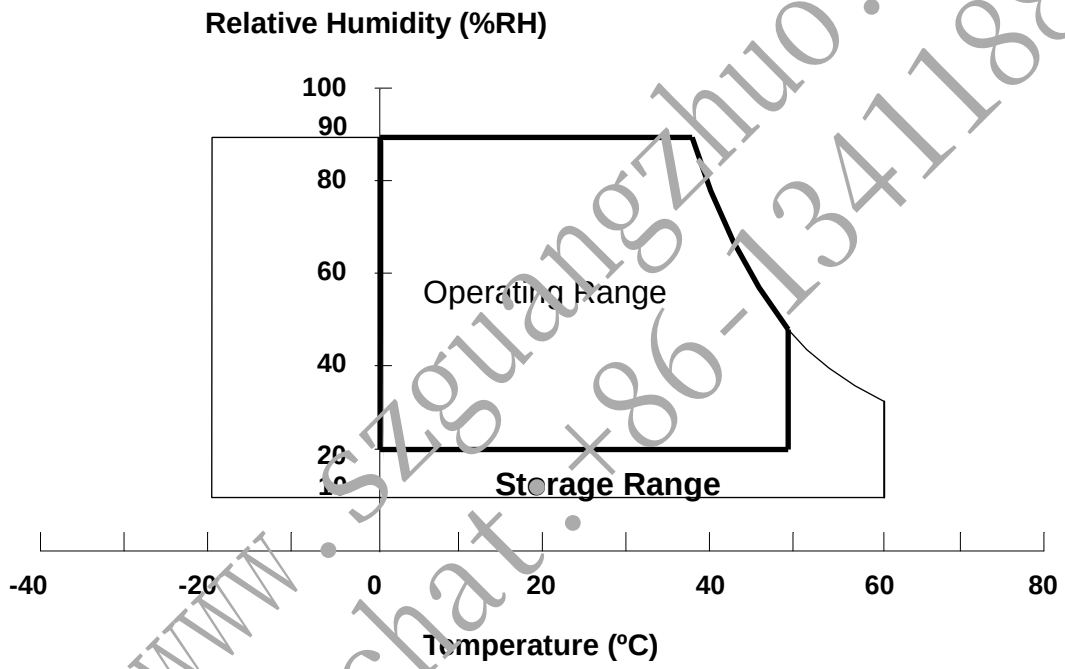
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)

Note (1) (a) 90 %RH Max. (Ta < 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max.

(c) No condensation.

Note (2) The temperature of panel surface should be 0 ºC min. and 60 ºC max.



3.2 ELECTRICAL ABSOLUTE RATINGS

3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	VCCS+0.3	V	
Converter Input Voltage	LED_VCCS	-0.3	26	V	(1)
Converter Control Signal Voltage	LED_PWM,	-0.3	3.6	V	(1)
Converter Control Signal Voltage	LED_EN	-0.3	3.6	V	(1)

Note (1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “ELECTRICAL CHARACTERISTICS”.

4. OPTICAL CHARACTERISTICS

4.1 TEST CONDITIONS

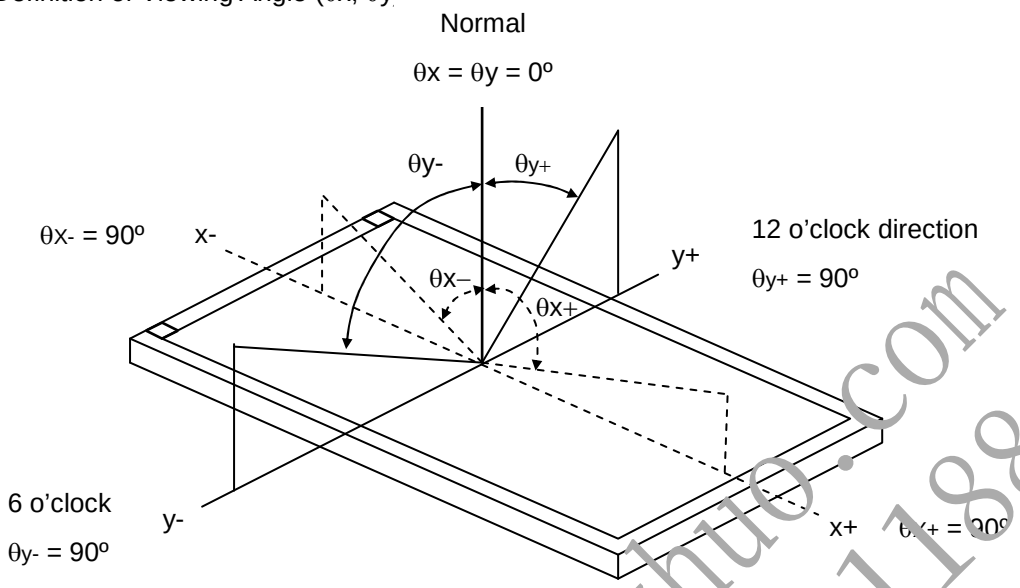
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	85.2	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

4.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	800	1000	-	-	(2), (5) (7)
Response Time		T_R		-	16	19	ms	(3), (7)
		T_F		-	14	16	ms	
Average Luminance of White		L_{AVE}		255	300	-	cd/m^2	(4), (6) ,(7)
Color Chromaticity	Red	Rx		Typ – 0.03	0.640	Typ + 0.03	-	(1),(7)
		Ry			0.330		-	
	Green	Gx			0.300		-	
		Gy			0.600		-	
	Blue	Bx			0.150		-	
		By			0.060		-	
	White	Wx			0.313		-	
		Wy			0.329		-	
Viewing Angle	Horizontal	θ_x+	CR≥10	80	89	-	Deg.	(1),(5), (7)
		θ_x-		80	89	-		
	Vertical	θ_Y+		80	89	-		
		θ_Y-		80	89	-		
White Variation of 5 Points		δW_{5p}	θ_x=0°, θ_Y =0°	-	-	1.25	-	(5),(6), (7)
		δW_{13p}				1.54		

Note (1) Definition of Viewing Angle (θx, θy)



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = Lw / Ld

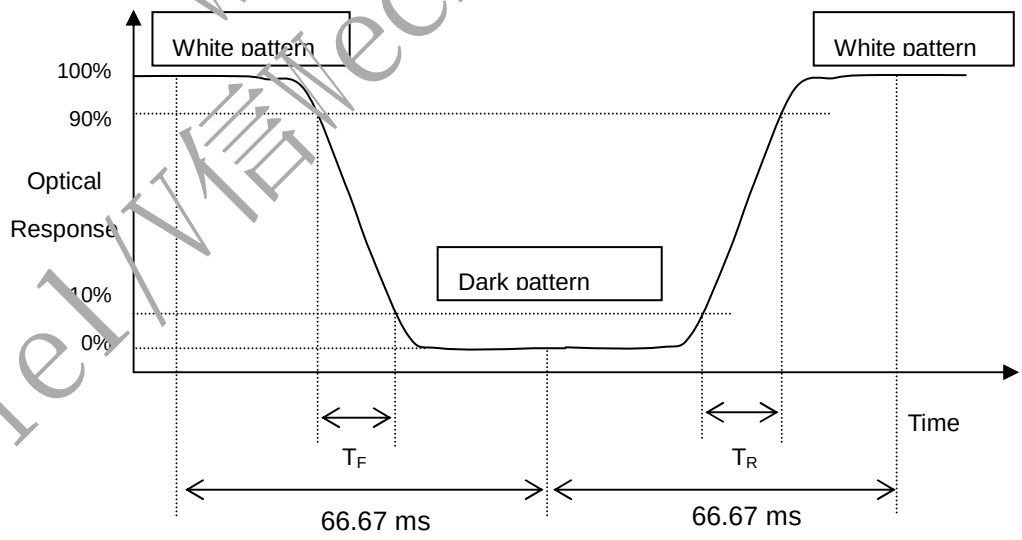
Lw : Luminance of white pattern

Ld: Luminance of dark pattern

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

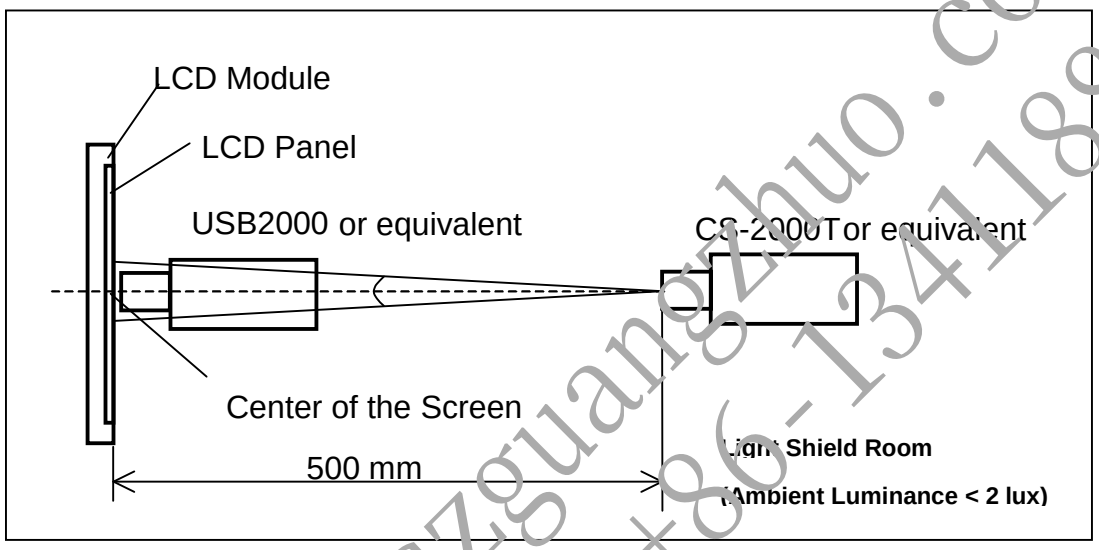
Measure the white pattern at 5 points

L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

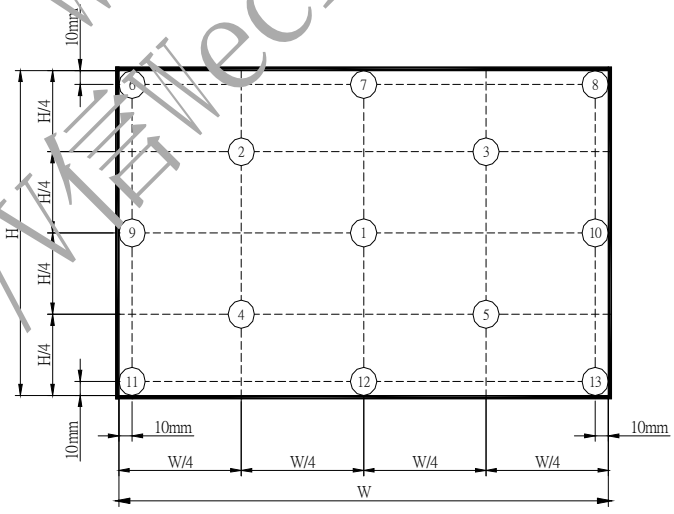


Note (6) Definition of White Variation (δW):

Measure the white pattern at 5 points

δW_{5p} = { Maximum [L (1)~ L (5)] / Minimum [L (1)~ L (5)]}*100%

δW_{13p} = { Maximum [L (1)~ L (13)] / Minimum [L (1)~ L (13)]}*100%



Ⓧ : Test Point

X=1 to 13

Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

5. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60ºC, 240 hours	(1) (2)
Low Temperature Storage Test	-20ºC, 240 hours	
Thermal Shock Storage Test	-20ºC, 0.5hour←→60℃, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	50ºC, 240 hours	
Low Temperature Operation Test	0ºC, 240 hours	
High Temperature & High Humidity Operation Test	50ºC, RH 80%, 240hours	
ESD Test (Operation)	150pF, 330Ω, 1sec/cycle Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±15KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave,1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

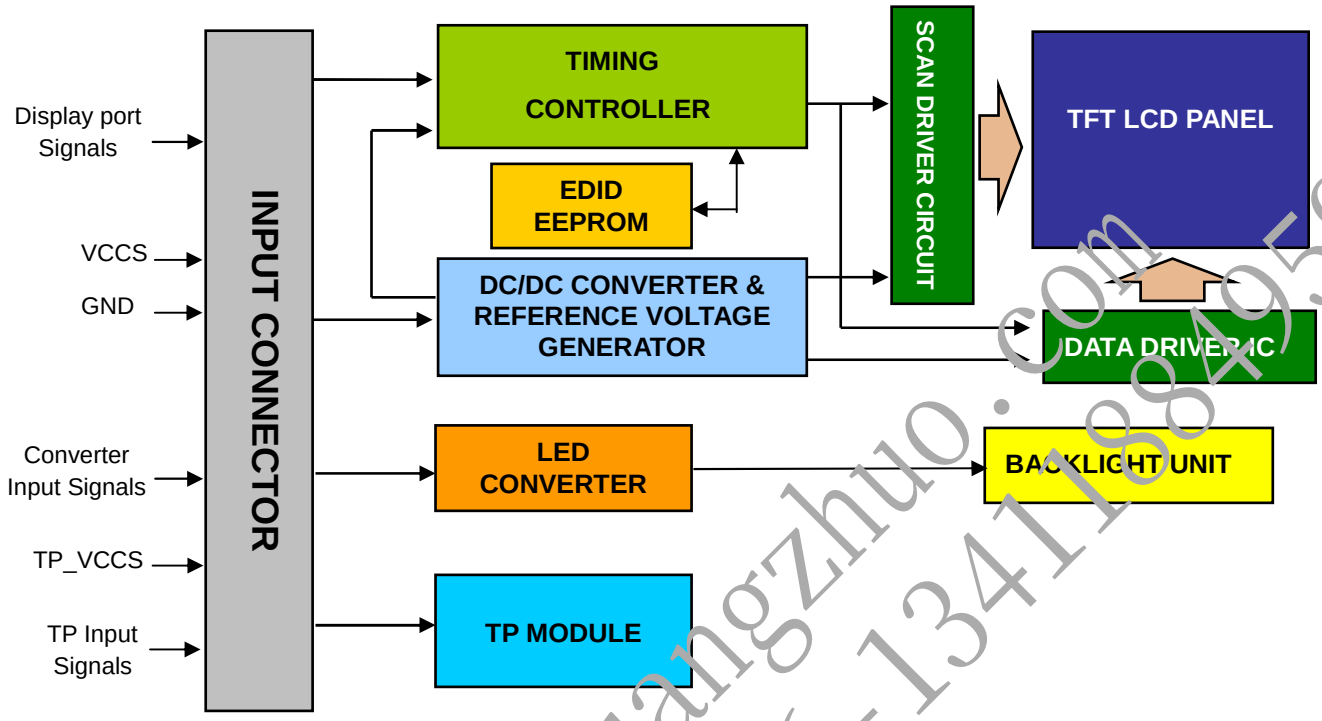
Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture

6. ELECTRICAL SPECIFICATIONS

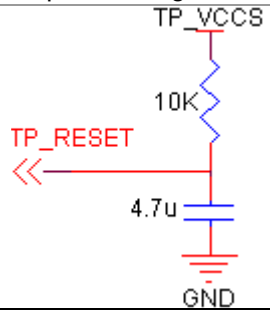
6.1 FUNCTION BLOCK DIAGRAM



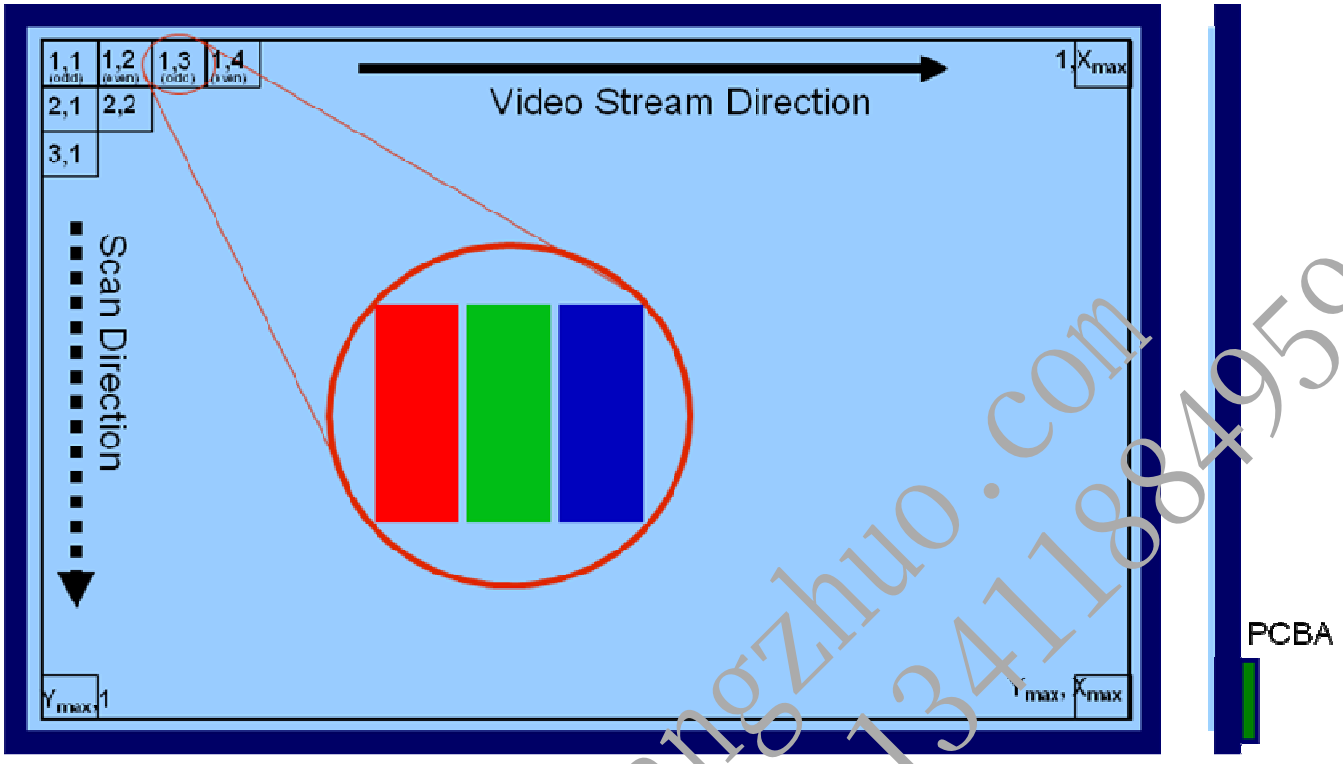
6.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	Reserved	Reserved for CABC function	-
2	H_GND	High Speed Ground	-
3	Lane1_N	Complement Signal Link Lane 1	-
4	Lane1_P	True Signal Link Lane 1	-
5	H_GND	High Speed Ground	-
6	Lane0_N	Complement Signal-Lane 0	-
7	Lane0_P	True Signal-Main Lane 0	-
8	H_GND	High Speed Ground	-
9	Aux_Ch_P	True Signal-Auxiliary Channel	-
10	Aux_Ch_N	Complement Signal-Auxiliary Channel	-
11	H_GND	High Speed Ground	-
12	VCCS	Power Supply for LCD	-
13	VCCS	Power Supply for LCD	-
14	BIST_EN	Panel Built In Self Test Enable	-
15	VSS	Ground	-
16	VSS	Ground	-
17	HPD	Hot Plug Detect	-
18	LED_GND	LED Ground	-
19	LED_GND	LED Ground	-
20	LED_GND	LED Ground	-

21	LED_GND	LED Ground	-
22	LED_EN	Enable Control Signal of LED Converter	-
23	LED_PWM	PWM Control Signal of LED Converter	-
24	NC	No Connection (Reserve)	-
25	NC	No Connection (Reserve)	-
26	LED_VCCS	LED Power Supply	-
27	LED_VCCS	LED Power Supply	-
28	LED_VCCS	LED Power Supply	-
29	LED_VCCS	LED Power Supply	-
30	NC	No Connection (Reserve)	-
31	NC	No Connection (Reserved for USB Data-)	-
32	NC	No Connection (Reserved for USB Data+)	-
33	TP_VSS	Ground for Touch panel	-
34	TP_VCCS	Power Supply for Touch panel	Typical 3.3V
35	TP_VCCS	Power Supply for Touch panel	Typical 3.3V
36	TP_RS	Touch panel report switch (High: Enable, Low: Disable)	Input, Pull high 10kΩ
37	TP_SCL	I^2C Clock for Touch	Open Drain, Pull high 2.2kΩ
38	TP_SDA	I^2C Data for Touch	Open Drain, Pull high 2.2kΩ
39	TP_INT	Interrupt for Touch	Output, Pull high 10kΩ
40	TP_RESET	Reset signal for Touch panel (High: Normal, Low: Reset)	

Note (1) The first pixel is odd as shown in the following figure.



Note (2) The setting of CABC, BIST function are as follows.

Pin	Enable	Disable
CABC_EN	Hi	Lo or Open
BIST_EN	Hi	Lo or Open

Hi = High level, Lo = Low level.

7. LCD MODULE ELECTRICAL SPECIFICATIONS

7.1. LCD ELECTRICAL CHARACTERISTICS

7.1.1 LCD ELECTRICAL ABSOLUTE RATINGS

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	VCCS+0.3	V	
Converter Input Voltage	LED_VCCS	-0.3	26	V	(1)
Converter Control Signal Voltage	LED_PWM,	-0.3	3.6	V	(1)
Converter Control Signal Voltage	LED_EN	-0.3	3.6	V	(1)

Note (1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “LCD ELETRONICS SPECIFICATION”

7.1.2 LCD ELETRONICS SPECIFICATION

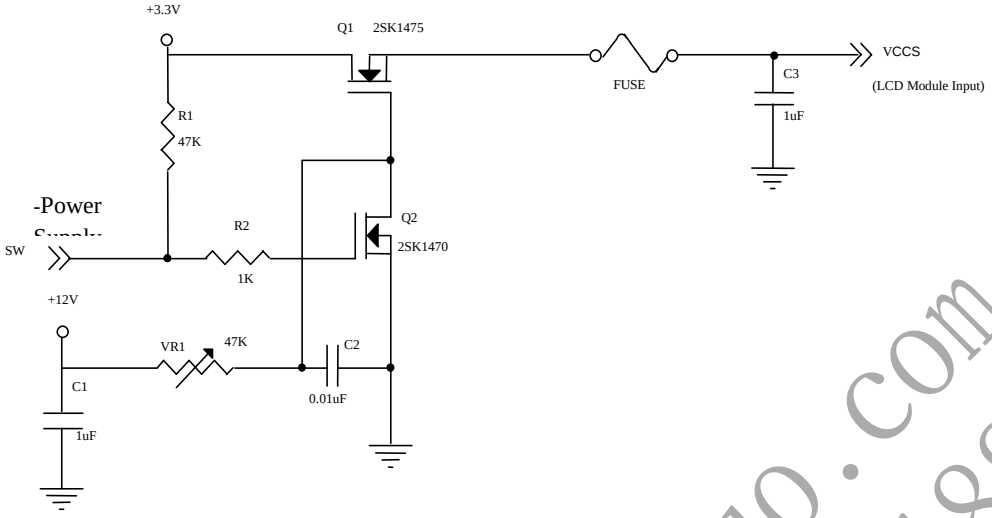
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)(7)
HPD	High Level	-	2.25	-	3.6	V	(6)
	Low Level		0	-	0.4	V	(6)
HPD Impedance		R_{HPD}	30K			ohm	(5)
Ripple Voltage		V_{RP}	-	-	100	mV	(1)
CABC_EN Input Voltage	High Level	V_{IHCABC}	2.3	-	3.6	V	(5)
	Low Level	V_{ILCABC}	0	-	0.5	V	(5)
CABC_EN Impedance		R_{CABC_EN}	30K	-	-	ohm	(5)
Inrush Current		I_{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Mosaic	Icc	150	166	212	mA	(3)a
	Black		142	158	212	mA	(3)
	Solid Pattern		-	166	212	mA	-
Power per EBL WG		P_{EBL}	-	1.25	-	-	(4)

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

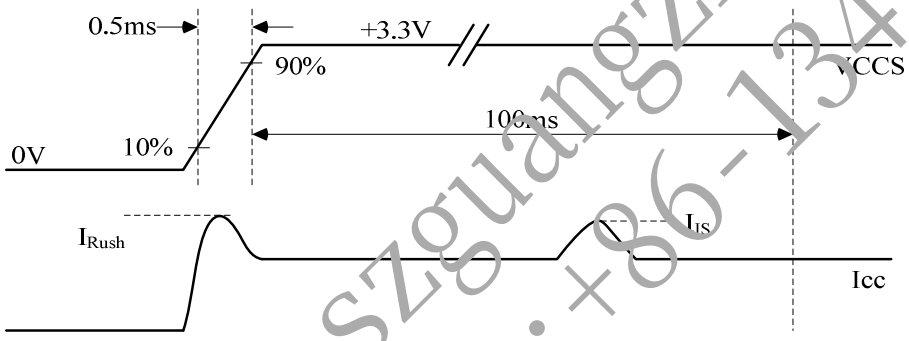
Note (2) I_{RUSH}: the maximum current when VCCS is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.

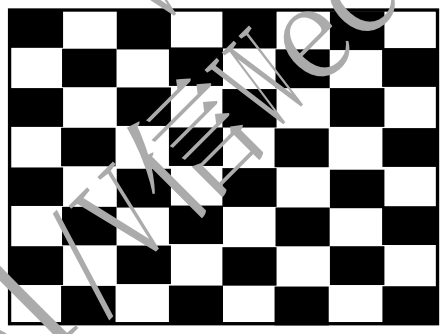


VCCS rising time is 0.5ms



Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ºC, DC Current and f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern



Active Area

Note (4) The specified power are the sum of LCD panel electronics input power and the converter input power. Test conditions are as follows.

(a) VCCS = 3.3 V, Ta = 25 ± 2 ºC, f_v = 60 Hz,

(b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file

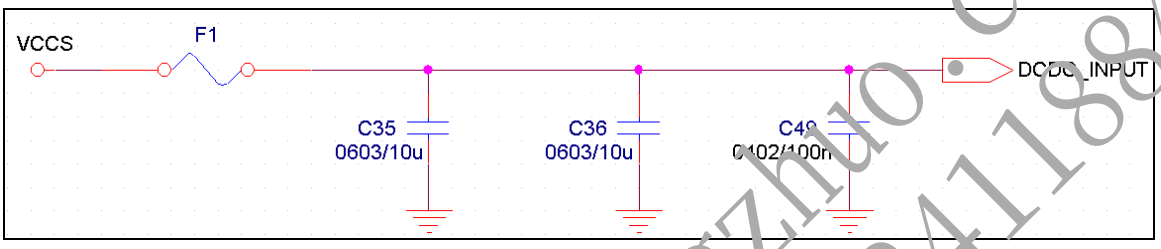
"Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.

(c) Luminance: 60 nits

Note (5) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. Please refer to Note (4) of 4.3.2 LED CONVERTER SPECIFICATION to obtain more information.

Note (6) When a source detects a low-going HPD pulse, it must be regarded as a HPD event. Thus, the source must read the link / sink status field or receiver capability field of the DPCD and take corrective action.

Note (7) Input VCC Circuit is as below



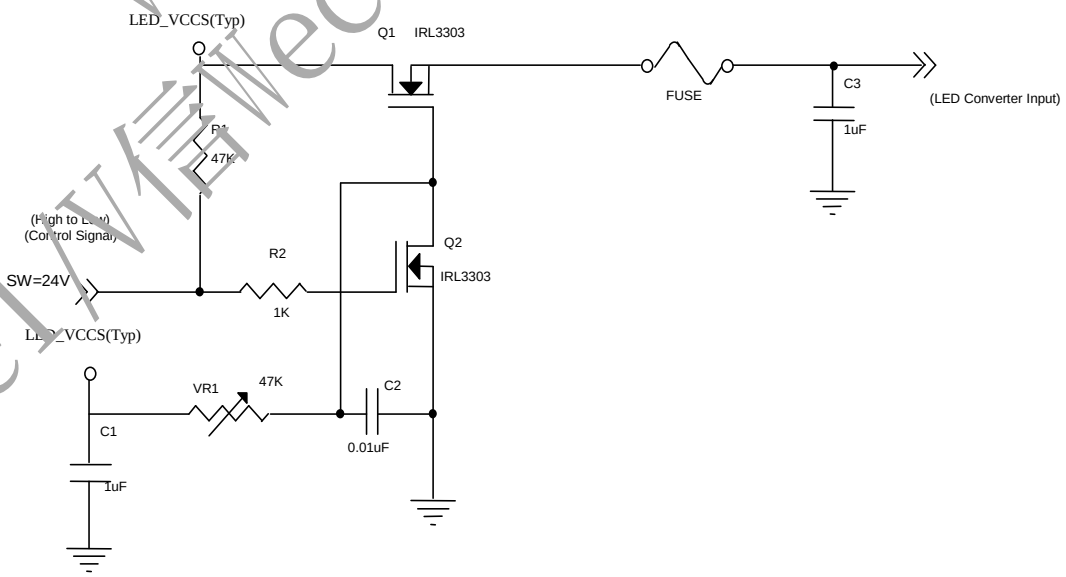
7.1.3 LED CONVERTER SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input Power Supply Voltage		LED_Vccs	5.0	12.0	21.0	V	-
Converter Inrush Current		$ILED_{RUSH}$	-	-	1.5	A	(1)
LED_EN Control Level	Backlight On	-	2.2	-	3.6	V	(4)
	Backlight Off		0	-	0.6	V	(4)
LED_EN Impedance		R_{LED_EN}	30K	-	-	ohm	(4)
PWM Control Level	PWM High Level	-	2.2	-	3.6	V	(4)
	PWM Low Level		0	-	0.6	V	(4)
PWM Impedance		R_{PWM}	30K	-	-	ohm	(4)
PWM Control Duty Ratio		-	5	-	100	%	(5)
PWM Control Permissive Ripple Voltage		V_{PWM_pp}	-	-	100	mV	-
PWM Control Frequency		f_{PWM}	190	-	2K	Hz	(2)
LED Power Current	LED_VCCS =Typ.	ILED	151	234	245	mA	(3)

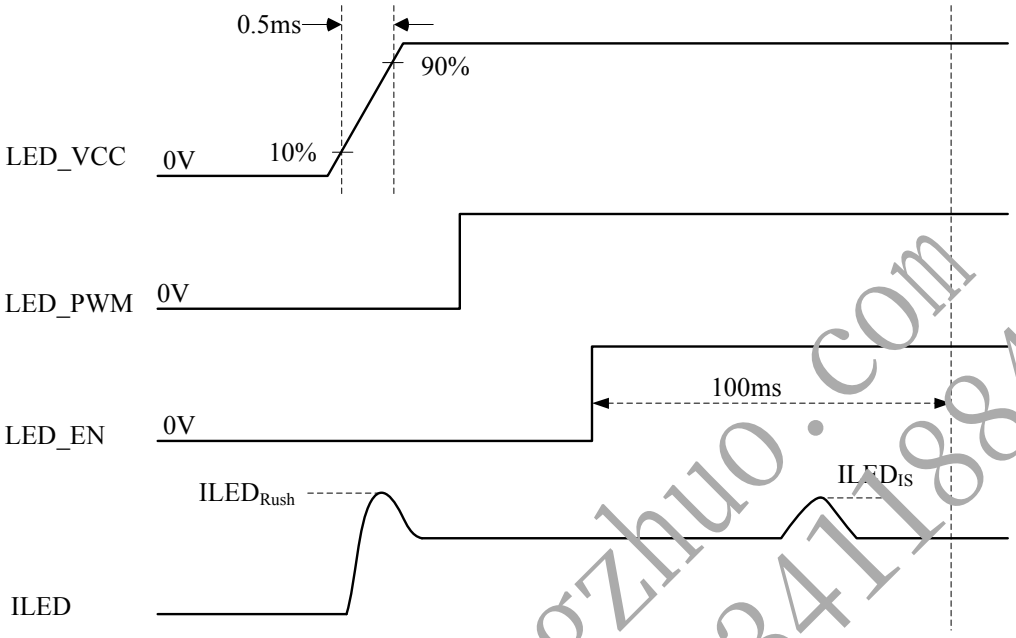
Note (1) $ILED_{RUSH}$: the maximum current when LED_VCCS is rising,

$ILED_{IS}$: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.



VLED rising time is 0.5ms



Note (2) If PWM control frequency is applied in the range less than 1KHz, the "waterfall" phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

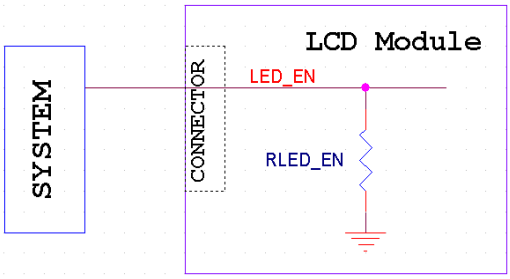
$$(N + 0.33) * f \leq f_{PWM} \leq (N + 0.66) * f$$

N : Integer $(N \geq 3)$

f : Frame rate

Note (3) The specified LED power supply current is under the conditions at "LED_VCCS = Typ.", Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.

Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. For example, the figure below describes the equivalent pull down impedance of LED_EN (if it exists). The rest pull down impedances of other signals (eg. HPD, PWM …) are in the same concept.



Note (5) If the cycle-to-cycle difference of PWM duty exceeds 0.1%, especially when the PWM duty is low, slight brightness change might be observed.

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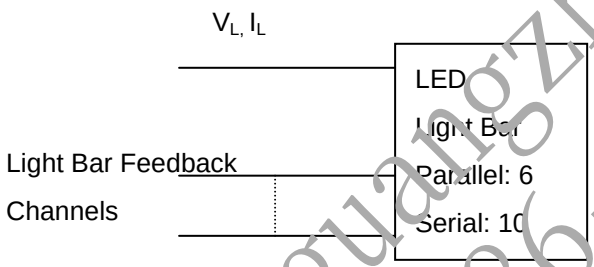
7.2 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	26	28.5	30	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L	-	85.2	-	mA	
Power Consumption	P_L	-	2.428	2.556	W	(3)
LED Life Time	L_{BL}	15000	-	-	Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below:



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 oC and IL = 14.2 mA(Per EA) until the brightness becomes ≦ 50% of its original value

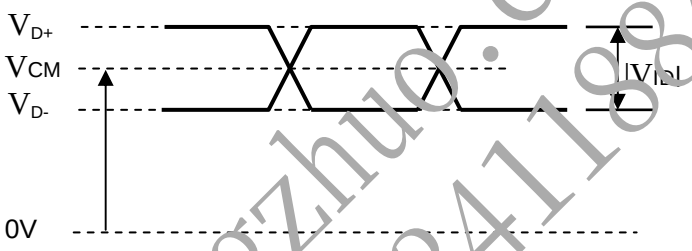
7.3 DISPLAY PORT SIGNAL TIMING SPECIFICATION

7.3.1 DISPLAY PORT INTERFACE

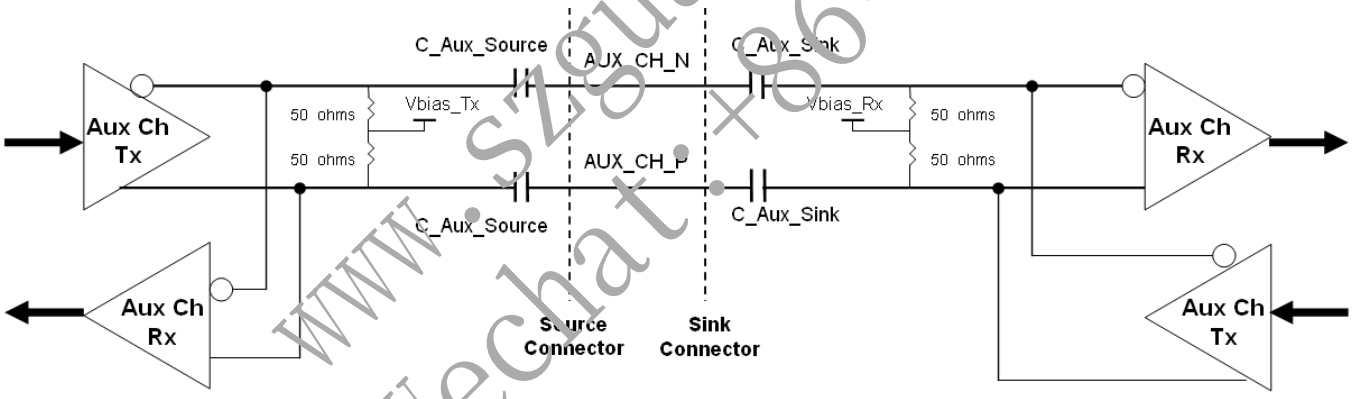
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Signal Common Mode Voltage(MainLink and AUX)	VCM	0		2	V	(1)(4)
AUX AC Coupling Capacitor	C_Aux_Source	75		200	nF	(2)
Main Link AC Coupling Capacitor	C_ML_Source	75		200	nF	(3)

Note (1)Display port interface related AC coupled signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2. There are many optional items described in eDP1.2. If some optional item is requested, please contact us

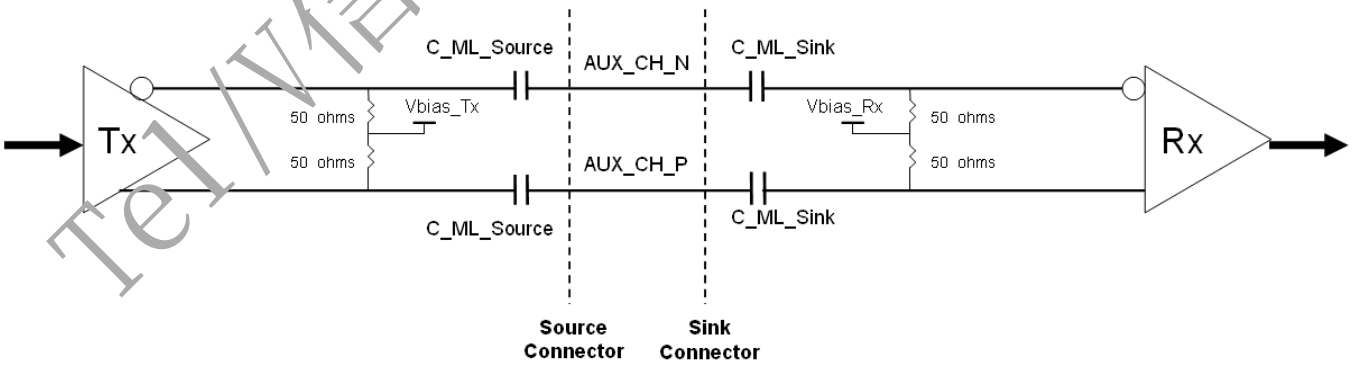
Single Ended



((2) Recommended eDP AUX Channel topology is as below and the AUX AC Coupling Capacitor (C_Aux_Source) should be placed on the source device.



(3) Recommended Main Link Channel topology is as below and the Main Link AC Coupling Capacitor (C_ML_Source) should be placed on the source device.



(4) The source device should pass the test criteria described in DisplayPortCompliance Test Specification (CTS) 1.1.

7.3.2 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

7.4 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Refresh Rate 60Hz

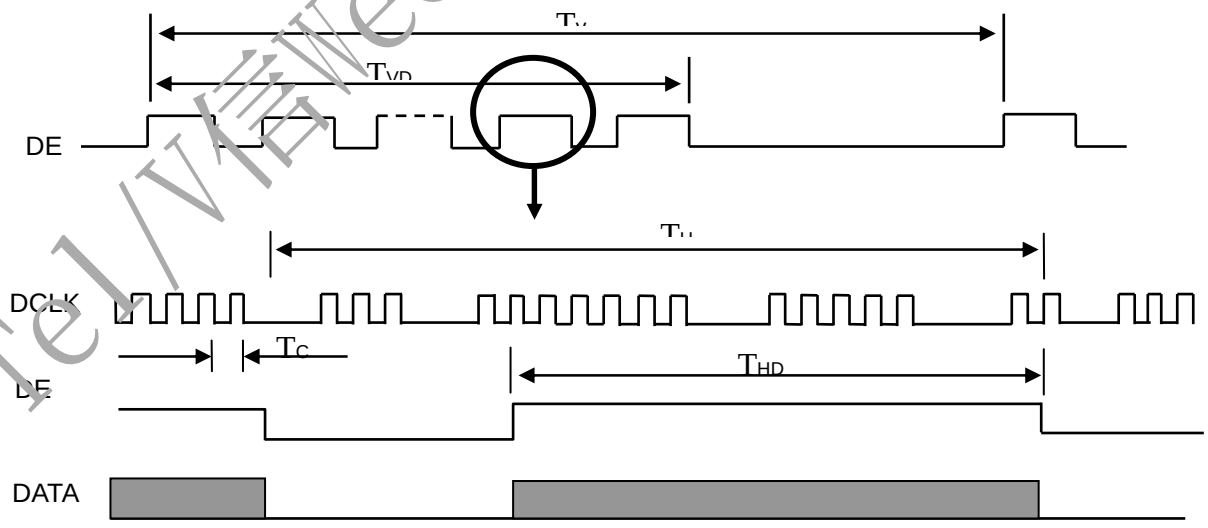
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	152.28	154.26	156.24	MHz	-
DE	Vertical Total Time	TV	1232	1236	1240	TH	-
	Vertical Active Display Period	TVD	1200	1200	1200	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	36	TV-TVD	TH	-
	Horizontal Total Time	TH	2060	2080	2100	Tc	-
	Horizontal Active Display Period	THD	1920	1920	1920	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	160	TH-THD	Tc	-

Refresh rate 48Hz (Power Saving Mode)

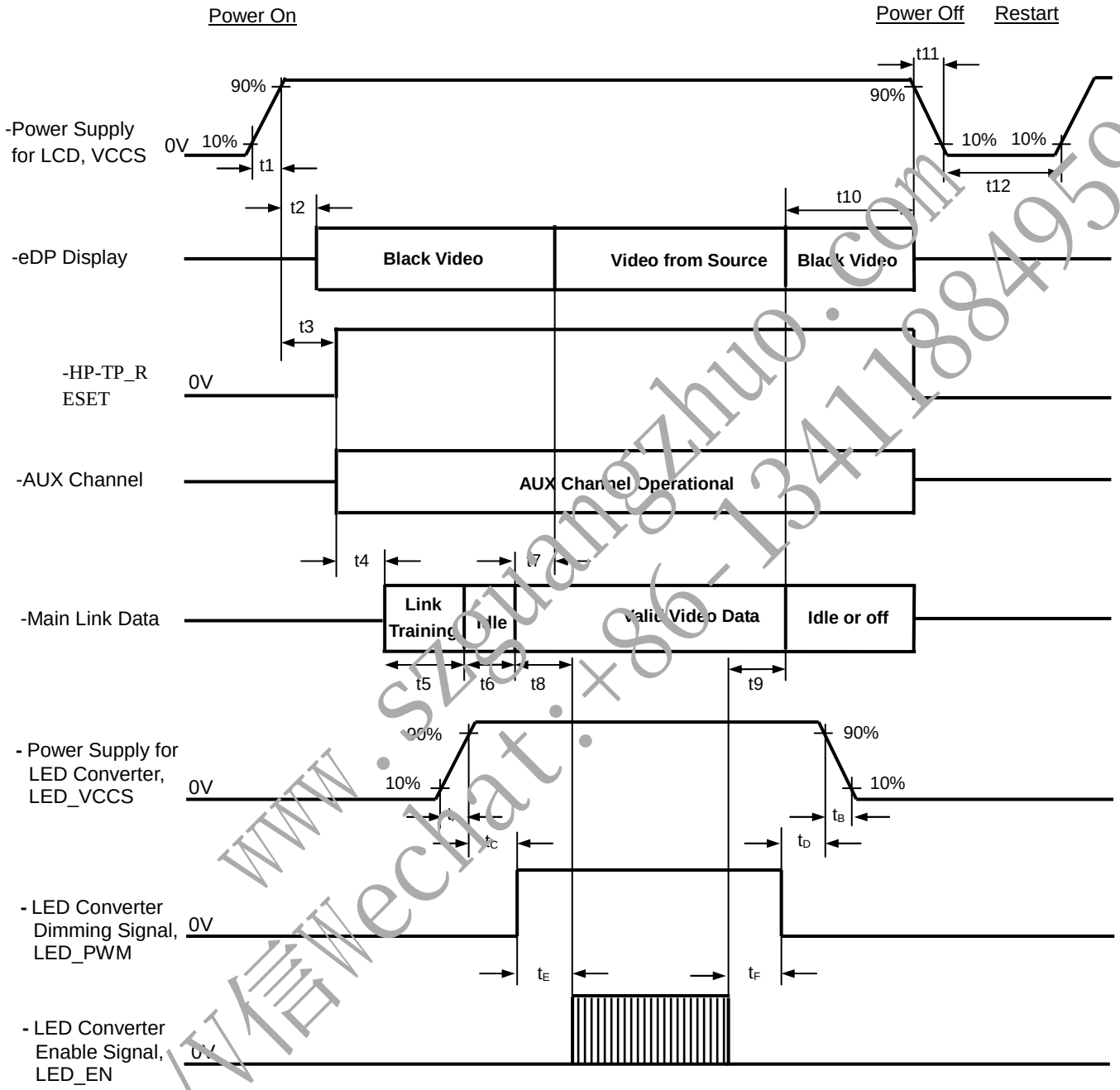
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	152.28	154.26	156.24	MHz	(1)
DE	Vertical Total Time	TV	1541	1545	1549	TH	(1)
	Vertical Active Display Period	TVD	1200	1200	1200	TH	(1)
	Vertical Active Blanking Period	TVB	TV-TVD	345	TV-TVD	TH	(1)
	Horizontal Total Time	TH	2060	2080	2100	Tc	(1)
	Horizontal Active Display Period	THD	1920	1920	1920	Tc	(1)
	Horizontal Active Blanking Period	THB	TH-THD	160	TH-THD	Tc	(1)

Note (1) The panel can operate at 60Hz normal mode and power saving mode, respectively. All reliability tests are based on specific timing of 60Hz refresh rate. We can only assure the panel's electrical function at power saving mode.

INPUT SIGNAL TIMING DIAGRAM



7.5 POWER ON/OFF SEQUENCE



Timing Specifications:

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	Power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t2	Delay from LCD,VCCS to black video generation	Sink	0	200	ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source (see Notes:2 and 3 below)
t3	Delay from LCD,VCCS to HPD high	Sink	0	200	ms	Sink AUX Channel must be operational upon HPD high (see Note:4 below)
t4	Delay from HPD high to link training initialization	Source	0	-	ms	Allows for Source to read Link capability and initialize
t5	Link training duration	Source	0		ms	Dependant on Source link training protocol
t6	Link idle	Source	0	-	ms	Min Accounts for required BS-Idle pattern. Max allows for Source frame synchronization
t7	Delay from valid video data from Source to video on display	Sink	0	50	ms	Max value allows for Sink to validate video data and timing. At the end of T7, Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and Sink will no longer generate automatic Black Video
t8	Delay from valid video data from Source to backlight on	Source	80	-	ms	Source must assure display video is stable *: Recommended by INX. To avoid garbage image.
t9	Delay from backlight off to end of valid video data	Source	50	-	ms	Source must assure backlight is no longer illuminated. At the end of T9, Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and Sink will automatically display Black Video. (See Notes: 2 and 3 below) *: Recommended by INX. To avoid garbage image.
t10	Delay from end of valid video data from Source to power off	Source	0	500	ms	Black video will be displayed after receiving idle or off signals from Source
t11	VCCS power rail fall time, 90% to 10%	Source	0.5	10	ms	-

t12	VCCS Power off time	Source	500	-	ms	-
t_A	LED power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t_B	LED power rail fall time, 90% to 10%	Source	0	10	ms	-
t_C	Delay from LED power rising to LED dimming signal	Source	1	-	ms	-
t_D	Delay from LED dimming signal to LED power falling	Source	1	-	ms	-
t_E	Delay from LED dimming signal to LED enable signal	Source	0	-	ms	-
t_F	Delay from LED enable signal to LED dimming signal	Source	0	-	ms	-

Note (1) Please don't plug or unplug the interface cable when system is turned on. Before LCD_VCCS and LED_VCCS are ready, it is recommended to pull down the backlight control signals

Note (2) The Sink must include the ability to automatically generate Black Video autonomously. The Sink must automatically enable Black Video under the following conditions:

- Upon LCDVCC power-on (within T2 max)
- When the "NoVideoStream_Flag" (VB-ID Bit 3) is received from the Source (at the end of T9)

Note (3) The Sink may implement the ability to disable the automatic Black Video function, as described in Note (2), above, for system development and debugging purposes.

Note (4) The Sink must support AUX Channel polling by the Source immediately following LCDVCC power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to response to an AUX Channel transaction with the time specified within T3 max.

8. TP MODULE ELECTRICAL CHARACTERISTICS

8.1 TP MODULE ELECTRICAL ABSOLUTE RATINGS

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Voltage from TP_VCCS to AGND and DGND	TP_VCCS	-	3.6	V	-
Logic Input Voltage	-	-	3.6	V	

8.2 TP MODULE ELECTRICAL CHARACTERISTICS

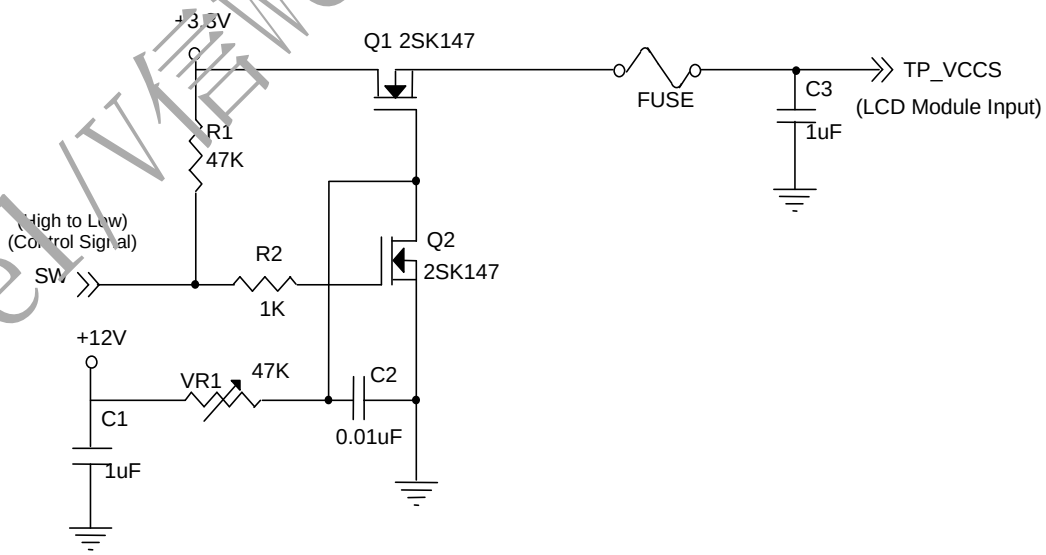
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		TP_VCCS	3.0	3.3	3.6	V	(1)
Ripple Voltage		TP_V_{RP}	-	-	100	mV	(1)
Inrush Current		TP_I_{RUSH}	-	-	1.1	A	(1),(2)
Power Supply Current	Active Mode	TP_I_{CC}	-	-	60.6	mA	-
	Idle Mode		-	-	20.3	mA	-
Reset	Normal	TP_RESET	2.5	-	TP_VCCS	V	(3)
	Active		0	-	0.5	V	(3)
Report Switch	RS High Level	TP_RS	2.5	-	TP_VCCS	V	-
	RS Low Level		0	-	0.5	V	-
I^2C Signal	High Level	TP_SCL, TP_SDA	2.7	-	TP_VCCS	V	-
	Low Level		0	-	0.4	V	

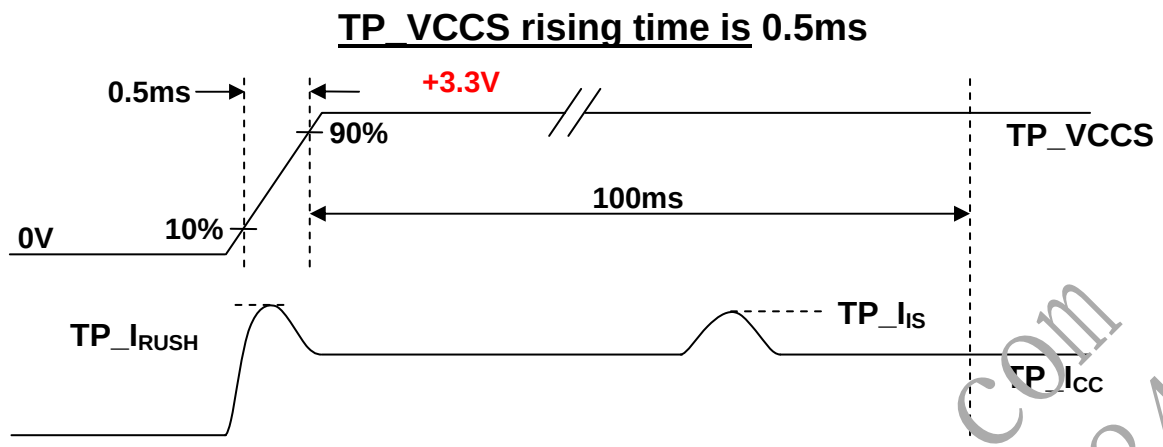
Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

Note (2) TP_I_{RUSH}: the maximum current when TP_VCCS is rising

TP_I_{IS}: the maximum current of the first 100ms after power-on

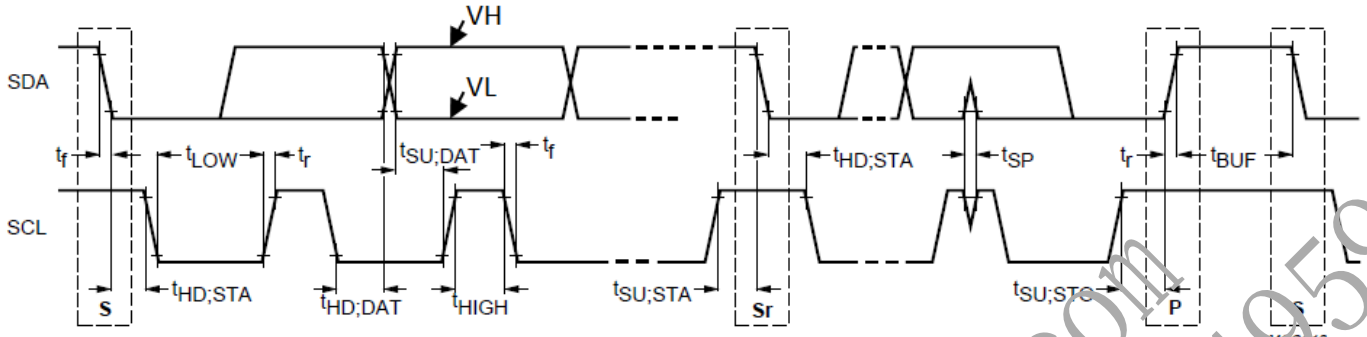
Measurement Conditions: Shown as the following figure. Test pattern: white





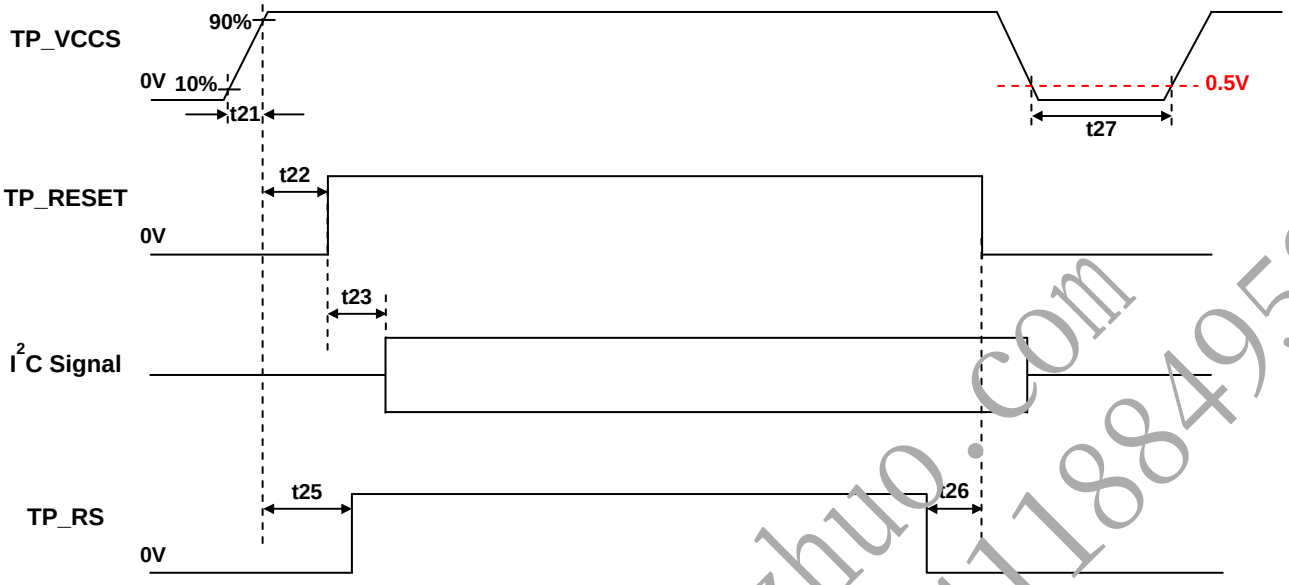
Note (3) TP_RESET is a Schmitt Trigger input.

8.3 I²C AC ELECTRICAL CHARACTERISTICS



Signal		Description	Min.	Typ.	Max.	Unit
INT	VL, LH	Low level voltage	NONE	NONE	0.4	V
		High level voltage	2.7	NONE	NONE	V
SCL	VL, VH	Low level voltage	NONE	NONE	0.4	V
		High level voltage	2.7	NONE	NONE	V
	Freq	Clock frequency (Max spec)	0	NONE	400	kHz
	T_low	Low period clock	1.3	NONE	NONE	us
	T_high	High period clock	0.6	NONE	NONE	us
	Tr	Rise time	20	NONE	300	ns
	Tf	Fall time	20	NONE	300	ns
SDA	VL, VH	Low level voltage	NONE	NONE	0.4	V
		High level voltage	2.7	NONE	NONE	V
	Tr	Rise time	20	NONE	300	ns
	Tf	Fall time	20	NONE	300	ns
Bus lines	tHD_STA	Hold time START	0.6	NONE	NONE	us
	tHD_DAT	Data hold time	0.2	NONE	NONE	us
	tSU_DAT	Data set-up time	100	NONE	NONE	ns
	tSU_STO	Set-up time for STOP	0.6	NONE	NONE	us
	tSU_Sr	Set-up time for START repeated (Sr)	0.6	NONE	NONE	us
	tHD_Sr	Hold time for START repeated (Sr)	0.6	NONE	NONE	us
	tBUF	BUS free time	1.3	NONE	NONE	us

8.4 TP MODULE POWER ON/OFF SEQUENCE



Timing Specifications:

Parameter	Description	Value		Unit	Notes
		Min	Max		
t_{21}	TP_VCCS rail rise time, 10% to 90%	0.5	-	ms	-
t_{22}	Delay from TP_VCCS to TP_RESET	[illegible]	-	ms	-
t_{23}	Delay from TP_RESET to I²C Signal	20	-	ms	(1)
t_{25}	Delay from TP_VCCS to TP_RS	20	-	ms	-
t_{26}	Delay from TP_RS to TP_RESET	2	-	ms	-
t_{27}	TP_VCCS power off duration	500	-	ms	-

Note (1) It represents touch device is able to response ACK for host only. And it is recommended for host to do enumeration when t_{23} > 300ms.

9. PACKING

9.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

(a) Model Name: N140JCN-GE9

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X X X X X X X Y M D L N N N N

- Serial No.
- Product Line
- Year, Month, Date
- INX Internal Use
- Revision
- INX Internal Use

Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2010~2019

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

(e) UL Logo : XXXX is UL factory ID.

(f) Dell 2D label contains information as below:

(e-1) Serial ID: TW-0SSSSS-INT00-YMD-XXXX-ZZZ

- Serial Numbers
- Production Year, Month, Date
- Manufacturing ID
- Part Number

(e-2) Production location: Made in XXXX.

(e-3) ZZZ :Revision code: X00, X10, X20, A00..etc.

9.2 DELL CARTON LABEL

9.2 CARTON

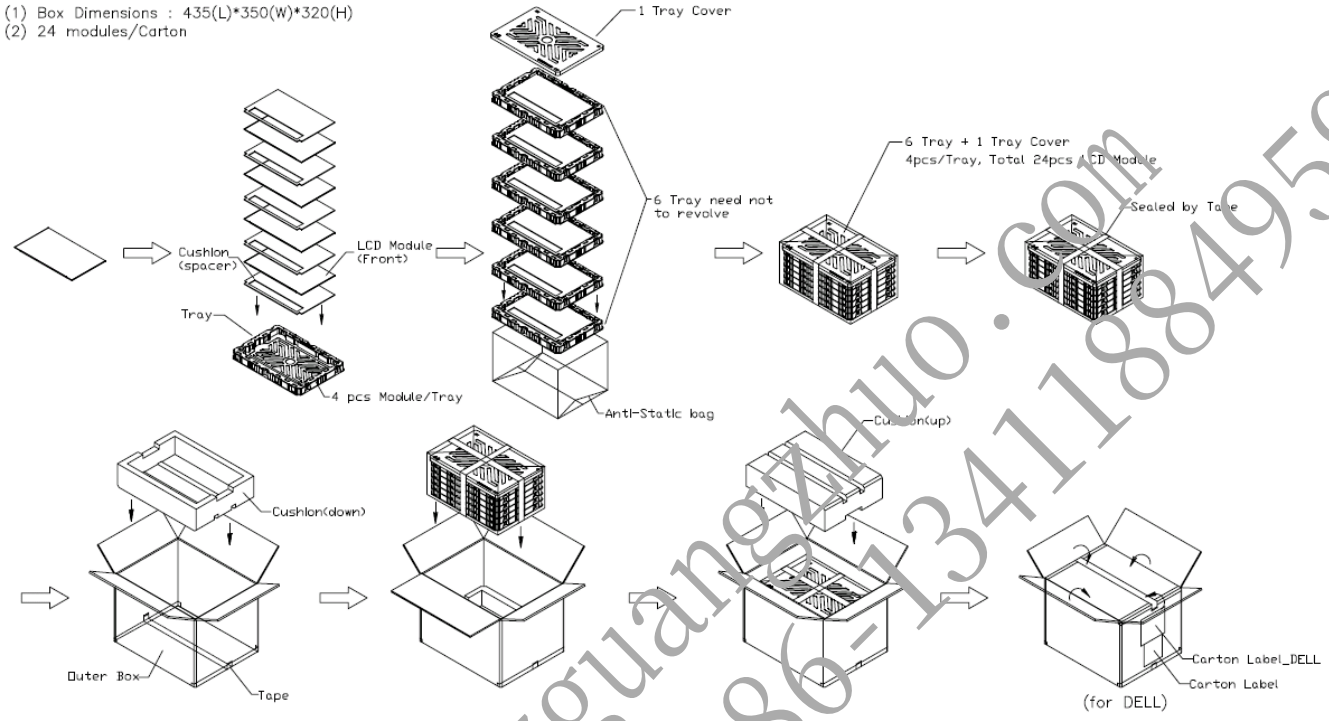


Figure. 9-2 Packing method

9.3 PALLET

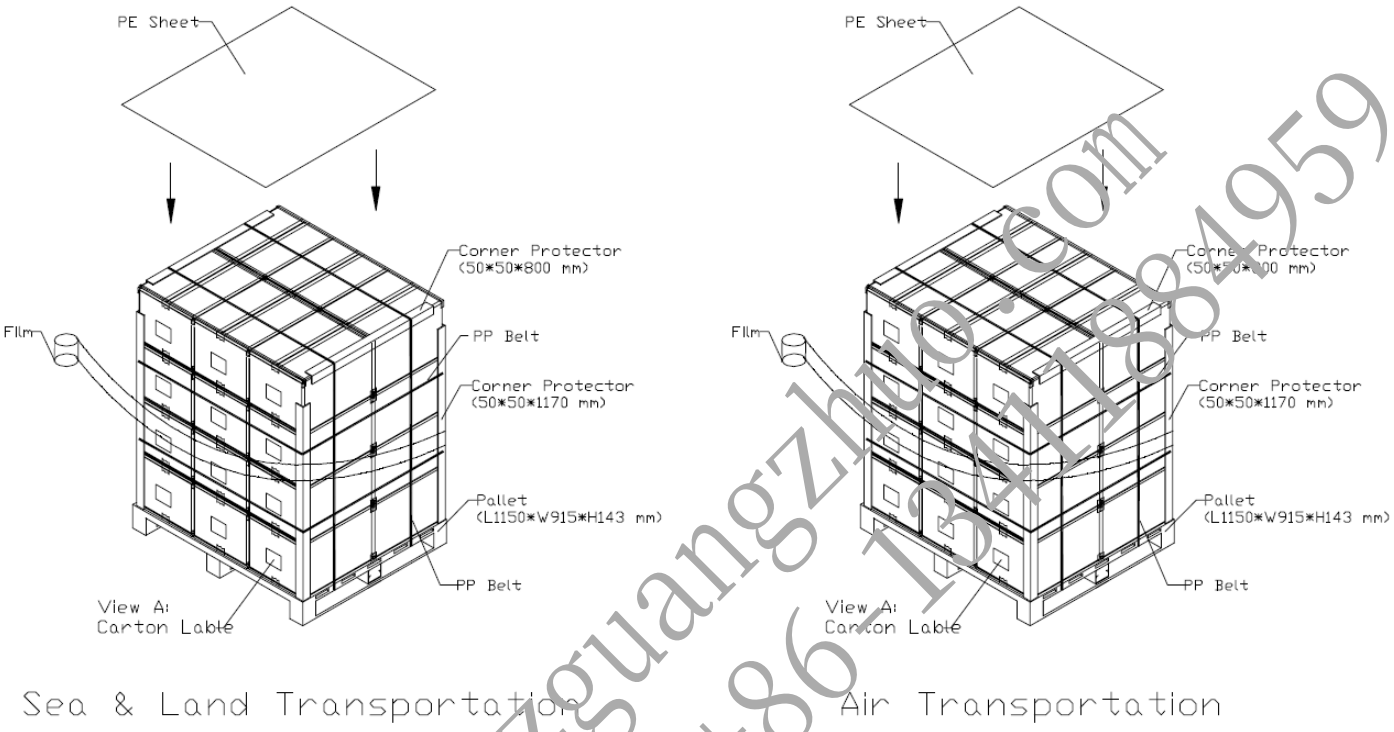


Figure. 9-3 Packing method

10. PRECAUTIONS

10.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

10.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

10.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

Appendix. EDID DATA STRUCTURE

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	00	Header	00	00000000
1	01	Header	FF	11111111
2	02	Header	FF	11111111
3	03	Header	FF	11111111
4	04	Header	FF	11111111
5	05	Header	FF	11111111
6	06	Header	FF	11111111
7	07	Header	00	00000000
8	08	ID system manufacturer name ("CMN")	0D	00001101
9	09	ID system manufacturer name	AE	10101110
10	0A	ID system Product Code (LSB)	4D	01001101
11	0B	ID system Product Code (MSB)	14	00010100
12	0C	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
13	0D	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
14	0E	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
15	0F	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
16	10	Week of manufacture (fixed week code)	0D	00001101
17	11	Year of manufacture (fixed year code)	20	00100000
18	12	Version=1	01	00000001
19	13	Revision=4	04	00000100
20	14	Vedio Input Definition	A5	10100101
21	15	Active area horizontal (“30.159cm“)	1E	00011110
22	16	Active area vertical (“18.85cm“)	13	00010011
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("RGB, Non-continous")	03	00000011
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	EE	11101110
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	95	10010101
27	1B	Rx=0.640	A3	10100011
28	1C	Ry=0.330	54	01010100
29	1D	Gx=0.300	4C	01001100
30	1E	Gy=0.600	99	10011001
31	1F	Bx=0.150	26	00100110
32	20	By=0.060	0F	00001111
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	No manufacturer's specific timing	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("154.26MHz")	42	01000010
55	37	# 1 Pixel clock (hex LSB first)	3C	00111100
56	38	# 1 H active ("1920")	80	10000000
57	39	# 1 H blank ("160")	A0	10100000
58	3A	# 1 H active : H blank	70	01110000
59	3B	# 1 V active ("1200")	B0	10110000
60	3C	# 1 V blank ("36")	24	00100100
61	3D	# 1 V active : V blank	40	01000000
62	3E	# 1 H sync offset ("48")	30	00110000
63	3F	# 1 H sync pulse width ("32")	20	00100000
64	40	# 1 V sync offset : V sync pulse width ("10 : 6")	A6	10100110
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width	00	00000000
66	42	# 1 H image size ("301 mm")	2D	00101101
67	43	# 1 V image size ("188 mm")	BC	10111100
68	44	# 1 H image size : V image size	10	00010000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71	47	Non-interlaced, Normal Display, Digital separate, Positive Hsync, Negative Vsync	1A	00011010
72	48	Indicates that this 18 byte descriptor is a Display Descriptor	00	00000000
73	49	Indicates that this 18 byte descriptor is a Display Descriptor	00	00000000
74	4A	Set to 00h when 18 byte descriptor is used as a Display Descriptor	00	00000000
75	4B	Tag Number for Display Range Limits Descriptor	FD	11111101
76	4C	Display Range Limits Offset : FLAGs	00	00000000
77	4D	Minimum Vertical Rate ("48Hz")	30	00110000
78	4E	Maximum Vertical Rate ("60Hz")	3C	00111100
79	4F	Minimum Horizontal Rate ("74KHz")	4A	01001010
80	50	Maximum Horizontal Rate ("74KHz")	4A	01001010
81	51	Maximum Pixel Clock ("154.26MHz")	0F	00001111
82	52	Video Timing Support Flags : Bytes 10 --> 17 indicate support for additional video timings	01	00000001
83	53	Line Feed (0Ah if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	0A	00001010
84	54	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	20	00100000
85	55	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	20	00100000

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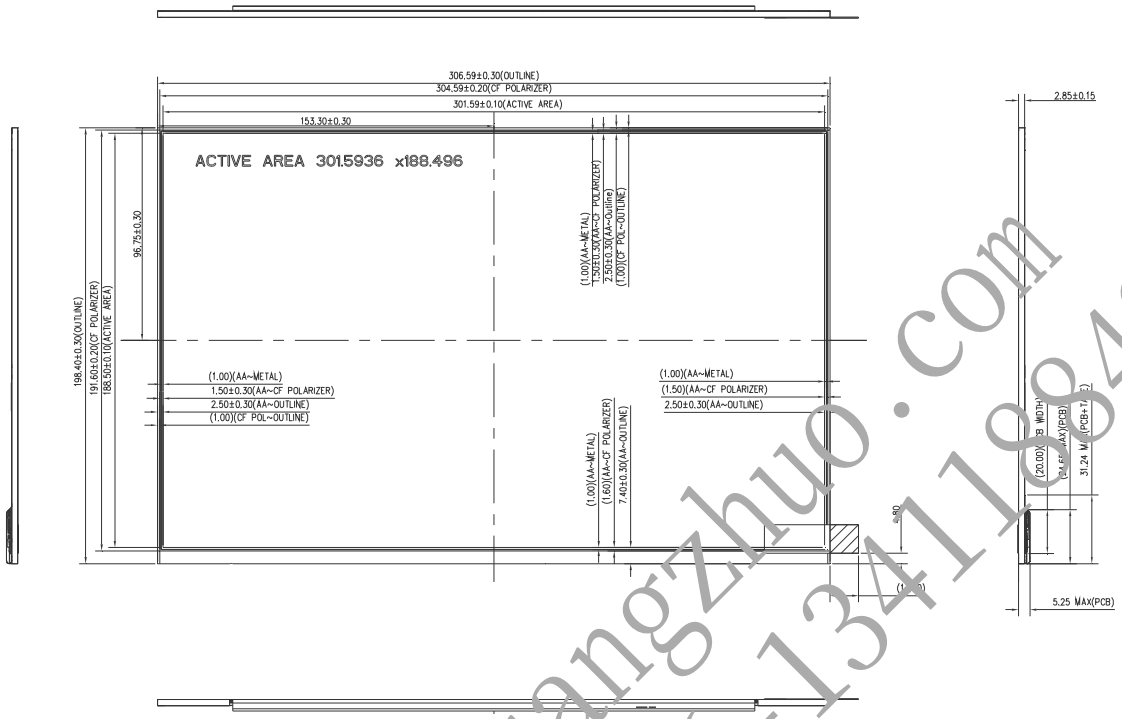
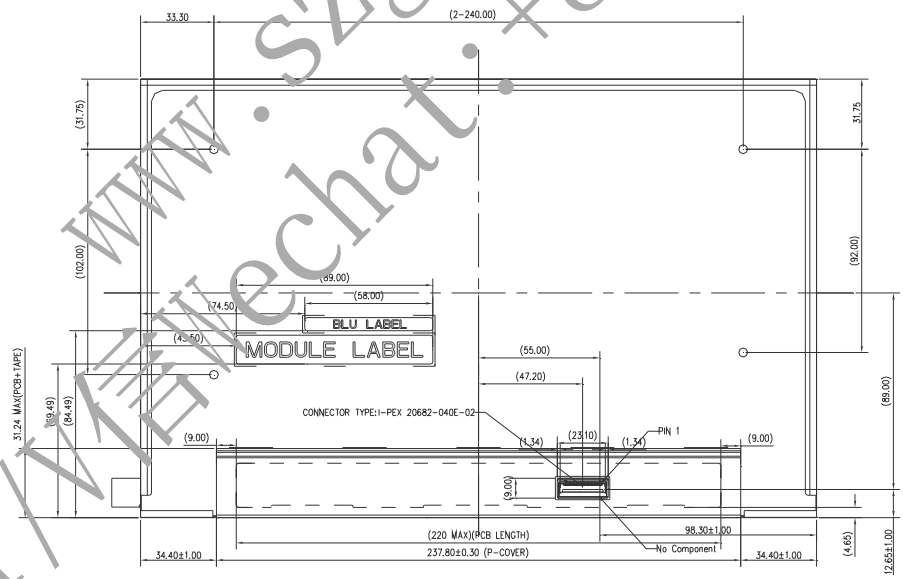
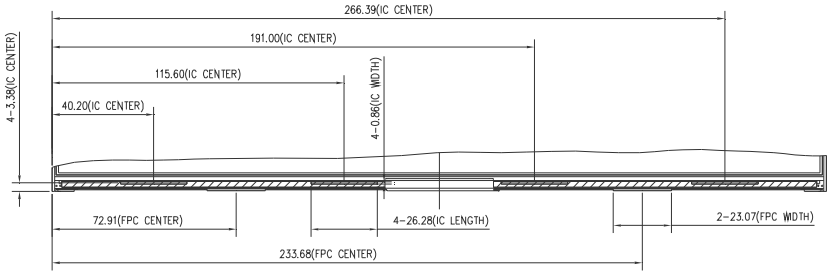
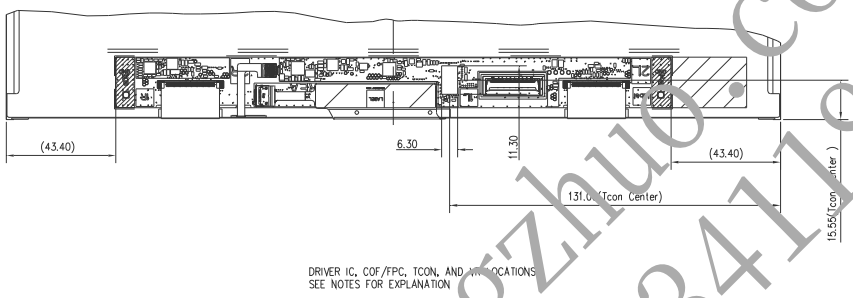
86	56	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	20	00100000
87	57	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	20	00100000
88	58	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	20	00100000
89	59	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	20	00100000
90	5A	Flag	00	00000000
91	5B	Flag	00	00000000
92	5C	Flag	00	00000000
93	5D	Data Type Tag: Alphanumeric Data String (ASCII)	FE	11111110
94	5E	Flag	00	00000000
95	5F	Dell P/N 1st Character "P"	50	01010000
96	60	Dell P/N 2nd Character "G"	47	01000111
97	61	Dell P/N 3rd Character "C"	43	01000011
98	62	Dell P/N 4th Character "W"	57	01010111
99	63	Dell P/N 5th Character "T"	54	01010100
100	64	EDID Revision	80	00000000
101	65	Manufacturer P/N "1"	31	00110001
102	66	Manufacturer P/N "4"	34	00110100
103	67	Manufacturer P/N "0"	30	00110000
104	68	Manufacturer P/N "J"	4A	01001010
105	69	Manufacturer P/N "C"	43	01000011
106	6A	Manufacturer P/N "N"	4E	01001110
107	6B	New line character indicates end of ASCII string	0A	00001010
108	6C	Flag	00	00000000
109	6D	Flag	00	00000000
110	6E	Flag	00	00000000
111	6F	Data Type Tag: Manufacturer Specified Data 00	00	00000000
112	70	Flag	00	00000000
113	71	Color Management	01	00000001
114	72	Panel Type and Revision	41	01000001
115	73	Frame Rate	01	00000001
116	74	Light Controller Interface and Maximum Luminance	9E	10011110
117	75	Front Surface / Polarizer and Pixel Structure	00	00000000
118	76	Multi-Media Features	00	00000000
119	77	Multi-Media Features	00	00000000
120	78	Special Features	00	00000000
121	79	Special Features	0A	00001010
122	7A	Special Features	01	00000001
123	7B	New line character indicates end of ASCII string	0A	00001010
124	7C	Padding with "Blank" character	20	00100000
125	7D	Padding with "Blank" character	20	00100000
126	7E	No extension	00	00000000
127	7F	Checksum	6A	11011010

Appendix. OUTLINE DRAWING



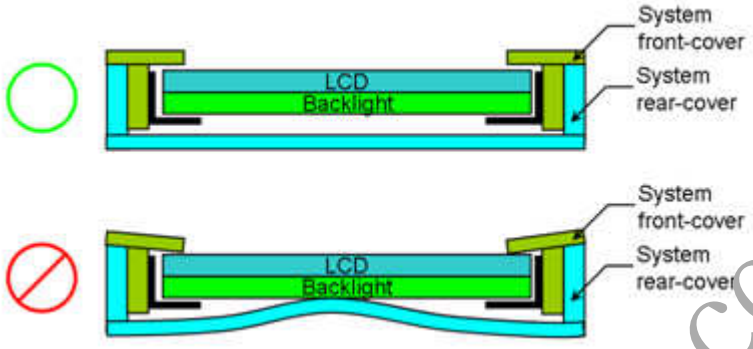
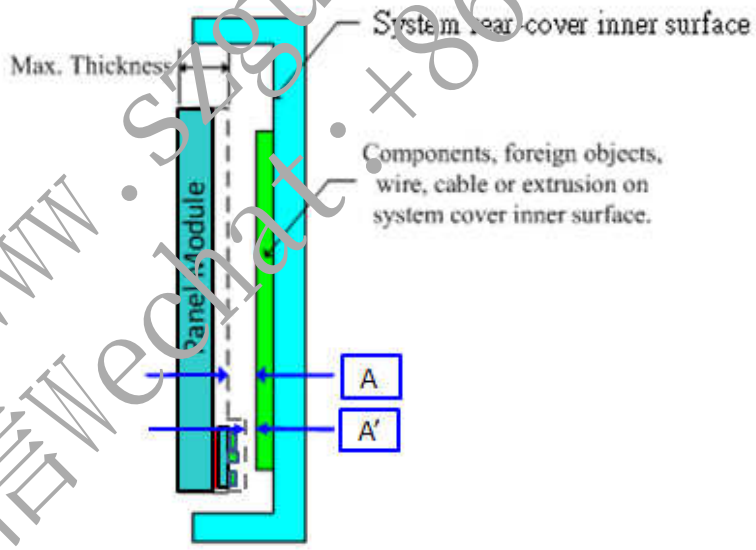


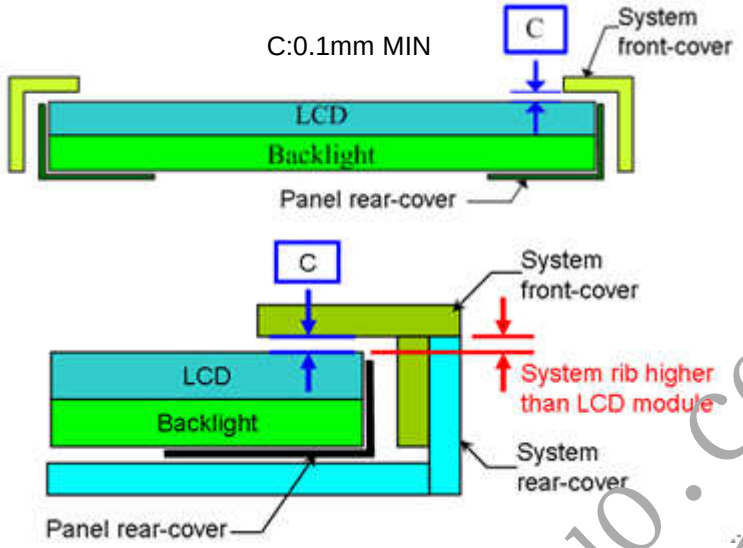
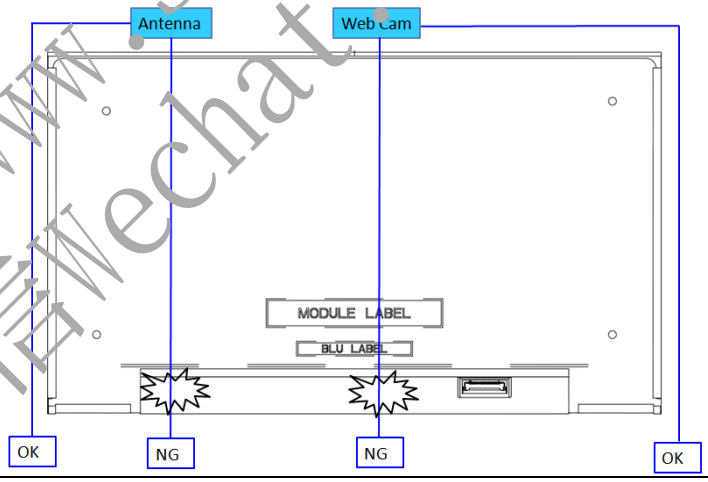




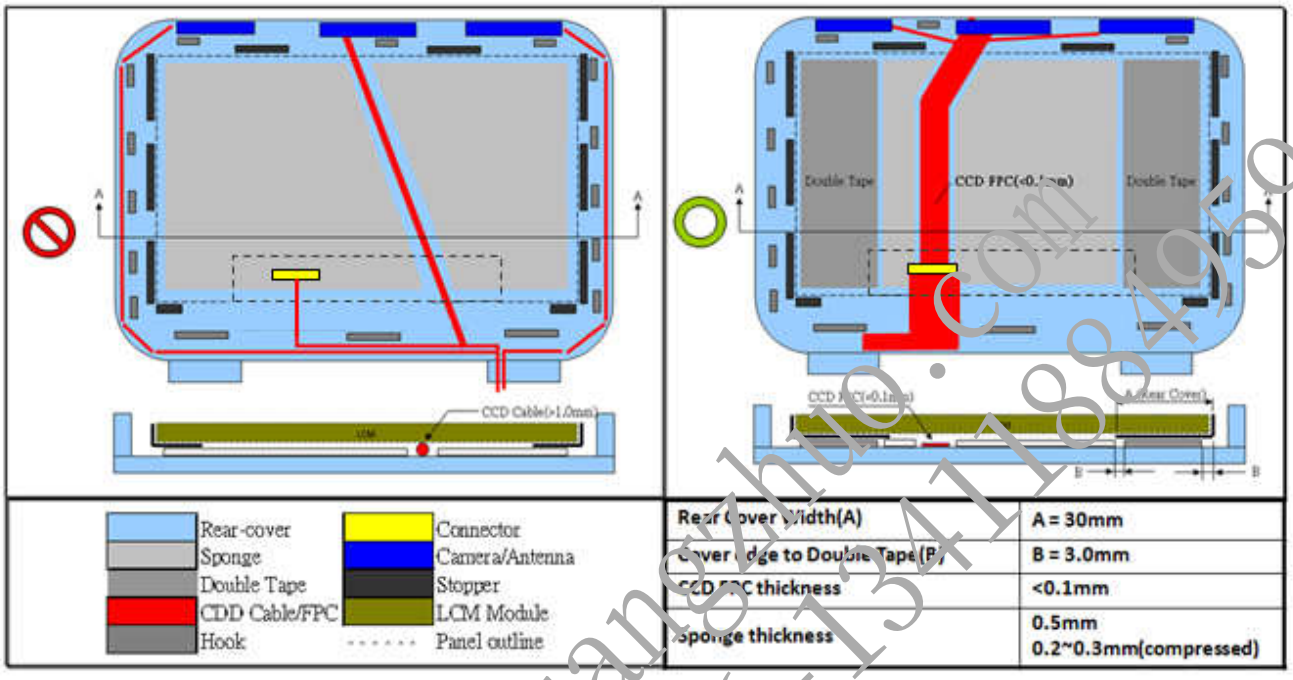
NOTES :
1. IN ORDER TO AVOID ABNORMAL DISPLAY, POOLING AND WHITE SPOT, NO OVERLAPPING IS SUGGESTED AT CABLES, ANTENNAS, CAMERA, WLAN, WAN OR FOREIGN OBJECTS OVER FPC, T-CON AND OVR LOCATIONS.
2. LVDS/EDP CONNECTOR IS MEASURED AT PIN1 AND ITS MATING LINE.
3. MODULE FLATNESS SPEC (0.5mm) MAX. (SPEC WILL BE MODIFIED AFTER DVT CHECK).
4. "( )" MARKS THE REFERENCE DIMENSION.
5. MEASUREMENT OF THICKNESS MUST BE MEASURED BY CALIPER OR MICROMETER.

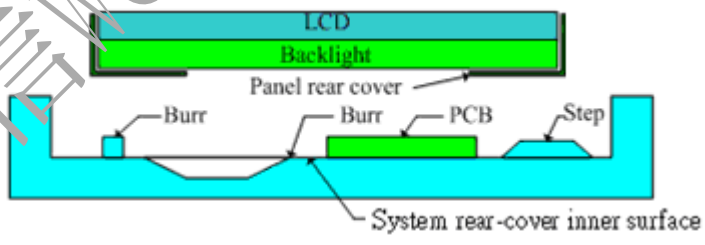
Appendix. SYSTEM COVER DESIGN GUIDANCE

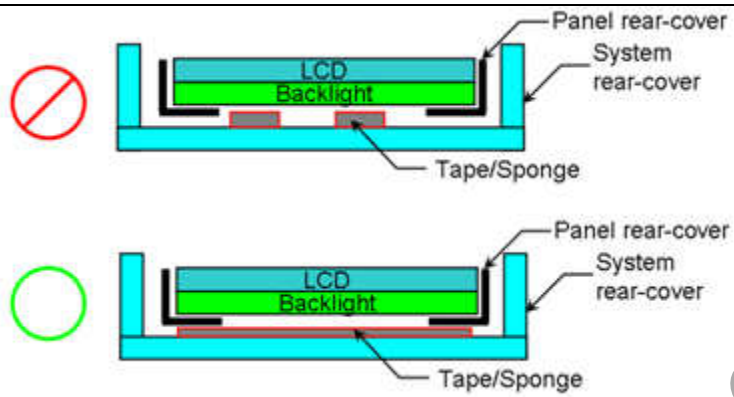
0.	**Permanent deformation of system cover after reliability test**
	
Definition	System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
1	**Design gap A and A' between panel & any components on system rear-cover**
	
Definition	Gap between panel's maximum thickness boundary & system's inner surface components such as wire, cable, extrusion is needed for preventing from backpack or pogo test fail. Because zero gap or interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur. Maximum flatness of panel and system rear-cover should be taken into account for gap design. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
2	**Design gap C between system front-cover & panel surface.**

<table>
<tr><td colspan="2"> 
</td></tr>
<tr><td>Definition</td><td>Gap between system front-cover & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system font-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test, or during pooling inspection procedure.
To remain sufficient gap, design with system rib higher than maximum panel thickness is recommended.
Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</td></tr>
<tr><td>3</td><td>Interference examination of antenna cable and WebCam wire</td></tr>
<tr><td colspan="2"> 
</td></tr>
<tr><td>Definition</td><td>Antenna cable or WebCam wire should not overlap with panel outline. Because issue such as abnormal display & white spot after backpack test, hinge test, twist test or pogo test may occur.
Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</td></tr>
<tr><td>4</td><td>Interference examination of antenna cable and Web Cam wire</td></tr>
</table>

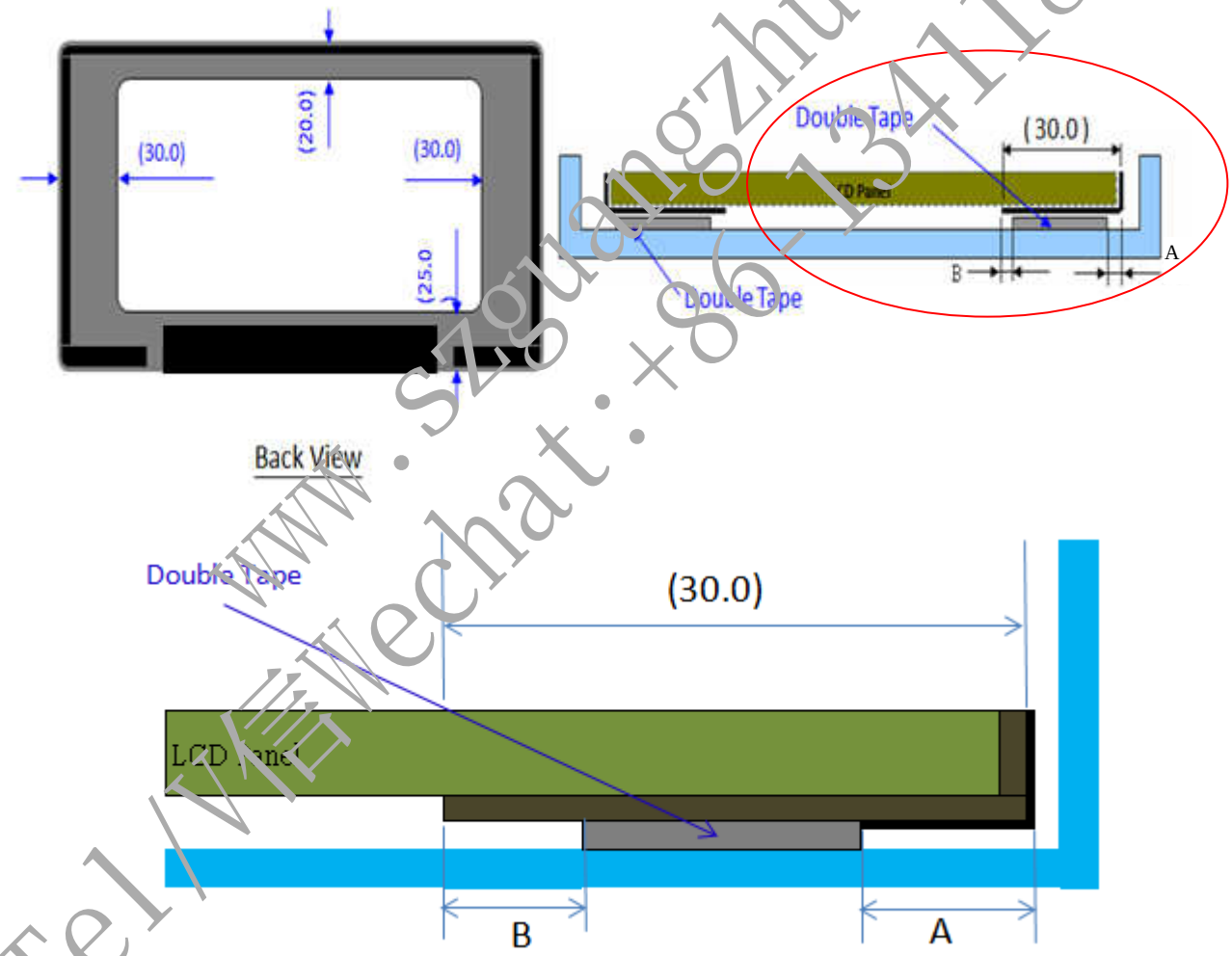
- To prevent panel damage, we suggest using CCD FPC to replace CCD cable
- Using double tape to fix LCM module for no bracket design.



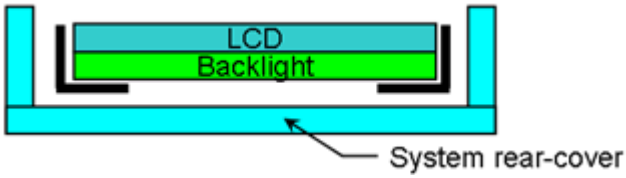
	If the antenna cable or Web Cam wire must overlap with the panel outline, both sides of the antenna cable or Web Cam wire must have a sponge(Sponge material can not contain NH3) and sponge require higher antenna cable or Web Cam wire.(Antenna cable or Web Cam wire should not overlap with TCON,COF/FPC,Driver IC) Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
5	**System rear-cover inner surface examination**
	
Definition	Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.
6-1	**Tape/sponge design on system inner surface**



Definition	To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, tape/sponge should be well covered under panel rear-cover. Because tape/sponge in separate location may act as pressure concentration location.
6-2	**Tape/sponge design on system inner surface**

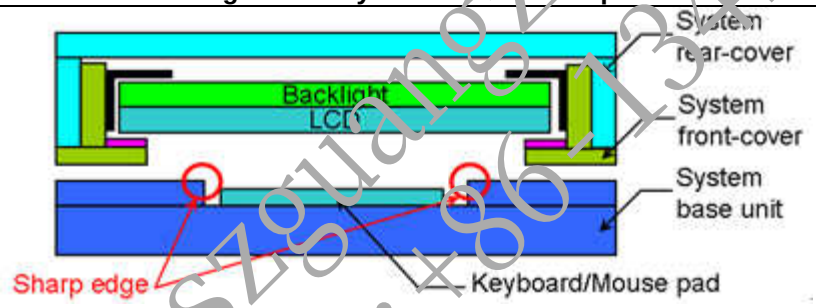


Definition	To prevent peeling the bezel tape in rework process. The length of double tape is 30 – (A+B), A is bezel tape length and B is the double tape attaching tolerance. Ex :A :2mm, B:2mm, the length of double tape is 30-(2+2)=26mm.
7	**Material used for system rear-cover**

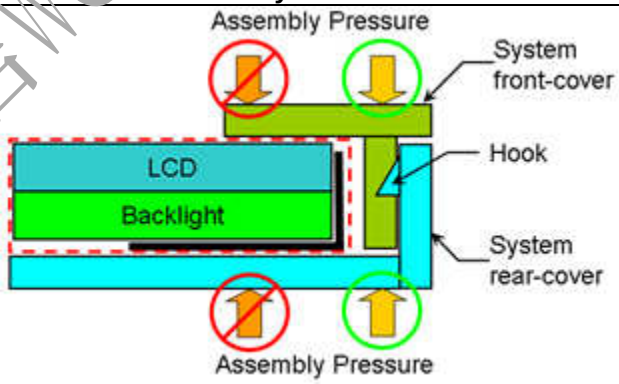


System rear-cover material: Al-Mg alloy

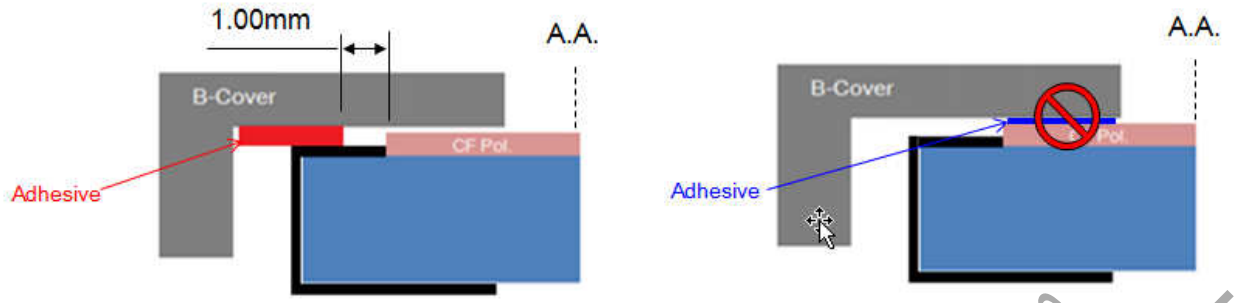
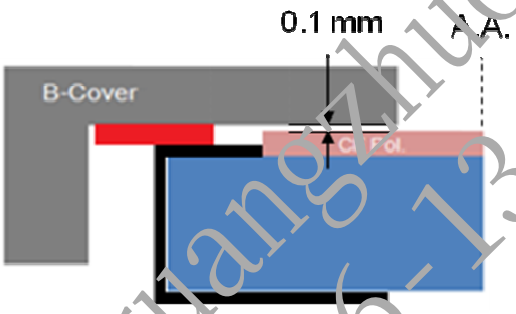
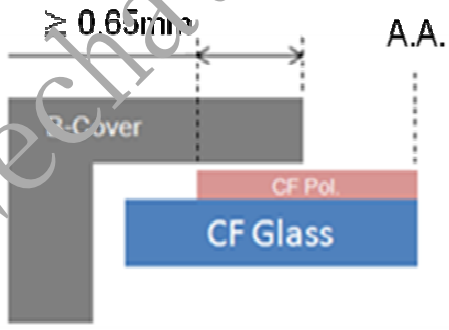
Definition	System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Solid structure design of system rear cover may also influence the rigidity of system rear-cover. The deformation of system rear cover should not caused interference.
8	**System base unit design near keyboard and mouse pad**



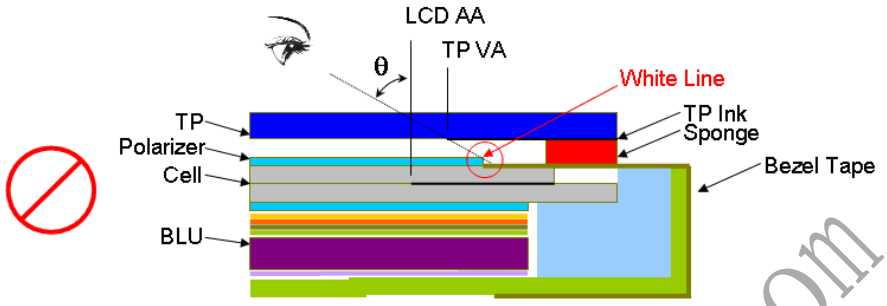
Definition	To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, sharp edge design in keyboard surface may damage panel during the test. We suggest to use slope edge design or to reduce the thickness difference of keyboard/mouse pad from the nearby surface.
9	**Assembly SOP examination for system front-cover with Hook design**

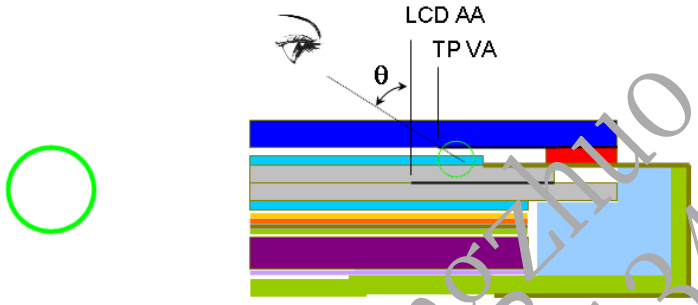


Definition	To prevent panel crack during system front-cover assembly process with hook design, it is not recommended to press panel or any location that related directly to the panel.
10	**Assembly SOP examination for system front-cover with Double tape design**

	
Definition	To prevent panel crack during system front-cover assembly process with double tape design, When system applied adhesive between B-Cover and LCD module, please design a distance 1.00mm between B-Cover's adhesive and CF pol.Do **NOT** put adhesive on CF pol
11	**System front-cover assembly reference with Double tape design**
	
Definition	To prevent system front-cover peeling at double tape contact area, A gap between B-Cover & CF-Pol. Is 0.1mm min.
12	System front-cover opening area reference with TFT-LCD module
	
Definition	To prevent panel the noise of B-cover & CF Pol. Distance from CF Pol. edge to front-cover edge more than 0.65mm.

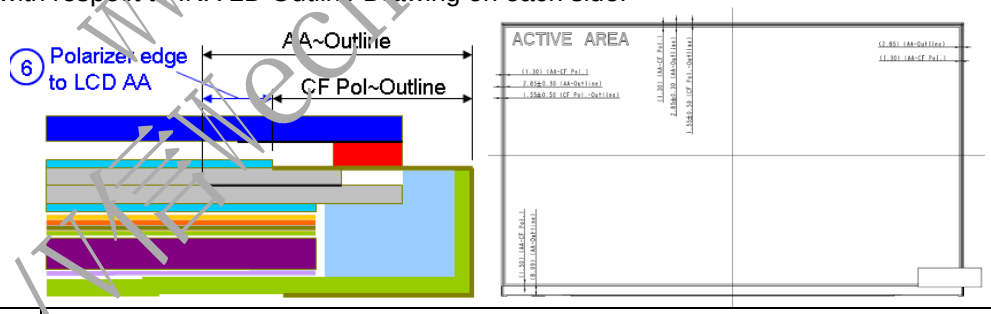
13	Touch Application : TP and LCD Module Combination for White Line Prevention



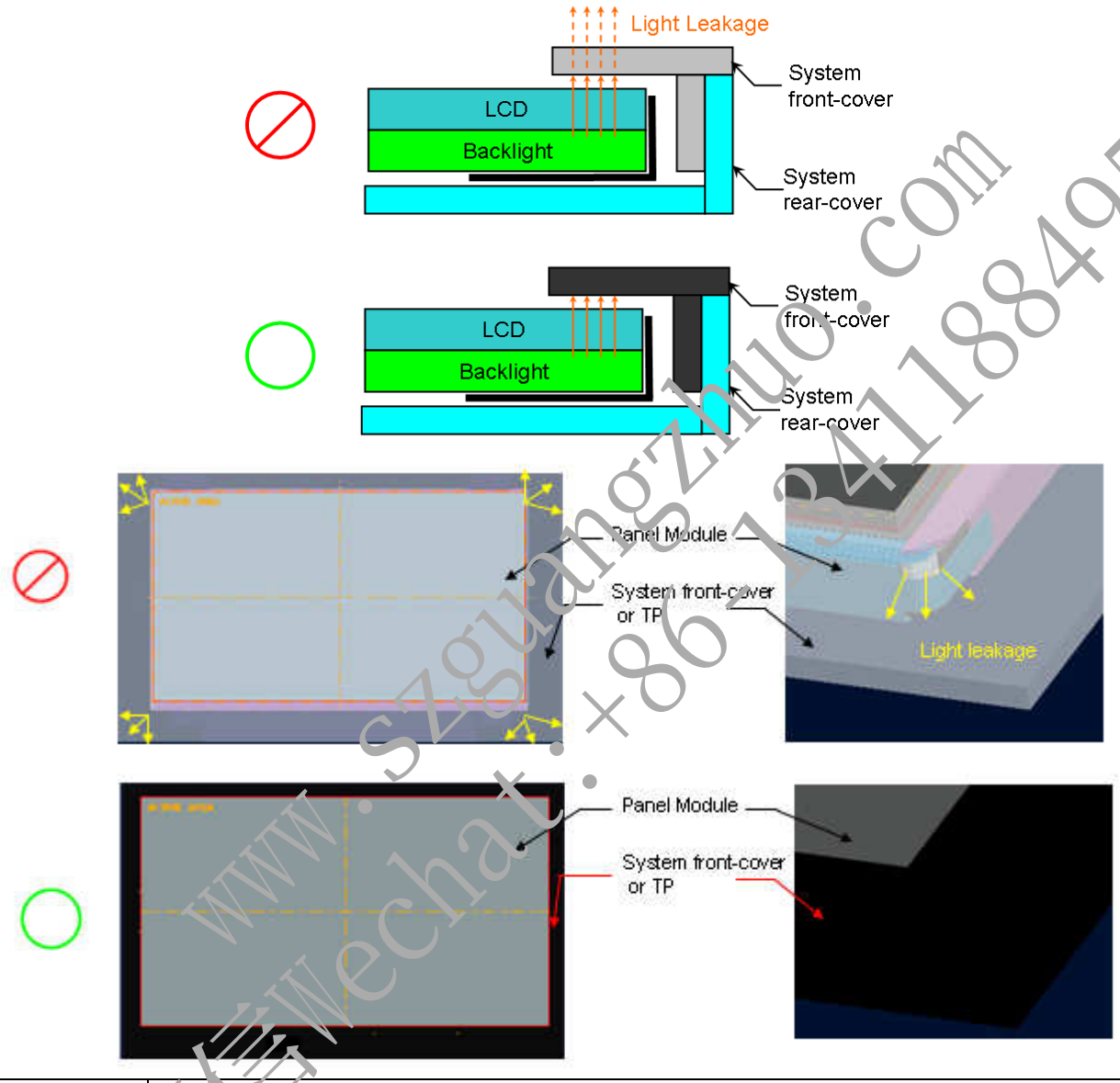


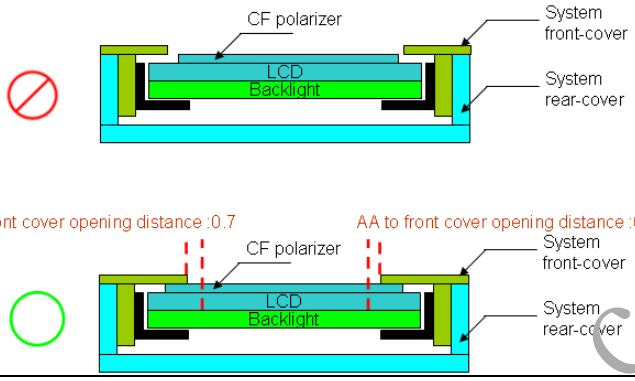
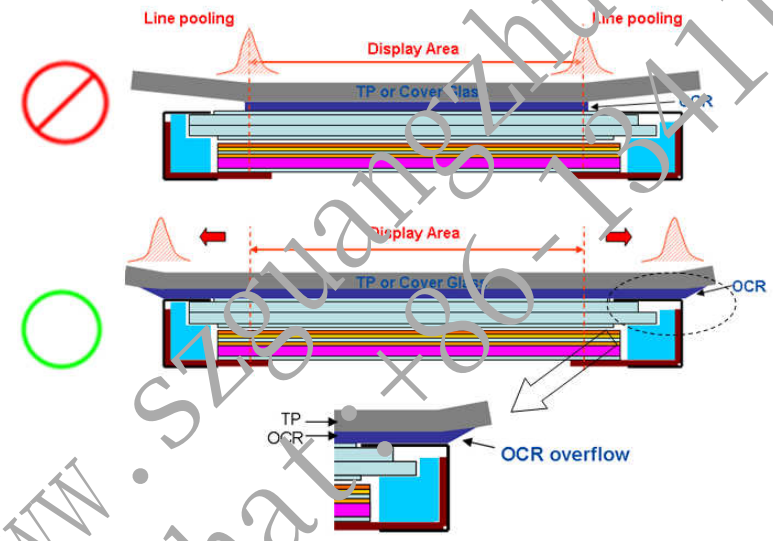
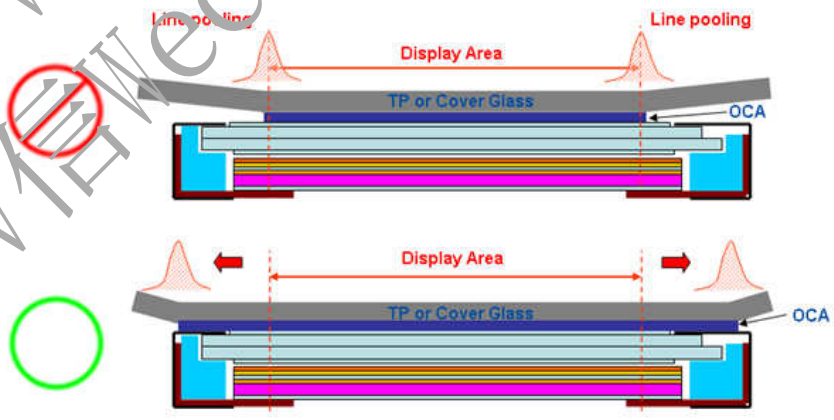
Parameter consideration for White Line Issue :	
1	TP VA to LCD AA distance
2	TP Assembly tolerance
3	TP Ink Printing tolerance
4	Sponge thickness and tolerance
5	Inspection/Viewing Angle specification
6	Polarizer edge to LCD AA distance and tolerance

Polarizer edge to LCD AA distance can be derived by “AA~Outline” – “CF Pol~Outline” with respect to INX 2D Outline Drawing on each side.



Definition	For using in Touch Application: to prevent White Line appears between TP and LCD module combination, the maximum inspection angle location must not fall onto LCD polarizer edge, otherwise light line near edge of polarizer will be appear. Parameters such as TP VA to LCD AA distance, TP assembly tolerance, TP Ink printing tolerance, Sponge thickness and tolerance, and Maximum Inspection/Viewing Angle, must be considered with respect to LCD module’s Polarizer edge location and tolerance. This consideration must be taken at all four edges separately. The goal is to find parameters combination that allow maximum inspection angle falls inside polarizer black margin area. Note: Information for Polarizer edge location and its tolerance can be derived from INX 2D Outline Drawing (“AA ~Outline“ - “CF Pol~Outline”). Note: Please feel free to contact INX FAE Engineer. By providing value of parameters above

	on each side, we can help to verify and pass the white line risk assessment for customer reference.
14	**Color of system front-cover material**
	
Definition	To prevent light leakage is seen at system front-cover due to material transparency, we suggest using dark color material (black) for system front-cover design.

15	**AA to front cover opening distance**
	
Definition	To prevent CF polarizer edge leakage .We suggest front cover opening no more than 0.7mm larger than active area on all 4 sides.
16	**Use OCR Lamination**
	
Definition	OCR glue as possible beyond module, in order to avoid Line Pooling
17	**Use OCA Lamination**
	
Definition	OCA glue as possible plastered throughout the module, in order to avoid Line Pooling.

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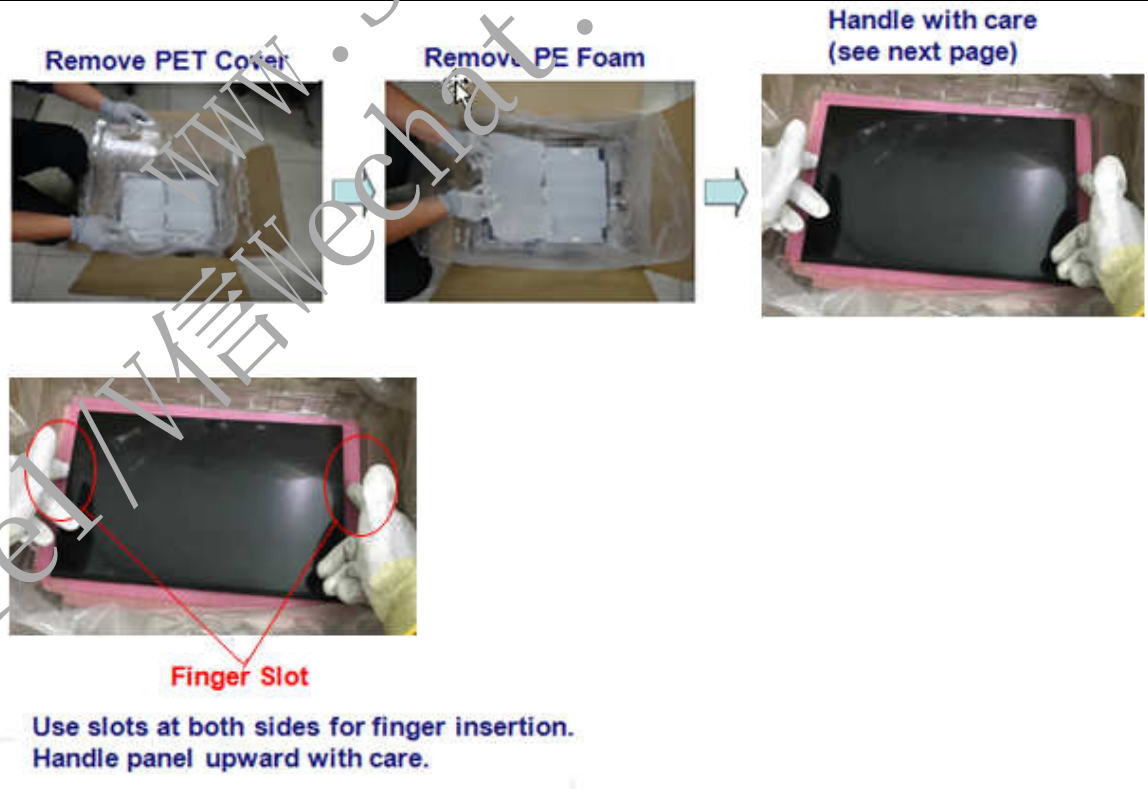
Appendix. LCD MODULE HANDLING MANUAL

Purpose	• **This SOP is prepared to prevent panel dysfunction possibility through incorrect handling procedure.** • **This manual provides guide in unpacking and handling steps.** • **Any person which may contact / related with panel, should follow guide stated in this manual to prevent panel loss.**
1.	**Unpacking**

2.	**Panel Lifting**



3.	Do and Don't

Do :

- Handle with both hands.
- Handle panel at left and right edge.

Don't :

- Lifting with one hand.

- Handle at PCBA side.

Don't :

- Stack panels.

- Press panel.

Don't :

- Put foreign stuff onto panel

- Put foreign stuff under panel

Don't :

- Hold at panel corner.

Don't :

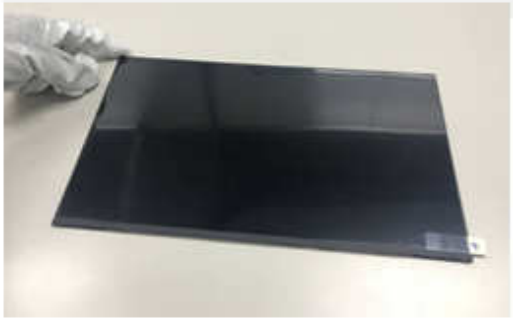
- Twist panel.

Do :

- Remove panel protector film starts from pull tape

Don't :

- Remove panel protector film From film another side.



Don't :

- Touch or Press PCBA Area.