Doc. Number:

☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

MODEL NO.: N140JCG-GS9
H/W:C5

Customer:

APPROVED BY SIGNATURE

Name / Title
Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By

CONTENTS

REVISION HISTORY

Version	Date	Page	Description
3.0	Jan.17, 2022	All	Approval Spec Ver.3.0 was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N140JCG-GS9 is a 14.0” (14.0” diagonal) TFT Liquid Crystal Display NB module with LED Backlight unit and 30 pins eDP interface. This module supports 1920 x 1200 WUXGA mode and can display 16,777,216 colors. This panel complies with low blue light and is certified as a component under certain conditions.

1.2 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Screen Size	14.0 diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1200	pixel	-
Pixel Pitch	0.15708 (H) x 0.15708 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16,777,216	color	-
Interface	eDP1.4		
LED IC Dimming Mode	DC mode		(2)
Transmissive Mode	Normally black	-	-
Surface Treatment	Hard coating , Anti-Glare	-	-
Luminance, White	400	Cd/m2	
Color Gamma	100%	sRGB	
Power Consumption	Total 2.73 W (Max.) @ cell 0.49 W (Max.), BL 2.24 W (Max.)		(1)
Special Function Support	Free-sync (40 Hz ~ 60Hz) PSR (PSR1 , PSR2...) Low Blue Light, TUV Method-2		

Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, fv = 60 Hz, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 ºC, whereas **Mosaic** pattern is displayed.

Note (2) Display port interface signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.4 (eDP1.4). There are many optional items described in eDP1.4. If some optional item is requested, please contact us.

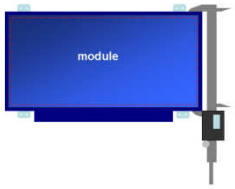
2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	306.99	307.29	307.59	mm	(1)(2)
	Vertical (V) (w/o PCB)	198.95	199.25	199.55	mm	
	Thickness (T) (w/o PCB)	1.8	1.9	2.00	mm	
Active Area	Horizontal	301.49	301.59	301.69	mm	
	Vertical	188.40	188.50	188.60	mm	
Weight		-	191.8	205.0	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

(2) Dimensions are measured by caliper.

(3) Panel thickness is measured with calipers clamping mylar or tape tightly



2.1 CONNECTOR TYPE

Please refer appendix outline drawing for detail design.

Connector Part No.: IPEX-20455-030E-76

User's connector Part No: IPEX-20453-030T-03

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

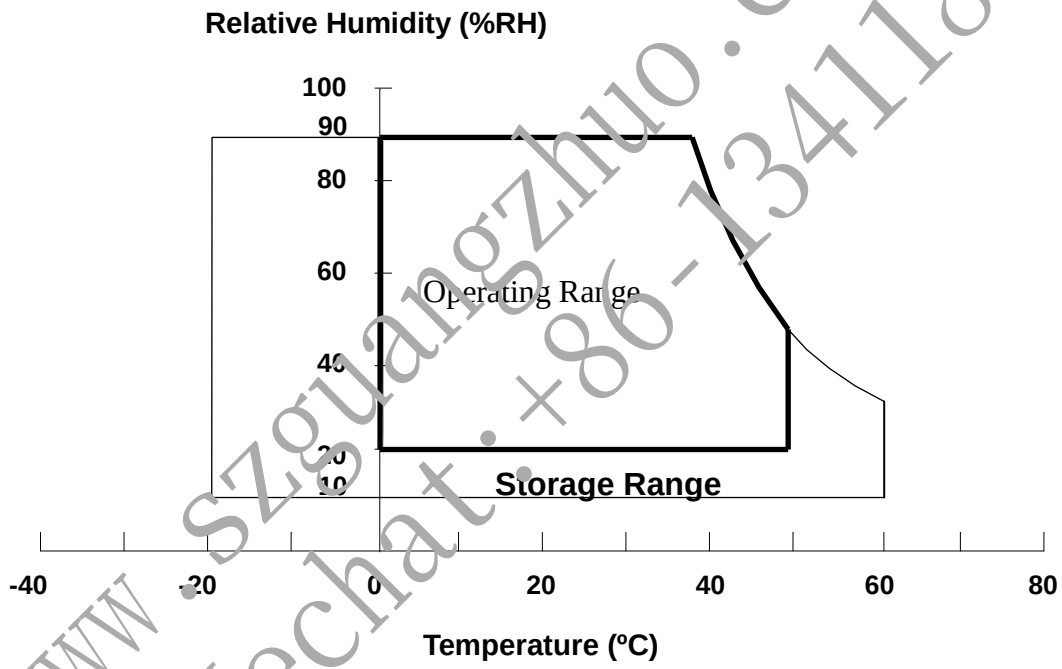
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)

Note (1) (a) 90 %RH Max. (Ta < 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max.

(c) No condensation.

Note (2) The temperature of panel surface should be 0 ºC min. and 50 ºC max.



3.2 ELECTRICAL ABSOLUTE RATINGS

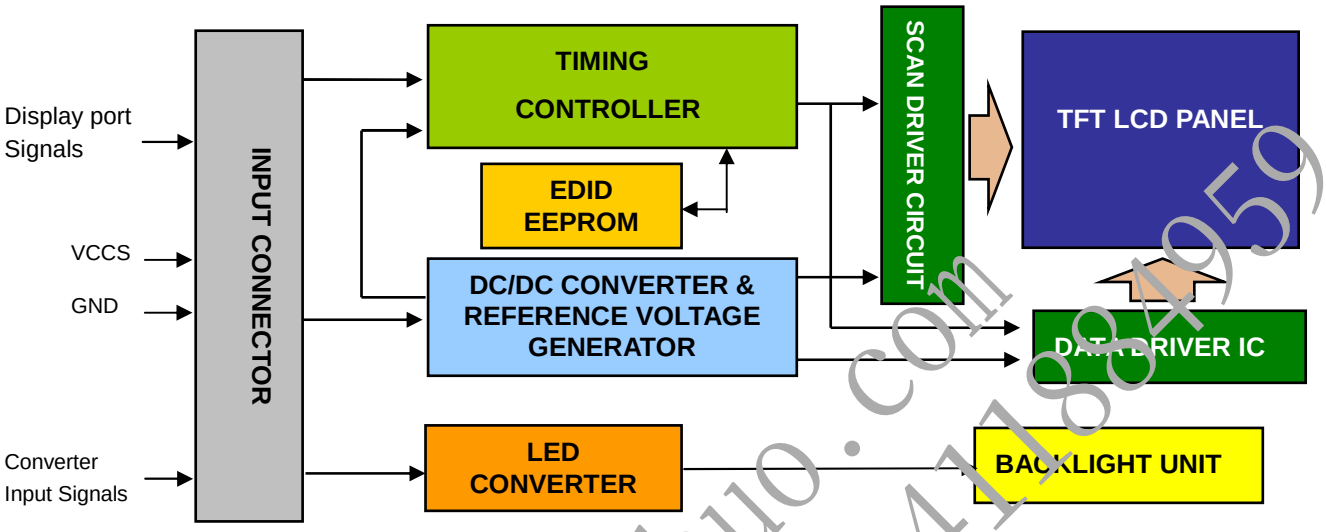
3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	+4.0	V	
Converter Input Voltage	LED_VCCS	-0.3	(25)	V	(1)
Converter Control Signal Voltage	LED_PWM,	-0.3	(6)	V	(1)
Converter Control Signal Voltage	LED_EN	-0.3	(6)	V	(1)

Note (1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “ELECTRICAL CHARACTERISTICS”.

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserved for LCD test)	
2	H_GND	High Speed Ground	
3	Lane1_N	Complement Signal Link Lane 1	
4	Lane1_P	True Signal Link Lane 1	
5	H_GND	High Speed Ground	
6	Lane0_N	Complement Signal-Lane 0	
7	Lane0_P	True Signal Main Lane 0	
8	H_GND	High Speed Ground	
9	AUX+	True Signal-Auxiliary Channel	
10	AUX-	Complement Signal-Auxiliary Channel	
11	H_GND	High Speed Ground	
12	VCCS	Power Supply +3.3 V (typical)	
13	VCCS	Power Supply +3.3 V (typical)	
14	NC	No Connection (Reserved for LCD test)	
15	GND	Ground	
16	GND	Ground	
17	HPD	Hot Plug Detect	
18	BL_GND	BL Ground	
19	BL_GND	BL Ground	
20	BL_GND	BL Ground	
21	BL_GND	BL Ground	
22	LED_EN	BL_Enable Signal of LED Converter	
23	LED_PWM	PWM Dimming Control Signal of LED Converter	
24	NC	No Connection (Reserved for LCD test)	
25	NC	No Connection (Reserved for LCD test)	

26	LED_VCCS	BL Power	
27	LED_VCCS	BL Power	
28	LED_VCCS	BL Power	
29	LED_VCCS	BL Power	
30	NC	No Connection (Reserved for LCD test)	

Note (1) The first pixel is odd as shown in the following figure.

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

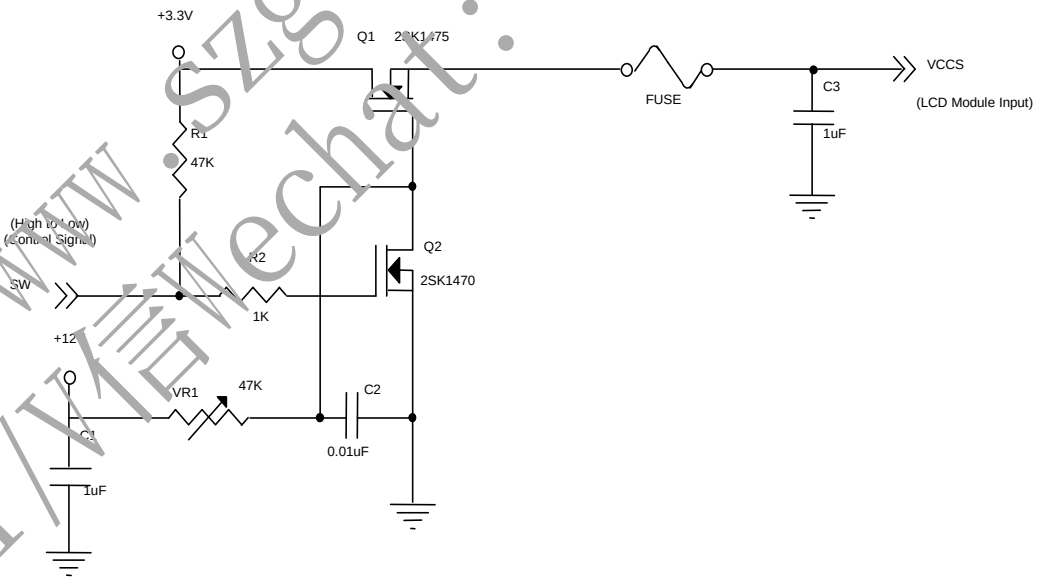
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)
Ripple Voltage		V_{RP}	-	-	100	mV	(1)
Inrush Current		I_{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Black	Icc		(126)	(149)	mA	(3)
	Mosaic			(133)	(149)	mA	(3)
	Solid Pattern			(133)	(213)	mA	(3)
	Mosaic @PSR			(133)	(149)	mA	(3)a
	Solid Pattern @ PSR			(133)	(213)	mA	(3)a
HPD Impedance		R_{HPD}	30K			ohm	(4)
HPD	High Level		2.25	-	3.6	V	(5)
	Low Level		0	-	0.8	V	(5)

Note (1) The ambient temperature is Ta = 25 ± 2 °C.

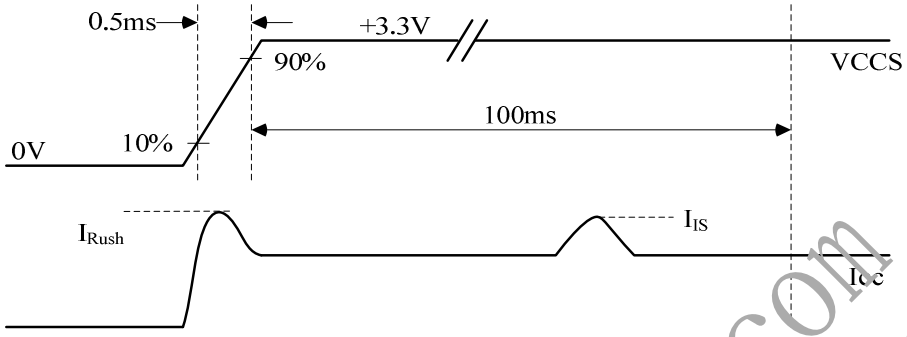
Note (2) I_{RUSH}: the maximum current when VCCS is rising

I_{IS}: the maximum current of the first 100ms after power on

Measurement Conditions: Shown as the following figure. Test pattern: black.

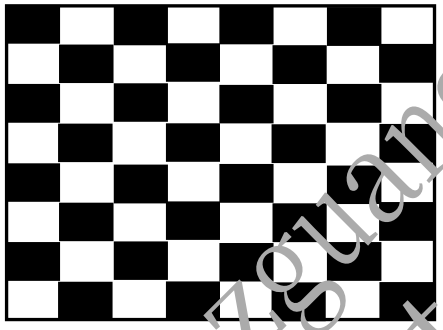


VCCS rising time is 0.5ms



Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ºC, DC Current and f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern



Active Area

b. The solid pattern is the largest one of R/G/B pattern.

Note (4) The specified power are the sum of LCD panel electronics input power and the converter input power. Test conditions are as follows.

(a) VCCS = 3.3 V, Ta = 25 ± 2 ºC, f_v = 60 Hz,

(b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.

(c) Luminance: 60 nits.

Note (5) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. Please refer to Note (4) of 4.3.2 LED CONVERTER SPECIFICATION to obtain more information.

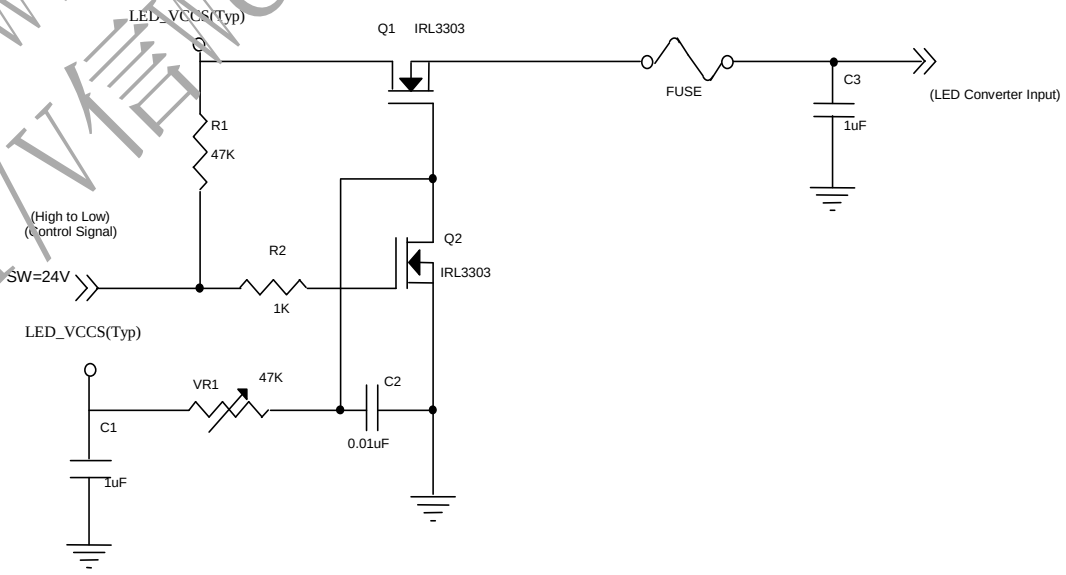
4.3.2 LED CONVERTER SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input power supply voltage		LED_Vccs	5	12	21	V	
Converter Inrush Current		$ILED_{RUSH}$	-	-	1.5	A	(1)
EN Control Level	Backlight On		2.3	-	3.6	V	(4)
	Backlight Off		0	-	0.6	V	(4)
LED_EN Impedance		R_{LED_EN}	30K	-	-	ohm	(4)
PWM Control Level	PWM High Level		2.3	-	3.6	V	(4)
	PWM Low Level		0	-	0.6	V	(4)
PWM Impedance		R_{PWM}	30K	-	-	ohm	(4)
PWM Control Duty Ratio			5	-	100	%	(5)
PWM Control Permissive Ripple Voltage		V_{PWM_pr}	-	-	100	mV	
PWM Control Frequency		f_{PWM}	190	-	1K	Hz	(2)
LED Power Current	LED_VCCS = Typ.	ILED	(150)	(178)	(187)	mA	(3)

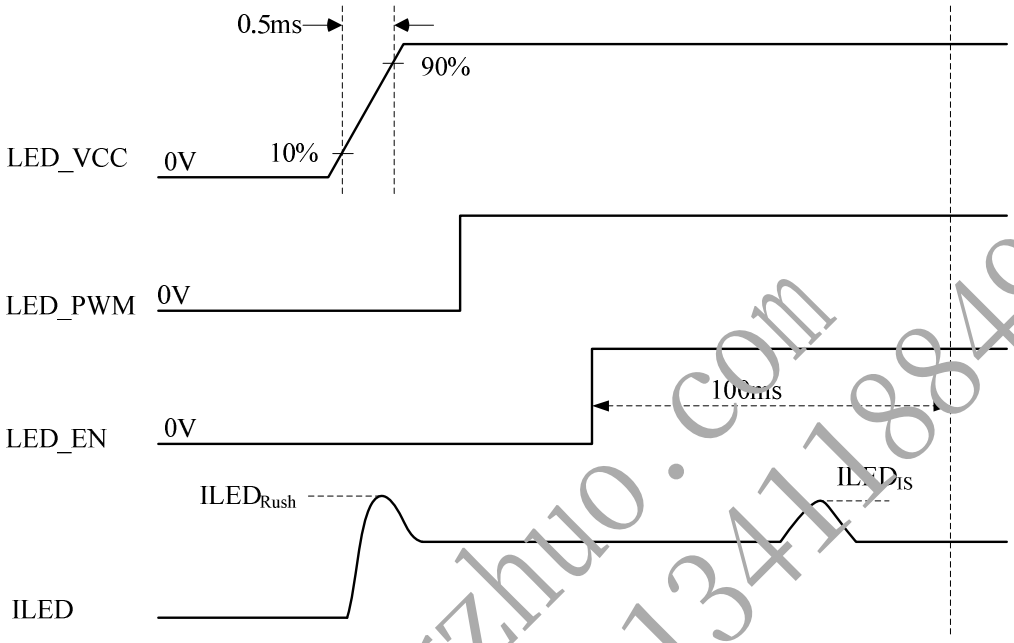
Note (1) $ILED_{RUSH}$: the maximum current when LED_VCCS is rising,

$ILED_{IS}$: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.



VLED rising time is 0.5ms



Note (2) If PWM control frequency is applied in the range less than 1kHz, the "waterfall" phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

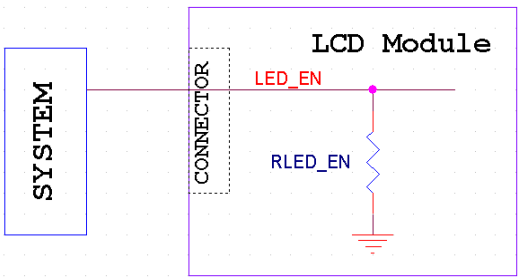
$$(N + 0.33) * f \leq f_{PWM} \leq (N + 0.66) * f$$

N : Integer $(N \geq 3)$

f : Frame rate

Note (3) The specified LED power supply current is under the conditions at "LED_VCCS = Typ.", Ta = 25 ± 2°C, f_{PWM} = 200 Hz, Duty=100%.

Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. For example, the figure below describes the equivalent pull down impedance of LED_EN (if it exists). The rest pull down impedances of other signals (eg. HPD, PWM …) are in the same concept.



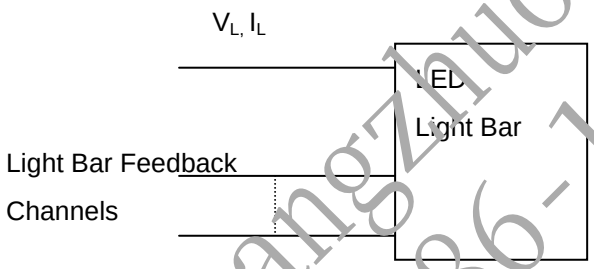
Note (5) If the cycle-to-cycle difference of PWM duty exceeds 0.1%, especially when the PWM duty is low, slight brightness change might be observed.

4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	33.6	34.2	36	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L	- -	57	- -	mA	
Power Consumption	P_L		1.9494	2.052	W	(3)
LED Life Time	L_{BL}	15000	-	-	Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below:



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 °C and I_L = (9.5) mA (Per EA) until the brightness becomes ≦ 50% of its original value.

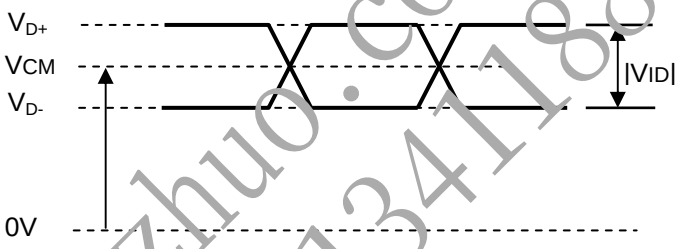
4.4 DISPLAY PORT INPUT SIGNAL TIMING SPECIFICATIONS

4.4.1 ELECTRICAL SPECIFICATIONS

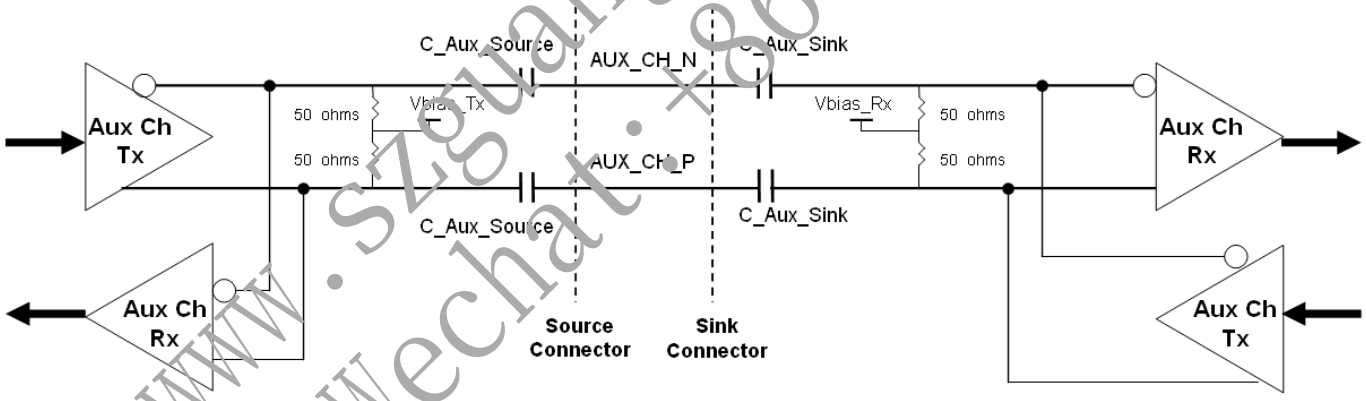
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Signal Common Mode Voltage(MainLink and AUX)	VCM	0		2	V	(1)(4)
AUX AC Coupling Capacitor	C_Aux_Source	75		200	nF	(2)
Main Link AC Coupling Capacitor	C_ML_Source	75		200	nF	(3)

Note (1)Display port interface related AC coupled signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2. There are many optional items described in eDP1.2. If some optional item is requested, please contact us.

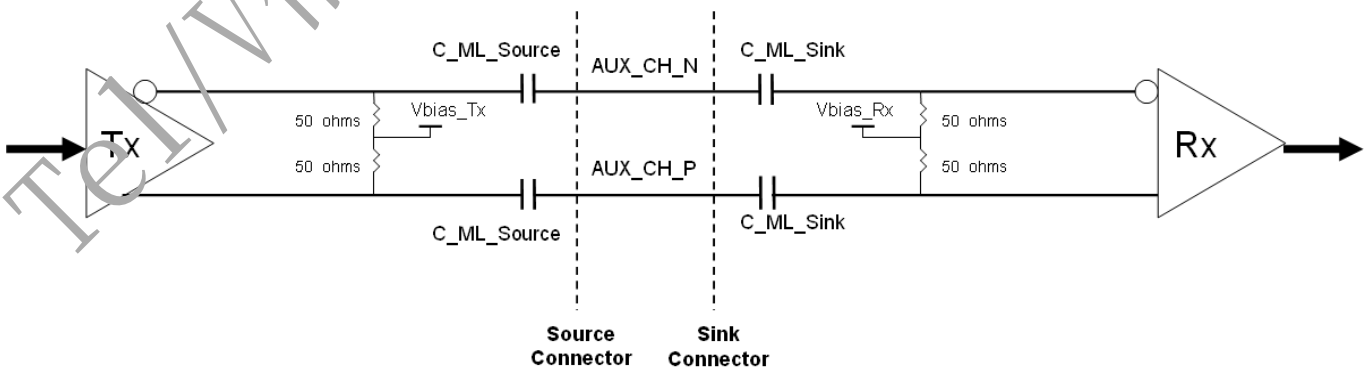
Single Ended



(2) Recommended eDP AUX Channel topology is as below and the AUX AC Coupling Capacitor (C_Aux_Source) should be placed on the source device.



(3) Recommended Main Link Channel topology is as below and the Main Link AC Coupling Capacitor (C_ML_Source) should be placed on the source device.



(4) The source device should pass the test criteria described in DisplayPortCompliance Test Specification (CTS) 1.1

4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Refresh Rate 60Hz

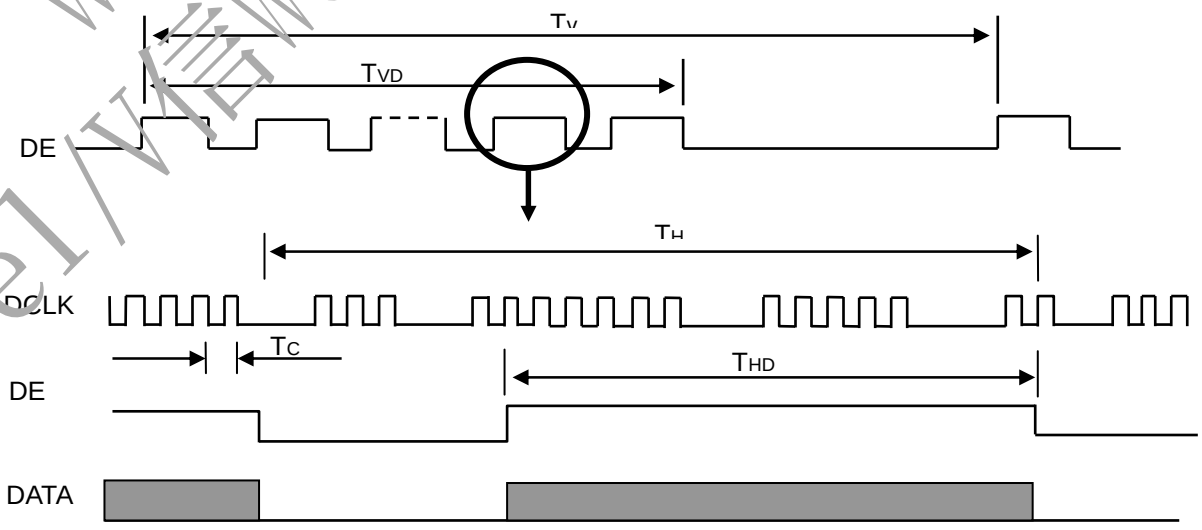
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	(152.28)	(154.26)	(156.24)	MHz	-
DE	Vertical Total Time	TV	(1232)	(1236)	(1240)	TH	-
	Vertical Active Display Period	TVD	(1200)	(1200)	(1200)	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	(32)	TV-TVD	TH	-
	Horizontal Total Time	TH	(2060)	(2080)	(2100)	Tc	-
	Horizontal Active Display Period	THD	(1920)	(1920)	(1920)	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	(160)	TH-THD	Tc	-

Refresh rate 40Hz (Power Saving Mode)

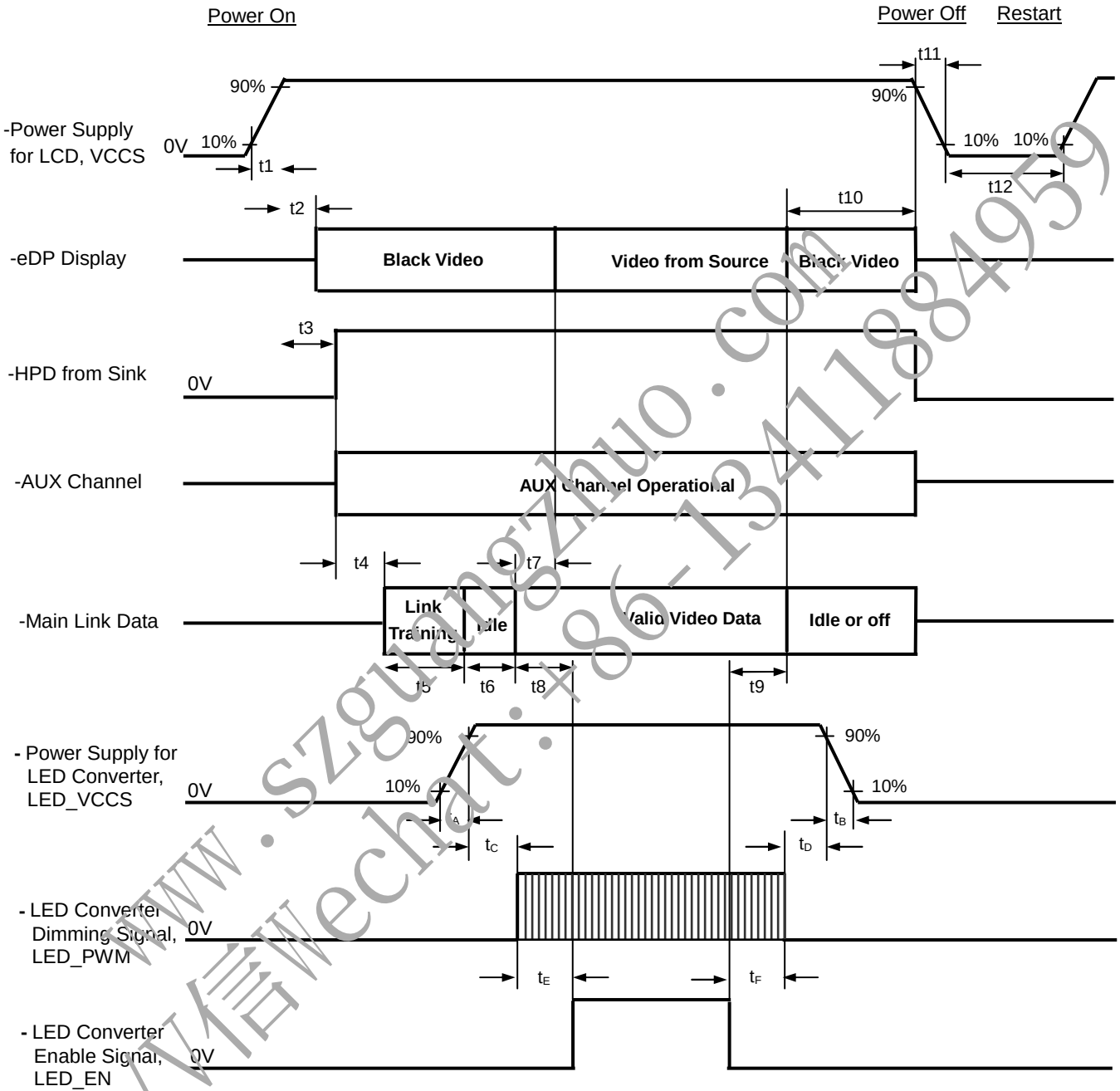
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	(101.52)	(102.84)	(104.16)	MHz	(1)
DE	Vertical Total Time	TV	(1232)	(1236)	(1240)	TH	(1)
	Vertical Active Display Period	TVD	(1200)	(1200)	(1200)	TH	(1)
	Vertical Active Blanking Period	TVB	TV-TVD	(32)	TV-TVD	TH	(1)
	Horizontal Total Time	TH	(2060)	(2080)	(2100)	Tc	(1)
	Horizontal Active Display Period	THD	(1920)	(1920)	(1920)	Tc	(1)
	Horizontal Active Blanking Period	THB	TH-THD	(160)	TH-THD	Tc	(1)

Note (1) The panel can operate at 60Hz normal mode and power saving mode, respectively. All reliability tests are based on specific timing of 60Hz refresh rate. We can only assure the panel's electrical function at power saving mode.

INPUT SIGNAL TIMING DIAGRAM



4.6 POWER ON/OFF SEQUENCE



Timing Specifications

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	Power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t2	Delay from LCD,VCCS to black video generation	Sink	0	200	ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source (see Notes:2 and 3 below)
t3	Delay from LCD,VCCS to HPD high	Sink	0	200	ms	Sink AUX Channel must be operational upon HPD high (see Note:4 below)
t4	Delay from HPD high to link training initialization	Source	0	-	ms	Allows for Source to read Link capability and initialize
t5	Link training duration	Source	0	-	ms	Dependant on Source link training protocol
t6	Link idle	Source	0	-	ms	Min Accounts for required BS-Idle pattern. Max allows for Source frame synchronization
t7	Delay from valid video data from Source to video on display	Sink	0	50	ms	Max value allows for Sink to validate video data and timing. At the end of T7, Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and Sink will no longer generate automatic Black Video
t8	Delay from valid video data from Source to backlight on	Source	80	-	ms	Source must assure display video is stable *: Recommended by INX. To avoid garbage image.
t9	Delay from backlight off to end of valid video data	Source	0	-	ms	Source must assure backlight is no longer illuminated. At the end of T9, Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and Sink will automatically display Black Video. (See Notes: 2 and 3 below)
t10	Delay from end of valid video data from Source to power off	Source	0	500	ms	Black video will be displayed after receiving idle or off signals from Source
t11	VCCS power rail fall time, 90% to 10%	Source	0.5	10	ms	-
t12	VCCS Power off time	Source	500	-	ms	-
t_A	LED power rail rise time, 10% to 90%	Source	0.5	10	ms	-

t_B	LED power rail fall time, 90% to 10%	Source	0	10	ms	-
t_C	Delay from LED power rising to LED dimming signal	Source	1	-	ms	-
t_D	Delay from LED dimming signal to LED power falling	Source	1	-	ms	-
t_E	Delay from LED dimming signal to LED enable signal	Source	(0)	-	ms	-
t_F	Delay from LED enable signal to LED dimming signal	Source	(0)	-	ms	-

Note (1) Please don't plug or unplug the interface cable when system is turned on.

Note (2) The Sink must include the ability to automatically generate Black Video autonomously. The Sink must automatically enable Black Video under the following conditions:

- Upon LCDVCC power-on (within T2 max)
- When the "NoVideoStream_Flag" (VB-ID Bit 3) is received from the Source (at the end of T9)

Note (3) The Sink may implement the ability to disable the automatic Black Video function, as described in Note (2), above, for system development and debugging purposes.

Note (4) The Sink must support AUX Channel polling by the Source immediately following LCDVCC power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to response to an AUX Channel transaction with the time specified within T3 max.

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

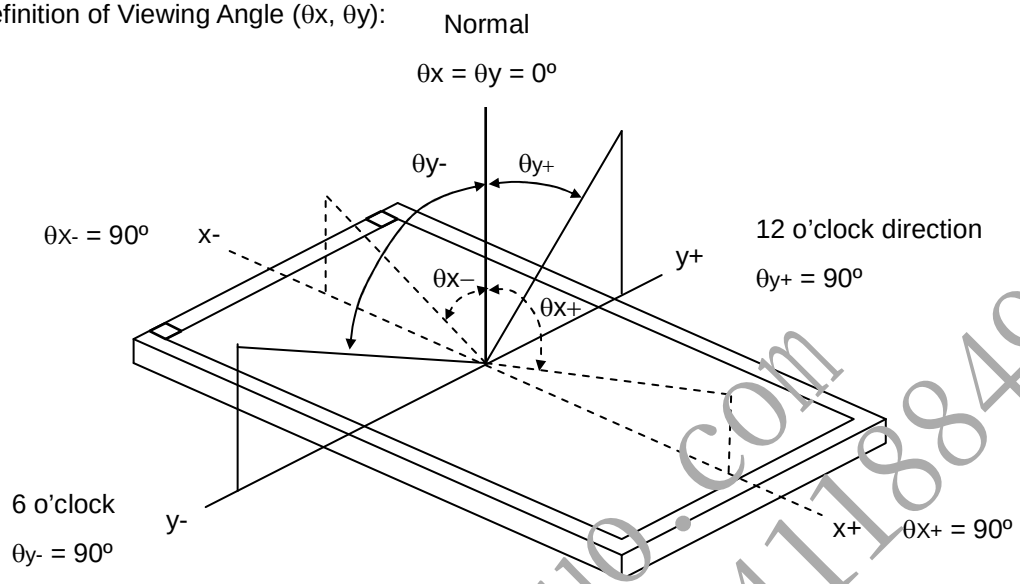
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	57	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	1000	1500	-	-	(2), (5) ,(7)
Response Time		T_R		-	16	19	ms	(3) ,(7)
		T_F		-	14	16	ms	
Average Luminance of White		L_{AVE}		340	400	-	cd/m^2	(4), (6) ,(7)
Color Chromaticity	Red	Rx		Typ – 0.03	0.640	Typ + 0.03	-	(1) ,(7)
		Ry			0.330		-	
	Green	Gx			0.300		-	
		Gy			0.600		-	
	Blue	Bx			0.150		-	
		By			0.060		-	
	White	Wx			0.313		-	
		Wy			0.329		-	
Viewing Angle	Horizontal	θ_x+	CR≥10	80	89		Deg.	(1),(5) , (7)
		θ_x-		80	89	-		
	Vertical	θ_Y+		80	89	-		
		θ_Y-		80	89	-		
White Variation		δW_{5p}	θ_x=0°, θ_Y =0°		1.13	1.25	-	(5),(6) , (7)
		δW_{13p}	θ_x=0°, θ_Y =0°		1.35	1.54	-	
Low Blue Light		BLR	θx=0°, θY =0°	-	-	50	%	(1), (5), (7), (8)
		CCT		5500	-	7000	K	

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

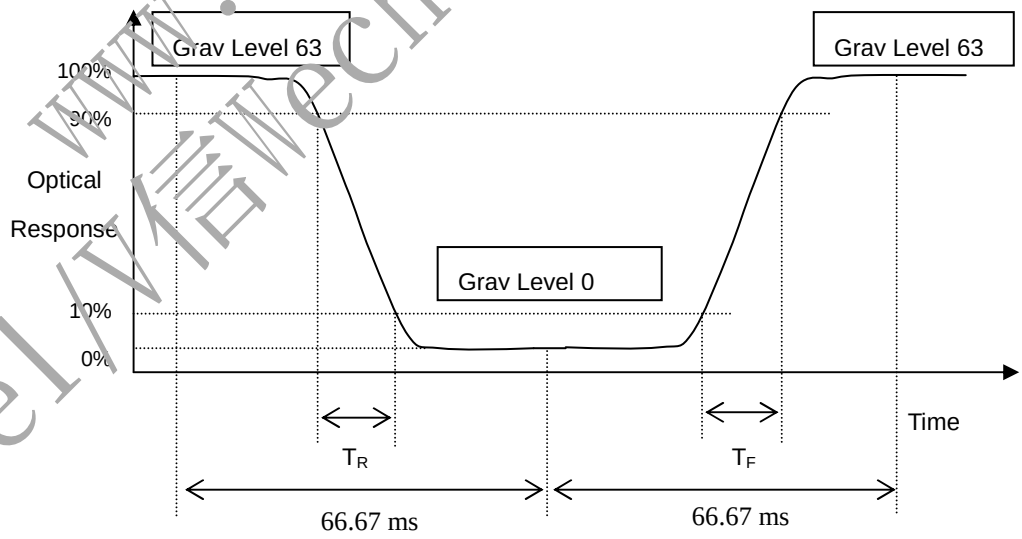
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

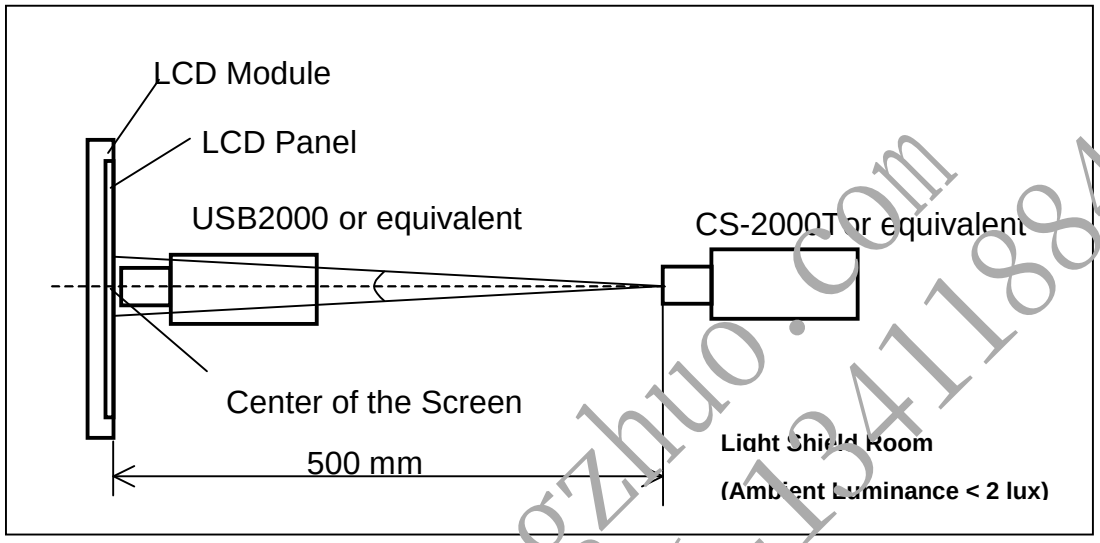
Measure the luminance of gray level 63 at 5 points

L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

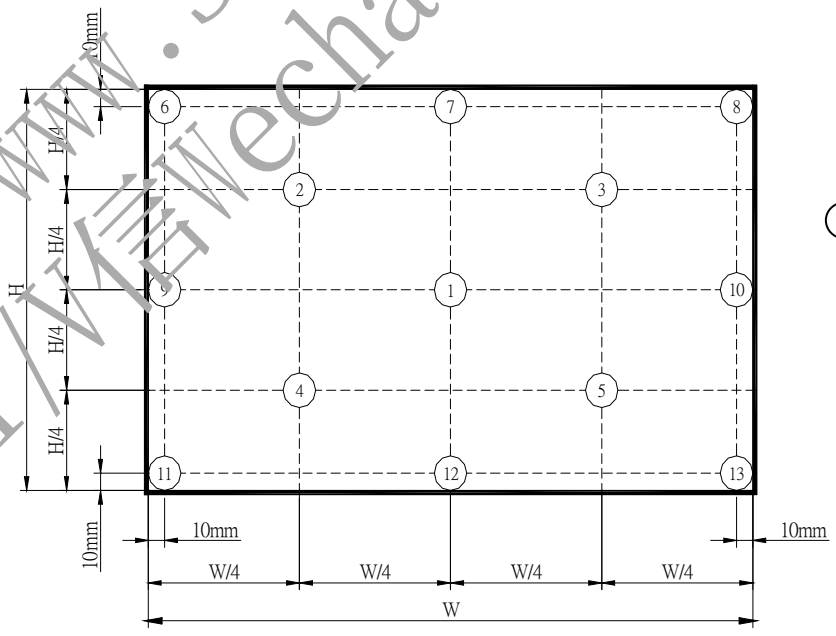


Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

δW_{5p} = Maximum [L(1) ～ L(5)] / Minimum [L(1) ～ L(5)]

δW_{13p} = Maximum [L(1) ～ L(13)] / Minimum [L(1) ～ L(13)]



Ⓧ : Test Point

X=1 to 13

Active area

Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

Note (8) Definition of Low Blue Light (LBL)

Measure the luminance of gray level 255 at center points

$$Blue\ Light\ Ratio(BLR) = \left[\frac{\text{Range (415~455 nm)}}{\text{Range (400~500 nm)}}\right] \text{x } 100\%$$

Range (415~455 nm): Light intensity between 415 nm and 455 nm

Range (400~500 nm): Light intensity between 400 nm and 500 nm

LBL = LBL (1)

LBL (X) is corresponding to the Low Blue Light of the point X at Figure in Note (6)

6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60ºC, 240 hours	(1) (2)
Low Temperature Storage Test	-20ºC, 240 hours	
Thermal Shock Storage Test	-20ºC, 0.5hour←→60℃, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	50ºC, 240 hours	
Low Temperature Operation Test	0ºC, 240 hours	
High Temperature & High Humidity Operation Test	50ºC, RH 80%, 240hours	
ESD Test (Operation)	150pF, 330Ω, 1sec/cycle Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±15KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave,1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect.

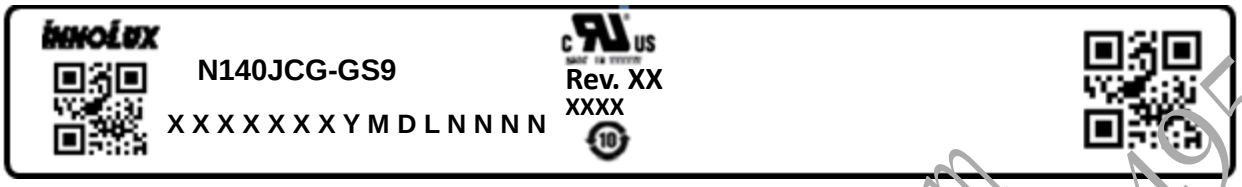
Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

7. PACKING

7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: N140JCG-GS9

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X X X X X X Y M D L N N N N

- Serial No.
- Product Line
- Year, Month, Date
- CMI Internal Use
- Revision
- CMI Internal Use

(d) Production Location: MADE IN XXXX.

(e) UL Logo: XXXX is UL factory ID.

(f) X: A means A Born, B means B Born etc.,

Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2010~2019

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

7.2 CARTON

(1)Box Dimensions : 435(L)*350(W)*320(H)
(2)20 Module/Carton

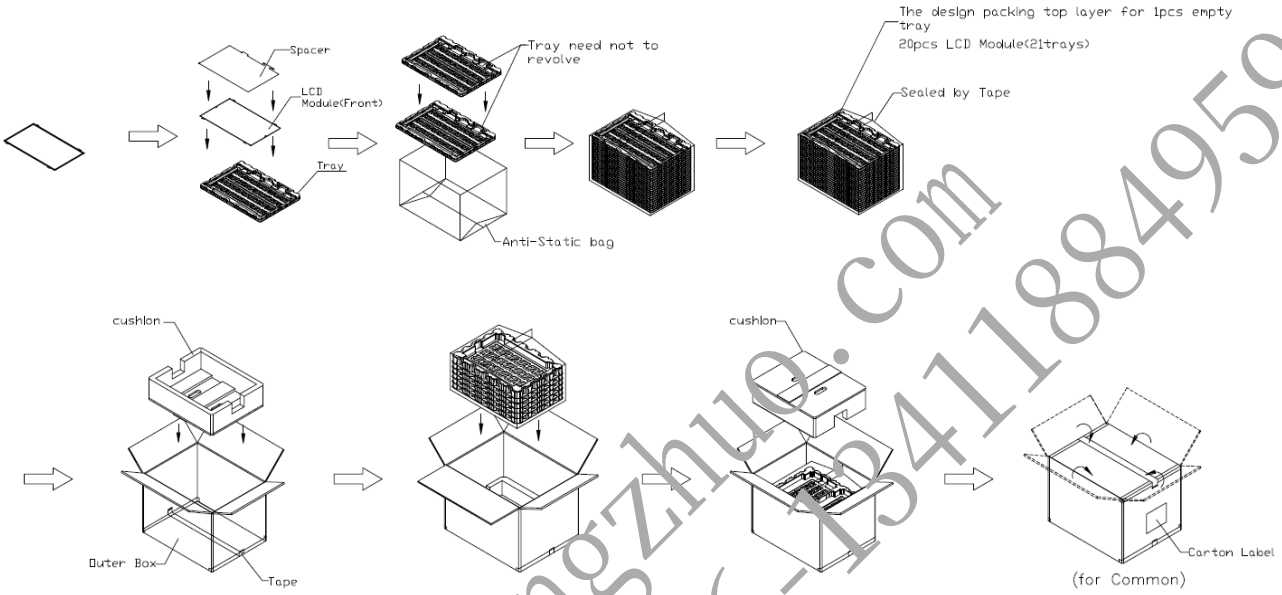


Figure 7-2 Packing method

7.3 PALLET

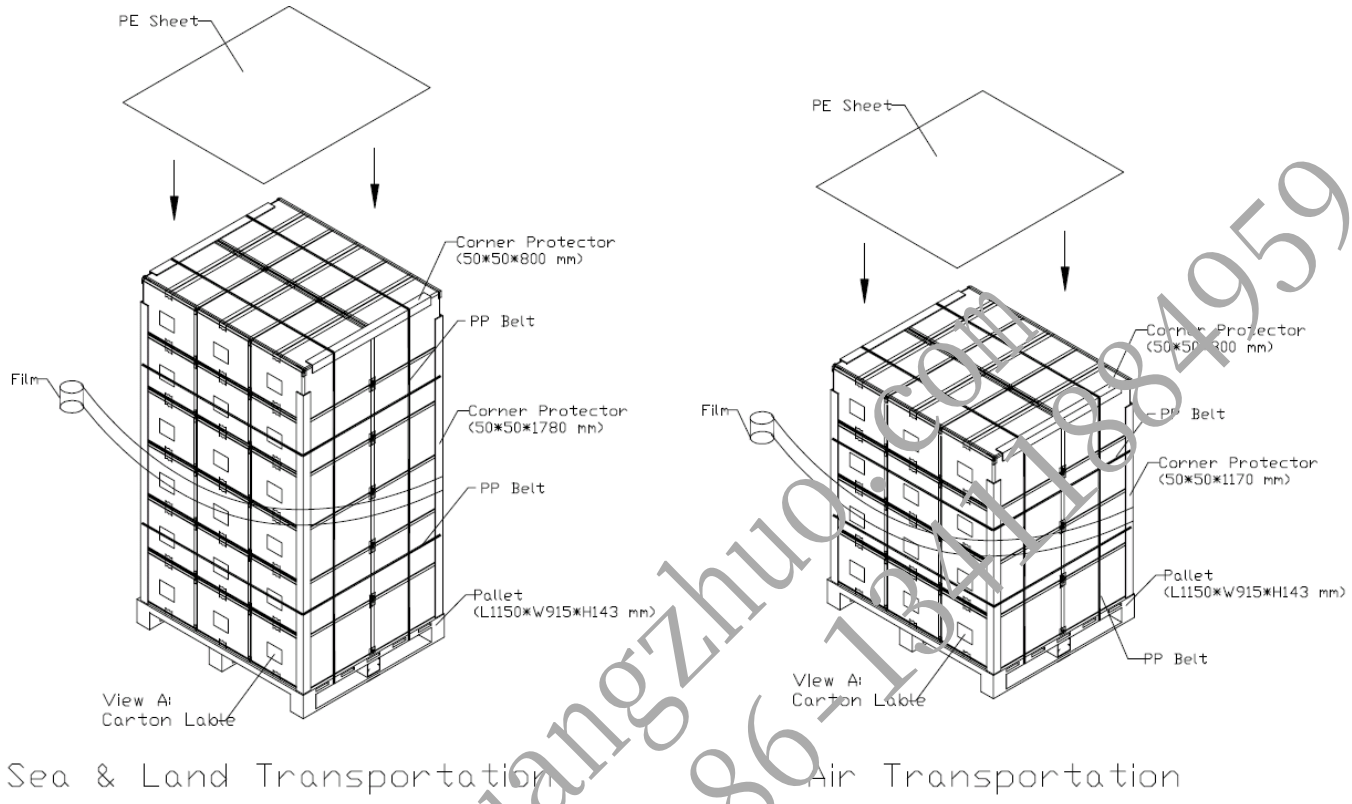
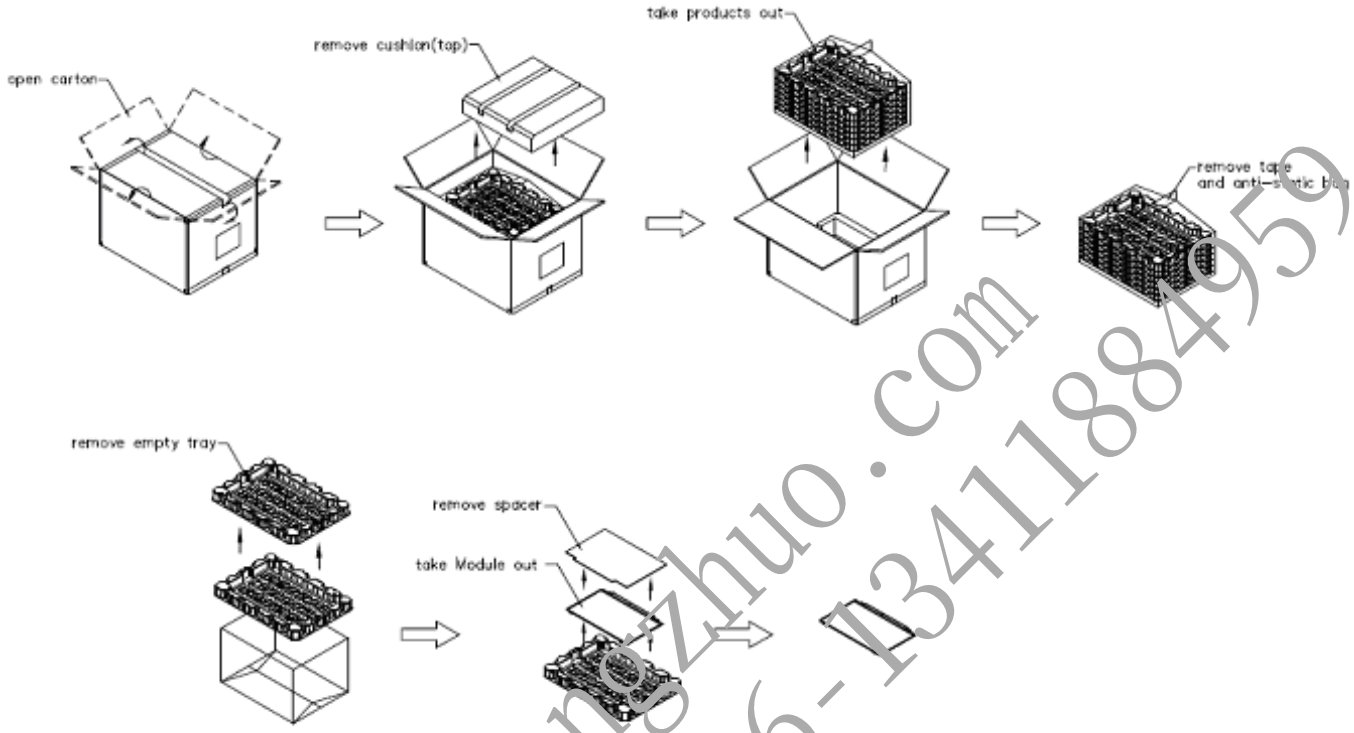


Figure. 7-3 Packing method

7.4 UN-PACK METHOD



8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMIS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

Appendix. EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	00	Header	00	00000000
1	01	Header	FF	11111111
2	02	Header	FF	11111111
3	03	Header	FF	11111111
4	04	Header	FF	11111111
5	05	Header	FF	11111111
6	06	Header	FF	11111111
7	07	Header	00	00000000
8	08	EISA ID manufacturer name ("CMN")	0D	00001101
9	09	EISA ID manufacturer name	AE	10101110
10	0A	ID product code (LSB)	35	00110101
11	0B	ID product code (MSB)	14	00010100
12	0C	ID S/N (fixed "0")	00	00000000
13	0D	ID S/N (fixed "0")	00	00000000
14	0E	ID S/N (fixed "0")	00	00000000
15	0F	ID S/N (fixed "0")	00	00000000
16	10	Week of manufacture (fixed week code)	0D	00001101
17	11	Year of manufacture (fixed year code)	1F	00011111
18	12	EDID structure version ("1")	01	00000001
19	13	EDID revision ("4")	04	00000100
20	14	Video I/P definition ("Digital")	A5	10100101
21	15	Active area horizontal ("30.159cm")	1E	00011110
22	16	Active area vertical ("18.85cm")	13	00010011
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("RGB, Continous")	03	00000011
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	EE	11101110
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	95	10010101
27	1B	Rx=0.640	A3	10100011
28	1C	Ry=0.330	54	01010100
29	1D	Gx=0.300	4C	01001100
30	1E	Gy=0.600	99	10011001
31	1F	Bx=0.150	26	00100110
32	20	By=0.060	0F	00001111
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer's reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

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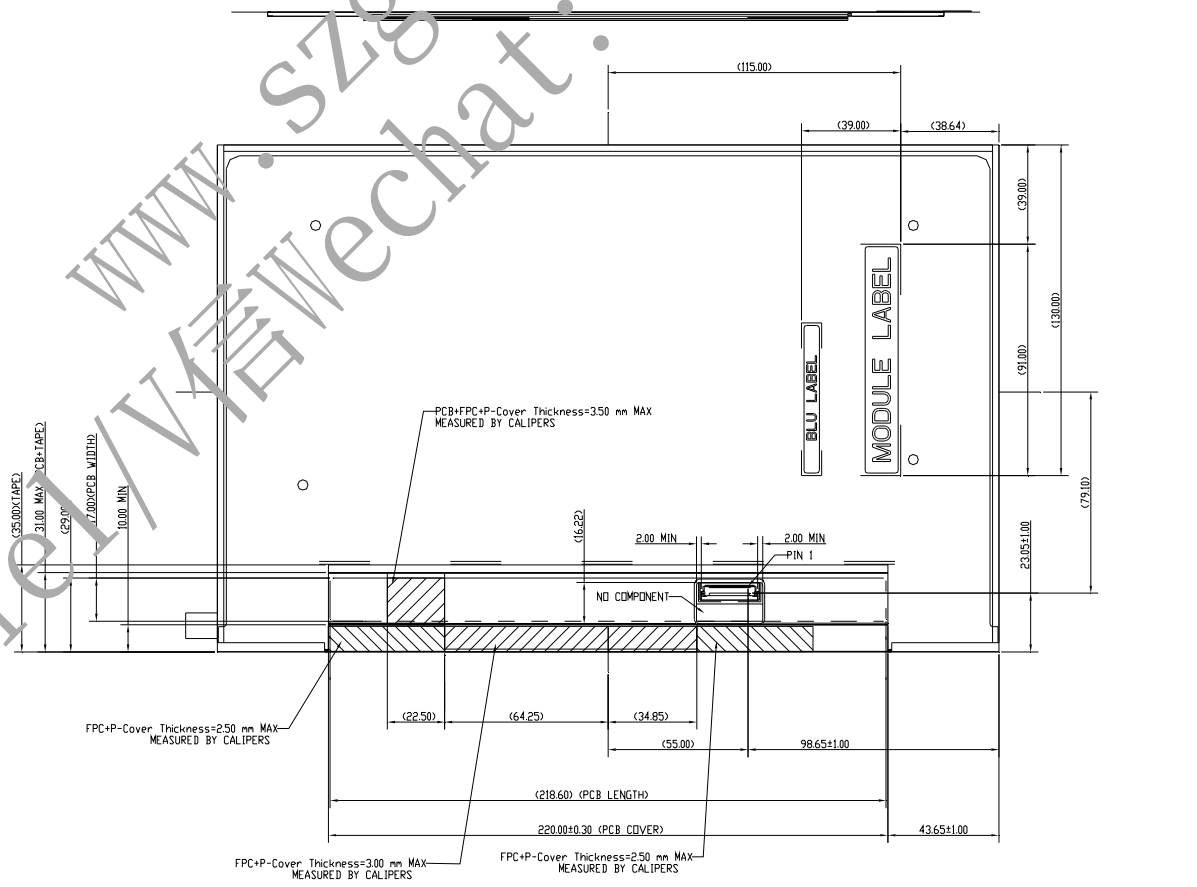
Byte # (decimal)				
	2A	Standard timing ID # 3	01	00000001
42	2B	Standard timing ID # 3	01	00000001
43	2C	Standard timing ID # 4	01	00000001
44	2D	Standard timing ID # 4	01	00000001
45	2E	Standard timing ID # 5	01	00000001
46	2F	Standard timing ID # 5	01	00000001
47	30	Standard timing ID # 6	01	00000001
48	31	Standard timing ID # 6	01	00000001
49	32	Standard timing ID # 7	01	00000001
50	33	Standard timing ID # 7	01	00000001
51	34	Standard timing ID # 8	01	00000001
52	35	Standard timing ID # 8	01	00000001
53	36	Detailed timing description # 1 Pixel clock ("154.26"MHz, According to VESA CVT Rev1.4)	42	01000010
54	37	# 1 Pixel clock (hex LSB first)	3C	00111100
55	38	# 1 H active ("1920")	80	10000000
56	39	# 1 H blank ("160")	A0	10100000
57	3A	# 1 H active : H blank ("1920 : 160")	70	01110000
58	3B	# 1 V active ("1200")	B0	10110000
59	3C	# 1 V blank ("36")	24	00100100
60	3D	# 1 V active : V blank ("1200 : 36")	40	01000000
61	3E	# 1 H sync offset ("46")	2E	00101110
62	3F	# 1 H sync pulse width ("30")	1E	00011110
63	40	# 1 V sync offset : V sync pulse width ("10 : 6")	A6	10100110
64	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width ("46 : 30 : 10 :6")	00	00000000
65	42	# 1 H image size ("301 mm")	2D	00101101
66	43	# 1 V image size ("188 mm")	BC	10111100
67	44	# 1 H image size : V image size	10	00010000
68	45	# 1 H boarder ("0")	00	00000000
69	46	# 1 V boarder ("0")	00	00000000
70	47	Non-interlaced, Normal Display, Digital separate, Positive Hsync, Negative Vsync	1A	00011010
71	48	Detailed timing description # 2 Pixel clock ("102.88"MHz, According to VESA CVT Rev1.4)	30	00110000
72	49	# 2 Pixel clock (hex LSB first)	28	00101000
73	4A	# 2 H active ("1920")	80	10000000
74	4B	# 2 H blank ("160")	A0	10100000
75	4C	# 2 H active : H blank ("1920 : 160")	70	01110000
76	4D	# 2 V active ("1200")	B0	10110000
77	4E	# 2 V blank ("36")	24	00100100
78	4F	# 2 V active : V blank ("1200 : 36")	40	01000000
79	50	# 2 H sync offset ("46")	2E	00101110
80	51	# 2 H sync pulse width ("30")	1E	00011110
81	52	# 2 V sync offset : V sync pulse width ("10 : 6")	A6	10100110
82	53	# 2 H sync offset : H sync pulse width : V sync offset : V sync width ("46 : 30 : 10 :6")	00	00000000

83	54	# 2 H image size (“301 mm“)	2D	00101101
84	55	# 2 V image size (“188 mm“)	BC	10111100
85	56	# 2 H image size : V image size	10	00010000
Byte #(decimal)	57	# 2 H boarder ("0")	00	00000000
86	58	# 2 V boarder ("0")	00	00000000
87	59	Non-interlaced, Normal Display, Digital separate, Positive Hsync, Negative Vsync	1A	00011010
88	5A	NA	00	00000000
89	5B	NA	00	00000000
90	5C	NA	00	00000000
91	5D	NA	00	00000000
92	5E	NA	00	00000000
93	5F	NA	00	00000000
94	60	NA	00	00000000
95	61	NA	00	00000000
96	62	NA	00	00000000
97	63	NA	00	00000000
98	64	NA	00	00000000
99	65	NA	00	00000000
100	66	NA	00	00000000
101	67	NA	00	00000000
102	68	NA	00	00000000
103	69	NA	00	00000000
104	6A	NA	00	00000000
105	6B	NA	00	00000000
106	6C	Detailed Timing Description #1	00	00000000
107	6D	Flags	00	00000000
108	6E	Reserved	00	00000000
109	6F	For Brightness Table and Power Consumption	02	00000010
110	70	Flags	00	00000000
111	71	PWM % [7:0] @ Step 0 = 5%	0C	00001100
112	72	PWM % [7:0] @ Step 5 = 15%	26	00100110
113	73	PWM % [7:0] @ Step 10 = 100%	FF	11111111
114	74	Nits [7:0] @ Step 0 = 20nits	14	00010100
115	75	Nits [7:0] @ Step 5 = 60nits	3C	00111100
116	76	Nits [7:0] @ Step 10 = 400nits	C8	11001000
117	77	Panel Electronics Power @32x32 Chess Pattern =460mW	0B	00001011
118	78	Backlight Power @60 nits =321mW	08	00001000
119	79	Backlight Power @Step 10 =2137mW	1A	00011010
120	7A	Nits @ 100% PWM Duty =400nit	C8	11001000
121	7B	Flags	00	00000000
122	7C	Flags	00	00000000
123	7D	Flags	00	00000000
124	7E	Extension flag	00	00000000
125	7F	Checksum	D0	11010000

Appendix. OUTLINE DRAWING



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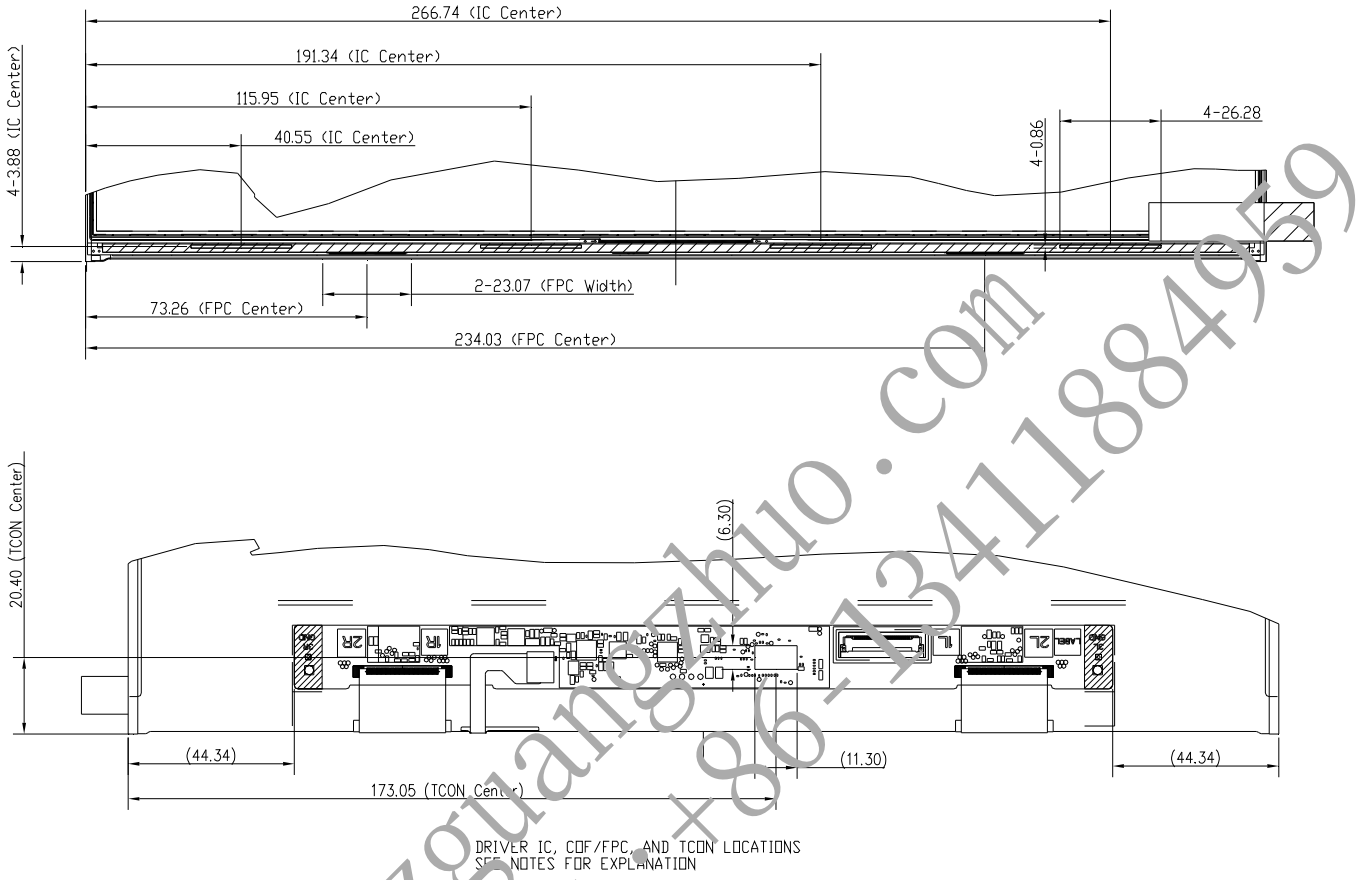
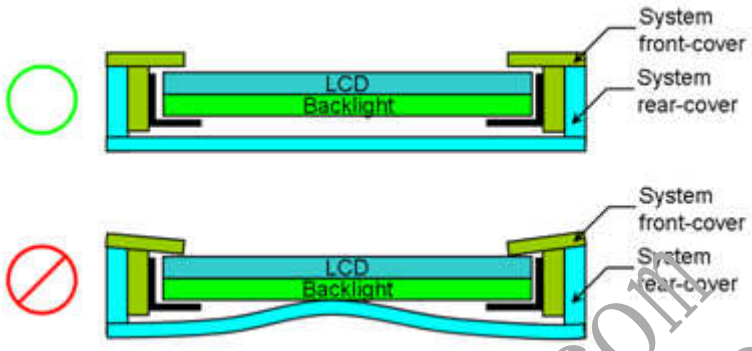
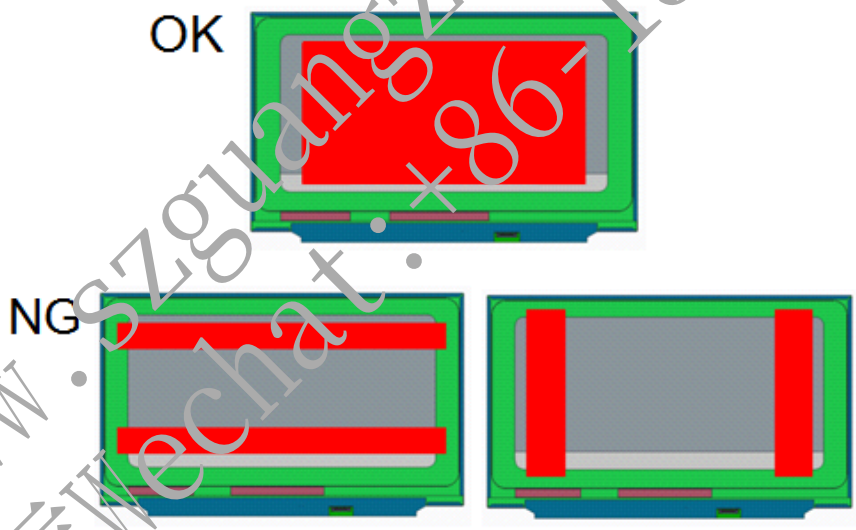
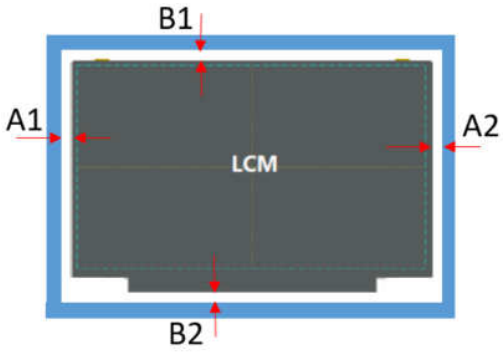


Note. Dimensions measuring instruments as below,

1. Length/ Width/Thickness : Caliper
2. Height : Height gauge

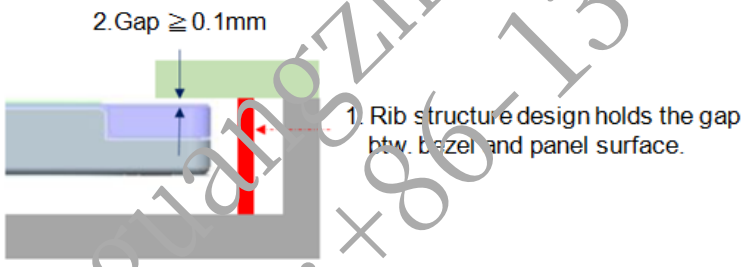
Appendix. SYSTEM COVER DESIGN GUIDANCE

0.	**Permanent deformation of system cover after reliability test**
	
Definition	System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
1	**Sponge area design behind panel**
	
Definition	Sponge area design behind panel can not be across the panel metal rear and the reflector at the same time. It can be on the reflector area only.
2	**Gap between system rear-cover & panel**
	
Definition	The maximum thickness of sponge on the system rear-cover can not interfere to the maximum thickness of panel. Because the interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
3	**Gap Design between panel & around structure**

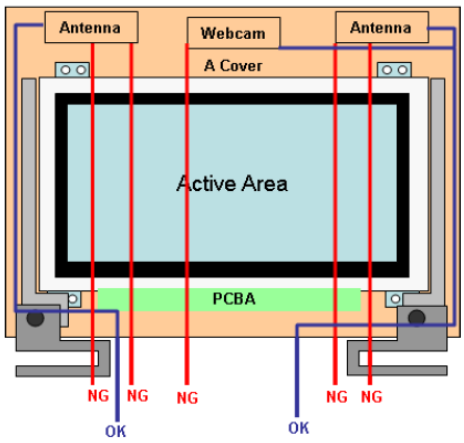


Item	Suggestion	Remark
A1	A1≧0.5	Gap≧ Panel outline max. tolerance + Assembly max. tolerance
A2	A2≧0.5	
B1	B1≧0.5	
B2	B2≧0.8	

Definition	Gap Design between panel & around structure needs to consider the maximum tolerances of panel outline and assembly at the same time. Gap Design suggestion is shown as A1/A2/B1/B2 on the chart.
4	**Gap between panel & bezel**

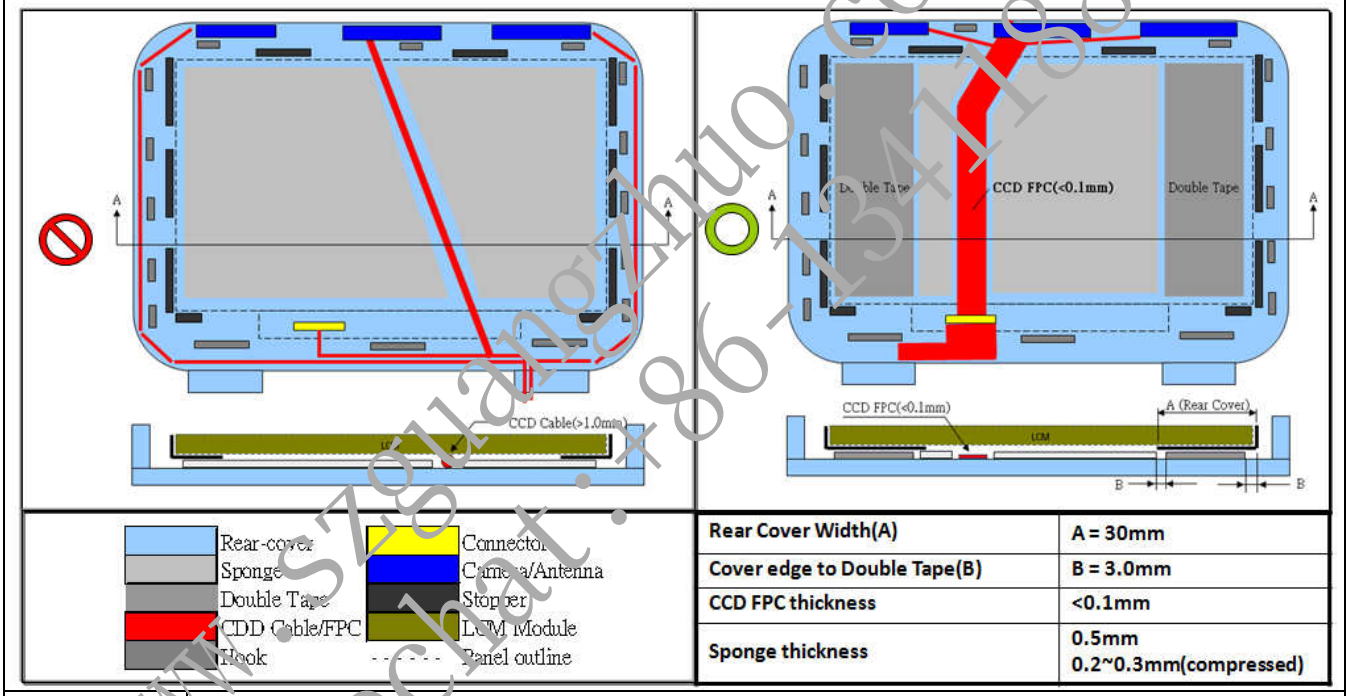


Definition	The gap between system bezel & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system front-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test, or during pooling inspection procedure. To remain the sufficient gap, design with system rib higher than maximum panel thickness is recommended. The sufficient gap design is greater or equal to 0.1mm.
5	**Cable routing behind panel**



Definition	It is strongly recommended that cables route around the panel outline, not overlap with the panel outline (including PCB). Because issue such as abnormal display & white spot after backpack test, hinge test, twist test or pogo test may occur. If any routings across panel outline are needed, we suggest design as below: -Using FFC/FPC to replace cables. -Routing at the right or left area of panel metal rear. -Avoid any routings at the step of panel or A cover. -No interference to panel. -It should not overlap TCON, COF/FPC, Driver IC
6	**Interference examination of antenna cable and Web Cam wire**

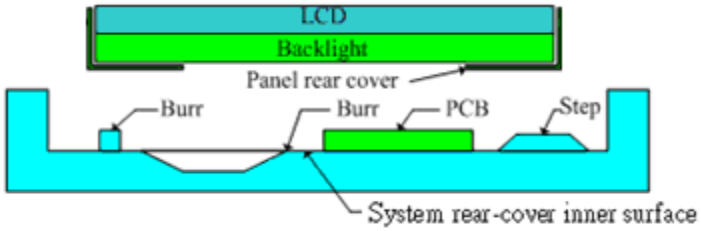
- To prevent panel damage, we suggest using CCD FPC to replace CCD cable
- Using double tape to fix LCM module for no bracket design.



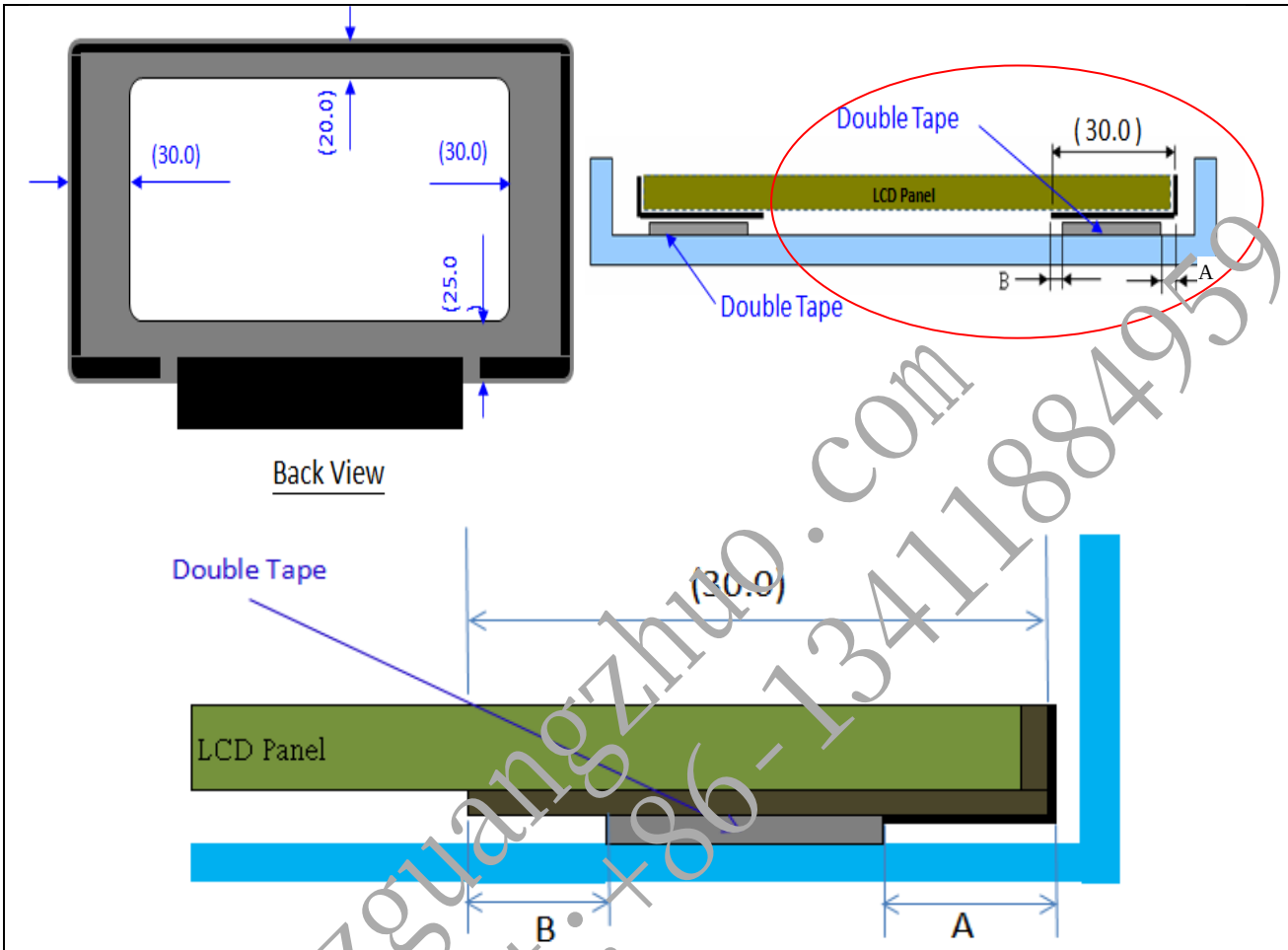
Rear Cover Width(A)	**A = 30mm**
Cover edge to Double Tape(B)	**B = 3.0mm**
CCD FPC thickness	**<0.1mm**
Sponge thickness	**0.5mm 0.2~0.3mm(compressed)**

If the antenna cable or Web Cam wire must overlap with the panel outline, both sides of the antenna cable or Web Cam wire must have a sponge(Sponge material can not contain NH3) and sponge require higher antenna cable or Web Cam wire.(Antenna cable or Web Cam wire should not overlap with TCON,COF/FPC,Driver IC)
Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.

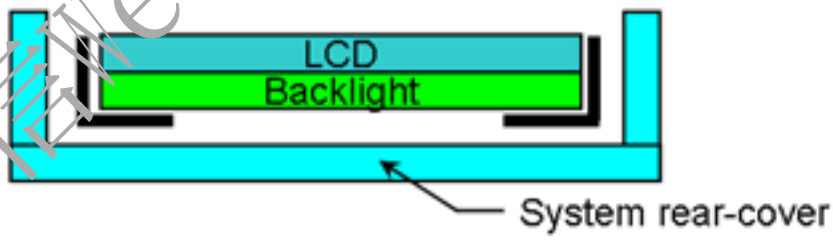
7	**System rear-cover inner surface examination**



Definition	Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.
8	**Tape/sponge design on system inner surface**



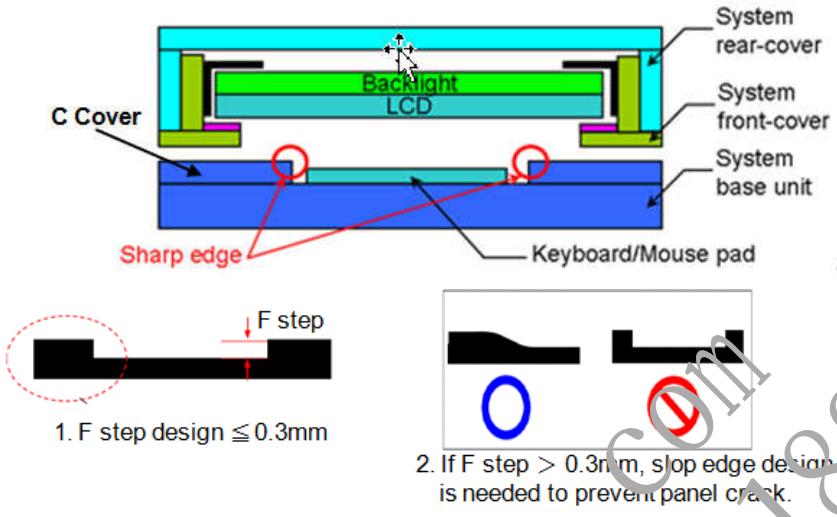
Definition	To prevent peeling the bezel tape in rework process. The length of double tape is 30 – (A+B), A is bezel tape length and B is the double tape attaching tolerance. Ex :A :2mm, B:2mm, the length of double tape is 30-(2+2)=26mm.
9	**Material used for system rear-cover**



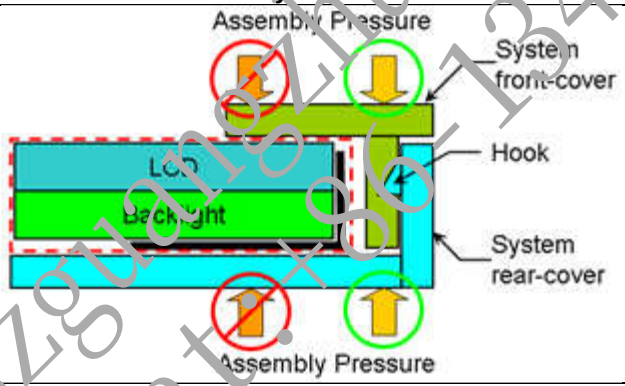
System rear-cover material: Al-Mg alloy

System rear-cover thickness:1.5mm MIN

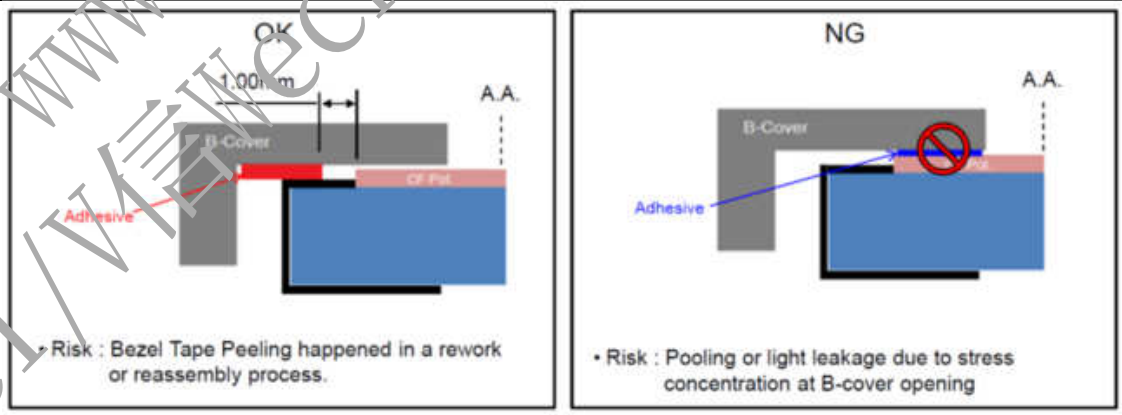
Definition	System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.
10	**C cover shape design**



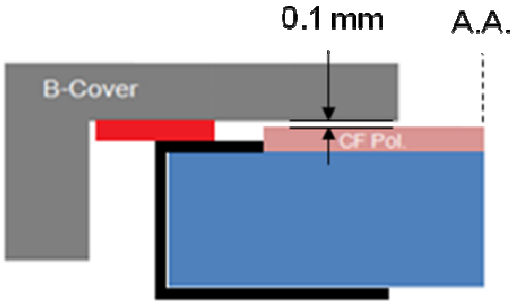
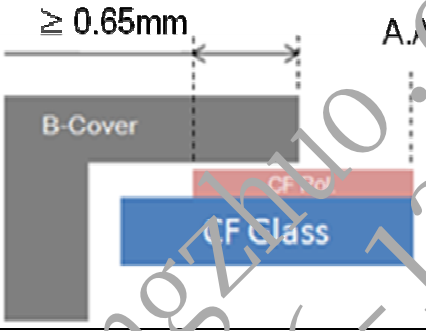
Definition	The F step design on C Cover less than or equal to 0.3mm is recommended. If F step exceeds 0.3mm, the slop edge design is necessary to prevent panel crack.
11	**Assembly SOP examination for system front-cover with Hook design**



Definition	To prevent panel crack during system front-cover assembly process with hook design, it is not recommended to press panel or any location that related directly to the panel.
12	**Adhesive design between panel & bezel**



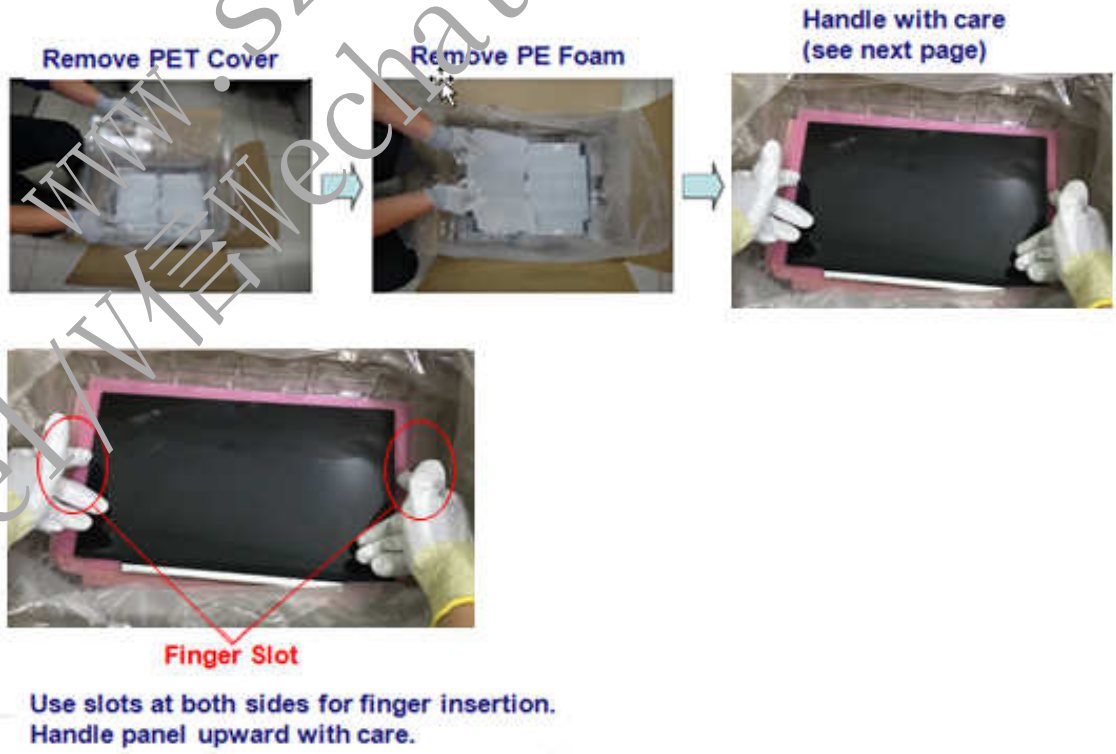
Definition	To prevent panel crack during system front-cover assembly process with double tape design, When system applied adhesive between B-Cover and LCD module, please design a distance 1.00mm between B-Cover's adhesive and CF pol. Do **NOT** put adhesive on CF pol. Adhesive material need be qualified to prevent from doing damage to cell tape after rework. Adhesive material need be qualified to prevent abnormal noise when hinge swinging test.
13	**System front-cover assembly reference with Double tape design**

	
Definition	To prevent system front-cover peeling at double tape contact area, A gap between B-Cover & CF-Pol. Is 0.1mm min.
14	System front-cover opening area reference with TFT-LCD module
	
Definition	To prevent panel the noise of B cover & CF Pol. Distance from CF Pol. edge to front-cover edge more than 0.65mm.

Appendix. LCD MODULE HANDLING MANUAL

Purpose	• **This SOP is prepared to prevent panel dysfunction possibility through incorrect handling procedure.** • **This manual provides guide in unpacking and handling steps.** • **Any person which may contact / related with panel, should follow guide stated in this manual to prevent panel loss.**
1.	**Unpacking**

2.	**Panel Lifting**



3.	Do and Don't

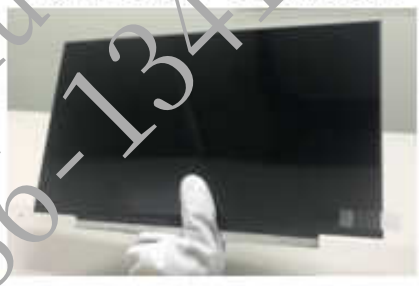
Do :

- Handle with both hands.
- Handle panel at left and right edge.

Don't :

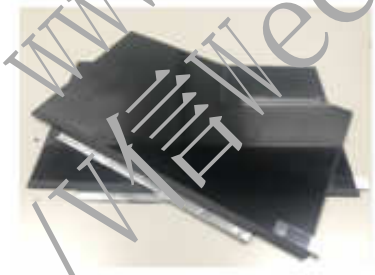
- Lifting with one hand.

- Handle at PCBA side.



Don't :

- Stack panels.



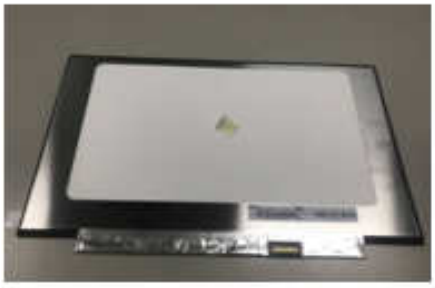
- Press panel.

Don't :

- Put foreign stuff onto panel

- Put foreign stuff under panel

Don't :
- Paste any material unto white reflector sheet



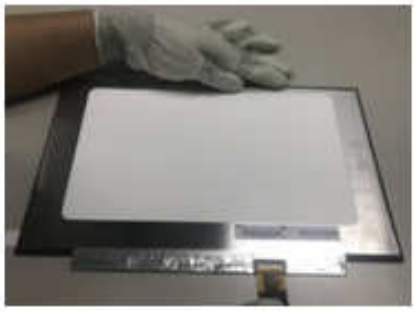
Don't :
- Pull / Push white reflector sheet

Don't :
- Hold at panel corner.

Don't :
- Twist panel.

Do :

- Hold panel at top edge while inserting connector.



Don't :

- Press white reflector sheet while inserting connector.

Do :

- Remove panel protector film starts from pull tape

Don't :

- Remove panel protector film From film another side.

Do:
- Remove panel protector film starts from Lower-right corner to Top-left

Don't:
- Remove panel protector Film parallel X-direction

Don't :
- Touch or Press PCBA Area.