

PRODUCT SPECIFICATION

- ☐ Tentative Specification
☐ Preliminary Specification
☒ Approval Specification

MODEL NO.: N140JCA
SUFFIX: ELK Rev.C2

Customer: Common

APPROVED BY SIGNATURE

Name / Title

Note

Please return 1 copy for your confirmation with your signature and comments.

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PRODUCT SPECIFICATION

CONTENTS

REVISION HISTORY	1. GENERAL DESCRIPTION	3
1. GENERAL DESCRIPTION		4
1.1 OVERVIEW		4
1.2 GENERAL SPECIFICATIONS		4
2. MECHANICAL SPECIFICATIONS		5
2.1 CONNECTOR TYPE		5
3. ABSOLUTE MAXIMUM RATINGS		6
3.1 ABSOLUTE RATINGS OF ENVIRONMENT		6
Operating Range		6
3.2 ELECTRICAL ABSOLUTE RATINGS		7
3.2.1 TFT LCD MODULE		7
4. ELECTRICAL SPECIFICATIONS		7
4.1 FUNCTION BLOCK DIAGRAM		7
4.2. INTERFACE CONNECTIONS		8
4.3 ELECTRICAL CHARACTERISTICS		10
4.3.1 LCD ELETRONICS SPECIFICATION		10
4.3.2 LED CONVERTER SPECIFICATION		12
4.3.3 BACKLIGHT UNIT		14
4.4 DISPLAY PORT SIGNAL TIMING SPECIFICATION		15
4.4.1 DISPLAY PORT INTERFACE		15
4.5 DISPLAY TIMING SPECIFICATIONS		16
4.6 POWER ON/OFF SEQUENCE		17
4.7 MOMENTARY VOLTAGE DROIS		19
5. OPTICAL CHARACTERISTICS		20
5.1 TEST CONDITIONS		20
5.2 OPTICAL SPECIFICATIONS		20
6. RELIABILITY TEST ITEM		24
7. PACKING		25
7.1 MODULE LABEL		25
7.2 CARTON		26
8. PRECAUTIONS		28
8.1 HANDLING PRECAUTIONS		28
8.2 STORAGE PRECAUTIONS		28
8.3 OPERATION PRECAUTIONS		28
Appendix. EDID DATA STRUCTURE		29
Appendix. LCD MODULE HANDLING MANUAL		46



PRODUCT SPECIFICATION

REVISION HISTORY

Version	Date	Page	Description
1.0	Dec. 8, 2021	ALL	Spec Ver.1.0 was first issued.
2.0	Dec. 23, 2021	ALL	Spec Ver.2.0 was first issued.
3.0	Jan. 05, 2022	ALL	Spec Ver.3.0 was first issued.
3.1	Feb. 10, 2022	36	Modify outline drawing

PRODUCT SPECIFICATION

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N140JCA-ELK is a 14.0" (14.0" diagonal) TFT Liquid Crystal Display NB module with LED Backlight unit and 30 pins eDP interface. This module supports 1920 x 1200 WUXGA AAS mode and can display 16,777,216 colors.

1.2 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Screen Size	14.0" diagonal	inch	-
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1200	pixel	-
Pixel Pitch	0.157 (H) x 0.157 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	Color	-
Color depth	6bit +FRC	-	-
Transmissive Mode	Normally Black	-	-
Surface Treatment	Hard coating (3H), Anti-Glare	-	-
Luminance, White	300	Cd/m2	-
Color Gamut	45%	NTSC	-
Response Time	Typ:Tr 5 / Tf 4	ms	-
Contrast Ratio	Typ:1000/Min:300	-	-
Border size(L/R/U)	2.85/2.85/2.85	mm	-
View Angle(U/D/R/L)	89/89/89/89	Deg	-
Backlight Unit	LEDs 3 strings x 6 parallel	-	-
Electrical Interface	eDP 1.2	-	(2)
RoHs Compliance	Yes	-	-
Power Consumption	Total 3.95 (max.) @ cell 0.63W (max.), BL 3.32 W (max.)	-	(1)
Special Function	Item	Support	Note
	G-sync DG	N	-
	G-sync VSR	N	-
	Free sync	Y	-
	Static DRRS	N	-
	Seamless DRRS(sDRRS)	N	-
	PSR Version(PSR1)	N	-
	PSR 1+ sDRRS	N	-
	PSR 2+ LRR	N	-
	CABC	N	-

Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, fv = 60 Hz, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 °C, whereas **Mosaic** pattern is displayed.

Note (2) Display port interface signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2 (eDP1.2). There are many optional items described in eDP1.2. If some optional item is requested, please contact us.

PRODUCT SPECIFICATION

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	306.99	307.29	307.59	mm	(1)(2)(3)
	Vertical (V)	197.85	198.15	198.45	mm	
	Thickness (T)	-	2.85	3.0	mm	
Active Area	Horizontal	301.49	301.59	301.69	mm	
	Vertical	188.40	188.50	188.60	mm	
Weight		-	277	290	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions

Note (2) Dimensions are measured by caliper

Note (3) Panel thickness is measured with calipers clamping mylar or tape tightly



2.1 CONNECTOR TYPE

Please refer Appendix Outline Drawing for detail design.

Connector Part No.: 1st IPEX-20455-030E-12, 2nd JAE-HD2S030HA3

or follow customer approval connector vendor list

User's connector Part No: IPEX-20452-040T-03

Customer approval connector vendor list

Item	Description				
Item	Pin 數	Pitch	廠商	廠商料號	
LCD Panel Connector Pool	1	40	I-PEX	20455-040E-02/12	
				20455-040E-76/66	
				20765-040E-11	
			Starconn	111A40-0000RA-G3	
			STM	MSAK 240 25P40	
			Tyco	5-2069716-3	
			LSMtrom	GT05Q-40S-10H	
			Foxconn	GS13401-1S10S-7H	
			JAE	HD1S040HA1	
				HD1S040HA2	
				HD1S040HA3	
	2	30	UJU	ISC05-L40B-C10	
			MOLEX	MOLEX-104062-4011	
			I-PEX	20455-030E-02/12	
				20455-030E-76/66	
				20765-030E-11	
	3	40	Starconn	300E30-0010RA-G3	
			JAE	HD2S030HA1	
				HD2S030HA2	
				HD2S030HA3	
			LSMtrom	GT05Q-30S-H10-MN	
			STM	MSAK 240 25P30	
			UJU	ISC05-L30B-C10	
			I-PEX	20682-040E-02	

PRODUCT SPECIFICATION

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

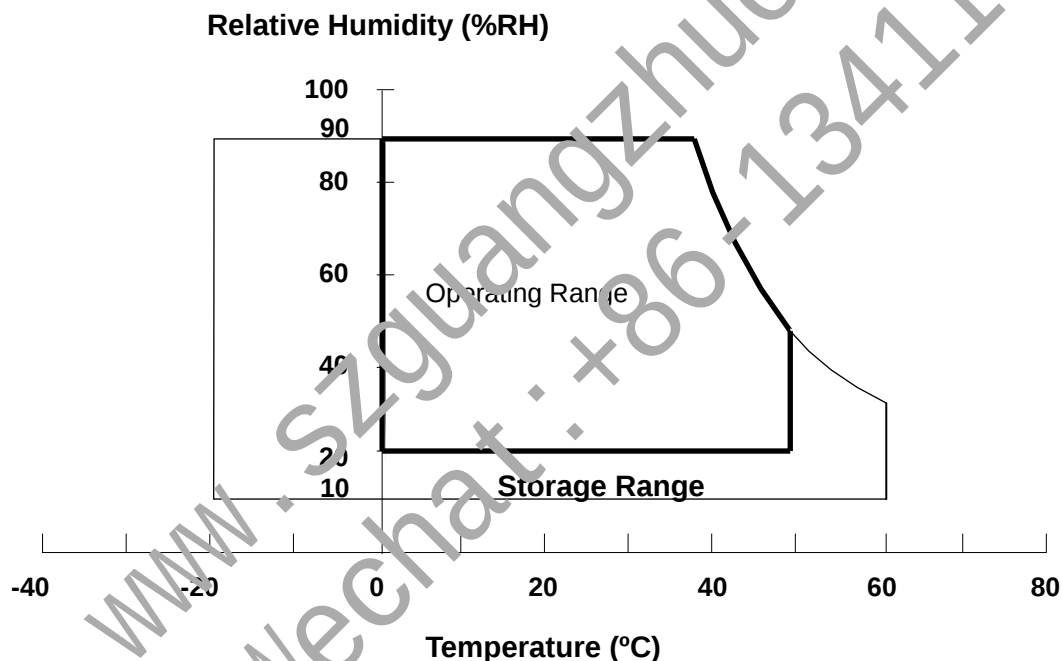
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (2)
Shock (Non-Operating)	S _{NOP}	--	220/2	G/ms	(3),(4),(5)
Vibration (Non-Operating)	V _{NOP}	--	1.5	G	(3),(4),(6)

Note (1) (a) 90 %RH Max. (Ta < 40 °C).

(b) Wet-bulb temperature should be 39 °C Max.

(c) No condensation.

Note (2) The temperature of panel surface should be 0 °C min. and 60 °C max.



Note (3) criteria: Normal display image with no obvious non-uniformity and no line defect.

Note (4) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

Note (5) half sine wave, 1 time for each direction of $\pm X, \pm Y, \pm Z$

Note (6) 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z

PRODUCT SPECIFICATION

3.2 ELECTRICAL ABSOLUTE RATINGS

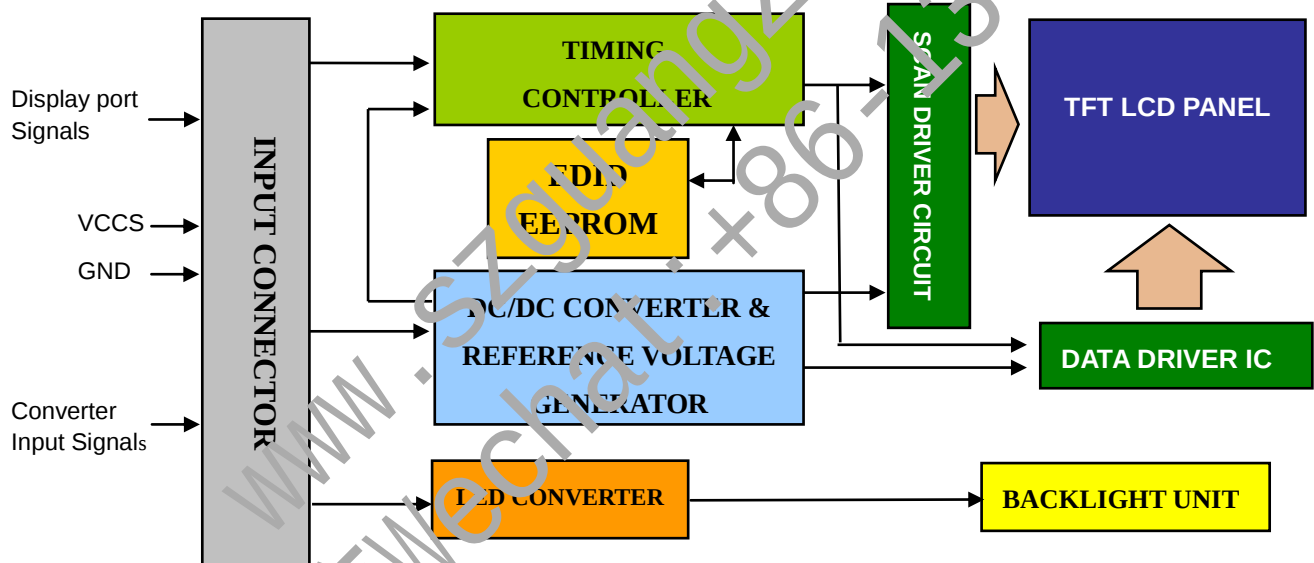
3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V _{IN}	-0.3	+4.0	V	
Converter Input Voltage	LED_VCCS	-0.3	26	V	(1)
Converter Control Signal Voltage	LED_PWM,	-0.3	5	V	(1)
Converter Control Signal Voltage	LED_EN	-0.3	5	V	(1)

Note (1) Stresses beyond those listed in above "ELECTRICAL ABSOLUTE RATINGS" may cause permanent damage to the device. Normal operation should be restricted to the conditions described in "ELECTRICAL CHARACTERISTICS".

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



PRODUCT SPECIFICATION

4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserved for LCD test)	
2	H_GND	High Speed Ground	
3	Lane1_N	Complement Signal Link Lane 1	
4	Lane1_P	True Signal Link Lane 1	
5	H_GND	High Speed Ground	
6	Lane0_N	Complement Signal Link Lane 0	
7	Lane0_P	True Signal Link Lane 0	
8	H_GND	High Speed Ground	
9	AUX_CH_P	True Signal Auxiliary Channel	
10	AUX_CH_N	Complement Signal Auxiliary Channel	
11	H_GND	High Speed Ground	
12	VCCS	LCD logic and driver power	
13	VCCS	LCD logic and driver power	
14	BIST_EN	Panel Built In Self Test Enable	Note (2)
15	GND	LCD logic and driver ground	
16	GND	LCD logic and driver ground	
17	HPD	HPD signal pin	
18	BL_GND	Backlight ground	
19	BL_GND	Backlight ground	
20	BL_GND	Backlight ground	
21	BL_GND	Backlight ground	
22	LED_EN	Backlight on/off	
23	LED_PWM	System PWM signal input for dimming	
24	NC	No Connection (Reserved for LCD test)	
25	NC	No Connection (Reserved for LCD test)	
26	LED_VCCS	Backlight power	
27	LED_VCCS	Backlight power	
28	LED_VCCS	Backlight power	
29	LED_VCCS	Backlight power	
30	NC	No Connection (Reserved for LCD test)	

Note (1) The first pixel is red as shown in the following figure.

PRODUCT SPECIFICATION



PRODUCT SPECIFICATION

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

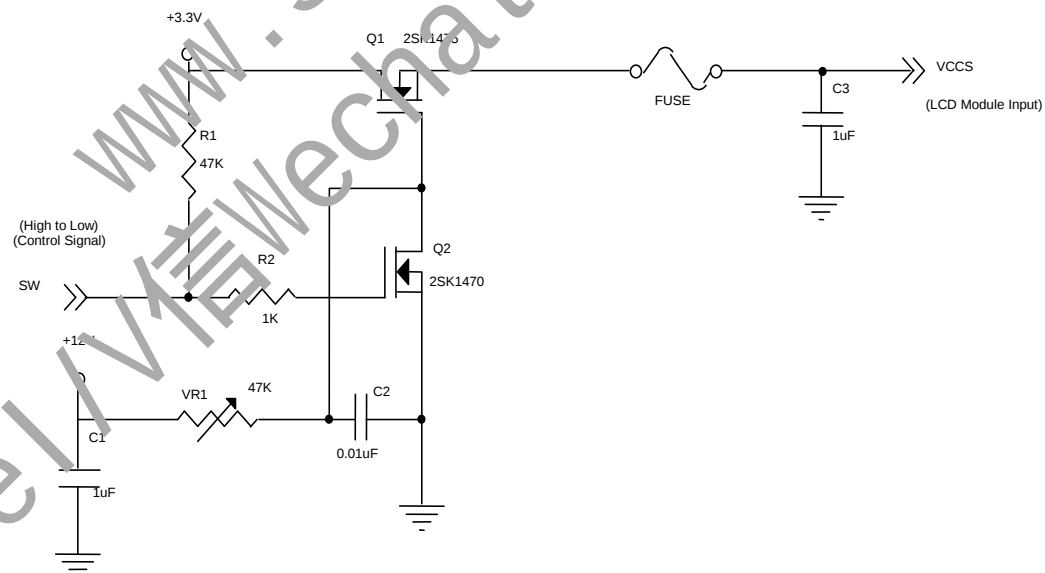
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)
Ripple Voltage		V _{RP}	-	50	-	mV	(1)
Inrush Current		I _{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Mosaic	I _{CC}		147	191	mA	(3)a
	Black			147	191	mA	(3)
	(Solid Pattern)			267	330	mA	(3)
Power Consumption	Mosaic	P _{CC}		0.49	0.62	W	(3)
	Solid Pattern			0.49	0.63	W	(3)
	Heavy Pattern			0.82	0.99	W	(3)
HPD Impedance		R _{HPD}	30K			ohm	(4)
HPD	High Level		2.2V	-	2.7V	V	(5)
	Low Level		0	-	0.4	V	(5)
BIST_EN	High Level		3.0	-	3.6	V	
	Low Level		0		0.6	V	

Note (1) The ambient temperature is $T_a = 25 \pm 2^\circ\text{C}$.

Note (2) I_{RUSH}: the maximum current when VCCS is rising

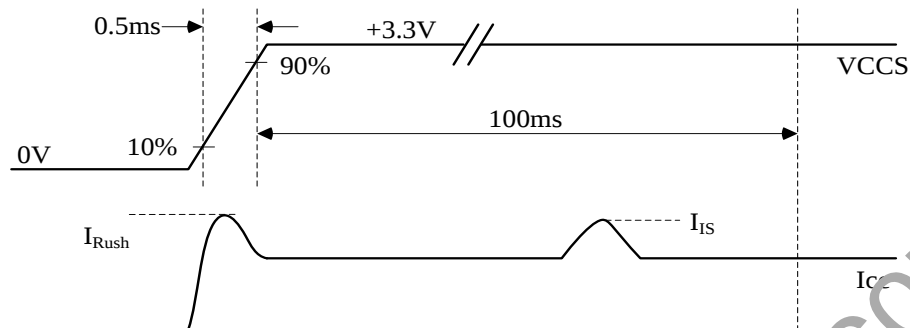
I_S: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.



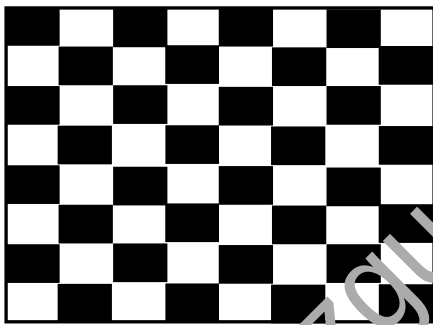
PRODUCT SPECIFICATION

VCCS rising time is 0.5ms



Note (3) The specified power supply current is under the conditions at $V_{CCS} = 3.3\text{ V}$, $T_a = 25 \pm 2^\circ\text{C}$, DC Current and $f_v = 60\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern



Active Area

b. The solid pattern is the largest one of R/G/B pattern.

Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. Please refer to Note (4) of 4.3.2 LED CONVERTER SPECIFICATION to obtain more information.

Note (5) When a source detects a low-going HPD pulse, it must be regarded as a HPD event. Thus, the source must read the link / sink status field or receiver capability field of the DPCD and take corrective action.

PRODUCT SPECIFICATION

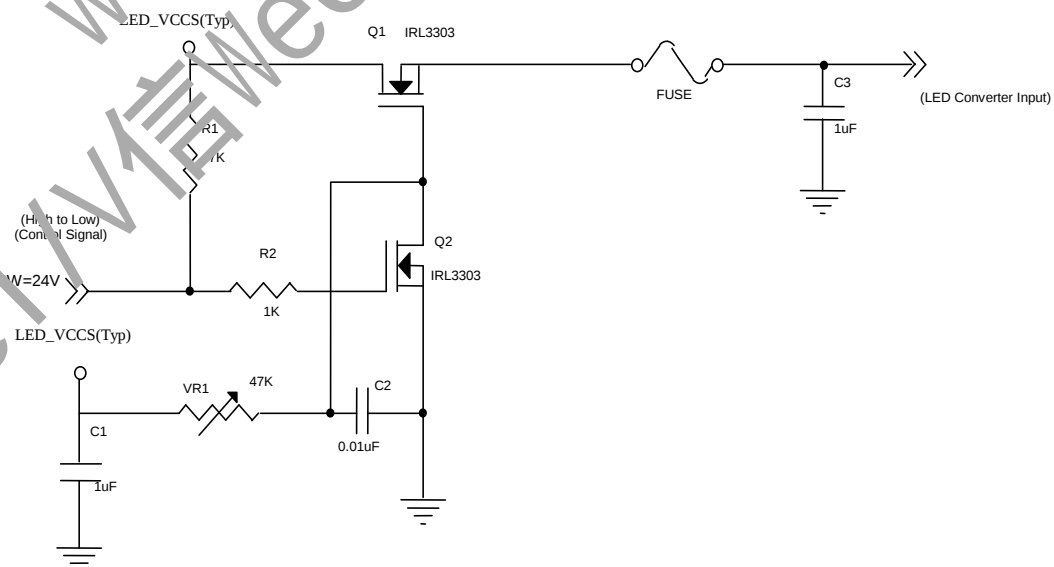
4.3.2 LED CONVERTER SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input Power Supply Voltage		LED_VCCS	5.0	12.0	21.0	V	
Converter Inrush Current		I _{LED_RUSH}	-	-	1.5	A	(1)
LED_EN Control Level	Backlight On		2.2	-	5.0	V	(4)
	Backlight Off		0	-	0.6	V	(4)
LED_EN Impedance		R _{LED_EN}	30K	-	-	ohm	(4)
PWM Control Level	PWM High Level		2.2	-	5	V	(4)
	PWM Low Level		0	-	0.6	V	(4)
PWM Impedance		R _{PWM}	30K	-	-	ohm	(4)
PWM Control Duty Ratio			5	-	100	%	
PWM Control Permissive Ripple Voltage		V _{PWM_pp}	-	-	100	mV	
PWM Control Frequency		f _{PWM}	190	-	2K	Hz	(2)
LED Power Current	LED_VCCS = Typ.	I _{LED}	257	265	277	mA	(3)
LED Power Consumption	LED_VCCS = Typ.	P _{BL}	2.6	3.18	3.32	W	

Note (1) I_{LED_RUSH}: the maximum current when LED_VCCS is rising,

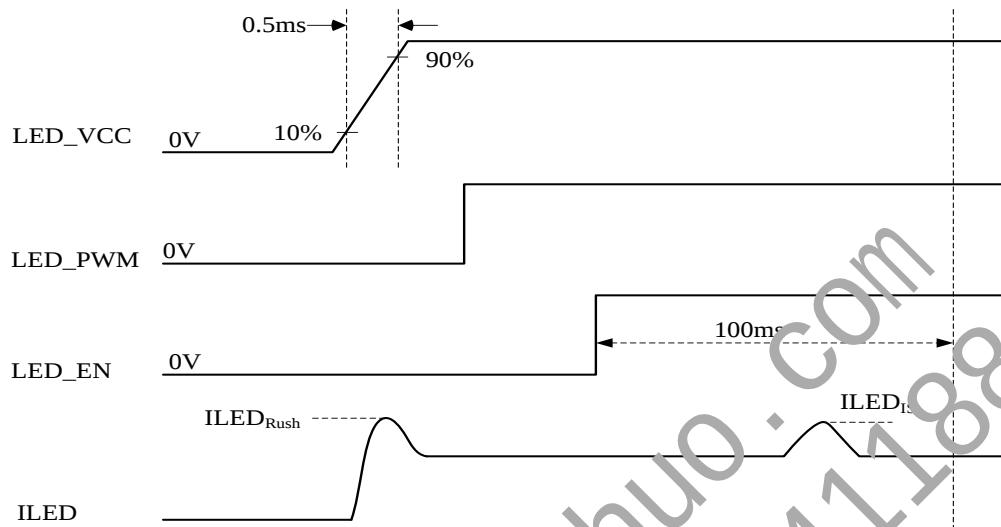
I_{LED_IS}: the maximum current of the first 100ms after power-on,

Measurement Conditions: Show as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 °C, f_{PWM} = 200 Hz, Duty = 100%.



PRODUCT SPECIFICATION

VLED rising time is 0.5ms



Note (2) If PWM control frequency is applied in the range less than 1KHz, the "waterfall" phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

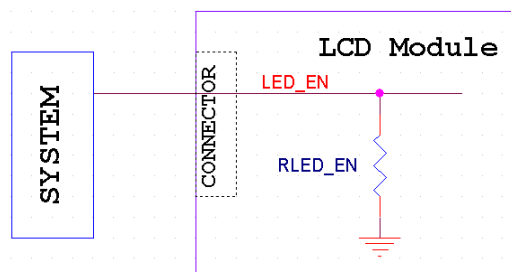
$$(N + 0.33) * f \leq f_{PWM} < (N + 0.66) * f$$

N : Integer ($N \geq 3$)

f : Frame rate

Note (3) The specified LED power supply current is under the conditions at "LED_VCCS = Typ.", $T_a = 25 \pm 2^\circ\text{C}$, $f_{PWM} = 200\text{ Hz}$, Duty=100%.

Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. For example, the figure below describes the equivalent pull down impedance of LED_EN (If it exists). The rest pull down impedances of other signals (eg. HPD, PWM ...) are in the same concept.



Note (5) If the cycle-to-cycle difference of PWM duty exceeds 0.1%, especially when the PWM duty is low, slight brightness change might be observed.

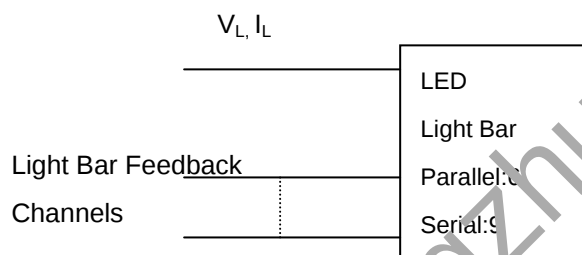
PRODUCT SPECIFICATION

4.3.3 BACKLIGHT UNIT

 $T_a = 25 \pm 2 \text{ }^{\circ}\text{C}$

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	24.3	25.65	27	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L	-	93		mA	
Power Consumption	P_L	-	2.39	2.51	W	(3)
LED Life Time	L_{BL}	15000			Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at $T_a = 25 \pm 2 \text{ }^{\circ}\text{C}$ and $I_L = 15.5 \text{ mA}$ (Per EA) until the brightness becomes $\leq 50\%$ of its original value.

PRODUCT SPECIFICATION

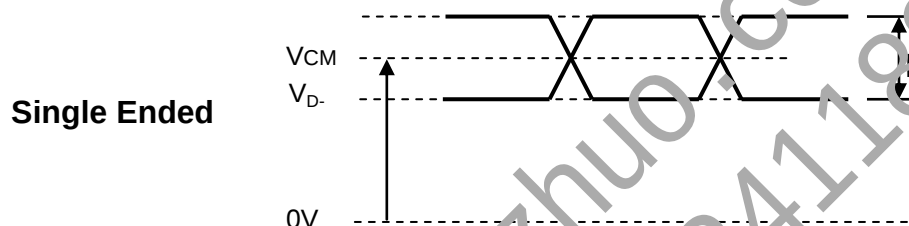
4.4 DISPLAY PORT SIGNAL TIMING SPECIFICATION

4.4.1 DISPLAY PORT INTERFACE

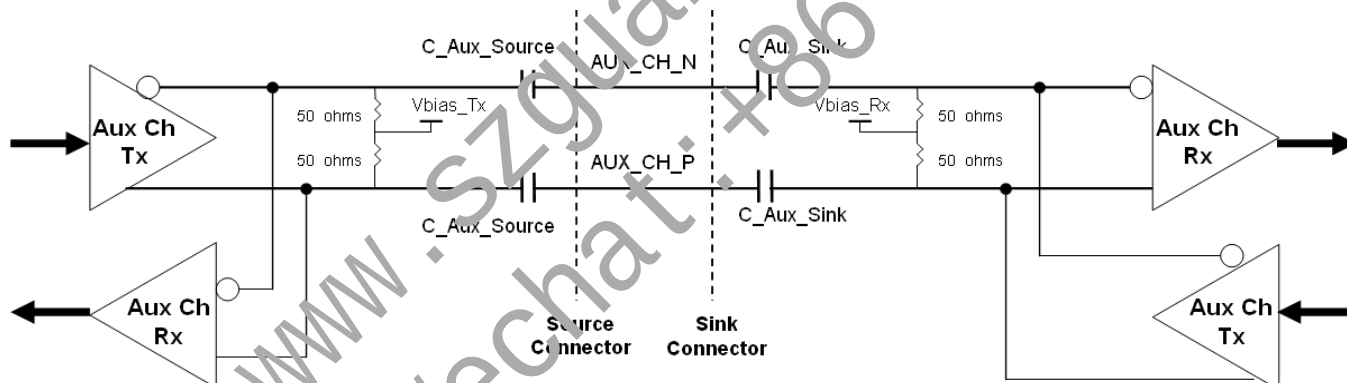
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Signal Common Mode Voltage(MainLink and AUX)	VCM	0		2	V	(1)(4)
AUX AC Coupling Capacitor	C_Aux_Source	75		200	nF	(2)
Main Link AC Coupling Capacitor	C_ML_Source	75		200	nF	(3)

Note (1) Display port interface related AC coupled signals are following VESA DisplayPort Standard

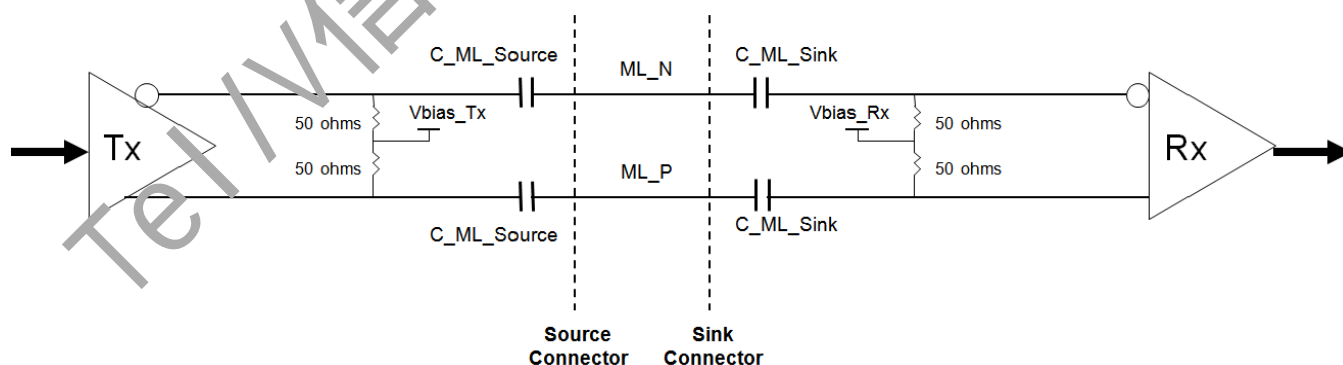
Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2. There are many optional items described in eDP1.2. If some optional item is requested, please contact us.



(2) Recommended eDP AUX Channel topology is as below and the AUX AC Coupling Capacitor (C_Aux_Source) should be placed on the source device.



(3) Recommended Main Link Channel topology is as below and the Main Link AC Coupling Capacitor (C_ML_Source) should be placed on the source device.



(4) The source device should pass the test criteria described in DisplayPortCompliance Test Specification (CTS) 1.1

PRODUCT SPECIFICATION

4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Refresh rate 60Hz

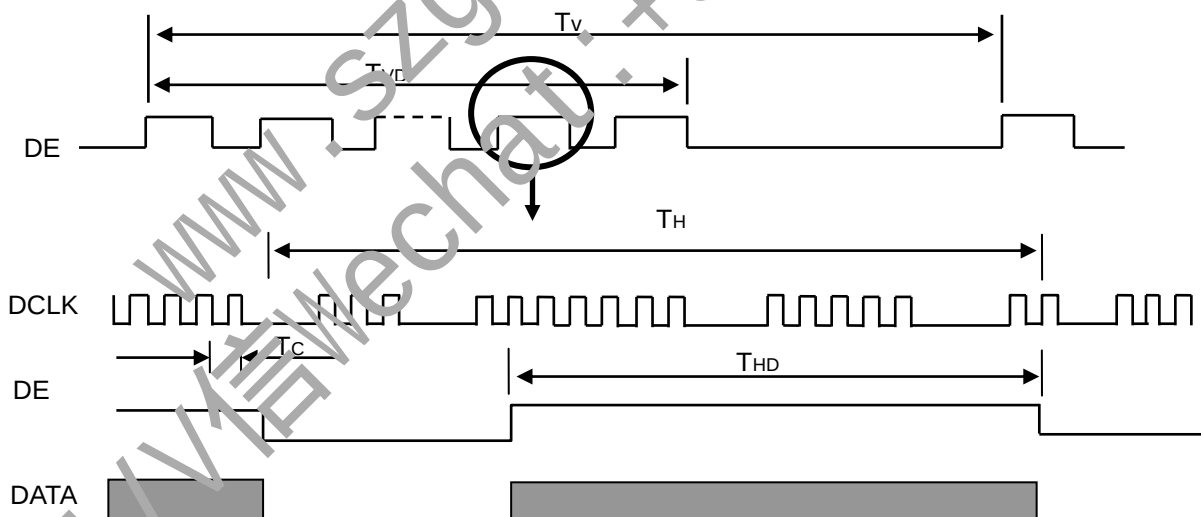
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	152.28	154.26	156.24	MHz	-
DE	Vertical Total Time	TV	1232	1236	1240	TH	-
	Vertical Active Display Period	TVD	1200	1200	1200	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	36	TV-TVD	TH	-
	Horizontal Total Time	TH	2060	2080	2100	Tc	-
	Horizontal Active Display Period	THD	1920	1920	1920	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	160	TH-THD	Tc	-

Refresh rate 48Hz (Power Saving Mode)

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	152.28	154.26	156.24	MHz	-
DE	Vertical Total Time	TV	1541	1545	1549	TH	-
	Vertical Active Display Period	TVD	1200	1200	1200	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	345	TV-TVD	TH	-
	Horizontal Total Time	TH	2060	2080	2100	Tc	-
	Horizontal Active Display Period	THD	1920	1920	1920	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	160	TH-THD	Tc	-

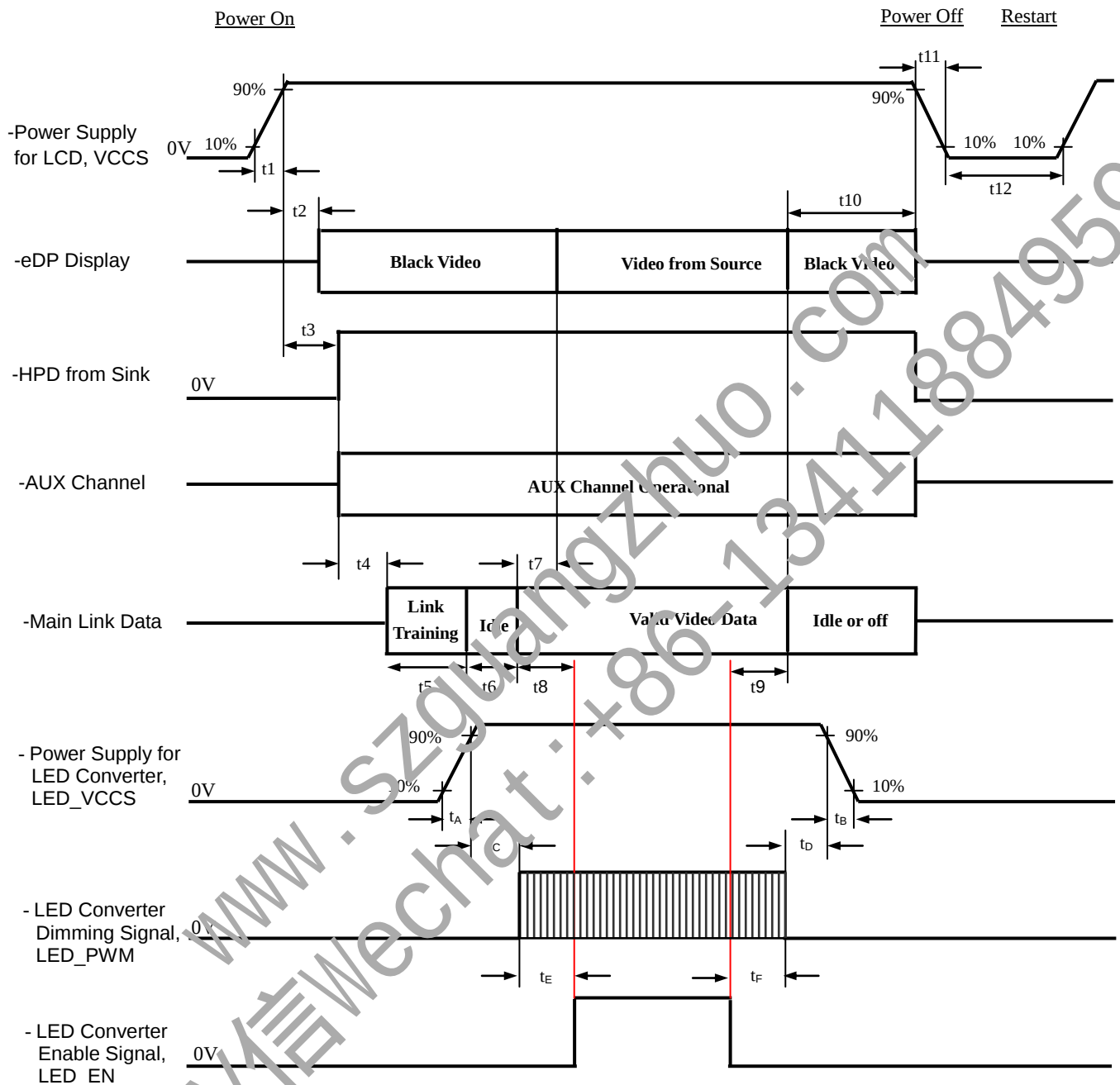
Note (1) The panel can operate at 60Hz normal mode and power saving mode respectively. All reliability tests are based on specific timing of 60Hz refresh rate. We can only assure the panel's electrical function at power saving mode.

INPUT SIGNAL TIMING DIAGRAM



PRODUCT SPECIFICATION

4.6 POWER ON/OFF SEQUENCE



PRODUCT SPECIFICATION

Timing Specifications

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	Power rail rise time, 10% to 90%	Source	0.5	10	ms	See Note 5 below--
t2	Delay from LCD,VCCS to black video generation	Sink	0	200	ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source (see Notes:2 and 3 below)
t3	Delay from LCD,VCCS to HPD high	Sink	0	200	ms	Sink AUX Channel must be operational upon HPD high (see Note:4 below)
t4	Delay from HPD high to link training initialization	Source	0	-	ms	Allows for Source to read link capability and initialize
t5	Link training duration	Source	0	-	ms	Dependent on Source link training protocol
t6	Link idle	Source	0	-	ms	Min Accounts for required BS-Idle pattern. Max allows for Source frame synchronization
t7	Delay from valid video data from Source to video on display	Sink	0	50	ms	Max value allows for Sink to validate video data and timing. At the end of T7, Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and Sink will no longer generate automatic Black Video
t8	Delay from valid video data from Source to backlight on	Source	80	-	ms	Source must assure display video is stable *: Recommended by INX. To avoid garbage image.
t9	Delay from backlight off to end of valid video data	Source	50	-	ms	Source must assure backlight is no longer illuminated. At the end of T9, Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and Sink will automatically display Black Video. (See Notes: 2 and 3 below) *: Recommended by INX. To avoid garbage image.
t10	Delay from end of valid video data from Source to power off	Source	0	500	ms	Black video will be displayed after receiving idle or off signals from Source
t11	VCCS power rail fall time, 90% to 10%	Source	0.5	10	ms	See Note 5 below

PRODUCT SPECIFICATION

t ₁₂	VCCS Power off time	Source	500	-	ms	-
t _A	LED power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t _B	LED power rail fall time, 90% to 10%	Source	0	10	ms	-
t _C	Delay from LED power rising to LED dimming signal	Source	1	-	ms	-
t _D	Delay from LED dimming signal to LED power falling	Source	1	-	ms	-
t _E	Delay from LED dimming signal to LED enable signal	Source	0	-	ms	-
t _F	Delay from LED enable signal to LED dimming signal	Source	0	-	ms	-

Note (1) Please don't plug or unplug the interface cable when system is turned on.

Note (2) The Sink must include the ability to automatically generate Black Video autonomously. The Sink must automatically enable Black Video under the following conditions:

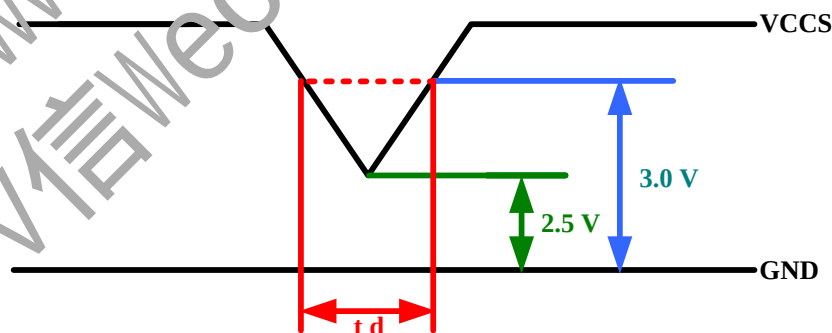
- Upon LCDVCC power-on (within T2 max)
- When the "NoVideoStream_Flag" (VB-ID Bit 3) is received from the Source (at the end of T9)

Note (3) The Sink may implement the ability to disable the automatic Black Video function, as described in Note (2), above, for system development and debugging purposes.

Note (4) The Sink must support AUX Channel polling by the Source immediately following LCDVCC power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to response to an AUX Channel transaction with the time specified within T3 max.

Note (5) The VCCS power rail is recommended to rise and fall linearly. If not, please contact us to conduct risk assessment

4.7 MOMENTARY VOLTAGE DROPS



(1) When $2.5V \leq V_{cc} < 3.0V$ and $t_d \leq 10ms$, the unit must work normally when VCC return to 3.0V.

(2) When $V_{cc} < 2.5V$, momentary voltage shall conform to the input voltage sequence.

PRODUCT SPECIFICATION

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	3.2	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I _L	93	mA

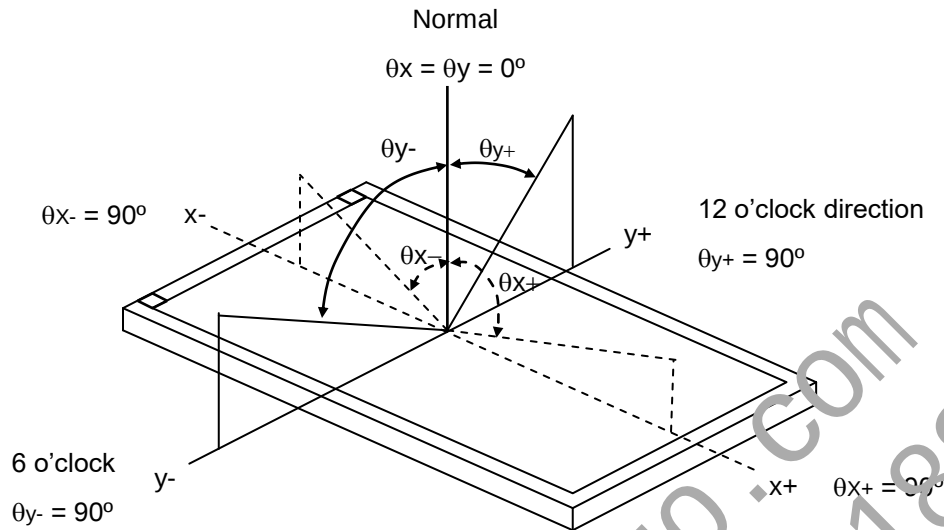
The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min	Typ.	Max.	Unit	Note	
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing Normal Angle $\theta_x=0^\circ, \theta_y=0^\circ$ Viewing Normal Angle	800	1000	-	-	(2), (5),(7)	
Response Time		T _R		-	11	14	ms	(3),(7)	
		T _F		-	9	11	ms		
Average Luminance of White		L _{Ave}		255	300		cd/m ²	(4), (6),(7)	
Color Chromaticity	Red	R _x		$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing Normal Angle	Typ – 0.03	0.590	Typ + 0.03	-	(1),(7)
		R _y				0.350		-	
	Green	G _x		$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing Normal Angle		0.330		-	
		G _y				0.555		-	
	Blue	B _x		0.153		-			
		B _y		0.119		-			
	White	W _x	0.313	-					
		W _y	0.329	-					
Color gamut		C.G	42	45		%	(8)		
Cross talk		CT	-	-	2	%	(5),(7),(9)		
Viewing Angle	Horizontal	θ_{x+}	CR≥10	80	89	-	Deg.	(1),(5), (7)	
		θ_y		80	89	-			
	Vertical	θ_{x-}		80	89	-			
		θ_{y-}		80	89	-			
White Variation		ΔW _{5p}	$\theta_x=0^\circ, \theta_y=0^\circ$	80	90		-	(5),(6),	
		ΔW _{13p}	$\theta_x=0^\circ, \theta_y=0^\circ$	65	75			(7)	

PRODUCT SPECIFICATION

Note (1) Definition of Viewing Angle (θ_x , θ_y):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{255} / L_0$$

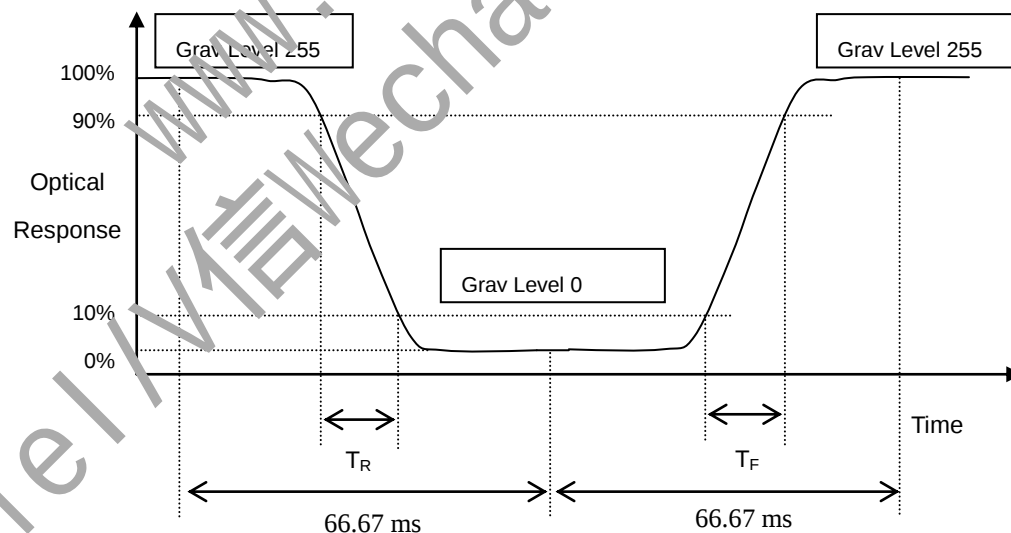
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

$$CR = CR(1)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R , T_F):



PRODUCT SPECIFICATION

Note (4) Definition of Average Luminance of White (L_{AVE}):

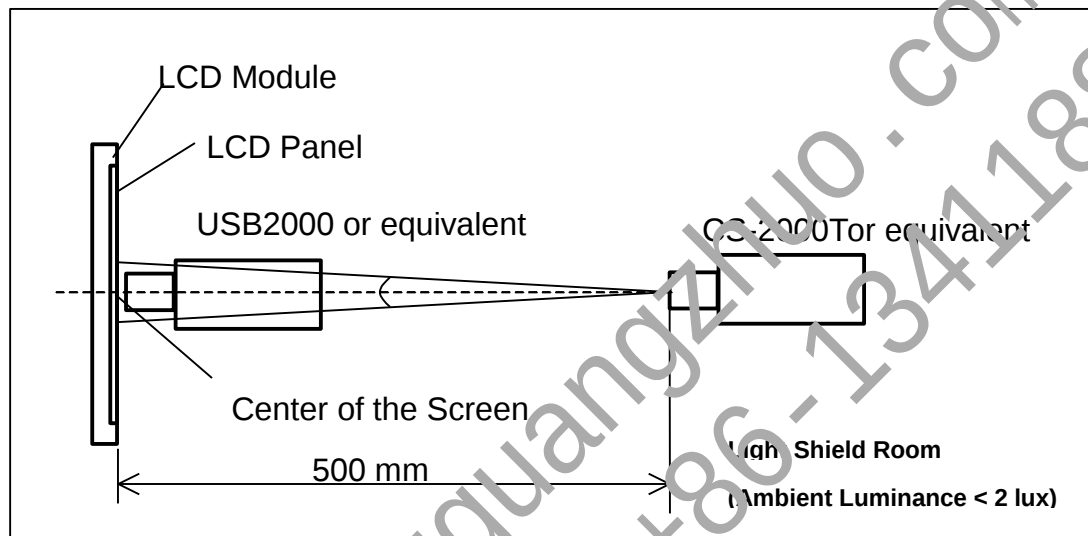
Measure the luminance of White at 5 points

$$L_{AVE} = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



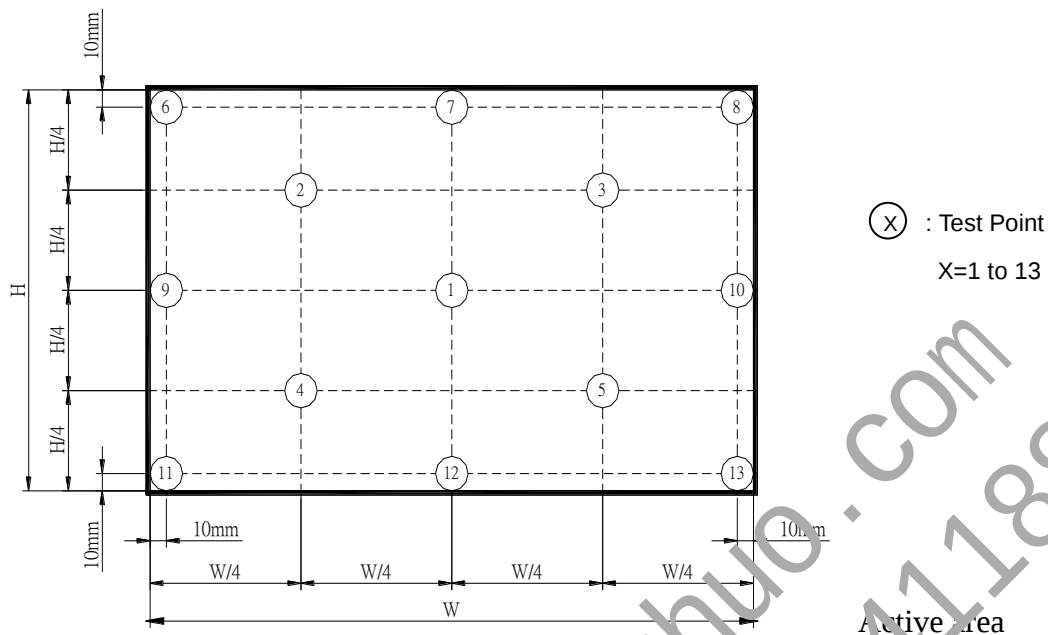
Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

$$\delta W_{5p} = \{ \text{Minimum} [L(1) \sim L(5)] / \text{Maximum} [L(1) \sim L(5)] \} * 100\%$$

$$\delta W_{13p} = \{ \text{Minimum} [L(1) \sim L(13)] / \text{Maximum} [L(1) \sim L(13)] \} * 100\%$$

PRODUCT SPECIFICATION



Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

Note (8) Definition of color gamut (C.G%):

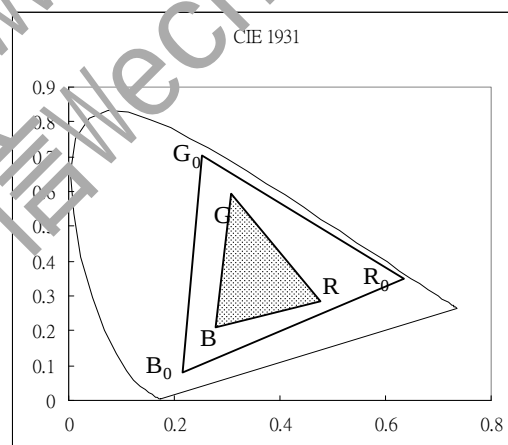
$$C.G\% = \frac{R G B}{R_0 G_0 B_0} \times 100\%$$

R_0, G_0, B_0 : color coordinates of red, green, and blue defined by NTSC, respectively.

R, G, B : color coordinates of module on 63 gray levels of red, green, and blue, respectively.

$R_0 G_0 B_0$: area of triangle defined by R_0, G_0, B_0

$R G B$: area of triangle defined by R, G, B



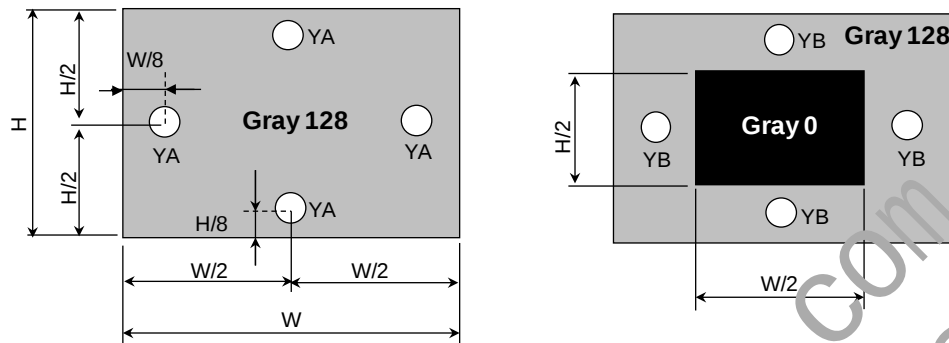
Note (9) Cross Talk (CT):

$$CT = |Y_B - Y_A| / Y_A \times 100\%$$

Where

PRODUCT SPECIFICATION

 Y_A =Luminance of measured location in left figure

 Y_B =Luminance of measured location in right figure


6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60°C, 240 hours	(1) (2)
Low Temperature Storage Test	-20°C, 240 hours	
Thermal Shock Storage Test	-20°C, 0.5hour $\longleftrightarrow$ 60°C, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	60°C, 240 hours	
Low Temperature Operation Test	0°C, 240 hours	
High Temperature & High Humidity Operation Test	50°C, 80% RH, 240 hours	
ESD Test (Operation)	100pF, 330 Ω , 1sec/cycle Condition 1 : Contact Discharge, $\pm 8KV$ Condition 2 : Air Discharge, $\pm 15KV$	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave, 1 time for each direction of $\pm X, \pm Y, \pm Z$	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

Note (1) Criteria: Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

PRODUCT SPECIFICATION

7. PACKING

7.1 MODULE LABEL

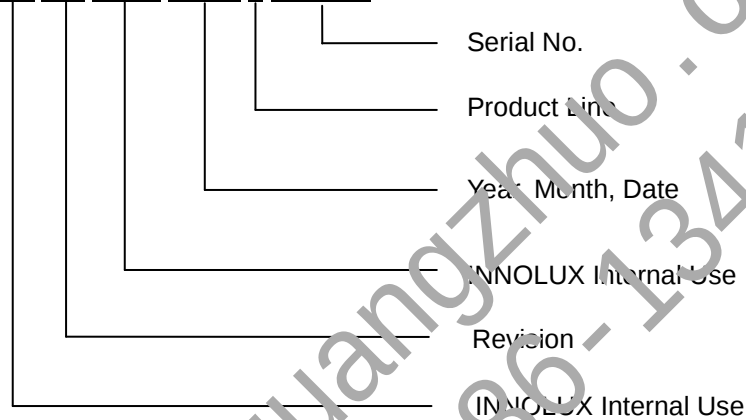
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: N140JCA-ELK

(b) Revision: Rev. XX, for example: C1, C2 ...etc.

(c) Serial ID: XXXXXXXXYMDLNNNN



(d) Production Location: MADE IN XXXX.

(e) UL logo: XXXX especially stands for panel manufactured by INNOLUX China satisfying UL requirement.

Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2010~2019

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I, O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, ...etc.

PRODUCT SPECIFICATION

7.2 CARTON

- (1) Box Dimensions : 435(L)*350(W)*320(H)
(2) 30 modules/Carton

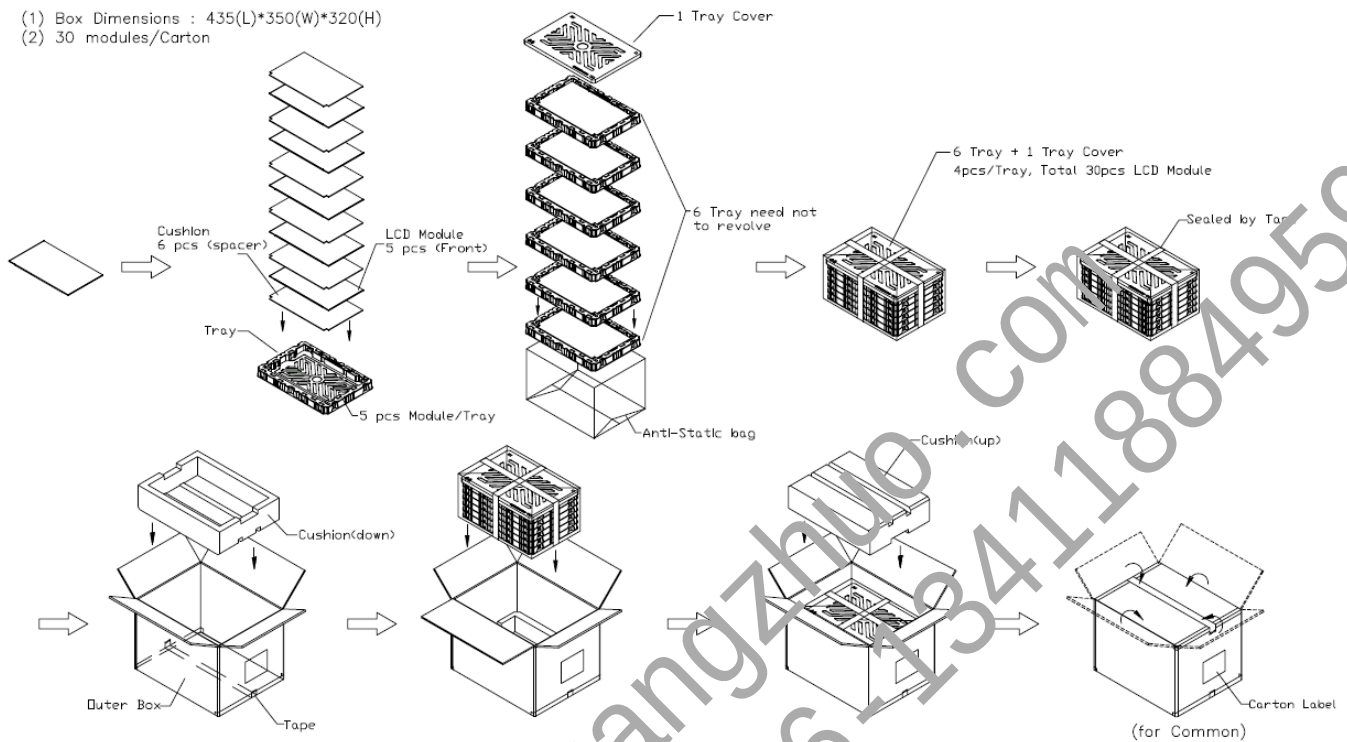


Figure. 7-2 Packing method

PRODUCT SPECIFICATION

7-3 PALLET

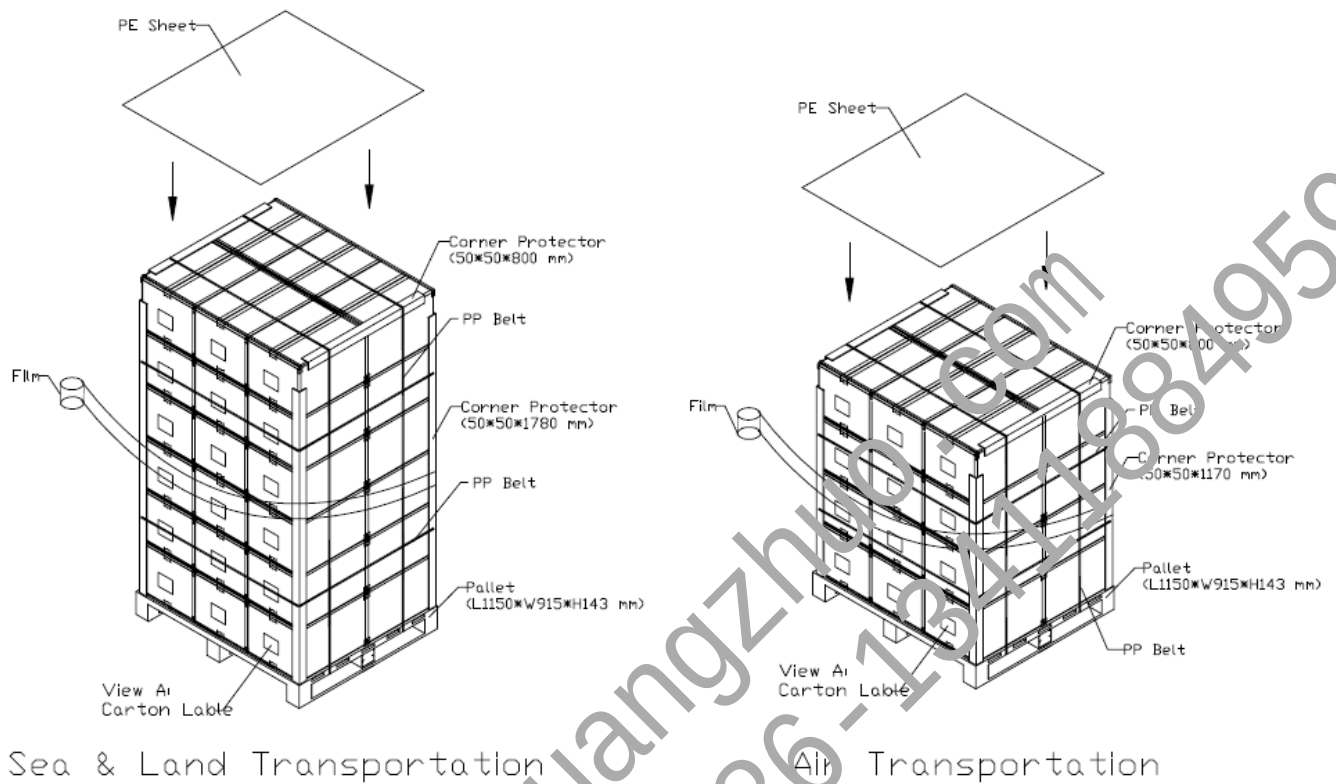


Figure. 7-3 Packing method

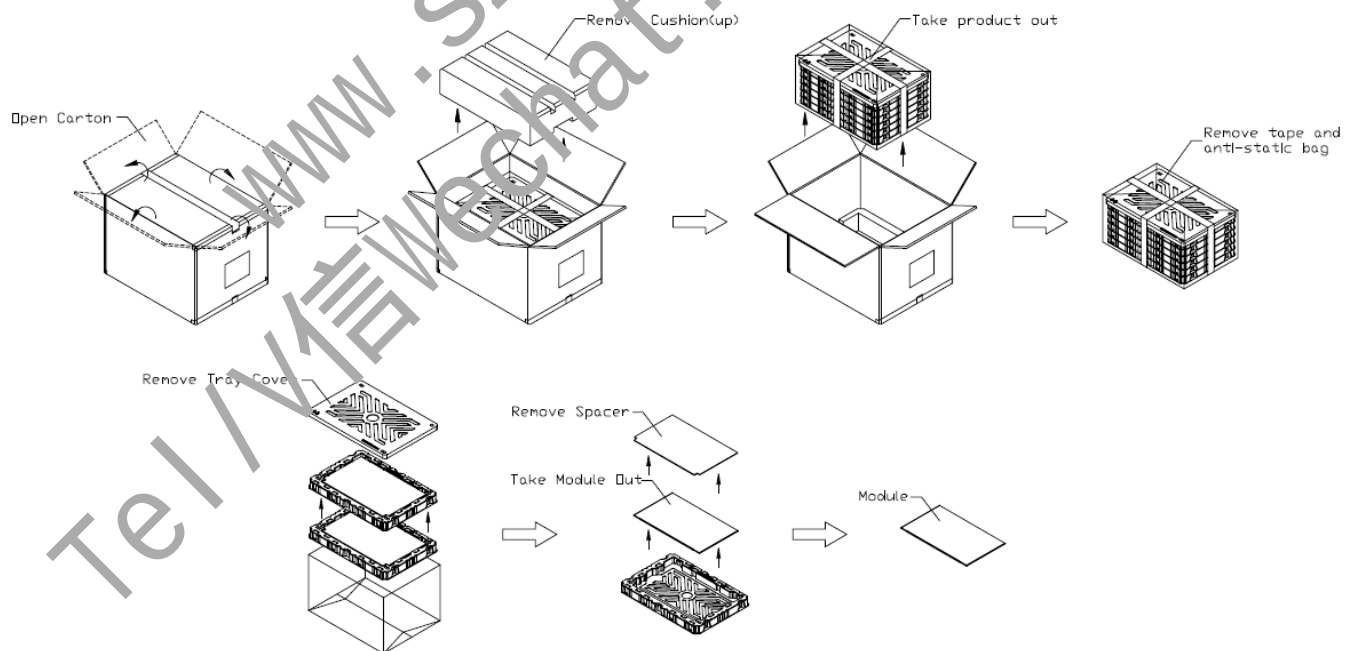


Figure. 7-3 Un-Packing method

PRODUCT SPECIFICATION

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

- (1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.
- (2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
- (3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
- (5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
- (6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.
- (9) Do not disassemble the module.
- (10) Do not pull or fold the LED wire.
- (11) Pins of I/F connector should not be touched directly with bare hands.
- (12) Do not re-attach protective film onto the polarizer because of risk of bubble mura and dust.

8.2 STORAGE PRECAUTIONS

- (1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
- (3) It may reduce the display quality if the ambient temperature is lower than 10 °C. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

- (1) Do not pull the I/F connector in or out while the module is operating.
- (2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMIS LSI chips from damage during latch-up.
- (3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

PRODUCT SPECIFICATION

Appendix. EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPD standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	00	Header	00	00000000
1	01	Header	FF	11111111
2	02	Header	FF	11111111
3	03	Header	FF	11111111
4	04	Header	FF	11111111
5	05	Header	FF	11111111
6	06	Header	FF	11111111
7	07	Header	00	00000000
8	08	ID system manufacturer name ("CMN")	0D	00001101
9	09	ID system manufacturer name	AE	10101110
10	0A	ID system Product Code (LSB)	41	01000001
11	0B	ID system Product Code (MSB)	14	00010100
12	0C	ID S/N (fixed "00")	00	00000000
13	0D	ID S/N (fixed "00")	00	00000000
14	0E	ID S/N (fixed "00")	00	00000000
15	0F	ID S/N (fixed "00")	00	00000000
16	10	Week of manufacture (fixed week code)	28	00101000
17	11	Year of manufacture (fixed year code)	1F	00011111
18	12	Version=1	01	00000001
19	13	Revision=4	04	00000100
20	14	Vedio Input Definition	A5	10100101
21	15	Active area horizontal ("30.159cm")	1E	00011110
22	16	Active area vertical ("18.85cm")	13	00010011
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("RGB, Non-continuous")	03	00000011
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	28	00101000
26	1A	Bx1, Bx0, Bv1, Bv0, Wx1, Wx0, Wy1, Wy0	65	01100101
27	1B	Rx=0.590	97	10010111
28	1C	Ry=0.350	59	01011001
29	1D	Gx=0.330	54	01010100
30	1E	Gy=0.555	8E	10001110
31	1F	Bx=0.153	27	00100111
32	20	By=0.119	1E	00011110
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	No manufacturer's specific timing	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

PRODUCT SPECIFICATION

42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("154.26MHz")	42	01000010
55	37	# 1 Pixel clock (hex LSB first)	30	00111100
56	38	# 1 H active ("1920")	80	10000000
57	39	# 1 H blank ("160")	A0	10100000
58	3A	# 1 H active : H blank	70	01110000
59	3B	# 1 V active ("1200")	B0	10110000
60	3C	# 1 V blank ("36")	24	00100100
61	3D	# 1 V active : V blank	40	01000000
62	3E	# 1 H sync offset ("46")	30	00110000
63	3F	# 1 H sync pulse width ("30")	20	00100000
64	40	# 1 V sync offset : V sync pulse width ("10:6")	A6	10100110
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width	00	00000000
66	42	# 1 H image size ("301 mm")	2D	00101101
67	43	# 1 V image size ("188 mm")	BC	10111100
68	44	# 1 H image size : V image size	10	00010000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71	47	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
72	48	Detailed timing description # 2 Pixel clock ("123.41MHz")	35	00110101
73	49	# 2 Pixel clock (hex LSB first)	30	00110000
74	4A	# 2 H active ("1920")	80	10000000
75	4B	# 2 H blank ("160")	A0	10100000
76	4C	# 2 H active : H blank	70	01110000
77	4D	# 2 V active ("1200")	B0	10110000
78	4E	# 2 V blank ("36")	24	00100100
79	4F	# 2 V active : V blank	40	01000000
80	50	# 2 H sync offset ("46")	30	00110000
81	51	# 2 H sync pulse width ("30")	20	00100000
82	52	# 2 V sync offset : V sync pulse width ("10:6")	A6	10100110
83	53	# 2 H sync offset : H sync pulse width : V sync offset : V sync width	00	00000000
84	54	# 2 H image size ("301 mm")	2D	00101101
85	55	# 2 V image size ("188 mm")	BC	10111100
86	56	# 2 H image size : V image size	10	00010000
87	57	# 2 H boarder ("0")	00	00000000

PRODUCT SPECIFICATION

88	58	# 2 V boarder ("0")	00	00000000
89	59	# 2 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
90	5A	Indicates that this 18 byte descriptor is a Display Descriptor	00	00000000
91	5B	Indicates that this 18 byte descriptor is a Display Descriptor	00	00000000
92	5C	Set to 00h when 18 byte descriptor is used as a Display Descriptor	00	00000000
93	5D	Tag Number for Display Range Limits Descriptor	FD	11111101
94	5E	Display Range Limits Offset : FLAGS	00	00000000
95	5F	Minimum Vertical Rate ("40Hz")	28	00101000
96	60	Maximum Vertical Rate ("60Hz")	3C	00111100
97	61	Minimum Horizontal Rate ("75KHz")	4B	01010111
98	62	Maximum Horizontal Rate ("75KHz")	4B	01010111
99	63	Maximum Pixel Clock ("154.26MHz")	10	00010000
100	64	Video Timing Support Flags : Bytes 10 --> 17 indicate support for additional video timings	01	00000001
101	65	Line Feed (0Ah if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	0A	00001010
102	66	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	20	00100000
103	67	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	20	00100000
104	68	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	20	00100000
105	69	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	20	00100000
106	6A	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	20	00100000
107	6B	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	20	00100000
108	6C	Detailed timing description # 4	00	00000000
109	6D	# 4 Flag	00	00000000
110	6E	# 4 Reserved	00	00000000
111	6F	# 4 ASCII string Model Name	FE	11111110
112	70	# 4 Flag	00	00000000
113	71	# 4 Character of Model name ("N")	4E	01001110
114	72	# 4 Character of Model name ("1")	31	00110001
115	73	# 4 Character of Model name ("4")	34	00110100
116	74	# 4 Character of Model name ("0")	30	00110000
117	75	# 4 Character of Model name ("J")	4A	01001010
118	76	# 4 Character of Model name ("C")	43	01000011
119	77	# 4 Character of Model name ("A")	41	01000001
120	78	# 4 Character of Model name ("-")	2D	00101101
121	79	# 4 Character of Model name ("E")	45	01000101
122	7A	# 4 Character of Model name ("L")	4C	01001100
123	7B	# 4 Character of Model name ("K")	4B	01001011
124	7C	# 4 New line character indicates end of ASCII string	0A	00001010
125	7D	# 4 Padding with "Blank" character	20	00100000
126	7E	No extension	01	00000001
127	7F	Checksum	13	00010011
128	80	DisplayID EDID extension block tag	02	00000010



PRODUCT SPECIFICATION

129	81	DisplayID version revision	03	00000011
130	82	Start of Timing Data (00:No detailed timing descriptors are provided and no data is provided in the reserved data block)	0D	00001101
131	83	Total number of Detailed Timing formats in entire E-EDID structure.	00	00000000
132	84	Datablock 1: AMD Vendor specific Data Block(Total :8 byte)	68	01101000
133	85	AMD IEEE OUI Value(0x00001A)	1A	00011010
134	86	AMD IEEE OUI Value(0x00001A)	00	00000000
135	87	AMD IEEE OUI Value(0x00001A)	00	00000000
136	88	AMD VSDB Version	01	00000001
137	89	Freesync Capability(01:Freesync support,00:Freesync no support.)	01	00000001
138	8A	Min Refresh Rate	28	00010000
139	8B	Max Refresh Rate	3C	00111100
140	8C	FreeSync MCCS VCP Code; required if EDID update not possible to indicate current state of FreeSync support.	00	00000000
141	8D	Reserved	00	00000000
142	8E	Reserved	00	00000000
143	8F	Reserved	00	00000000
144	90	Reserved	00	00000000
145	91	Reserved	00	00000000
146	92	Reserved	00	00000000
147	93	Reserved	00	00000000
148	94	Reserved	00	00000000
149	95	Reserved	00	00000000
150	96	Reserved	00	00000000
151	97	Reserved	00	00000000
152	98	Reserved	00	00000000
153	99	Reserved	00	00000000
154	9A	Reserved	00	00000000
155	9B	Reserved	00	00000000
156	9C	Reserved	00	00000000
157	9D	Reserved	00	00000000
158	9E	Reserved	00	00000000
159	9F	Reserved	00	00000000
160	A0	Reserved	00	00000000
161	A1	Reserved	00	00000000
162	A2	Reserved	00	00000000
163	A3	Reserved	00	00000000
164	A4	Reserved	00	00000000
165	A5	Reserved	00	00000000
166	A6	Reserved	00	00000000
167	A7	Reserved	00	00000000
168	A8	Reserved	00	00000000
169	A9	Reserved	00	00000000
170	AA	Reserved	00	00000000
171	AB	Reserved	00	00000000
172	AC	Reserved	00	00000000
173	AD	Reserved	00	00000000
174	AE	Reserved	00	00000000



PRODUCT SPECIFICATION

175	AF	Reserved	00	00000000
176	B0	Reserved	00	00000000
177	B1	Reserved	00	00000000
178	B2	Reserved	00	00000000
179	B3	Reserved	00	00000000
180	B4	Reserved	00	00000000
181	B5	Reserved	00	00000000
182	B6	Reserved	00	00000000
183	B7	Reserved	00	00000000
184	B8	Reserved	00	00000000
185	B9	Reserved	00	00000000
186	BA	Reserved	00	00000000
187	BB	Reserved	00	00000000
188	BC	Reserved	00	00000000
189	BD	Reserved	00	00000000
190	BE	Reserved	00	00000000
191	BF	Reserved	00	00000000
192	C0	Reserved	00	00000000
193	C1	Reserved	00	00000000
194	C2	Reserved	00	00000000
195	C3	Reserved	00	00000000
196	C4	Reserved	00	00000000
197	C5	Reserved	00	00000000
198	C6	Reserved	00	00000000
199	C7	Reserved	00	00000000
200	C8	Reserved	00	00000000
201	C9	Reserved	00	00000000
202	CA	Reserved	00	00000000
203	CB	Reserved	00	00000000
204	CC	Reserved	00	00000000
205	CD	Reserved	00	00000000
206	CE	Reserved	00	00000000
207	CF	Reserved	00	00000000
208	D0	Reserved	00	00000000
209	D1	Reserved	00	00000000
210	D2	Reserved	00	00000000
211	D3	Reserved	00	00000000
212	D4	Reserved	00	00000000
213	D5	Reserved	00	00000000
214	D6	Reserved	00	00000000
215	D7	Reserved	00	00000000
216	D8	Reserved	00	00000000
217	D9	Reserved	00	00000000
218	DA	Reserved	00	00000000
219	DB	Reserved	00	00000000
220	DC	Reserved	00	00000000
221	DD	Reserved	00	00000000

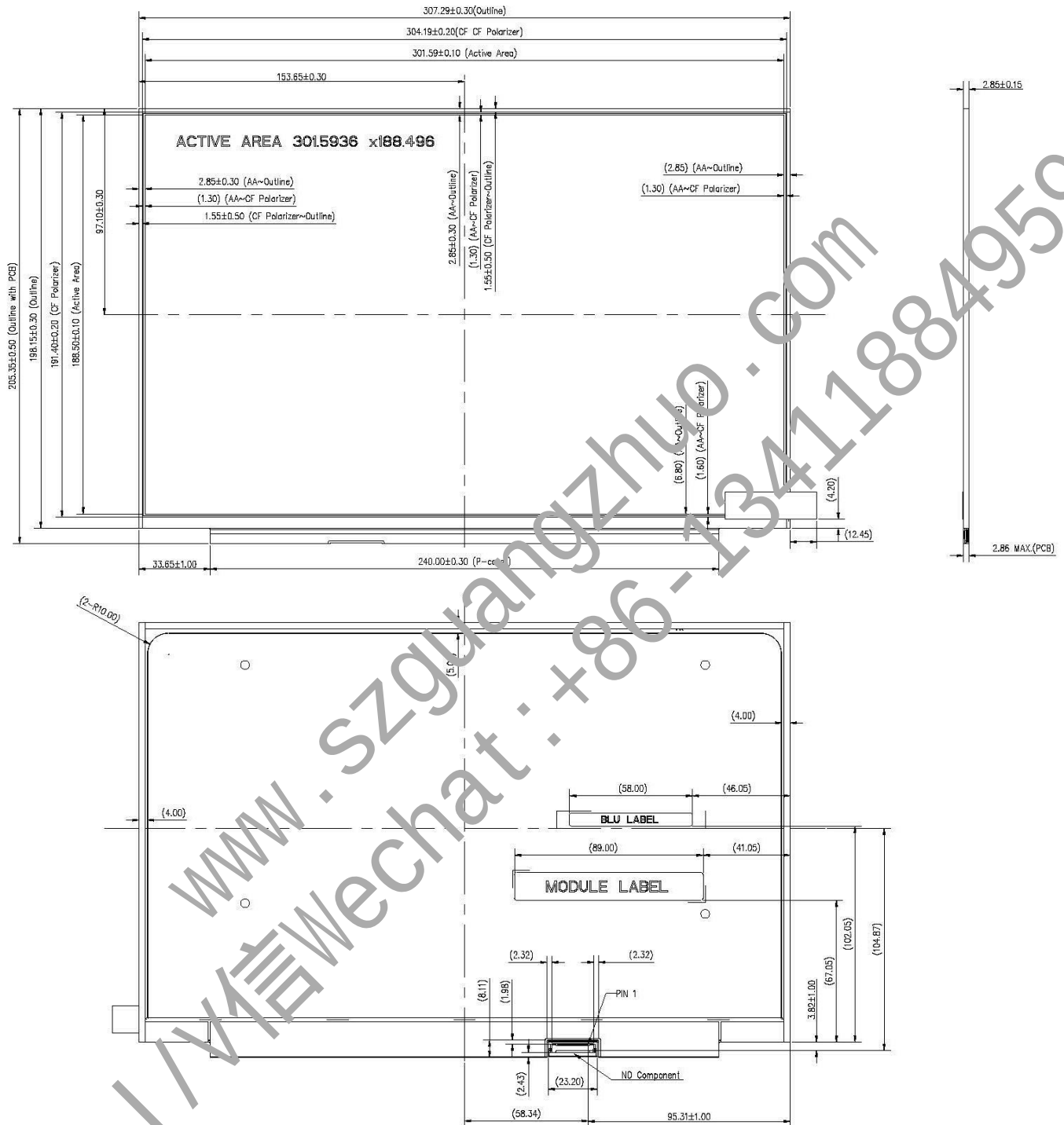


PRODUCT SPECIFICATION

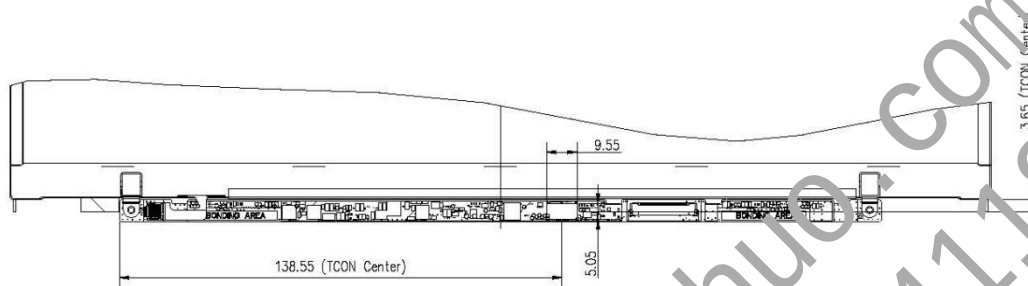
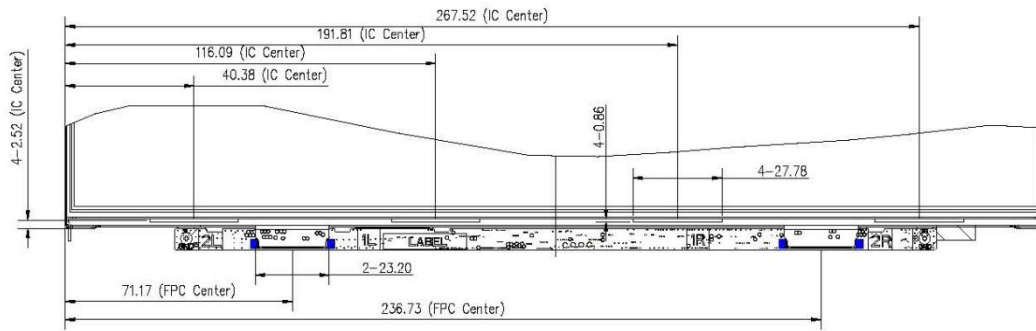
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230	E6	Manufacturer's S/N	00	00000000
231	E7	Manufacturer's S/N	00	00000000
232	E8	Manufacturer's S/N	00	00000000
233	E9	Manufacturer's S/N	00	00000000
234	EA	Manufacturer's S/N	00	00000000
235	EB	Manufacturer's S/N	00	00000000
236	EC	Manufacturer's S/N	00	00000000
237	ED	Manufacturer's S/N	00	00000000
238	EE	Manufacturer's S/N	00	00000000
239	EF	Manufacturer's S/N	00	00000000
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251	FB	Reserved	00	00000000
252	FC	Reserved	00	00000000
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PRODUCT SPECIFICATION

Appendix. OUTLINE DRAWING

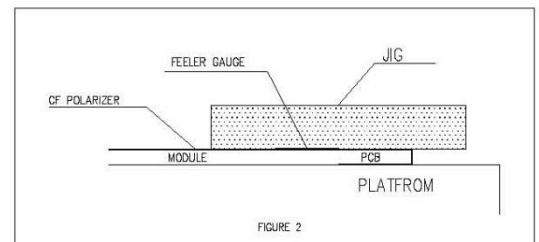
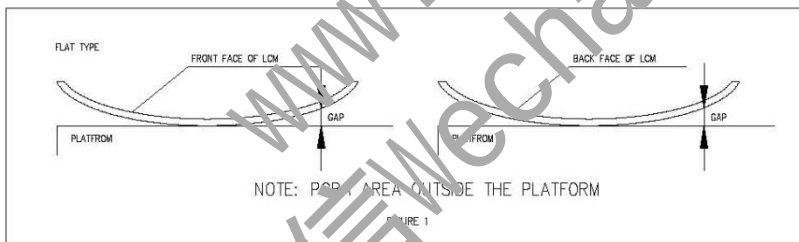


PRODUCT SPECIFICATION



NOTES :

1. IN ORDER TO AVOID ABNORMAL DISPLAY, POOLING AND WHITE SPOT, NO OVERLAPPING IS SUGGESTED AT CABLES, ANTENNAS, CAMERA, WAX, WAX OR FOREIGN OBJECTS OVER FPC/COF, T-CON AND VR LOCATION.
2. EDP CONNECTOR IS MEASURED AT PIN1 AND ITS MATING LINE.
3. MODULE FLATNESS SPEC 0.5 mm MAX. (SEE FIGURE 1) (SPEC. WILL BE MODIFIED AFTER DVT CHECK.)
4. "()" MARKS THE REFERENCE DIMENSION.
5. LCD HIGHEST PORTION MUST BE TOP POLARIZER AND OTHER LCM MATERIALS MUST BE LOWER THAN TOP POLARIZER. (MEASURED BY JIG (WEIGHT 100g) & FEELER GAUGE (0.1mm)) (SEE FIGURE 2)
6. THE SOP SHOULD REFER TO "DN0566762" IN XXXX.
6. MEASUREMENT OF THICKNESS MUST BE MEASURED BY CALIPER OR MICROMETER.

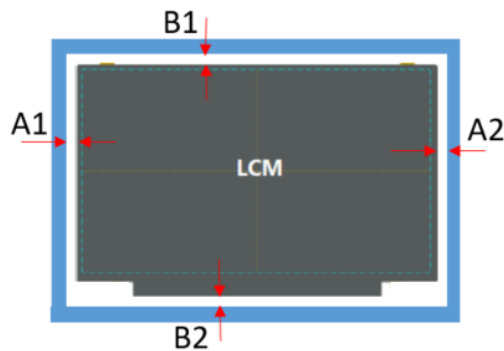


PRODUCT SPECIFICATION

Appendix. SYSTEM COVER DESIGN GUIDANCE

0.	Permanent deformation of system cover after reliability test
Definition	System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
1	Sponge area design behind panel
Definition	Sponge area design behind panel can not be across the panel metal rear and the reflector at the same time. It can be on the reflector area only.
2	Gap between system rear-cover & panel
Definition	The maximum thickness of sponge on the system rear-cover can not interfere to the maximum thickness of panel. Because the interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
3	Gap Design between panel & around structure

PRODUCT SPECIFICATION



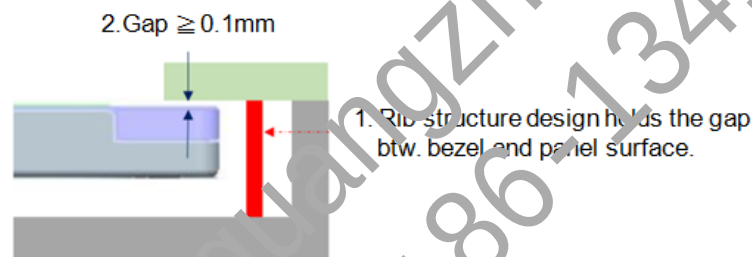
Item	Suggestion	Remark
A1	$A1 \geq 0.5$	Gap $\geq$ Panel outline max. tolerance + Assembly max. tolerance
A2	$A2 \geq 0.5$	
B1	$B1 \geq 0.5$	
B2	$B2 \geq 0.8$	

Definition

Gap Design between panel & around structure needs to consider the maximum tolerances of panel outline and assembly at the same time.
Gap Design suggestion is shown as A1/A2/B1/B2 on the chart.

4

Gap between panel & bezel

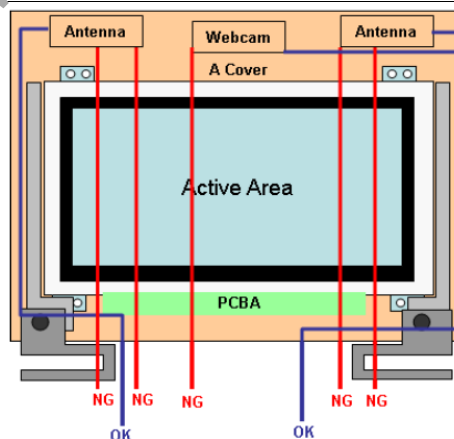


Definition

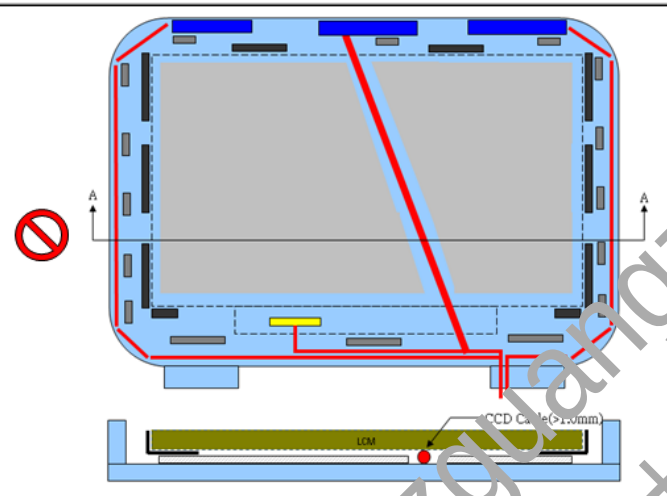
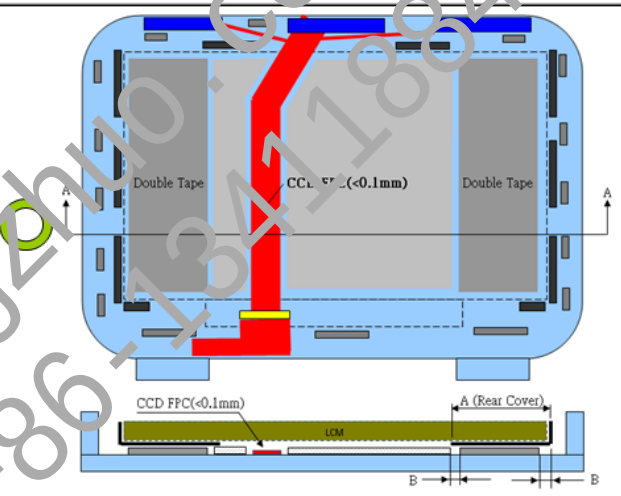
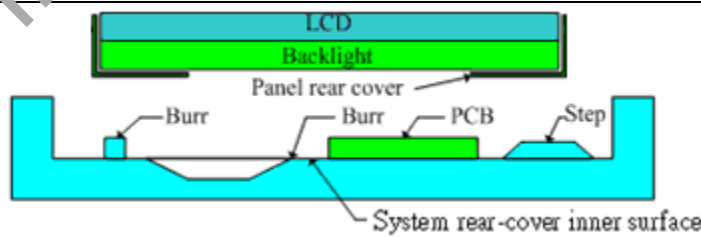
The gap between system bezel & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system for cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test or during pooling inspection procedure.
To remain the sufficient gap, design with system rib higher than maximum panel thickness is recommended.
The sufficient gap design is greater or equal to 0.1mm.

5

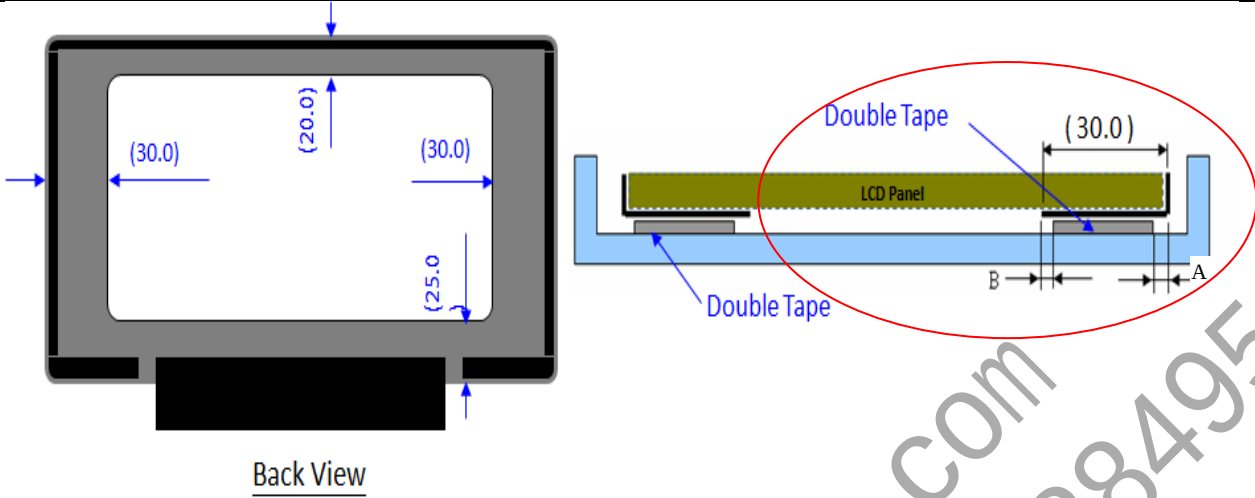
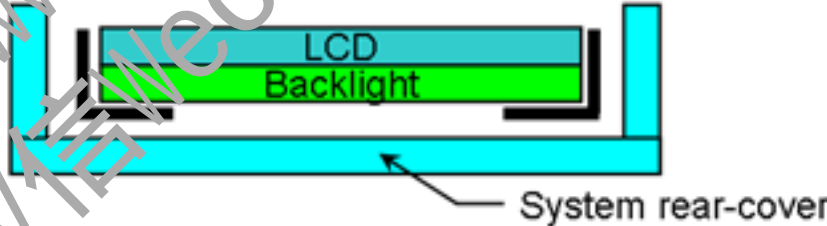
Cable routing behind panel



PRODUCT SPECIFICATION

Definition	It is strongly recommended that cables route around the panel outline, not overlap with the panel outline (including PCB). Because issue such as abnormal display & white spot after backpack test, hinge test, twist test or pogo test may occur. If any routings across panel outline are needed, we suggest design as below: -Using FFC/FPC to replace cables. -Routing at the right or left area of panel metal rear. -Avoid any routings at the step of panel or A cover. -No interference to panel. -It should not overlap TCON, COF/FPC, Driver IC										
6	Interference examination of antenna cable and Web Cam wire - To prevent panel damage, we suggest using CCD FPC to replace CCD cable - Using double tape to fix LCM module for no bracket design.   <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;"> Rear-cover Sponge Double Tape CCD Cable/FPC Hook Connector Camera/Antenna Stopper LCM Module Panel outline </td> <td style="width: 70%;"> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Rear Cover Width(A)</td><td style="padding: 2px;">A = 30mm</td></tr> <tr> <td style="padding: 2px;">Cover edge to Double Tape(B)</td><td style="padding: 2px;">B = 3.0mm</td></tr> <tr> <td style="padding: 2px;">CCD FPC thickness</td><td style="padding: 2px;"><0.1mm</td></tr> <tr> <td style="padding: 2px;">Sponge thickness</td><td style="padding: 2px;">0.5mm 0.2~0.3mm(compressed)</td></tr> </table> </td></tr> </table>	Rear-cover Sponge Double Tape CCD Cable/FPC Hook Connector Camera/Antenna Stopper LCM Module Panel outline	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Rear Cover Width(A)</td><td style="padding: 2px;">A = 30mm</td></tr> <tr> <td style="padding: 2px;">Cover edge to Double Tape(B)</td><td style="padding: 2px;">B = 3.0mm</td></tr> <tr> <td style="padding: 2px;">CCD FPC thickness</td><td style="padding: 2px;"><0.1mm</td></tr> <tr> <td style="padding: 2px;">Sponge thickness</td><td style="padding: 2px;">0.5mm 0.2~0.3mm(compressed)</td></tr> </table>	Rear Cover Width(A)	A = 30mm	Cover edge to Double Tape(B)	B = 3.0mm	CCD FPC thickness	<0.1mm	Sponge thickness	0.5mm 0.2~0.3mm(compressed)
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Sponge thickness	0.5mm 0.2~0.3mm(compressed)										
	If the antenna cable or Web Cam wire must overlap with the panel outline, both sides of the antenna cable or Web Cam wire must have a sponge(Sponge material can not contain NH3) and sponge require higher antenna cable or Web Cam wire.(Antenna cable or Web Cam wire should not overlap with TCON,COF/FPC,Driver IC) Note: If no interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.										
7	System rear-cover inner surface examination 										
Definition	Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.										
8	Tape/sponge design on system inner surface										

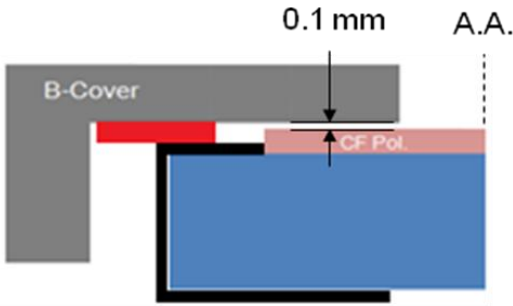
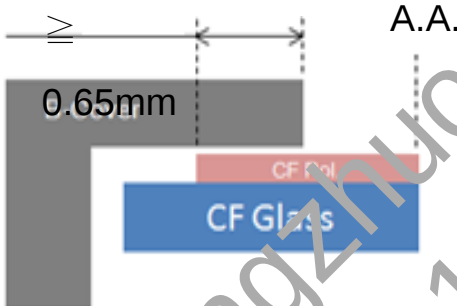
PRODUCT SPECIFICATION

	 Back View Double Tape LCD Panel Double Tape (30.0) (20.0) (30.0) (25.0) B A
Definition	To prevent peeling the bezel tape in rework process. The length of double tape is $30 - (A+B)$, A is bezel tape length and B is the double tape attaching tolerance. Ex :A :2mm, B:2mm, the length of double tape is $30-(2+2)=26\text{mm}$.
9	Material used for system rear-cover
	 LCD Backlight System rear-cover System rear-cover material: Al-Mg alloy System rear-cover thickness:1.5mm MIN
Definition	System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.
10	C cover shape design

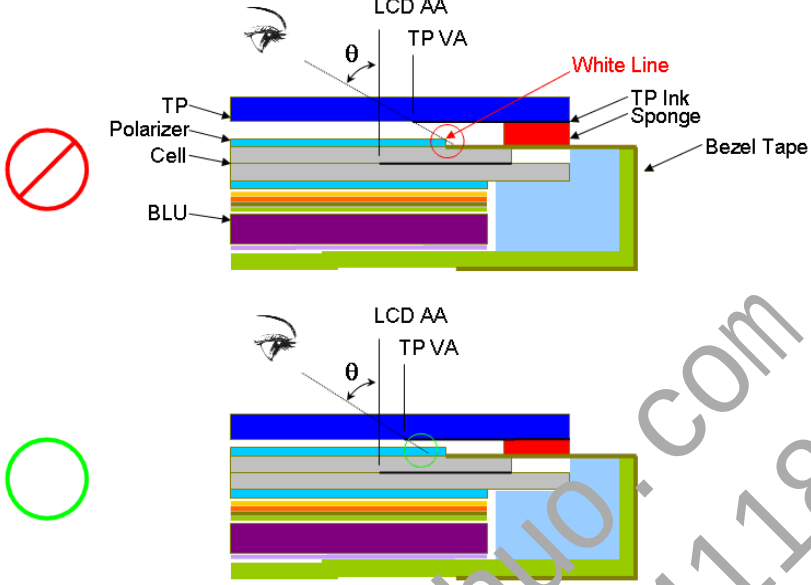
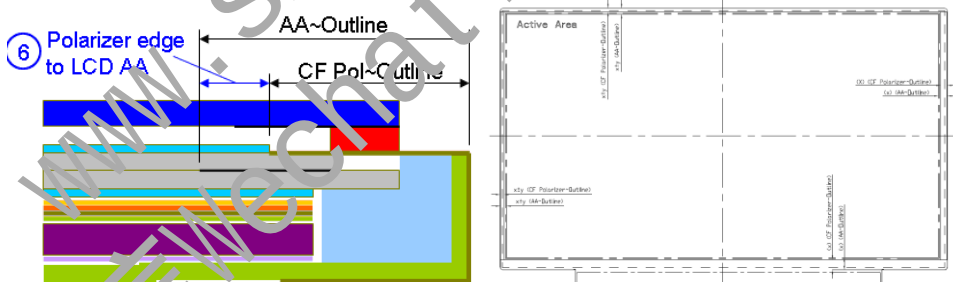
PRODUCT SPECIFICATION

1. F step design $\leq 0.3\text{mm}$ 2. If F step $> 0.3\text{mm}$, slop edge design is needed to prevent panel crack.	
Definition	The F step design on C Cover less than or equal to 0.3mm is recommended. If F step exceeds 0.3mm, the slop edge design is necessary to prevent panel crack.
11	Assembly SOP examination for system front-cover with Hook design
Definition	To prevent panel crack during system front-cover assembly process with hook design, it is not recommended to press panel or any location that related directly to the panel.
12	Adhesive Design between panel & bezel
OK • Risk : Bezel Tape Peeling happened in a rework or reassembly process. NG • Risk : Pooling or light leakage due to stress concentration at B-cover opening	
Definition	To prevent panel crack during system front-cover assembly process with double tape design, When system applied adhesive between B-Cover and LCD module, please design a distance 1.00mm between B-Cover's adhesive and CF pol. Do NOT put adhesive on CF pol. Adhesive material need be qualified to prevent from doing damage to cell tape after rework. Adhesive material need be qualified to prevent abnormal noise when hinge swinging test.
13	System front-cover assembly reference with Double tape design

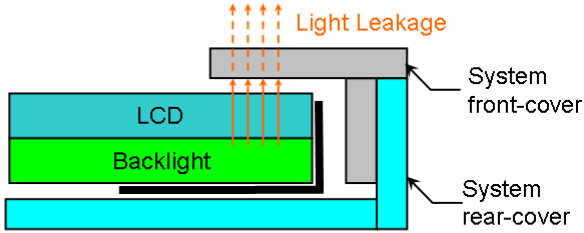
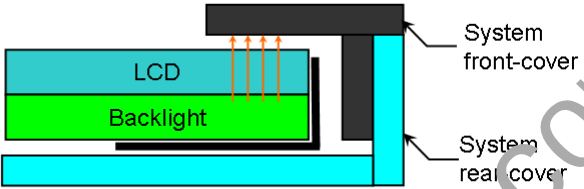
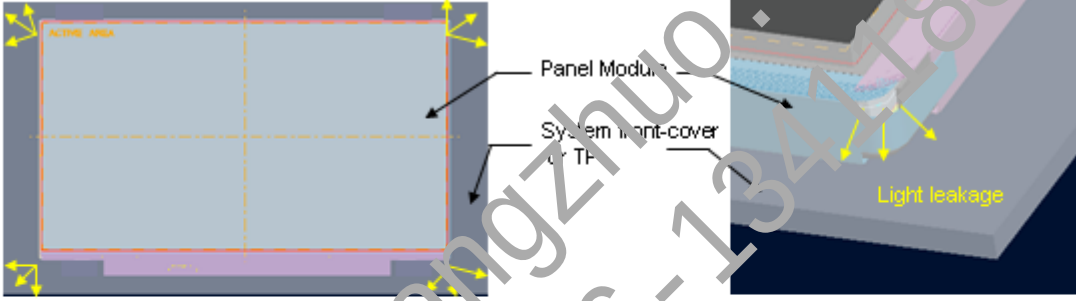
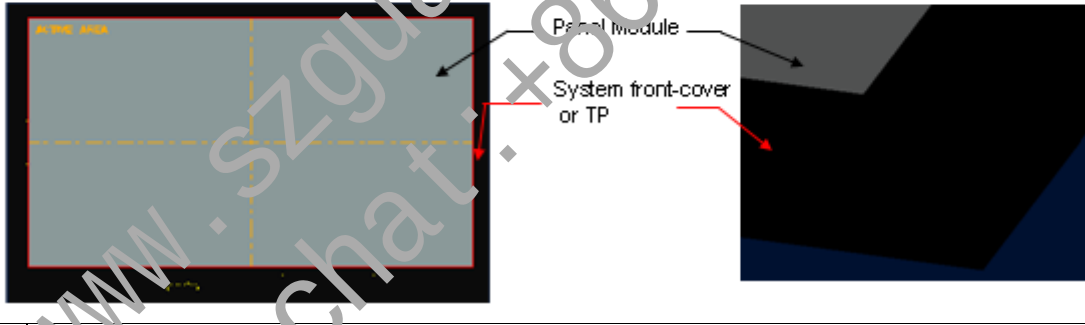
PRODUCT SPECIFICATION

	
Definition	To prevent system front-cover peeling at double tape contact area, A gap between B-Cover & CF-Pol. Is 0.1mm min.
14	System front-cover opening area reference with TFT-LCD module
	
Definition	To prevent panel the noise of B-cover & CF Pol. Distance from CF Pol. edge to front-cover edge more than 0.65mm.

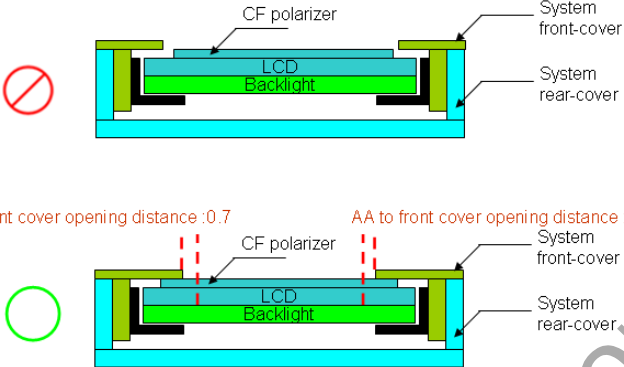
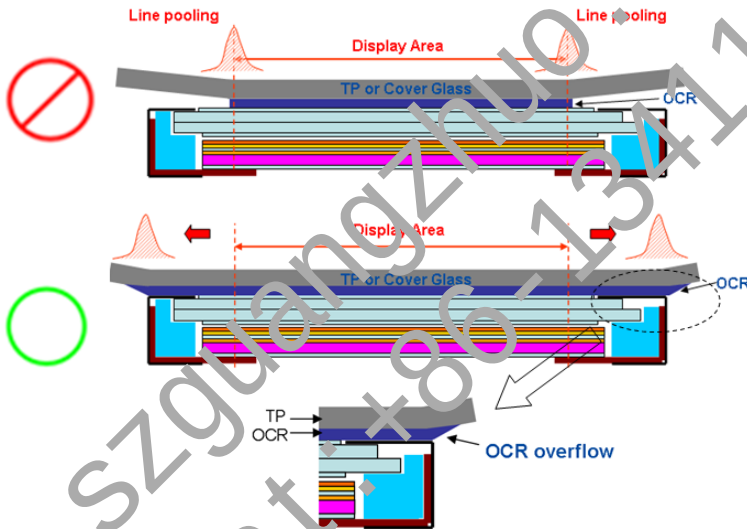
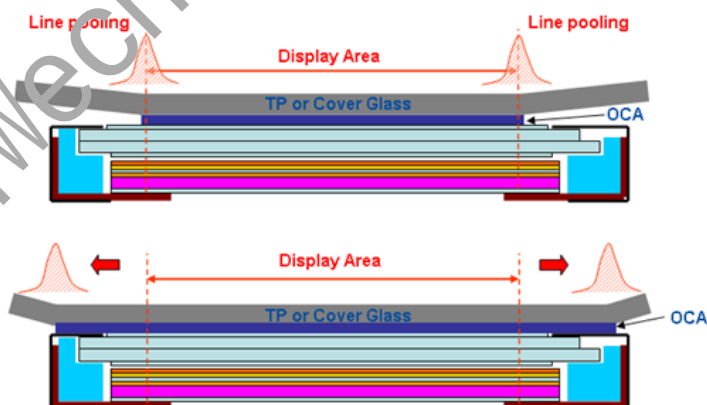
PRODUCT SPECIFICATION

15	Touch Application : TP and LCD Module Combination for White Line Prevention														
	 <table border="1" data-bbox="462 896 1181 1198"> <thead> <tr> <th colspan="2">Parameter consideration for White Line Issue :</th> </tr> </thead> <tbody> <tr><td>1</td><td>TP VA to LCD AA distance</td></tr> <tr><td>2</td><td>TP Assembly tolerance</td></tr> <tr><td>3</td><td>TP Ink Printing tolerance</td></tr> <tr><td>4</td><td>Sponge thickness and tolerance</td></tr> <tr><td>5</td><td>Inspection/Viewing angle specification</td></tr> <tr><td>6</td><td>Polarizer edge to LCD AA distance and tolerance</td></tr> </tbody> </table> Polarizer edge to LCD AA distance can be derived by "AA~Outline" – "CF Pol~Outline" with respect to INX 2D Outline Drawing on each side. 	Parameter consideration for White Line Issue :		1	TP VA to LCD AA distance	2	TP Assembly tolerance	3	TP Ink Printing tolerance	4	Sponge thickness and tolerance	5	Inspection/Viewing angle specification	6	Polarizer edge to LCD AA distance and tolerance
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3	TP Ink Printing tolerance														
4	Sponge thickness and tolerance														
5	Inspection/Viewing angle specification														
6	Polarizer edge to LCD AA distance and tolerance														
Definition	For using in Touch Application: to prevent White Line appears between TP and LCD module combination, the maximum inspection angle location must not fall onto LCD polarizer edge, otherwise light line near edge of polarizer will be appear. Parameters such as TP VA to LCD AA distance, TP assembly tolerance, TP Ink printing tolerance, Sponge thickness and tolerance, and Maximum Inspection/Viewing Angle, must be considered with respect to LCD module's Polarizer edge location and tolerance. This consideration must be taken at all four edges separately. The goal is to find parameters combination that allow maximum inspection angle falls inside polarizer black margin area. Note: Information for Polarizer edge location and its tolerance can be derived from INX 2D Outline Drawing ("AA ~Outline" - "CF Pol~Outline"). Note: Please feel free to contact INX FAE Engineer. By providing value of parameters above on each side, we can help to verify and pass the white line risk assessment for customer reference.														
16	Color of system front-cover material														

PRODUCT SPECIFICATION

	 Light Leakage LCD Backlight System front-cover System rear-cover
	 LCD Backlight System front-cover System rear-cover
	 ACTIVE AREA Panel Module System front-cover or TP Light leakage
	 ACTIVE AREA Panel Module System front-cover or TP
Definition	To prevent light leakage is seen at system front-cover due to material transparency, we suggest using dark color material (black) for system front-cover design.

PRODUCT SPECIFICATION

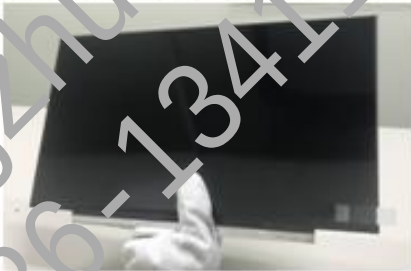
17	AA to front cover opening distance
	
Definition	To prevent CF polarizer edge leakage .We suggest front cover opening no more than 0.7mm larger than active area on all 4 sides.
18	Use OCR Lamination
	
Definition	OCR glue as possible beyond module, in order to avoid Line Pooling
19	Use OCA Lamination
	
Definition	OCA glue as possible plastered throughout the module, in order to avoid Line Pooling.

PRODUCT SPECIFICATION

Appendix. LCD MODULE HANDLING MANUAL

Purpose	- This SOP is prepared to prevent panel dysfunction possibility through incorrect handling procedure. - This manual provides guide in unpacking and handling steps. - Any person which may contact / related with panel, should follow guide stated in this manual to prevent panel loss.
1.	Unpacking
  Open carton  Remove EPE Cushion  Open plastic bag  Cut Adhesive Tape  Remove EPE Cushion	
2.	Panel Lifting
 Remove PET Cover  Remove PE Foam  Handle with care (see next page)  Finger Slot Use slots at both sides for finger insertion. Handle panel upward with care.	

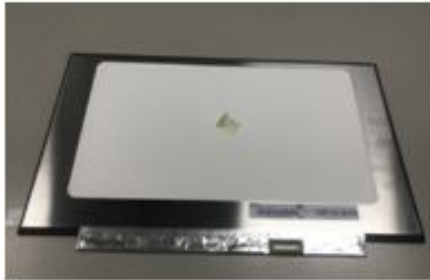
PRODUCT SPECIFICATION

3.	Do and Don't
Do : - Handle with both hands. - Handle panel at left and right edge. 	Don't : - Lifting with one hand.  - Handle at PCBA side. 
Don't : - Stack panels.  - Press panel. 	Don't : - Put foreign stuff onto panel   - Put foreign stuff under panel  

PRODUCT SPECIFICATION

Don't :

- Paste any material unto white reflector sheet



Don't :

- Pull / Push white reflector sheet



Don't :

- Hold at panel corner.



Don't :

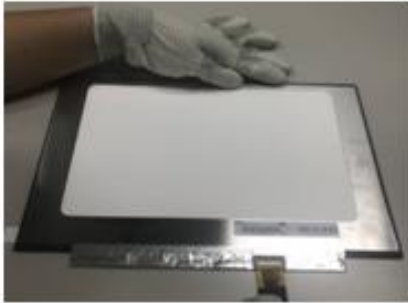
- Twist panel.



PRODUCT SPECIFICATION

Do :

- Hold panel at top edge while inserting connector.



Don't :

- Press white reflector sheet while inserting connector.



Do :

- Remove panel protector film starts from pull tape



Don't :

- Remove panel protector film from film another side.



PRODUCT SPECIFICATION

Do:

- Remove panel protector



Don't:

- Remove panel protector



Don't :

- Touch or Press PCBA Area.

