**Doc. Number:**

☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

# MODEL NO.: N140HCN-E5B
# H/W:C3

**Customer: HP**

**APPROVED BY SIGNATURE**

**Name / Title**
Note

Please return 1 copy for your confirmation with your signature and comments.

| Approved By | Checked By | Prepared By |
|---|---|---|
| 許君逖 | 何銘杰 | 李佩嬬 |

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## REVISION HISTORY

| Version | Date | Page | Description |
|---|---|---|---|
| 3.0 | Dec. 10, 2021 | All | Spec Ver.3.0 was first issued. |

# 1. GENERAL DESCRIPTION

## 1.1 OVERVIEW

N140HCN-E5B is a 14.0“ diagonal TFT Liquid Crystal Display module with LED Backlight unit and 40 pins eDP interface. This module supports 1920 x 1080 FHD and can display 262,144 colors.

## 1.2 GENERAL SPECIFICATIONS

| LCD TFT Module + TP Module Combination | | | |
|---|---|---|---|
| Item | Specification | Unit | Note |
| Luminance, White | 250 | Cd/m2 | - |
| Surface Hardness | Hard coating (3H), Anti-Glare | - | - |
| Color Gamma | 45% | NTSC | - |
| Thickness | 3.00 max (W/O PCB), 5.00 max. (With PCB) | mm | - |
| LCD TFT Module | | | |
| Driver Element | a-si TFT active matrix | - | - |
| Pixel Arrangement | RGB vertical stripe | - | - |
| Pixel Number | 1920 x R.G.B. x 1080 | pixel | -- |
| Pixel Pitch | 0.1611 (H) x 0.1611 (V) | mm | - |
| Display Colors | 262,144 | color | - |
| Interface | eDP 1.2 | - | (3) |
| Transmissive Mode | Normally Black | - | - |
| Power Consumption | Total 3.465 W (Max.)@cell 0.693 W (Max.), BL 2.772 W (Max.) | - | (1) |
| Special Function | G-Sync DD (Not support)<br>G-Sync nVSR (Not support)<br>Free-sync (Not support)<br>PSR (Not support) | - | - |
| TP Module | | | |
| Item | Specification | Unit | Note |
| Number of Channels | 40 x 70 | - | - |
| Touch Method | Finger | - | - |
| Numbers of Touch | 10 points | - | - |
| Accuracy | Meet WHLK | mm | - |
| Linearity | Meet WHLK | - | - |
| Reporting rate | Meet WHLK | Hz | - |
| Interface | HID/I2C | - | - |
| Power Consumption | Active mode 0.3W(Max), Idle mode 0.12W(Max) | - | (2) |
| MP Firmware Version | V5913T05W06 | - | - |

Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, fv = 60 Hz, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 ºC, whereas Black pattern is displayed.

Note (2) The active mode is under the conditions at 10 fingers touch.

Note (3) Display port interface signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2 (eDP1.2). There are many optional items described in eDP1.2. If some optional item is requested, please contact us.

## 2. MECHANICAL SPECIFICATIONS

| Item | | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Module Size | Horizontal (H) | 315.51 | 315.81 | 316.11 | mm | (1)(2) |
| | Vertical (V) | 185.77 | 186.07 | 186.37 | mm | |
| | Thickness (T) w/o PCB | - | 2.85 | 3.00 | mm | |
| | Thickness (T) with PCB | - | - | 5.00 | | |
| Active Area | Horizontal | 309.21 | 309.31 | 309.41 | mm | - |
| | Vertical | 173.89 | 173.99 | 174.09 | mm | - |
| Glass Thickness | CF | 0.35 | 0.40 | 0.45 | mm | - |
| | TFT | 0.35 | 0.40 | 0.45 | mm | - |
| Weight | | - | 292 | 300 | g | - |

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Dimensions are measured by caliper

Note (3) Panel thickness is measured with calipers clamping mylar or tape tightly


### 2.1 CONNECTOR TYPE

Please refer Appendix Outline Drawing for detail design.

Connector Part No.: IPEX-20455-040E-76

User's connector Part No: IPEX-20453-040T-03

## 3. ABSOLUTE MAXIMUM RATINGS of ENVIRONMENT

### 3.1 ABSOLUTE RATINGS OF ENVIRONMENT

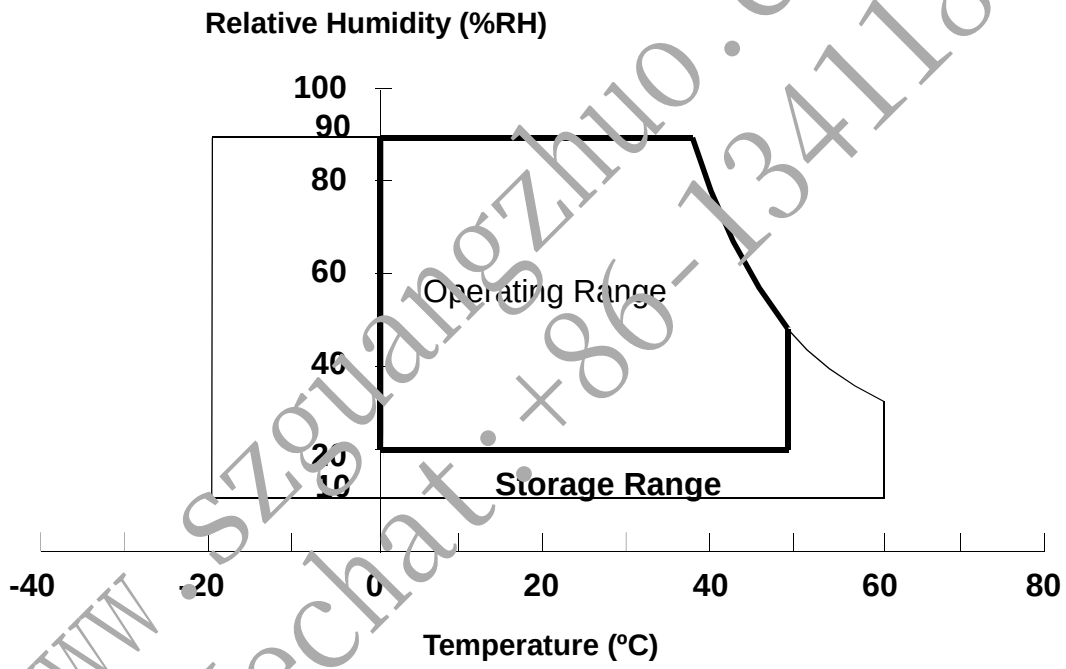
| Item | Symbol | Value | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Storage Temperature | $T_{ST}$ | -20 | +60 | ºC | (1) |
| Operating Ambient Temperature | $T_{OP}$ | 0 | +50 | ºC | (1), (2) |

Note (1) (a) 90 %RH Max. (Ta < 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max.

(c) No condensation.

Note (2) The temperature of panel surface should be 0 ºC min. and 60 ºC max.



# 4. OPTICAL CHARACTERISTICS

## 4.1 TEST CONDITIONS

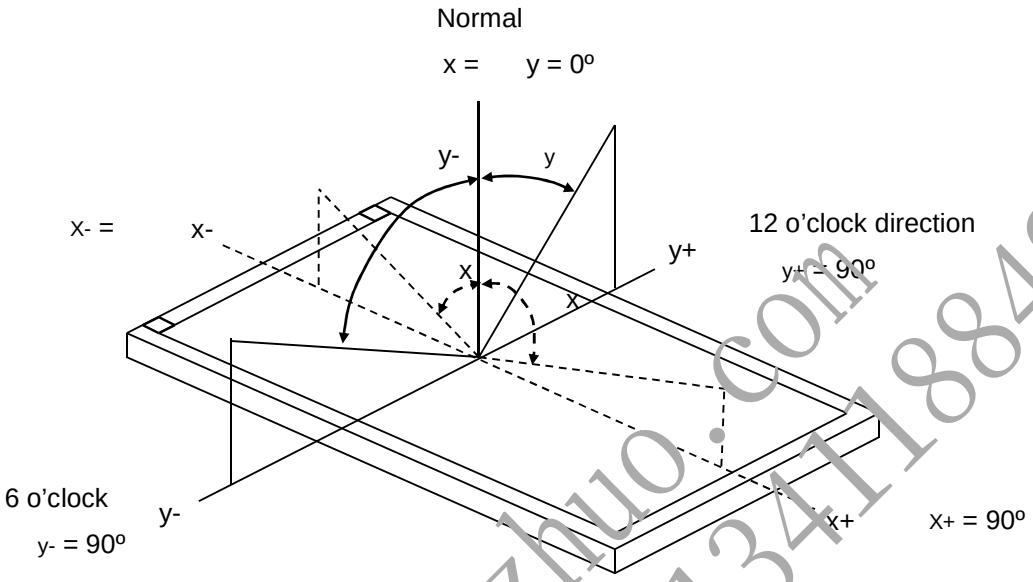
| Item | Symbol | Value | Unit |
|---|---|---|---|
| Ambient Temperature | Ta | 25±2 | °C |
| Ambient Humidity | Ha | 50±10 | %RH |
| Supply Voltage | $V_{CC}$ | 3.3 | V |
| Input Signal | According to typical value in "3. ELECTRICAL CHARACTERISTICS" | | |
| LED Light Bar Input Current | $I_L$ | 46.2 | mA |

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

## 4.2 OPTICAL SPECIFICATIONS

| Item | | Symbol | Condition | Min. | Typ | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| Contrast Ratio | | CR | $\theta_x$=0°, $\theta_Y$ =0° Viewing Normal Angle | 800 | 1000 | - | - | (2), (5) (7) |
| Response Time | | $T_R$ | | - | 14 | 16 | ms | (3), (7) |
| | | $T_F$ | | - | 11 | 14 | ms | |
| Average Luminance of White | | $L_{AVE}$ | | 212 | 250 | - | cd/m² | (4), (6) ,(7) |
| Color Chromaticity | Red | Rx | | Typ – 0.03 | 0.590 | Typ + 0.03 | - | (1),(7) |
| | | Ry | | | 0.350 | | - | |
| | Green | Gx | | | 0.330 | | - | |
| | | Gy | | | 0.555 | | - | |
| | Blue | Bx | | | 0.153 | | - | |
| | | By | | | 0.119 | | - | |
| | White | Wx | | | 0.313 | | - | |
| | | Wy | | | 0.329 | | - | |
| Viewing Angle | Horizontal | $\theta_x$+ | CR≥10 | 80 | 89 | - | Deg. | (1),(5), (7) |
| | | $\theta_x$- | | 80 | 89 | - | | |
| | Vertical | $\theta_Y$+ | | 80 | 89 | - | | |
| | | $\theta_Y$- | | 80 | 89 | - | | |
| White Variation of 5 Points | | $\delta W_{5p}$ | $\theta_x$=0°, $\theta_Y$ =0° | - | - | 1.25 | - | (5),(6), (7) |
| White Variation of 13 Points | | $\delta W_{13p}$ | θx=0°, θY =0° | - | 1.4 | 1.54 | - | (5),(6), (7) |

Note (1) Definition of Viewing Angle (θx, θy):




Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

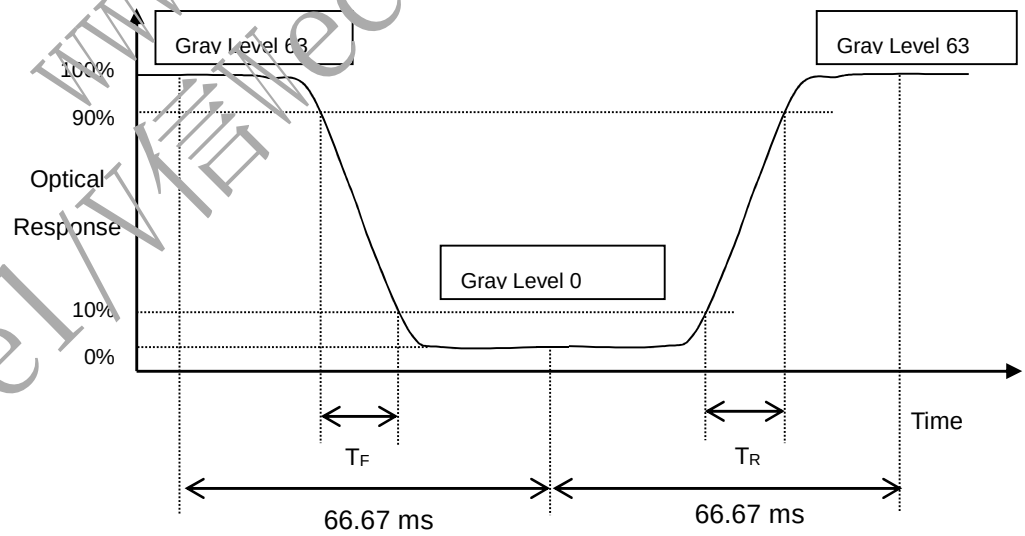
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time ($T_R$, $T_F$):




Note (4) Definition of Average Luminance of White ($L_{AVE}$):

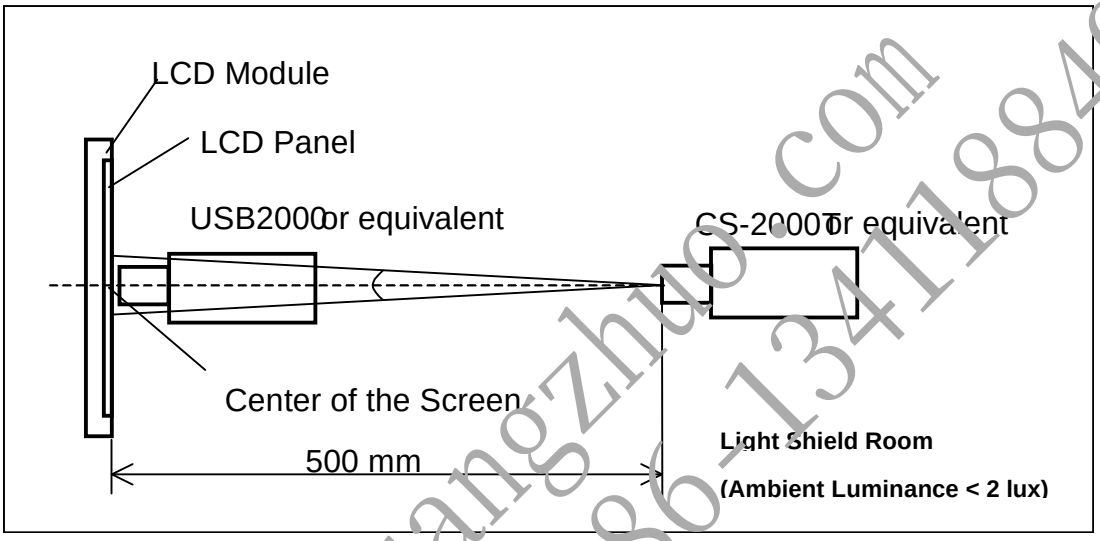
Measure the luminance of gray level 63 at 5 points

$L_{AVE}$ = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

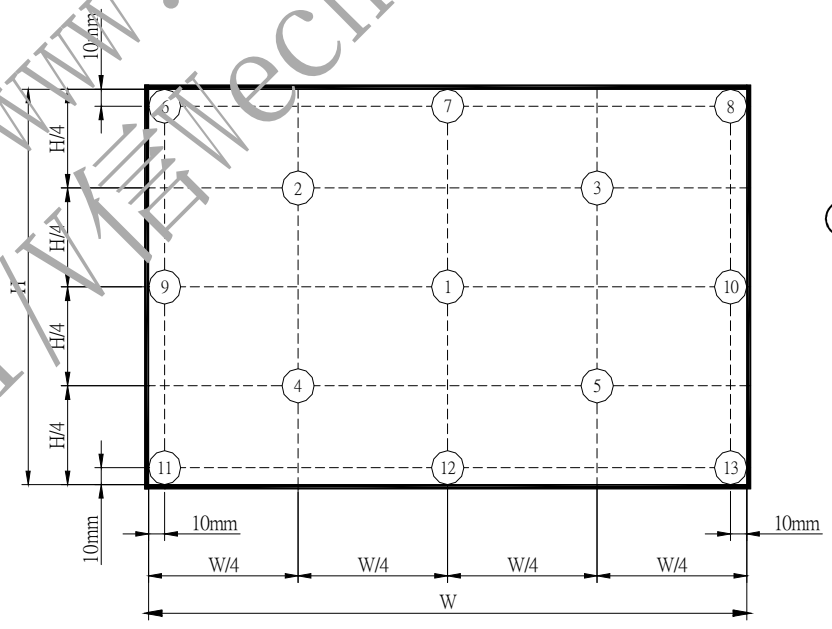



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

$\delta W_{5p}$ = { Maximum [L (1)~ L (5)] / Minimum [L (1)~ L (5)]}*100%

$\delta W_{13p}$ = {Maximum [L (1) ~ L (13)] / Minimum [L (1) ~ L (13)]} *100%




X : Test Point

X=1 to 13

Active area

Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of

the specifications after long-term operation will not be warranted.

## 5. RELIABILITY TEST ITEM

| Test Item | Test Condition | Note |
|---|---|---|
| High Temperature Storage Test | 60ºC, 240 hours | (1) (2) |
| Low Temperature Storage Test | -20ºC, 240 hours | |
| Thermal Shock Storage Test | -20ºC, 0.5hour←→60℃, 0.5hour; 100cycles, 1hour/cycle | |
| High Temperature Operation Test | 50ºC, 240 hours | |
| Low Temperature Operation Test | 0ºC, 240 hours | |
| High Temperature & High Humidity Operation Test | 50ºC, RH 80%, 240hours | |
| ESD Test (Operation) | 150pF, 330Ω, 1sec/cycle<br>Condition 1 : Contact Discharge, ±8KV<br>Condition 2 : Air Discharge, ±15KV | (1) |
| Shock (Non-Operating) | 220G, 2ms, half sine wave 1 time for each direction of ±X,±Y,±Z | (1)(3) |
| Vibration (Non-Operating) | 1.5G, 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z | (1)(3) |

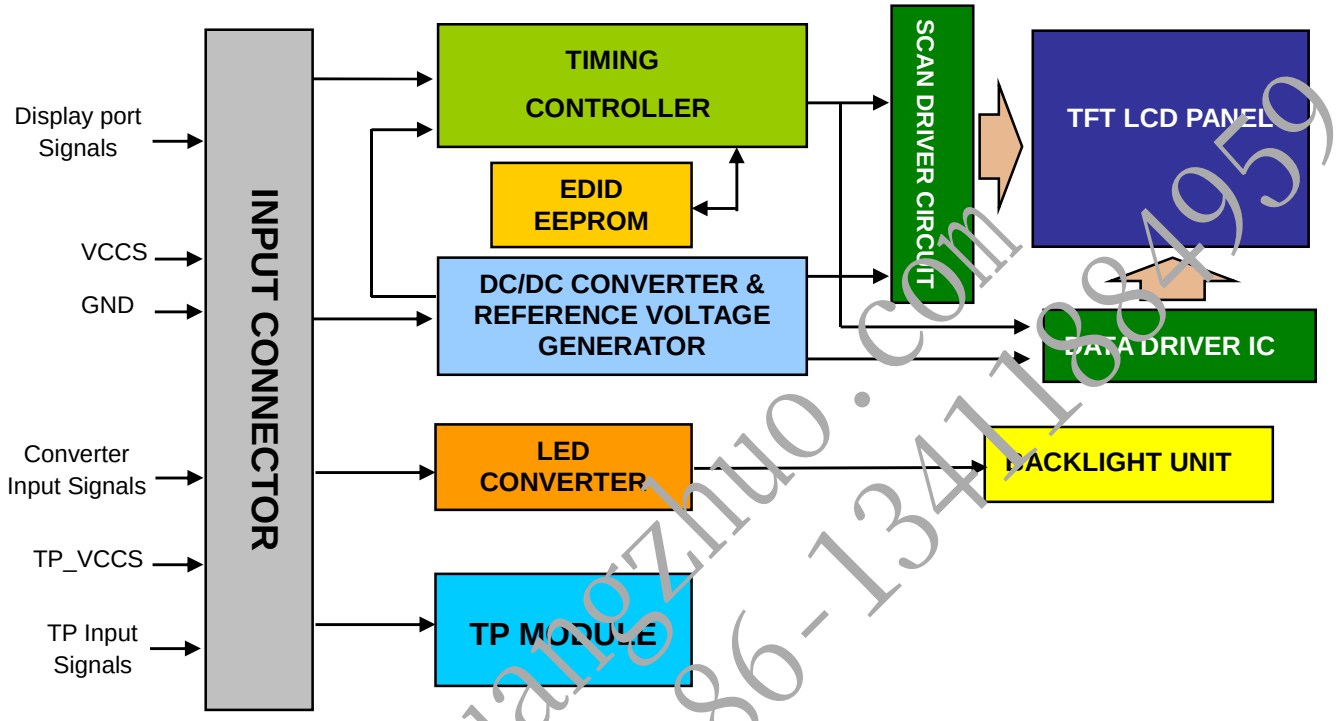
Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture

# 6. ELECTRICAL SPECIFICATIONS

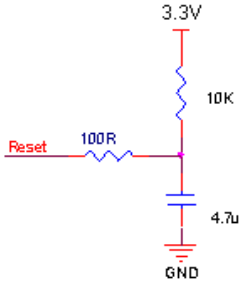
## 6.1 FUNCTION BLOCK DIAGRAM



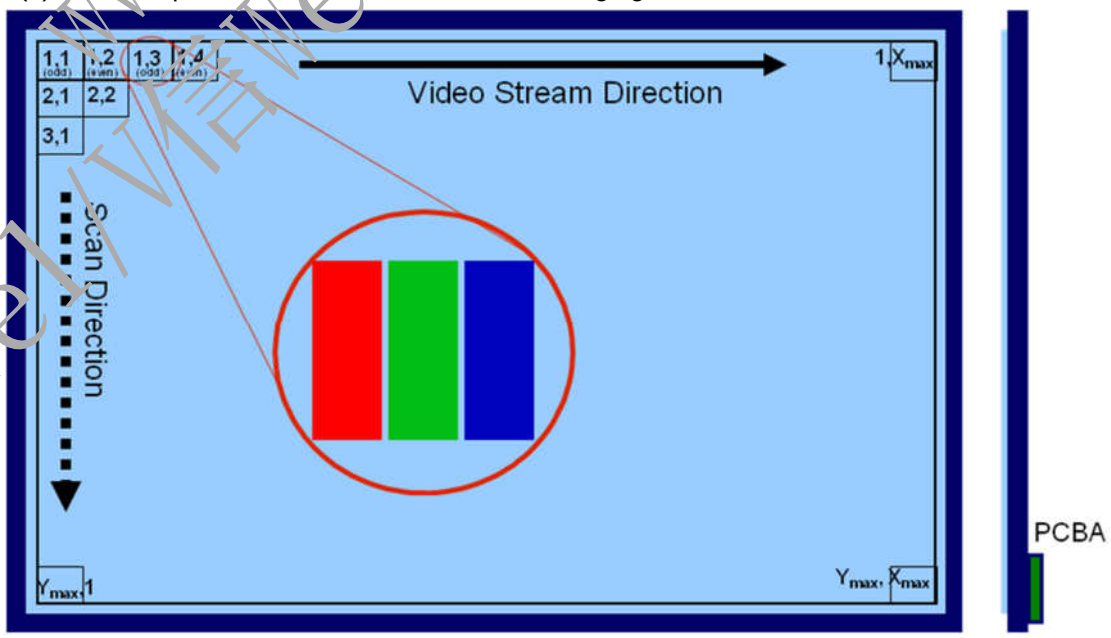

## 6.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

| Pin | Symbol | Description | Remark |
|---|---|---|---|
| 1 | NC | No Connection (Reserved for LCD test) | - |
| 2 | H_GND | High Speed Ground | - |
| 3 | Lane1_N | Complement Signal Link Lane 1 | - |
| 4 | Lane1_P | True Signal Link Lane 1 | - |
| 5 | H_GND | High Speed Ground | - |
| 6 | Lane0_N | Complement Signal Link Lane 0 | - |
| 7 | Lane0_P | True Signal Link Lane 0 | - |
| 8 | H_GND | High Speed Ground | - |
| 9 | AUX_CH_P | True Signal Auxiliary Channel | - |
| 10 | AUX_CH_N | Complement Signal Auxiliary Channel | - |
| 11 | H_GND | High Speed Ground | - |
| 12 | VCCS | LCD logic and driver power | - |
| 13 | VCCS | LCD logic and driver power | - |
| 14 | NC | No Connection (Reserved for LCD test) | - |
| 15 | GND | LCD logic and driver ground | - |
| 16 | GND | LCD logic and driver ground | - |
| 17 | HPD | HPD signal pin | - |
| 18 | BL_GND | Backlight ground | - |
| 19 | BL_GND | Backlight ground | - |
| 20 | BL_GND | Backlight ground | - |

| | | | |
|---|---|---|---|
| 21 | BL_GND | Backlight ground | - |
| 22 | LED_EN | Backlight on /off | - |
| 23 | LED_PWM | System PWM signal input for dimming | - |
| 24 | NC | No Connection (Reserved for LCD test) | - |
| 25 | NC | No Connection (Reserved for LCD test) | - |
| 26 | LED_VCCS | Backlight power | - |
| 27 | LED_VCCS | Backlight power | - |
| 28 | LED_VCCS | Backlight power | - |
| 29 | LED_VCCS | Backlight power | - |
| 30 | NC | No Connection (Reserved for LCD test) | - |
| 31 | NC | No Connection | - |
| 32 | NC | No Connection | - |
| 33 | TP_VSS | Ground for Touch panel | - |
| 34 | TP_VCCS | Power Supply for Touch panel | Typical 3.3V |
| 35 | TP_VCCS | Power Supply for Touch panel | Typical 3.3V |
| 36 | TP_RS | Touch panel report switch (High: Enable, Low: Disable) | Input,<br>Pull high 10Kohm |
| 37 | TP_SCL | I2C Clock for Touch | Open Drain,<br>Pull high 2.2Kohm |
| 38 | TP_SDA | I2C Data for Touch | Open Drain,<br>Pull high 2.2Kohm |
| 39 | TP_INT | Interrupt for Touch | Output,<br>Pull high 10Kohm |
| 40 | TP_Reset | Reset signal for Touch panel (High: Normal, Low: Reset) |  |

Note (1) The first pixel is odd as shown in the following figure.



# 7. LCD MODULE ELECTRICAL SPECIFICATIONS

## 7.1.1 LCD ELECTRICAL ABSOLUTE RATINGS

| Item | Symbol | Value | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Power Supply Voltage | VCCS | -0.3 | +4.0 | V | (1) |
| Logic Input Voltage | $V_{IN}$ | -0.3 | VCCS+0.3 | V | |
| Converter Input Voltage | LED_VCCS | -0.3 | 26 | V | (1) |
| Converter Control Signal Voltage | LED_PWM, | -0.3 | 5 | V | (1) |
| Converter Control Signal Voltage | LED_EN | -0.3 | 5 | V | (1) |

Note (1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “LCD ELETRONICS SPECIFICATION”

## 7.1.2 LCD ELETRONICS SPECIFICATION

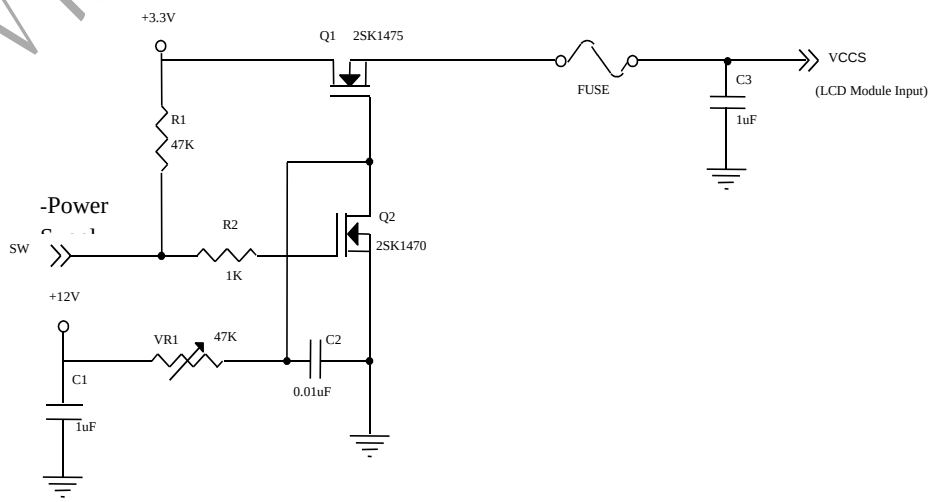
| Parameter | | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Power Supply Voltage | | VCCS | 3.0 | 3.3 | 3.6 | V | (1) |
| Ripple Voltage | | $V_{RP}$ | - | - | 100 | mV | (1) |
| Inrush Current | | $I_{RUSH}$ | - | - | 1.5 | A | (1),(2) |
| Power Supply Current | Mosaic | Icc | - | 180 | 210 | mA | (3)a |
| | White | | - | 170 | 190 | mA | (3) |
| | Solid Pattern | | - | 323 | 356 | mA | (3)b |
| HPD Impedance | | $R_{HPD}$ | 30K | - | - | ohm | (4) |
| HPD | High Level | - | 2.25 | - | 3.6 | V | (5) |
| | Low Level | - | 0 | - | 0.8 | V | (5) |
| Power per EBL WG | | $P_{EBL}$ | - | 1.358 | - | W | (6) |

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

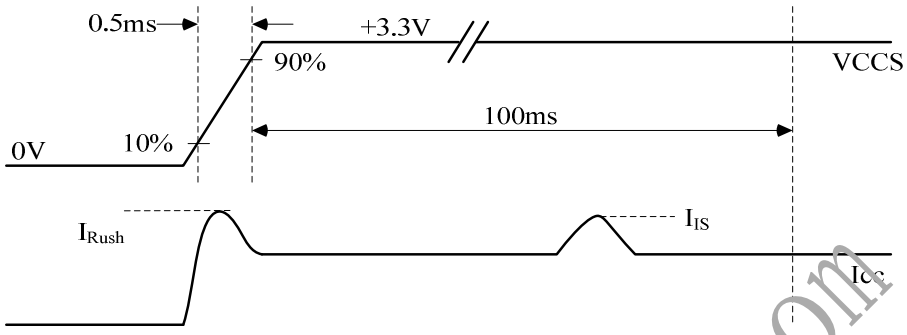
Note (2) $I_{RUSH}$: the maximum current when VCCS is rising

$I_{IS}$: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.

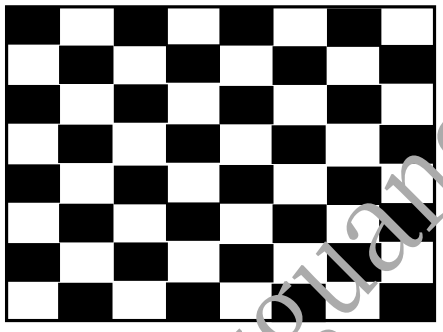


**VCCS rising time is 0.5ms**




Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 °C, DC Current and $f_v$ = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern



Active Area

b. The solid pattern is the largest one of R/G/B pattern.

Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. Please refer to Note (4) of 7.1.3 LED CONVERTER SPECIFICATION to obtain more information.

Note (5) When a source detects a low-going HPD pulse longer than 2ms in duration, it must be regarded as a hot-plug-event HPD pulse. Upon detecting this hot-plug-event HPD pulse, the source must read the receiver capability field and link / sink status field of the DPCD and take corrective action

Note (6) The specified power are the sum of LCD panel electronics input power and the converter input power. Test conditions are as follows.

(a) VCCS = 3.3 V, Ta = 25 ± 2 °C, $f_v$ = 60 Hz,

(b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file “Flat Panel Display Monitor Setup Patterns”, FPDMSU.ppt.

(c) Luminance: 60 nits.

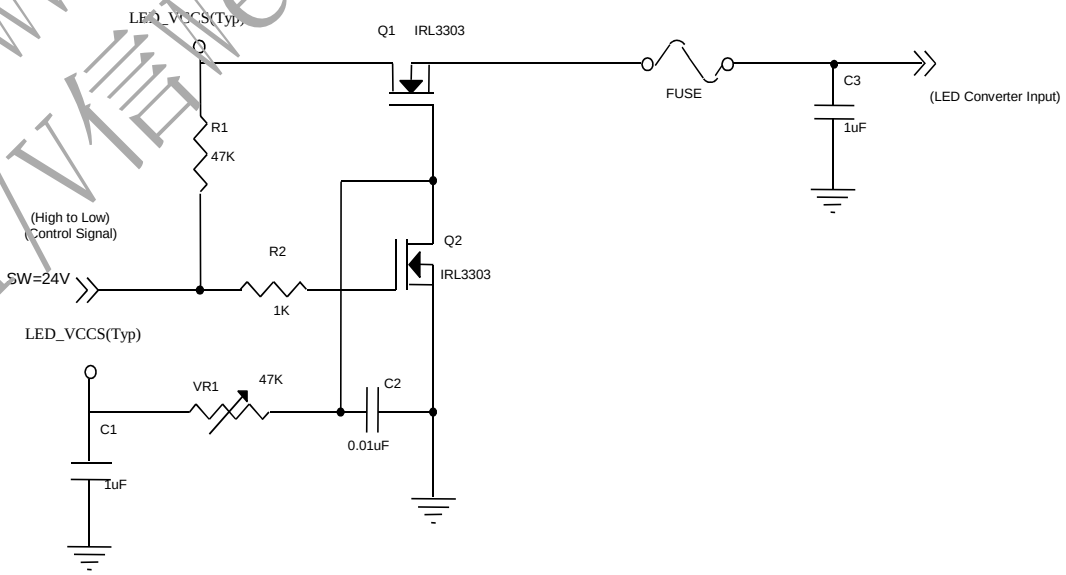
### 7.1.3 LED CONVERTER SPECIFICATION

| Parameter | | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Converter Input Power Supply Voltage | | LED_Vccs | 5.0 | 12.0 | 21.0 | V | - |
| Converter Inrush Current | | $ILED_{RUSH}$ | - | - | 1.5 | A | (1) |
| LED_EN Control Level | Backlight On | - | 2.2 | - | 5.0 | V | (4) |
| | Backlight Off | | 0 | - | 0.6 | V | (4) |
| LED_EN Impedance | | $R_{LED\_EN}$ | 30K | - | - | ohm | (4) |
| PWM Control Level | PWM High Level | - | 2.2 | - | 5 | V | (4) |
| | PWM Low Level | | 0 | - | 0.6 | V | (4) |
| PWM Impedance | | $R_{PWM}$ | 30K | - | - | ohm | (4) |
| PWM Control Duty Ratio | | - | 5 | - | 100 | % | (5) |
| PWM Control Permissive Ripple Voltage | | $V_{PWM\_pp}$ | - | - | 100 | mV | - |
| PWM Control Frequency | | $f_{PWM}$ | 190 | - | 2K | Hz | (2) |
| LED Power Current | LED_VCCS=Typ | ILED | 187 | 216 | 231 | mA | (3) |

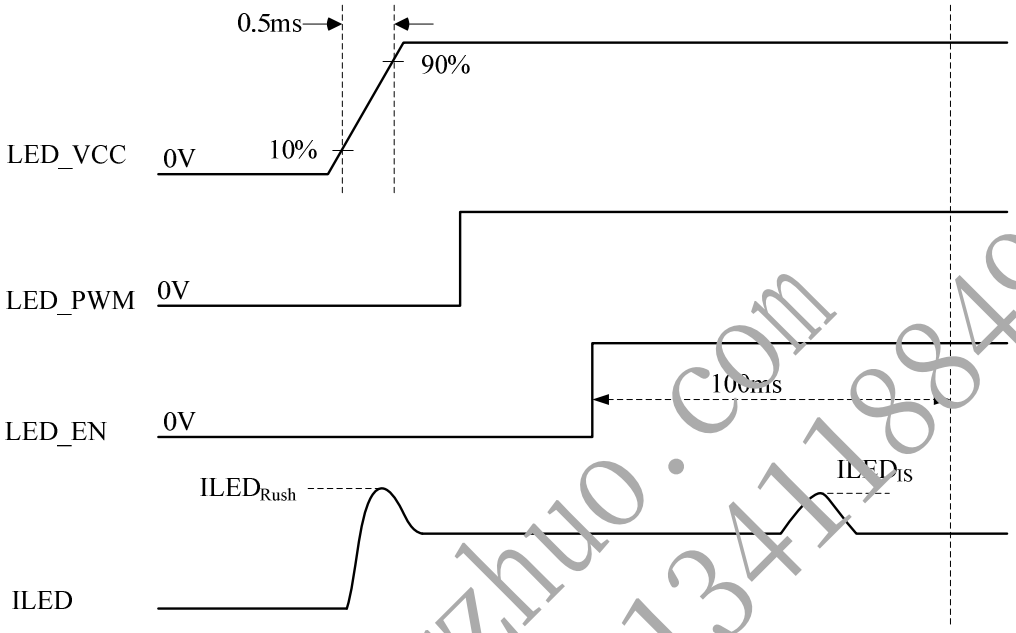
Note (1) $ILED_{RUSH}$: the maximum current when LED_VCCS is rising,

$ILED_{IS}$: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 ºC, $f_{PWM}$ = 200 Hz, Duty=100%.



**VLED rising time is 0.5ms**




Note (2) If PWM control frequency is applied in the range less than 1KHz, the "waterfall" phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency, $f_{PWM}$ should be in the range

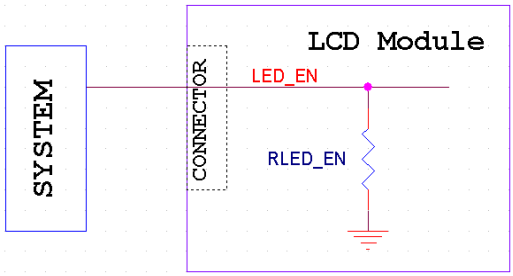
$$(N+0.33)*f \le f_{PWM} \le (N+0.66)*f$$

$N$ : Integer $(N \ge 3)$

$f$ : Frame rate

Note (3) The specified LED power supply current is under the conditions at "LED_VCCS = Typ.", Ta = 25 ± 2°C, $f_{PWM}$ = 200 Hz, Duty=100%.

Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. For example, the figure below describes the equivalent pull down impedance of LED_EN (If it exists). The rest pull down impedances of other signals (eg. HPD, PWM …) are in the same concept.



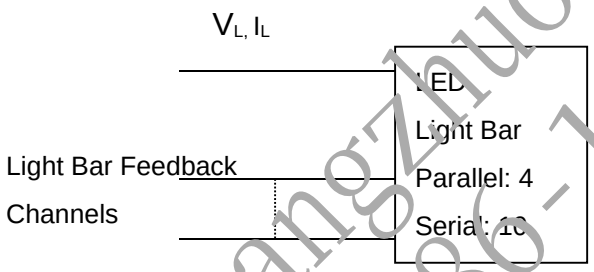

Note (5) If the cycle-to-cycle difference of PWM duty exceeds 0.1%, especially when the PWM duty is low, slight brightness change might be observed.

## 7.2 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

| Parameter | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| LED Light Bar Power Supply Voltage | $V_L$ | 27 | 28.5 | 30 | V | (1)(2)(Duty100%) |
| LED Light Bar Power Supply Current | $I_L$ | - | 76.8 | - | mA | |
| Power Consumption | $P_L$ | - | 2.188 | 2.736 | W | (3) |
| LED Life Time | $L_{BL}$ | 15000 | - | - | Hrs | (4) |

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :




Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 oC and $I_L$ = 19.2 mA(Per EA) until the brightness becomes ≦ 50% of its original value

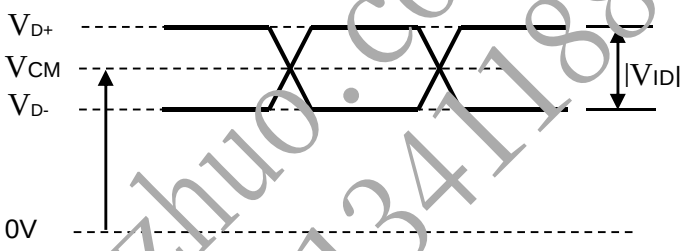
## 7.3 DISPLAY PORT SIGNAL TIMING SPECIFICATION

### 7.3.1 DISPLAY PORT INTERFACE

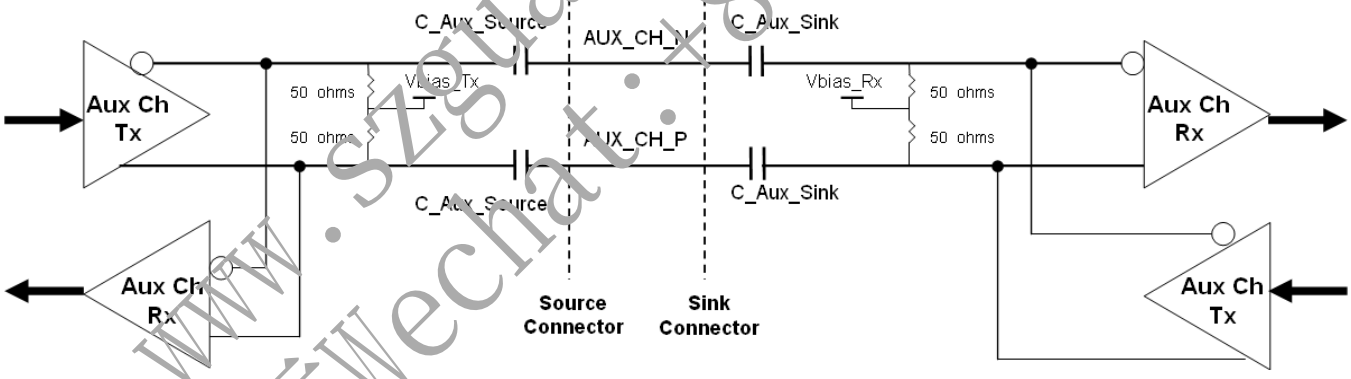
| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Differential Signal Common Mode Voltage(MainLink and AUX) | VCM | 0 | - | 2 | V | (1)(4) |
| AUX AC Coupling Capacitor | C_Aux_Source | 75 | - | 200 | nF | (2) |
| Main Link AC Coupling Capacitor | C_ML_Source | 75 | - | 200 | nF | (3) |

Note (1)Display port interface related AC coupled signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2. There are many optional items described in eDP1.2. If some optional item is requested, please contact us.

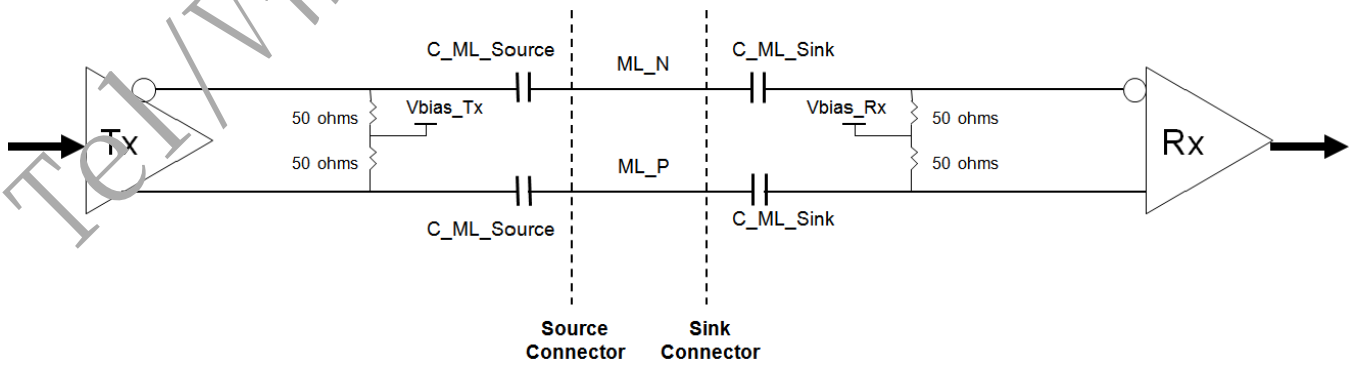
**Single Ended**




((2) Recommended eDP AUX Channel topology is as below and the AUX AC Coupling Capacitor (C_Aux_Source) should be placed on the source device.




(3) Recommended Main Link Channel topology is as below and the Main Link AC Coupling Capacitor (C_ML_Source) should be placed on the source device.




(4) The source device should pass the test criteria described in DisplayPortCompliance Test Specification (CTS) 1.1.

## 7.3 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

**Refresh Rate 60Hz**

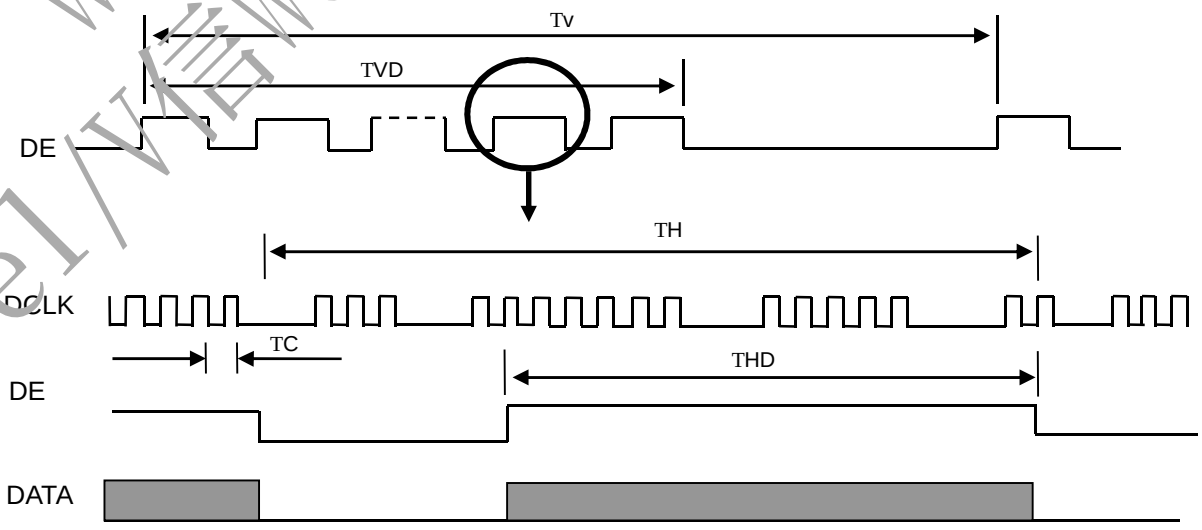
| Signal | Item | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| DCLK | Frequency | 1/Tc | 144.3 | 145.0 | 145.7 | MHz | - |
| DE | Vertical Total Time | TV | 1120 | 1124 | 1128 | TH | - |
| | Vertical Active Display Period | TVD | 1080 | 1080 | 1080 | TH | - |
| | Vertical Active Blanking Period | TVB | TV-TVD | 44 | TV-TVD | TH | - |
| | Horizontal Total Time | TH | 2230 | 2250 | 2270 | Tc | - |
| | Horizontal Active Display Period | THD | 1920 | 1920 | 1920 | Tc | - |
| | Horizontal Active Blanking Period | THB | TH-THD | 330 | TH-THD | Tc | - |

**Refresh rate 40Hz (Power Saving Mode)**

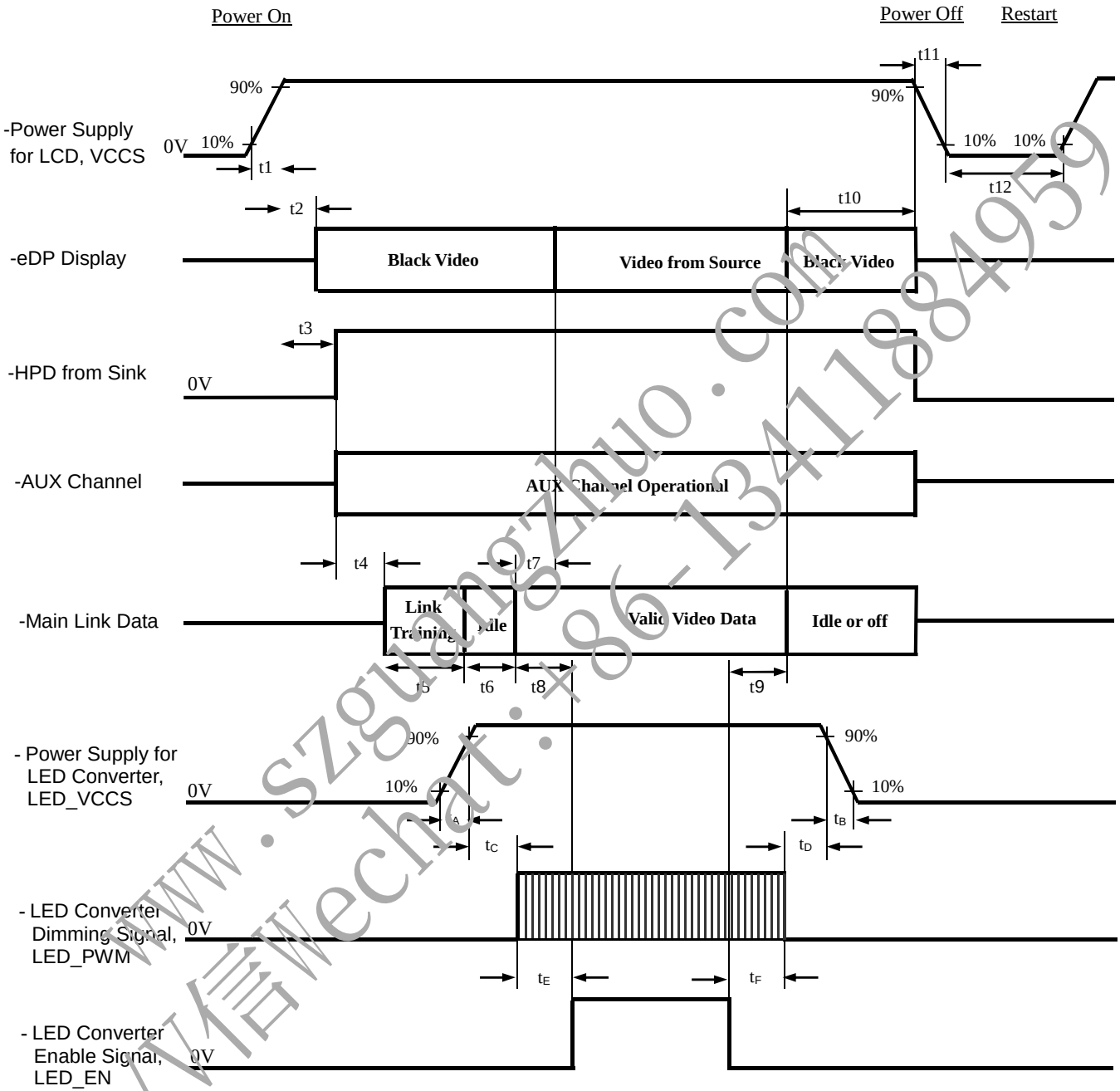
| Signal | Item | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| DCLK | Frequency | 1/Tc | 98.2 | 98.67 | 99.1 | MHz | (1) |
| DE | Vertical Total Time | TV | 1120 | 1124 | 1128 | TH | (1) |
| | Vertical Active Display Period | TVD | 1080 | 1080 | 1080 | TH | (1) |
| | Vertical Active Blanking Period | TVB | TV-TVD | 44 | TV-TVD | TH | (1) |
| | Horizontal Total Time | TH | 2230 | 2250 | 2270 | Tc | (1) |
| | Horizontal Active Display Period | THD | 1920 | 1920 | 1920 | Tc | (1) |
| | Horizontal Active Blanking Period | THB | TH-THD | 330 | TH-THD | Tc | (1) |

Note (1) The panel can operate at 60Hz normal mode and power saving mode, respectively. All reliability tests are based on specific timing of 60Hz refresh rate. We can only assure the panel's electrical function at power saving mode.

**INPUT SIGNAL TIMING DIAGRAM**



## 7.4 POWER ON/OFF SEQUENCE



Timing Specifications:

| Parameter | Description | Reqd. By | Value | | Unit | Notes |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| t1 | Power rail rise time, 10% to 90% | Source | 0.5 | 10 | ms | - |
| t2 | Delay from LCD,VCCS to black video generation | Sink | 0 | 200 | ms | Automatic Black Video generation prevents display noise until valid video data is received from the Source (see Notes:2 and 3 below) |
| t3 | Delay from LCD,VCCS to HPD high | Sink | 0 | 200 | ms | Sink AUX Channel must be operational upon HPD high (see Note:4 below ) |
| t4 | Delay from HPD high to link training initialization | Source | 0 | - | ms | Allows for Source to read Link capability and initialize |
| t5 | Link training duration | Source | 0 | - | ms | Dependant on Source link training protocol |
| t6 | Link idle | Source | 0 | - | ms | Min Accounts for required BS-Idle pattern. Max allows for Source frame synchronization |
| t7 | Delay from valid video data from Source to video on display | Sink | 0 | 50 | ms | Max value allows for Sink to validate video data and timing. At the end of T7, Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and Sink will no longer generate automatic Black Video |
| t8 | Delay from valid video data from Source to backlight on | Source | 80 | - | ms | Source must assure display video is stable<br>*: Recommended by INX. To avoid garbage image. |
| t9 | Delay from backlight off to end of valid video data | Source | 50 | - | ms | Source must assure backlight is no longer illuminated. At the end of T9, Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and Sink will automatically display Black Video. (See Notes: 2 and 3 below)<br>*: Recommended by INX. To avoid garbage image. |
| t10 | Delay from end of valid video data from Source to power off | Source | 0 | 500 | ms | Black video will be displayed after receiving idle or off signals from Source |
| t11 | VCCS power rail fall time, 90% to 10% | Source | 0.5 | 10 | ms | - |

| | | | | | | |
|---|---|---|---|---|---|---|
| t12 | VCCS Power off time | Source | 500 | - | ms | - |
| $t_A$ | LED power rail rise time, 10% to 90% | Source | 0.5 | 10 | ms | - |
| $t_B$ | LED power rail fall time, 90% to 10% | Source | 0 | 10 | ms | - |
| $t_C$ | Delay from LED power rising to LED dimming signal | Source | 1 | - | ms | - |
| $t_D$ | Delay from LED dimming signal to LED power falling | Source | 1 | - | ms | - |
| $t_E$ | Delay from LED dimming signal to LED enable signal | Source | 0 | - | ms | - |
| $t_F$ | Delay from LED enable signal to LED dimming signal | Source | 0 | - | ms | - |

Note (1) Please don't plug or unplug the interface cable when system is turned on. Before LCD_VCCS and LED_VCCS are ready, it is recommended to pull down the backlight control signals

Note (2) The Sink must include the ability to automatically generate Black Video autonomously. The Sink must automatically enable Black Video under the following conditions:

- Upon LCDVCC power-on (within T2 max)
- When the "NoVideoStream_Flag" (VB-ID Bit 3) is received from the Source (at the end of T9)

Note (3) The Sink may implement the ability to disable the automatic Black Video function, as described in Note (2), above, for system development and debugging purposes.

Note (4) The Sink must support AUX Channel polling by the Source immediately following LCDVCC power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to response to an AUX Channel transaction with the time specified within T3 max.

# 8. TP MODULE ELECTRICAL CHARACTERISTICS

## 8.1 TP MODULE ELECTRICAL ABSOLUTE RATINGS

| Item | Symbol | Value | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Voltage from TP_VCCS to AGND and DGND | TP_VCCS | - | 3.6 | V | - |
| Logic Input Voltage | - | - | 3.6 | V | |

## 8.2 TP MODULE ELECTRICAL CHARACTERISTICS

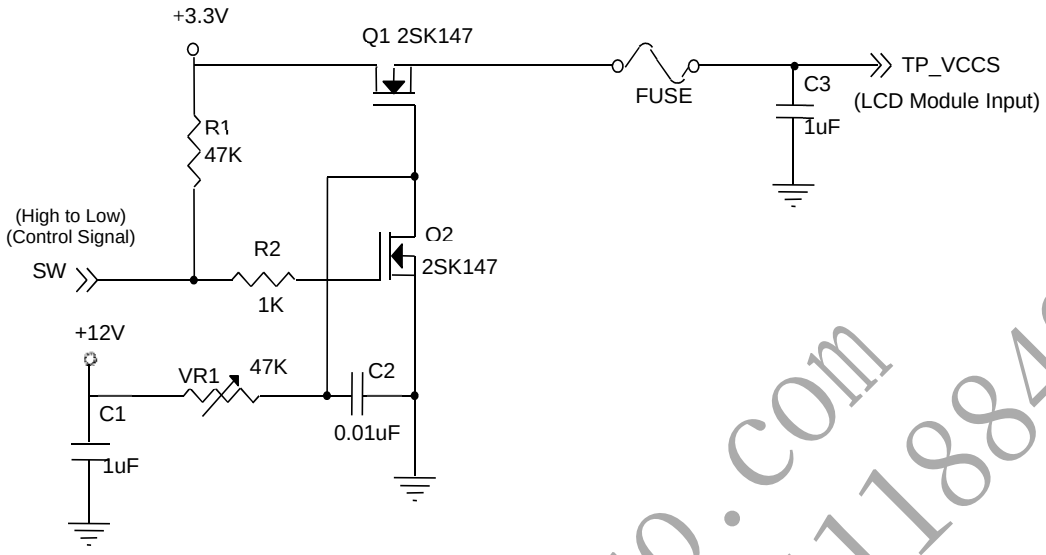
| Parameter | | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Power Supply Voltage | | TP_VCCS | 3.0 | 3.3 | 3.6 | V | (1) |
| Ripple Voltage | | $TP\_V_{RP}$ | - | - | 100 | mV | (1) |
| Inrush Current | | $TP\_I_{RUSH}$ | - | - | 1.1 | A | (1),(2) |
| Power Supply Current | Active Mode | $TP\_I_{CC}$ | - | - | 90.9 | mA | - |
| | Idle Mode | | - | - | 36.3 | mA | - |
| TP_RESET | Normal | - | 2.5 | - | TP_VCCS | V | (3) |
| | Active | | 0 | - | 0.5 | V | (3) |
| TP_RS | RS High Level | - | 2.5 | - | TP_VCCS | V | - |
| | RS Low Level | | 0 | - | 0.5 | V | - |
| I2C Signal (SCL, SDA) | High Level | SCL, SDA | 2.7 | - | TP_VCCS | V | - |
| | Low Level | | 0 | - | 0.4 | V | |

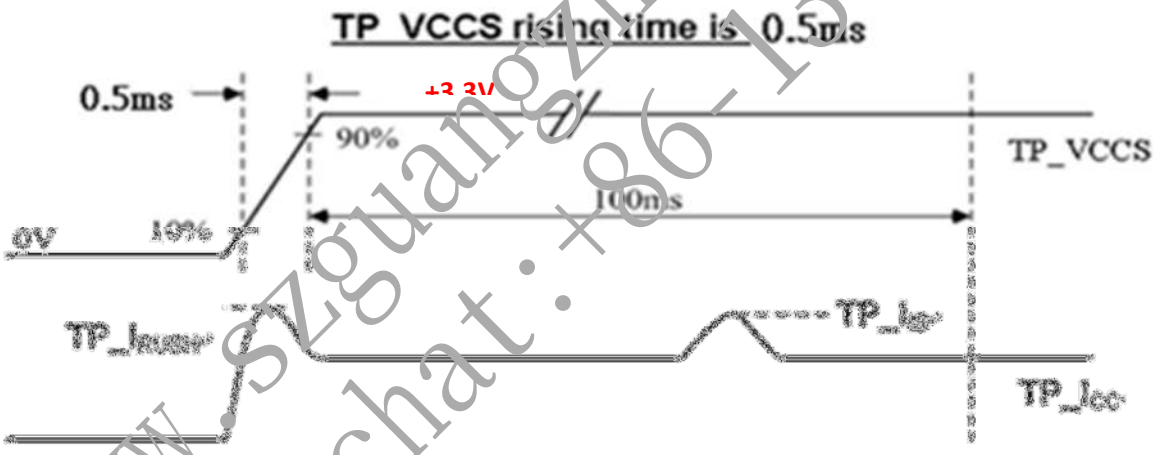
Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

Note (2) $TP\_I_{RUSH}$: the maximum current when TP_VCCS is rising

$TP\_I_{IS}$: the maximum current of the first 100ms after power-on

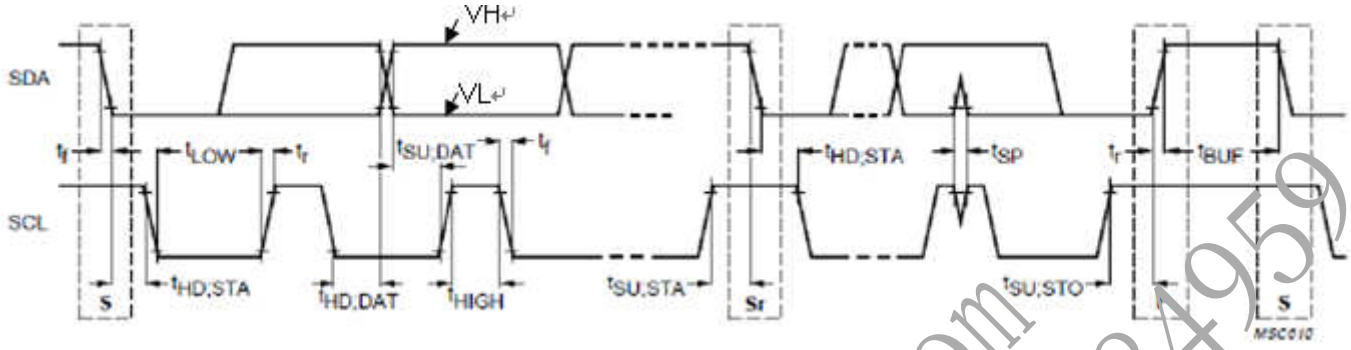
Measurement Conditions: Shown as the following figure. Test pattern: white



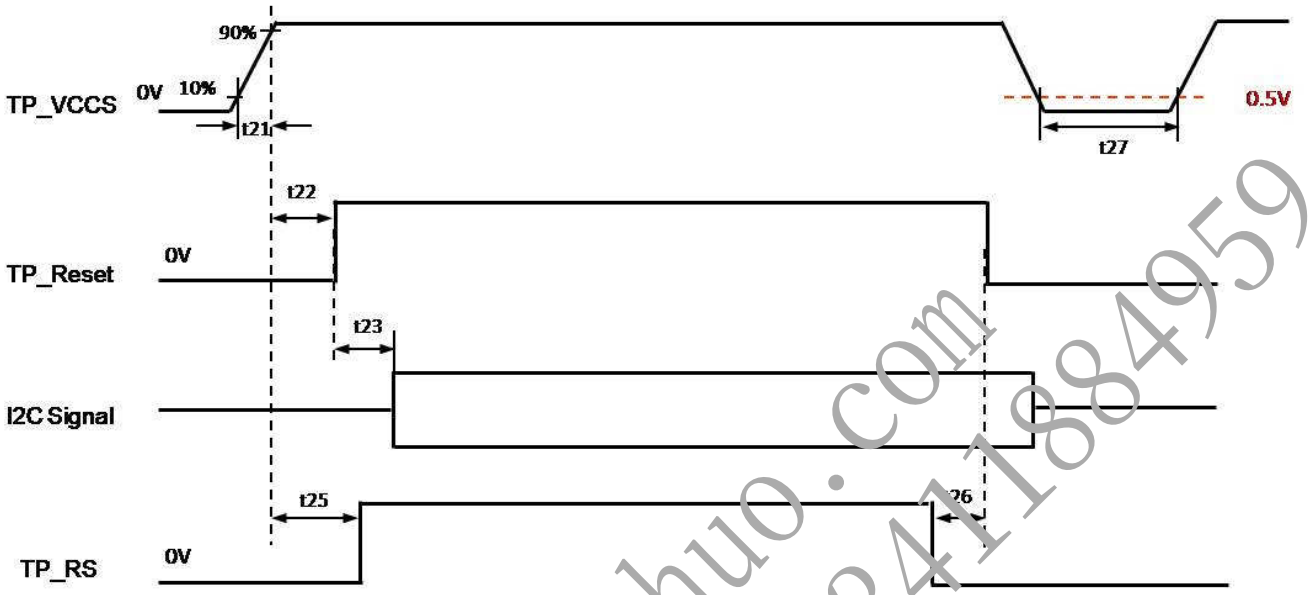

Note (3) TP_RESET is a Schmitt Trigger input.

### 8.3 I2C AC ELECTRICAL CHARACTERISTICS




| Signal | | Description | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| INT | VL,LH | Low level voltage | NONE | NONE | 0.4 | V |
| | | High level voltage | 2.7 | NONE | NONE | V |
| SCL | VL,VH | Low level voltage | NONE | NONE | 0.4 | V |
| | | High level voltage | 2.7 | NONE | NONE | V |
| | Freq | Clock frequency (Max spec) | 0 | NONE | 400 | KHZ |
| | T_low | Low period clock | 1.3 | NONE | NONE | us |
| | T_high | High period clock | 0.6 | NONE | NONE | us |
| | Tr | Rise time | 20 | NONE | 300 | ns |
| | Tf | Fall time | 20 | NONE | 300 | ns |
| SDA | VL,VH | Low level voltage | NONE | NONE | 0.4 | V |
| | | High level voltage | 2.7 | NONE | NONE | V |
| | Tr | Rise time | 20 | NONE | 300 | ns |
| | Tf | Fall time | 20 | NONE | 300 | ns |
| Bus lines | tHD_STA | Hold time START | 0.6 | NONE | NONE | us |
| | tHD_DAT | Data hold time | 0.2 | NONE | NONE | us |
| | tSU_DAT | Data set-up time | 100 | NONE | NONE | ns |
| | tSU_STO | Set-up time for STOP | 0.6 | NONE | NONE | us |
| | tSU_Sr | Set-up time for START repeated (Sr) | 0.6 | NONE | NONE | us |
| | tHD_Sr | Hold time for START repeated (Sr) | 0.6 | NONE | NONE | us |
| | tBUF | BUS free time | 1.3 | NONE | NONE | us |

## 8.4 TP MODULE POWER ON/OFF SEQUENCE




Timing Specifications:

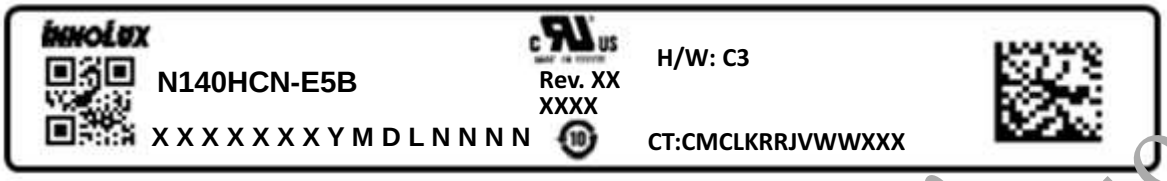
| Parameter | Description | Value | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $t_{21}$ | TP_VCCS rail rise time, 10% to 90% | 0.5 | - | ms | - |
| $t_{22}$ | Delay from TP_VCCS to TP_Reset | 5 | - | ms | - |
| $t_{23}$ | Delay from TP_Reset to I2C Signal | 20 | - | ms | (1) |
| $t_{25}$ | Delay from TP_VCCS to TP_RS | 20 | - | ms | - |
| $t_{26}$ | Delay from TP_RS to TP_Reset | 2 | - | ms | - |
| $t_{27}$ | TP_VCCS power off duration | 500 | - | ms | - |

Note (1) It represents touch device is able to response ACK for host only. And it is recommended for host to do enumeration when t23 > 300ms

# 9. PACKING

## 9.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation

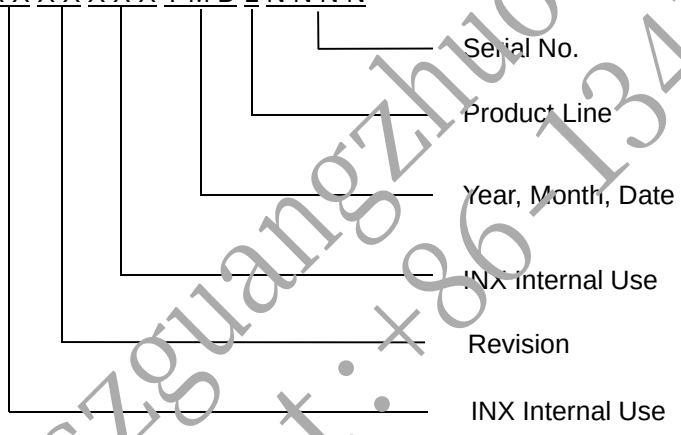



.

(a) Model Name: N140HCN–E5B

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X X X X X X Y M D L N N N N




Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2020~2029

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

CT: Label

| S/N | CT: CMCLKRRJVWWXXX |
|---|---|
| CT: | Title |
| C | LCD Display Module |
| MCLK | Assembly Code |
| RR | Revision |
| JV | Supplier /Site of MFG |
| WW | Week/Year of MFG |
| XXX | Serial number. From 000000 to 999999 |

## 9.2 CARTON

(1)Box Dimensions : 435(L)*350(W)*320(H)
(2)20 Module/Carton

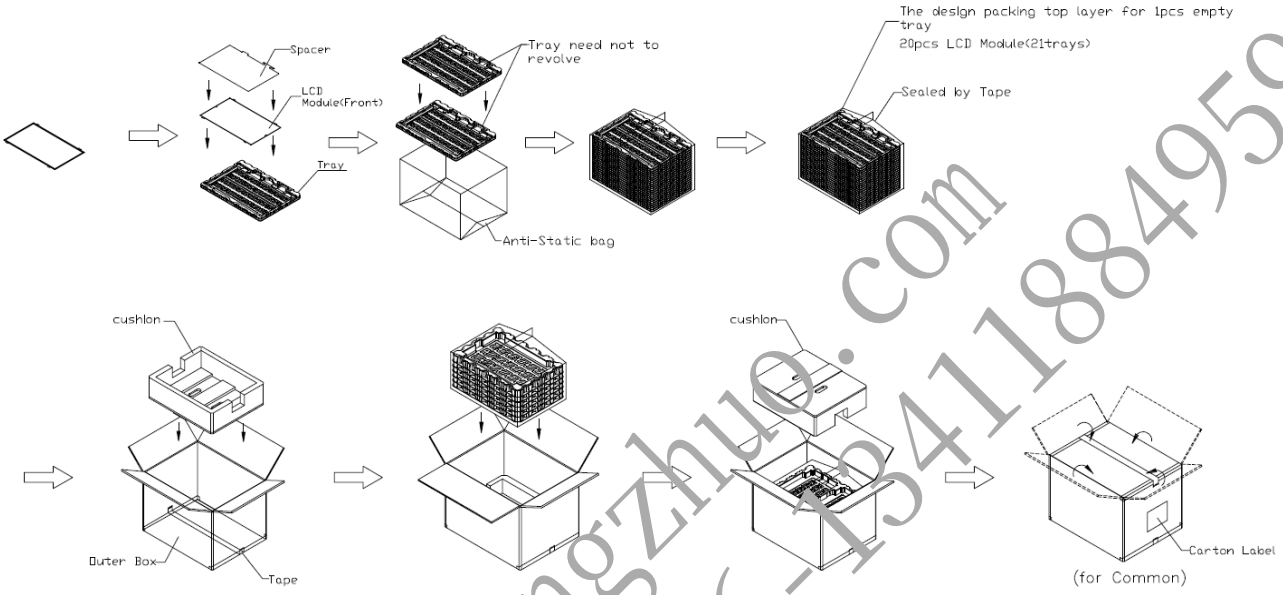



Figure 9-2 Packing method

## 9.3 PALLET

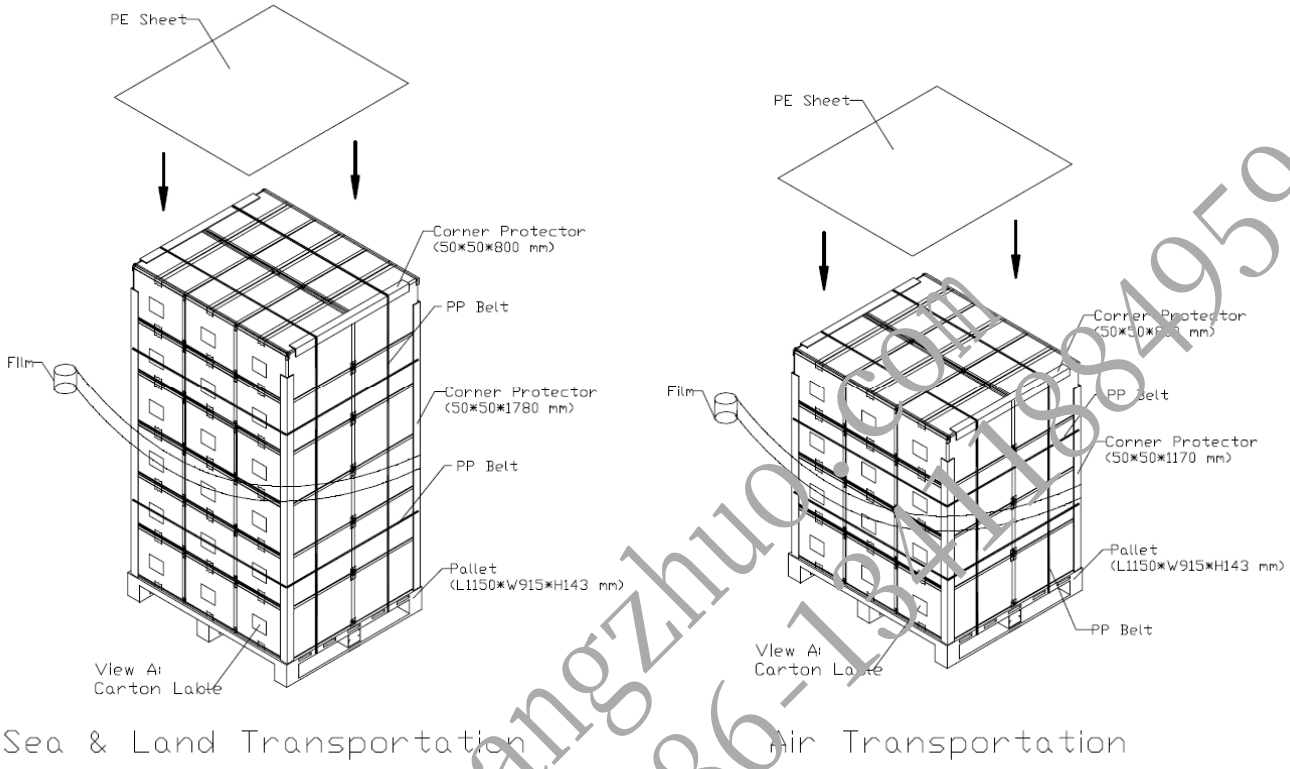



Figure. 9-3 Packing method

## 9.4 UN-PACK METHOD

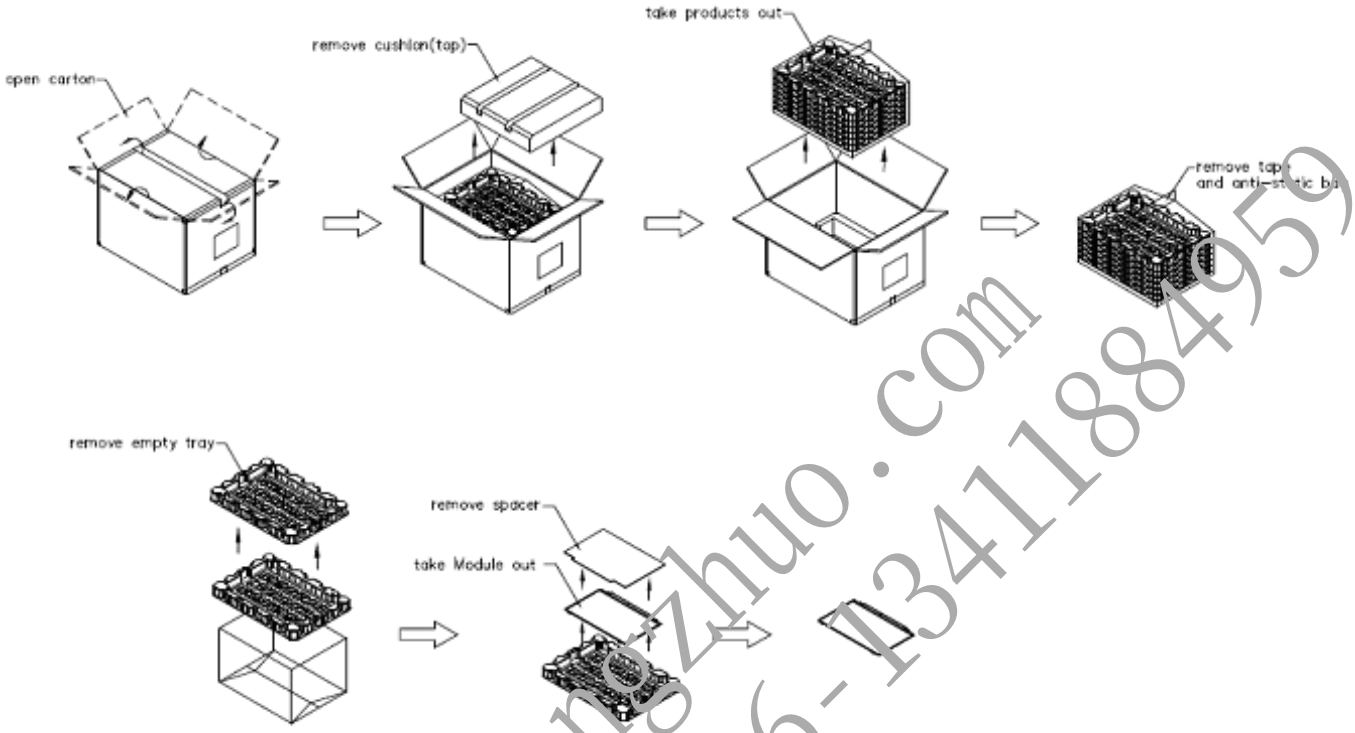



Figure. 9-4 Un-Packing method

# 10. PRECAUTIONS

## 10.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

## 10.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

## 10.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

## Appendix. EDID DATA STRUCTURE

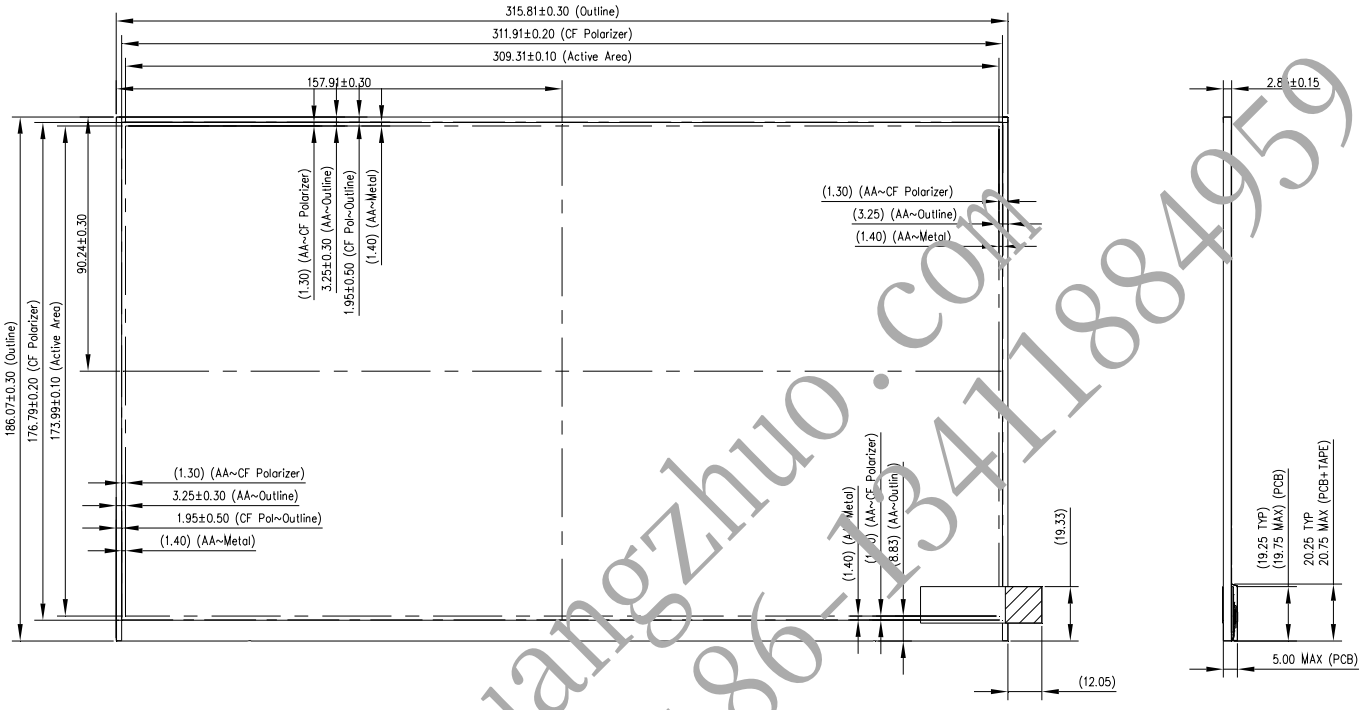
The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

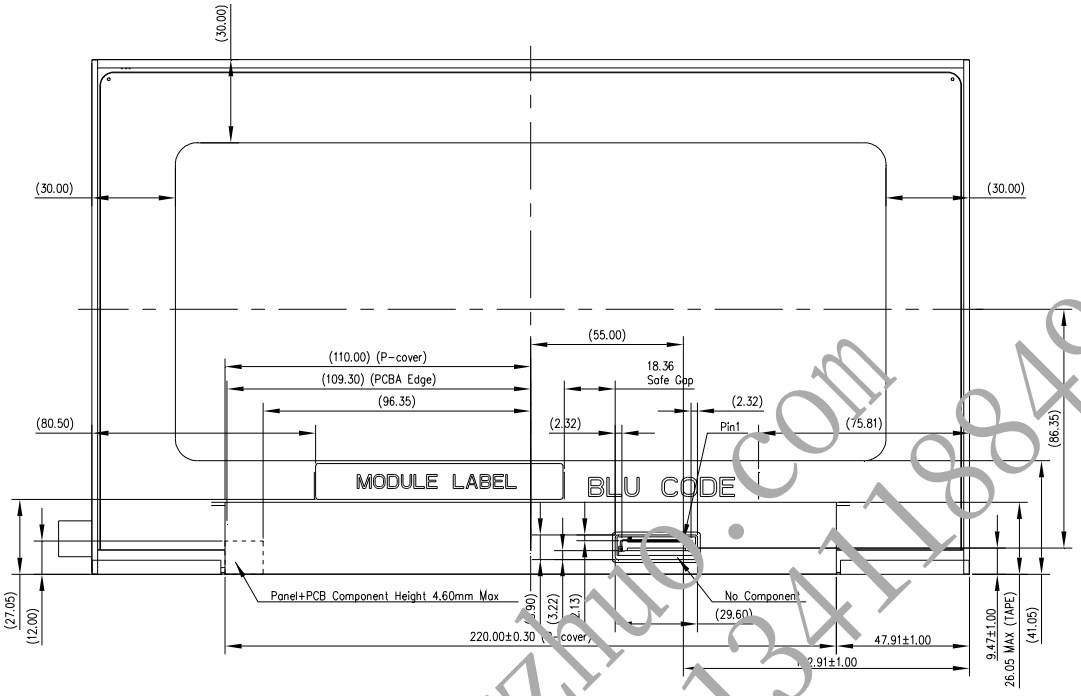
| Byte # (decimal) | Byte # (hex) | Field Name and Comments | Value (hex) | Value (binary) |
|---|---|---|---|---|
| 0 | 00 | Header | 00 | 00000000 |
| 1 | 01 | Header | FF | 11111111 |
| 2 | 02 | Header | FF | 11111111 |
| 3 | 03 | Header | FF | 11111111 |
| 4 | 04 | Header | FF | 11111111 |
| 5 | 05 | Header | FF | 11111111 |
| 6 | 06 | Header | FF | 11111111 |
| 7 | 07 | Header | 00 | 00000000 |
| 8 | 08 | EISA ID manufacturer name ("CMN") | 0D | 00001101 |
| 9 | 09 | EISA ID manufacturer name | AE | 10101110 |
| 10 | 0A | ID product code (LSB) | 3D | 00111101 |
| 11 | 0B | ID product code (MSB) | 14 | 00010100 |
| 12 | 0C | ID S/N (fixed "0") | 00 | 00000000 |
| 13 | 0D | ID S/N (fixed "0") | 00 | 00000000 |
| 14 | 0E | ID S/N (fixed "0") | 00 | 00000000 |
| 15 | 0F | ID S/N (fixed "0") | 00 | 00000000 |
| 16 | 10 | Week of manufacture (fixed week code) | 16 | 00010110 |
| 17 | 11 | Year of manufacture (fixed year code) | 1F | 00011111 |
| 18 | 12 | EDID structure version ("1") | 01 | 00000001 |
| 19 | 13 | EDID revision ("4") | 04 | 00000100 |
| 20 | 14 | Video I/P definition ("Digital") | 95 | 10010101 |
| 21 | 15 | Active area horizontal ("30.931cm") | 1F | 00011111 |
| 22 | 16 | Active area vertical ("17.399cm") | 11 | 00010001 |
| 23 | 17 | Display Gamma (Gamma = "2.2") | 78 | 01111000 |
| 24 | 18 | Feature support ("RGB, Continous") | 03 | 00000011 |
| 25 | 19 | Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0 | 28 | 00101000 |
| 26 | 1A | Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0 | 65 | 01100101 |
| 27 | 1B | Rx=0.590 | 97 | 10010111 |
| 28 | 1C | Ry=0.350 | 59 | 01011001 |
| 29 | 1D | Gx=0.330 | 54 | 01010100 |
| 30 | 1E | Gy=0.555 | 8E | 10001110 |
| 31 | 1F | Bx=0.153 | 27 | 00100111 |
| 32 | 20 | By=0.119 | 1E | 00011110 |
| 33 | 21 | Wx=0.313 | 50 | 01010000 |
| 34 | 22 | Wy=0.329 | 54 | 01010100 |
| 35 | 23 | Established timings 1 | 00 | 00000000 |
| 36 | 24 | Established timings 2 | 00 | 00000000 |
| 37 | 25 | Manufacturer's reserved timings | 00 | 00000000 |
| 38 | 26 | Standard timing ID # 1 | 01 | 00000001 |
| 39 | 27 | Standard timing ID # 1 | 01 | 00000001 |
| 40 | 28 | Standard timing ID # 2 | 01 | 00000001 |
| 41 | 29 | Standard timing ID # 2 | 01 | 00000001 |

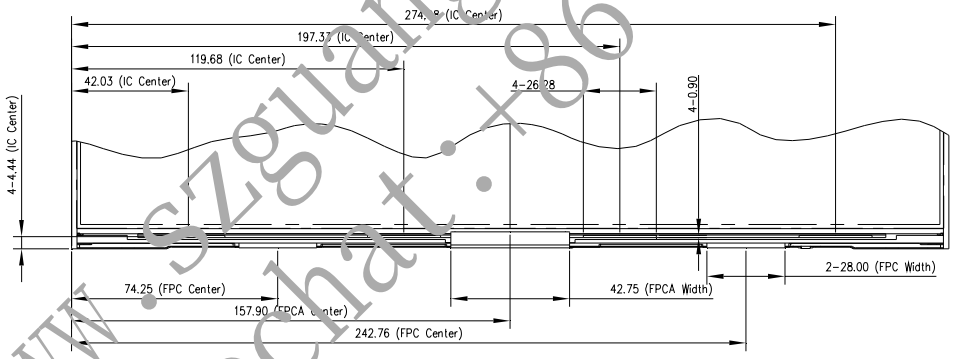
| | | | | |
|---|---|---|---|---|
| 42 | 2A | Standard timing ID # 3 | 01 | 00000001 |
| 43 | 2B | Standard timing ID # 3 | 01 | 00000001 |
| 44 | 2C | Standard timing ID # 4 | 01 | 00000001 |
| 45 | 2D | Standard timing ID # 4 | 01 | 00000001 |
| 46 | 2E | Standard timing ID # 5 | 01 | 00000001 |
| 47 | 2F | Standard timing ID # 5 | 01 | 00000001 |
| 48 | 30 | Standard timing ID # 6 | 01 | 00000001 |
| 49 | 31 | Standard timing ID # 6 | 01 | 00000001 |
| 50 | 32 | Standard timing ID # 7 | 01 | 00000001 |
| 51 | 33 | Standard timing ID # 7 | 01 | 00000001 |
| 52 | 34 | Standard timing ID # 8 | 01 | 00000001 |
| 53 | 35 | Standard timing ID # 8 | 01 | 00000001 |
| 54 | 36 | Detailed timing description # 1 Pixel clock ("145.00MHz") | A4 | 10100100 |
| 55 | 37 | # 1 Pixel clock (hex LSB first) | 38 | 00111000 |
| 56 | 38 | # 1 H active ("1920") | 80 | 10000000 |
| 57 | 39 | # 1 H blank ("230") | E6 | 11100110 |
| 58 | 3A | # 1 H active : H blank | 70 | 01110000 |
| 59 | 3B | # 1 V active ("1080") | 38 | 00111000 |
| 60 | 3C | # 1 V blank ("44") | 2C | 00101100 |
| 61 | 3D | # 1 V active : V blank | 40 | 01000000 |
| 62 | 3E | # 1 H sync offset ("80") | 50 | 01010000 |
| 63 | 3F | # 1 H sync pulse width ("60") | 3C | 00111100 |
| 64 | 40 | # 1 V sync offset : V sync pulse width ("6 : 8") | 68 | 01101000 |
| 65 | 41 | # 1 H sync offset : H sync pulse width : V sync offset : V sync width | 00 | 00000000 |
| 66 | 42 | # 1 H image size (“309 mm“) | 35 | 00110101 |
| 67 | 43 | # 1 V image size (“173 mm“) | AD | 10101101 |
| 68 | 44 | # 1 H image size : V image size | 10 | 00010000 |
| 69 | 45 | # 1 H boarder ("0") | 00 | 00000000 |
| 70 | 46 | # 1 V boarder ("0") | 00 | 00000000 |
| 71 | 47 | Non-interlaced, Normal Display, Digital separate, Positive Hsync, Negative Vsync | 1A | 00011010 |
| 72 | 48 | Detailed timing description # 2 Pixel clock ("96.67MHz") | C3 | 11000011 |
| 73 | 49 | # 2 Pixel clock (hex LSB first) | 25 | 00100101 |
| 74 | 4A | # 2 H active ("1920") | 80 | 10000000 |
| 75 | 4B | # 2 H blank ("230") | E6 | 11100110 |
| 76 | 4C | # 2 H active : H blank | 70 | 01110000 |
| 77 | 4D | # 2 V active ("1080") | 38 | 00111000 |
| 78 | 4E | # 2 V blank ("44") | 2C | 00101100 |
| 79 | 4F | # 2 V active : V blank | 40 | 01000000 |
| 80 | 50 | # 2 H sync offset ("80") | 50 | 01010000 |
| 81 | 51 | # 2 H sync pulse width ("60") | 3C | 00111100 |
| 82 | 52 | # 2 V sync offset : V sync pulse width ("6 : 8") | 68 | 01101000 |
| 83 | 53 | # 2 H sync offset : H sync pulse width : V sync offset : V sync width | 00 | 00000000 |
| 84 | 54 | # 2 H image size (“309 mm“) | 35 | 00110101 |
| 85 | 55 | # 2 V image size (“173 mm“) | AD | 10101101 |
| 86 | 56 | # 2 H image size : V image size | 10 | 00010000 |
| 87 | 57 | # 2 H boarder ("0") | 00 | 00000000 |

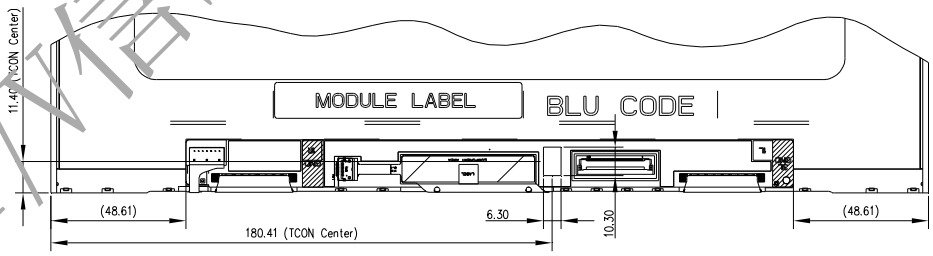
| | | | | |
|---|---|---|---|---|
| 88 | 58 | # 2 V boarder ("0") | 00 | 00000000 |
| 89 | 59 | Non-interlaced, Normal Display, Digital separate, Positive Hsync, Negative Vsync | 1A | 00011010 |
| 90 | 5A | NA | 00 | 00000000 |
| 91 | 5B | NA | 00 | 00000000 |
| 92 | 5C | NA | 00 | 00000000 |
| 93 | 5D | NA | 00 | 00000000 |
| 94 | 5E | NA | 00 | 00000000 |
| 95 | 5F | NA | 00 | 00000000 |
| 96 | 60 | NA | 00 | 00000000 |
| 97 | 61 | NA | 00 | 00000000 |
| 98 | 62 | NA | 00 | 00000000 |
| 99 | 63 | NA | 00 | 00000000 |
| 100 | 64 | NA | 00 | 00000000 |
| 101 | 65 | NA | 00 | 00000000 |
| 102 | 66 | NA | 00 | 00000000 |
| 103 | 67 | NA | 00 | 00000000 |
| 104 | 68 | NA | 00 | 00000000 |
| 105 | 69 | NA | 00 | 00000000 |
| 106 | 6A | NA | 00 | 00000000 |
| 107 | 6B | NA | 00 | 00000000 |
| 108 | 6C | Detailed Timing Description #4 | 00 | 00000000 |
| 109 | 6D | Flags | 00 | 00000000 |
| 110 | 6E | Reserved | 00 | 00000000 |
| 111 | 6F | For Brightness Table and Power Consumption | 02 | 00000010 |
| 112 | 70 | Flags | 00 | 00000000 |
| 113 | 71 | PWM % [7:0] @ Step 0 = 5% | 0C | 00001100 |
| 114 | 72 | PWM % [7:0] @ Step 5 = 24% | 3D | 00111101 |
| 115 | 73 | PWM % [7:0] @ Step 10 = 100% | FF | 11111111 |
| 116 | 74 | Nits [7:0] @ Step 0 = 13nits | 0D | 00001101 |
| 117 | 75 | Nits [7:0] @ Step 5 = 60nits | 3C | 00111100 |
| 118 | 76 | Nits [7:0] @ Step 10 = 250nits | 7D | 01111101 |
| 119 | 77 | Panel Electronics Power @32x32 Chess Pattern =594mW | 0E | 00001110 |
| 120 | 78 | Backlight Power @60 nits =622mW | 0F | 00001111 |
| 121 | 79 | backlight Power @Step 10 =2592mW | 20 | 00100000 |
| 122 | 7A | Nits @ 100% PWM Duty =250nit | 7D | 01111101 |
| 123 | 7B | Flags | 00 | 00000000 |
| 124 | 7C | Flags | 00 | 00000000 |
| 125 | 7D | Flags | 00 | 00000000 |
| 126 | 7E | Extension flag | 00 | 00000000 |
| 127 | 7F | Checksum | A6 | 10100110 |

## Appendix. OUTLINE DRAWING






DRIVER IC, COF/FPC, TCON, AND VR LOCATIONS
SEE NOTES FOR EXPLANATION

NOTES :
1. IN ORDER TO AVOID ABNORMAL DISPLAY, POOLING AND WHITE SPOT, NO OVERLAPPING IS SUGGESTED AT CABLES, ANTENNAS, CAMERA, WLAN, WAN OR FOREIGN OBJECTS OVER FPC, T-CON AND VR LOCATIONS.
2. LVDS/EDP CONNECTOR IS MEASURED AT PIN1 AND ITS MATING LINE.
3. "( )" MARKS THE REFERENCE DIMENSION.
4. MEASUREMENT OF THICKNESS MUST BE MEASURED BY CALIPER OR MICROMETER.



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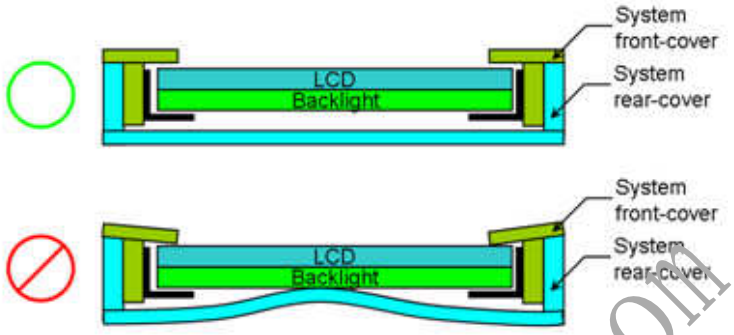
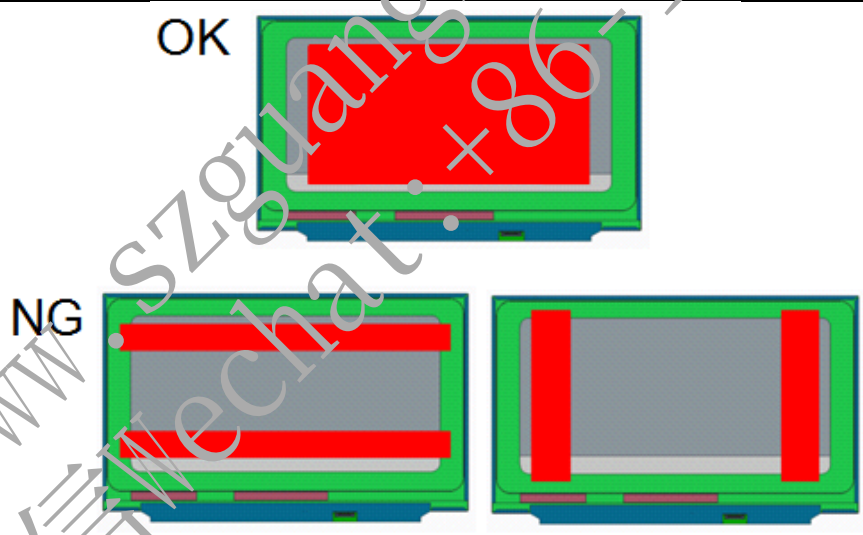
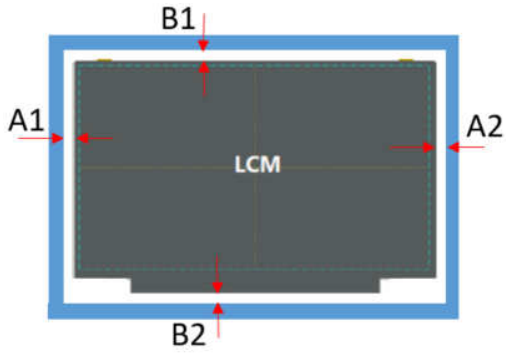
## Appendix. SYSTEM COVER DESIGN GUIDANCE FOR TOD

| | |
|---|---|
| **0** | **Permanent deformation of system cover after reliability test** |
| |  |
| Definition | System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack.<br>Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference. |
| 1 | Sponge area design behind panel |
| |  |
| Definition | Sponge area design behind panel can not be across the panel metal rear and the reflector at the same time. It can be on the reflector area only. |
| 2 | Gap between system rear-cover & panel |
| |  |
| Definition | The maximum thickness of sponge on the system rear-cover can not interfere to the maximum thickness of panel. Because the interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur.<br>Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference. |

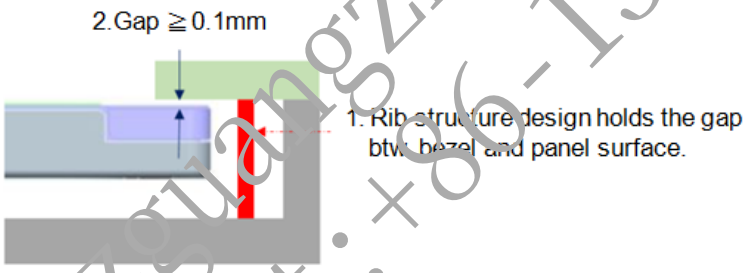
| 3 | **Gap Design between panel & around structure** |
|---|---|




| Item | Suggestion | Remark |
|---|---|---|
| A1 | A1≧0.5 | Gap≧ Panel outline max. tolerance + Assembly max. tolerance |
| A2 | A2≧0.5 | |
| B1 | B1≧0.5 | |
| B2 | B2≧0.8 | |

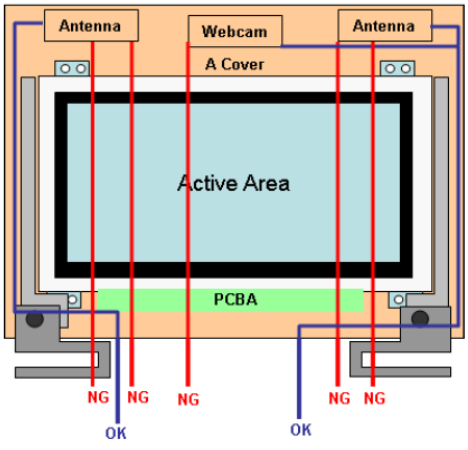
| Definition | Gap Design between panel & around structure needs to consider the maximum tolerances of panel outline and assembly at the same time.<br>Gap Design suggestion is shown as A1/A2/B1/B2 on the chart. |
|---|---|

| 4 | Gap between panel & bezel |
|---|---|



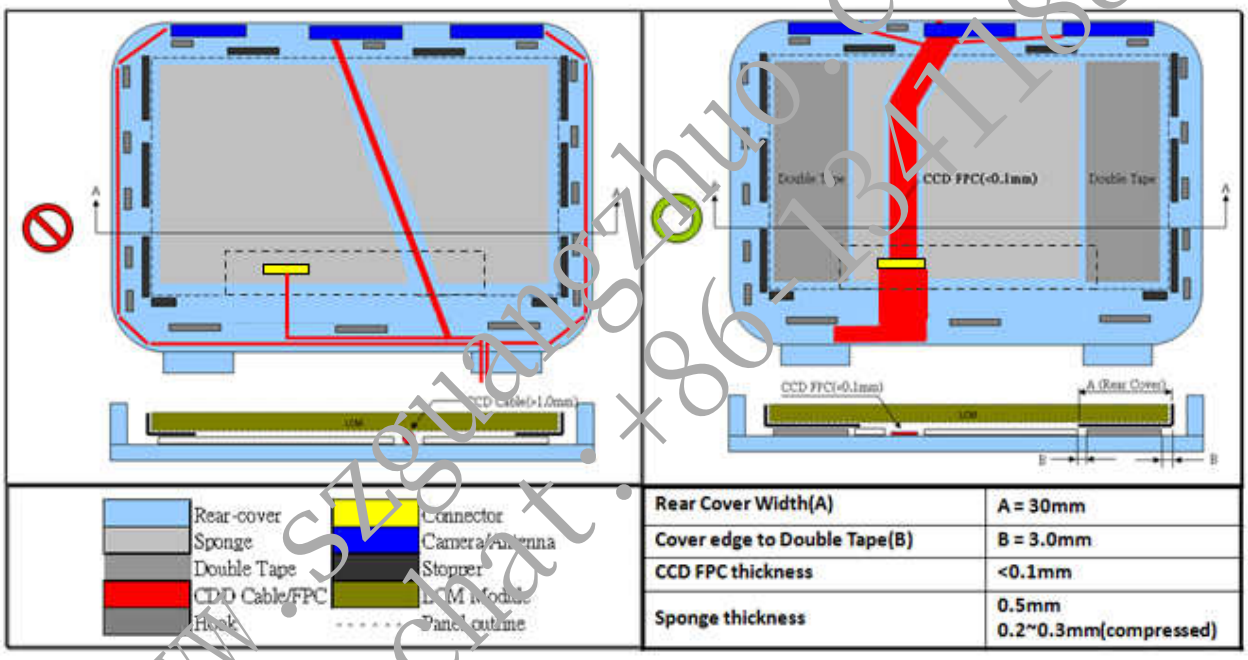

| Definition | The gap between system bezel & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system font-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test, or during pooling inspection procedure.<br>To remain the sufficient gap, design with system rib higher than maximum panel thickness is recommended.<br>The sufficient gap design is greater or equal to 0.1mm. |
|---|---|

| 5 | Cable routing behind panel |
|---|---|



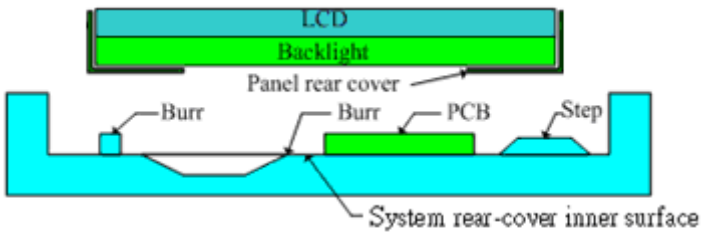
| | |
|---|---|
| Definition | It is strongly recommended that cables route around the panel outline, not overlap with the panel outline (including PCB). Because issue such as abnormal display & white spot after backpack test, hinge test, twist test or pogo test may occur.<br>If any routings across panel outline are needed, we suggest design as below:<br>-Using FFC/FPC to replace cables.<br>-Routing at the right or left area of panel metal rear.<br>-Avoid any routings at the step of panel or A cover.<br>-No interference to panel.<br>-It should not overlap TCON, COF/FPC, Driver IC |
| **6** | **Interference examination of antenna cable and WebCam wire** |

- To prevent panel damage, we suggest using CCD FPC to replace CCD cable
- Using double tape to fix LCM module for no bracket design.

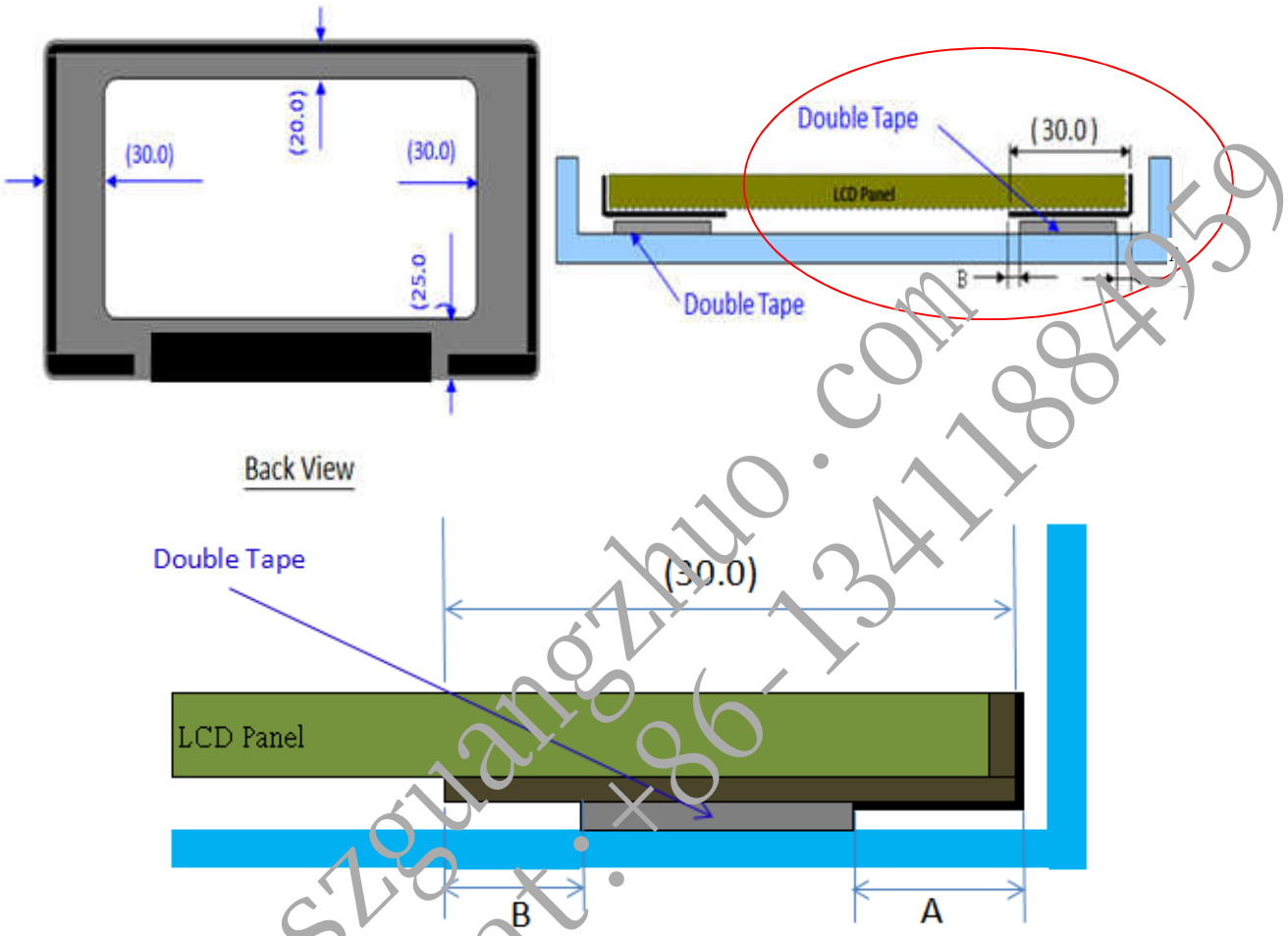
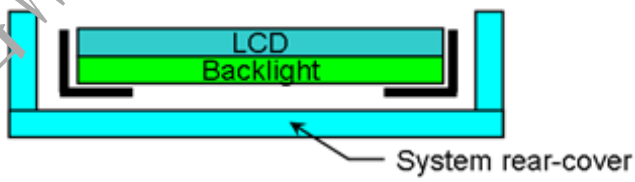


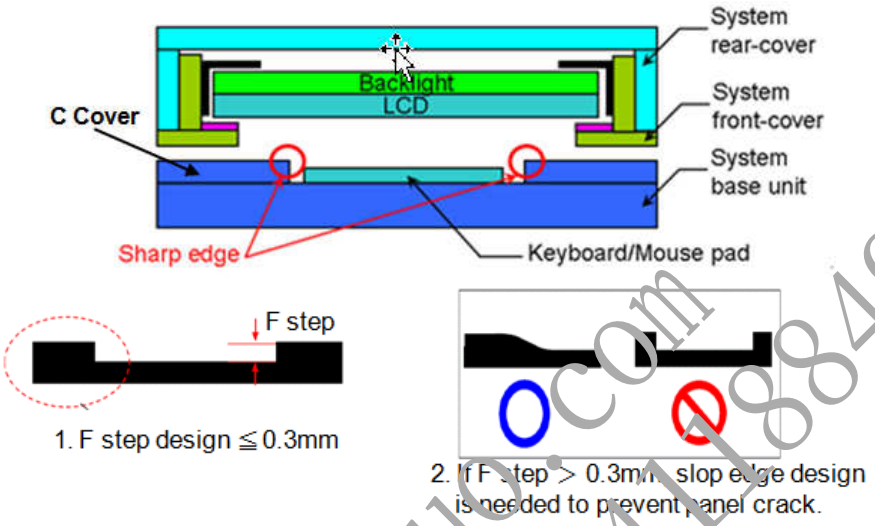
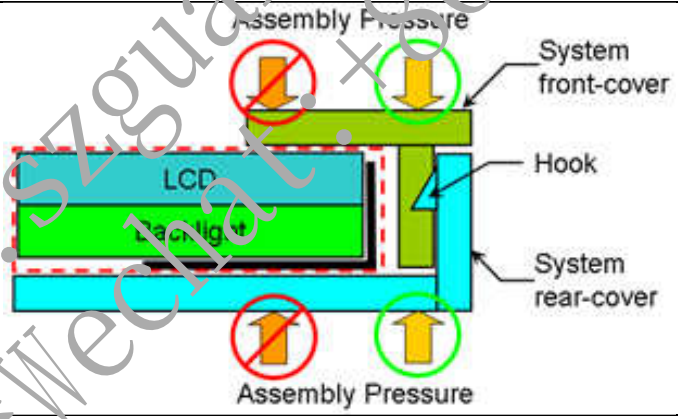

| | |
|---|---|
| Rear Cover Width(A) | A = 30mm |
| Cover edge to Double Tape(B) | B = 3.0mm |
| CCD FPC thickness | <0.1mm |
| Sponge thickness | 0.5mm<br>0.2~0.3mm(compressed) |

| | |
|---|---|
| Definition | If the antenna cable or Web Cam wire must overlap with the panel outline, both sides of the antenna cable or Web Cam wire must have a sponge(Sponge material can not contain NH3) and sponge require higher antenna cable or Web Cam wire.( Antenna cable or Web Cam wire should not overlap with TCON,COF/FPC,Driver IC)<br>Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference. |
| **7** | **System rear-cover inner surface examination** |

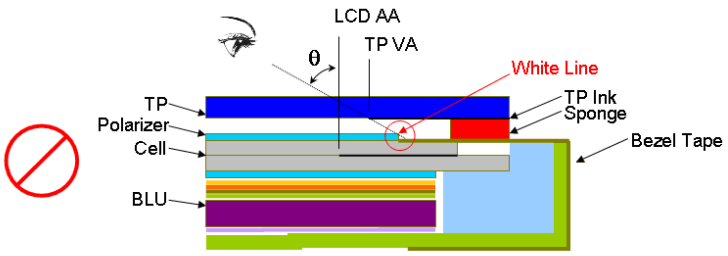


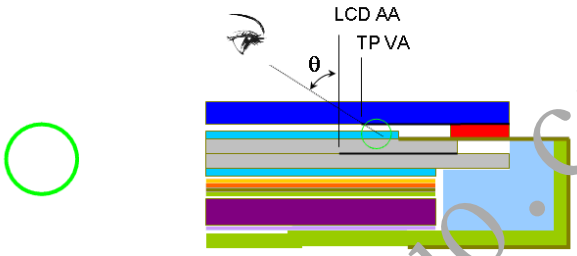

| | |
|---|---|
| Definition | Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test. |

| 8 | **Tape/sponge design on system inner surface** |
|---|---|
| |  |
| Definition | To prevent peeling the bezel tape in rework process. The length of double tape is 30 – (A+B), A is bezel tape length and B is the double tape attaching tolerance.<br>Ex :A :2mm, B:2mm, the length of double tape is 30-(2+2)=26mm. |
| **9** | **Material used for system rear-cover** |
| |  <br>System rear-cover material: Al-Mg alloy<br>System rear-cover thickness:1.5mm MIN |
| Definition | System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference. |

| | |
|---|---|
| **10** | **C cover shape design** |
| |  |
| Definition | The F step design on C Cover less than or equal to 0.3mm is recommended.<br>If F step exceeds 0.3mm, the slop edge design is necessary to prevent panel crack. |
| **11** | **Assembly SOP examination for system front-cover with Hook design** |
| |  |
| Definition | To prevent panel crack during system front-cover assembly process with hook design, it is not recommended to press panel or any location that related directly to the panel. |

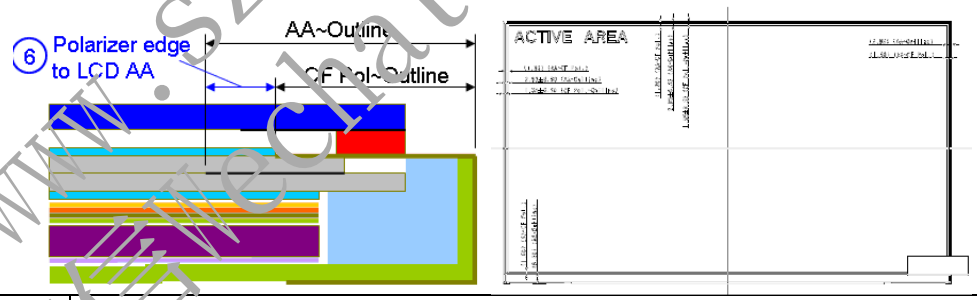
| 12 | Touch Application : TP and LCD Module Combination for White Line Prevention |
|---|---|



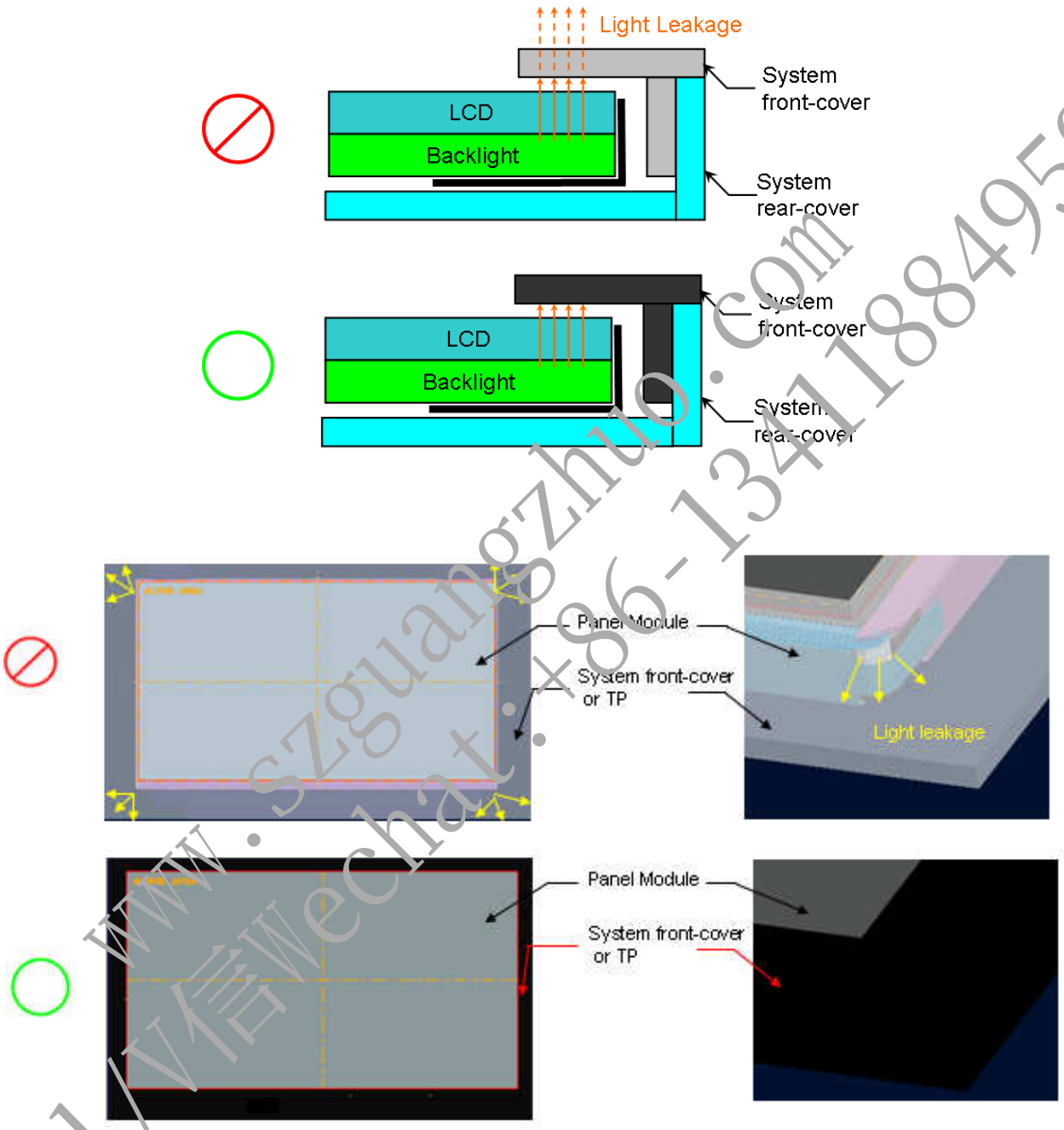




| Parameter consideration for White Line Issue : | |
|---|---|
| 1 | TP VA to LCD AA distance |
| 2 | TP Assembly tolerance |
| 3 | TP Ink Printing tolerance |
| 4 | Sponge thickness and tolerance |
| 5 | Inspection/Viewing Angle specification |
| 6 | Polarizer edge to LCD AA distance and tolerance |

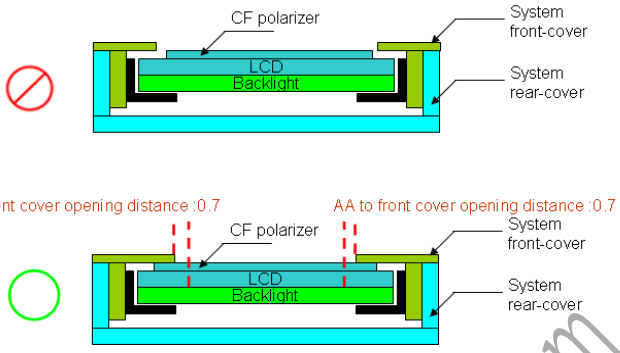
Polarizer edge to LCD AA distance can be derived by “AA~Outline” – “CF Pol~Outline” with respect to INX 2D Outline Drawing on each side.



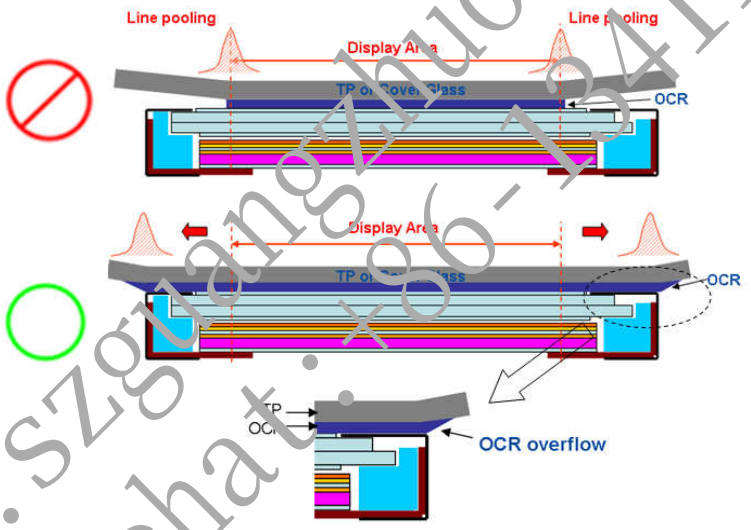

| Definition | For using in Touch Application: to prevent White Line appears between TP and LCD module combination, the maximum inspection angle location must not fall onto LCD polarizer edge, otherwise light line near edge of polarizer will be appear.<br>Parameters such as TP VA to LCD AA distance, TP assembly tolerance, TP Ink printing tolerance, Sponge thickness and tolerance, and Maximum Inspection/Viewing Angle, must be considered with respect to LCD module’s Polarizer edge location and tolerance. This consideration must be taken at all four edges separately.<br>The goal is to find parameters combination that allow maximum inspection angle falls inside polarizer black margin area.<br>Note: Information for Polarizer edge location and its tolerance can be derived from INX 2D Outline Drawing (“AA ~Outline“ - “CF Pol~Outline”).<br>Note: Please feel free to contact INX FAE Engineer. By providing value of parameters above on each side, we can help to verify and pass the white line risk assessment for customer reference. |
|---|---|
| **13** | **Color of system front-cover material** |



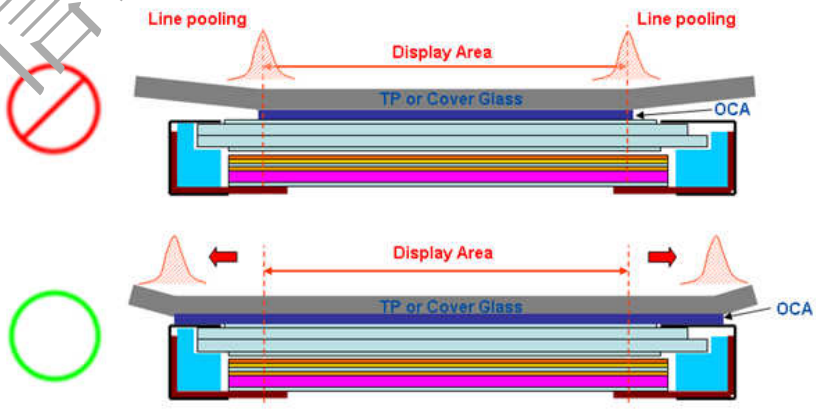

| | |
|---|---|
| Definition | To prevent light leakage is seen at system front-cover due to material transparency, we suggest using dark color material (black) for system front-cover design. |
| **14** | **AA to front cover opening distance** |



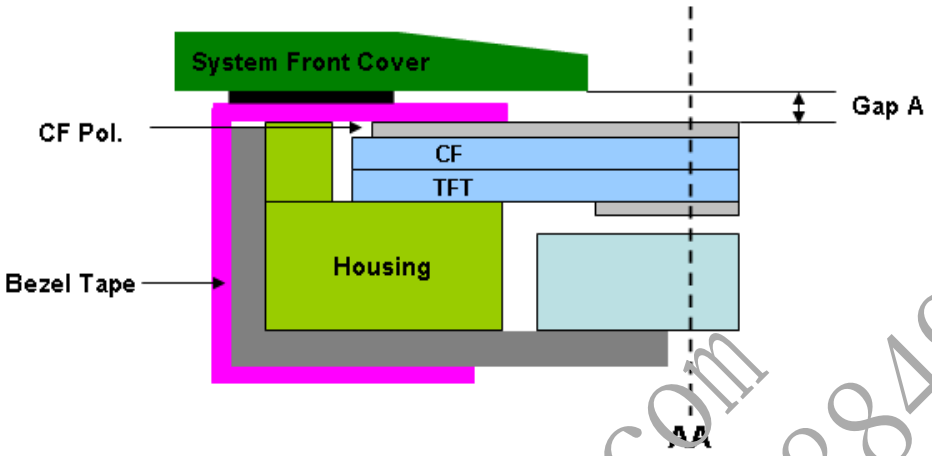

| | |
|---|---|
| Definition | To prevent CF polarizer edge leakage .We suggest front cover opening no more than 0.7mm larger than active area on all 4 sides. |
| **15** | **Use OCR Lamination** |




| | |
|---|---|
| Definition | OCR glue as possible beyond module, in order to avoid Line Pooling. |
| **16** | **Use OCA Lamination** |

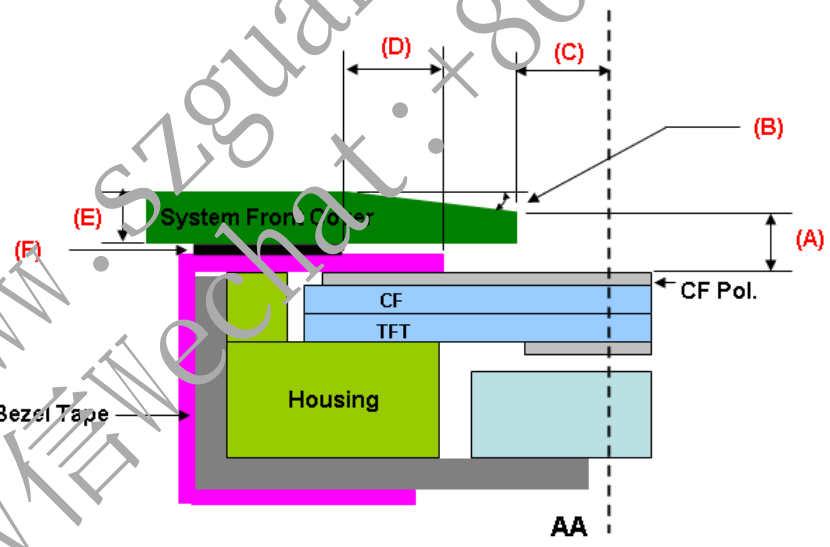



| | |
|---|---|
| Definition | OCA glue as possible plastered throughout the module, in order to avoid Line Pooling. |
| **17** | **Design Gap between System Front-cover & TOD LCD module surface** |




**0.15 ≦ Gap A ≦ 0.20 mm**

| | |
|---|---|
| Definition | Gap A between system front-cover & TOD LCD module surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system front-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test, or during pooling inspection procedure. To remain sufficient gap for first graph, design value for front-cover depth is recommended higher than module wing depth. |
| **18** | **System Front-cover dimension suggestion** |




| System Front Cover Open TOP to CF Pol. (A) | System Front Cover Chamfer (B) | System Front Cover Open to AA (C) | Bezel Tape Edge to Double Tape (D) | System Front Cover thickness (E) | Double Tape Thickness (F) |
|---|---|---|---|---|---|
| 0.8mm Max | 8~20° | 0.7≦ (B) ≦ 0.9mm | 1.0 mm Min | 1.2mm MAX | 0.05≦ (F) ≦ 0.08mm |

**CAUTION :**
In order to avoid the risk of bezel tape peeling, INX suggest not to attach any double tape on bezel tape; if necessary, the location of duuble tape attach must follow INX design guidance.

| | |
|---|---|
| Definition | To achieve better touch sensibility, INX suggests to follow design value as recommended , Recommended dimension is shown in above graph. |

## Appendix. LCD MODULE HANDLING MANUAL

| | |
|---|---|
| **Purpose** | • **This SOP is prepared to prevent panel dysfunction possibility through incorrect handling procedure.**<br>• **This manual provides guide in unpacking and handling steps.**<br>• **Any person which may contact / related with panel, should follow guide stated in this manual to prevent panel loss.** |
| **1.** | **Unpacking** |


| | |
|---|---|
| **2.** | **Panel Lifting** |

| 3. | Do and Don't |
|---|---|

Do :

- Handle with both hands.
- Handle panel at left and right edge.

Don't :

- Lifting with one hand.

- Handle at PCBA side.

Don't :

- Stack panels.

- Press panel.

Don't :

- Put foreign stuff onto panel

- Put foreign stuff under panel

Don't :

- Hold at panel corner.

Don't :

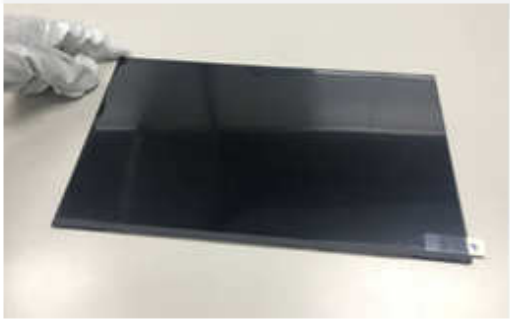
- Twist panel.

Do :

- Remove panel protector film starts from pull tape

Don't :

- Remove panel protector film From film another side.



Do:
- Remove panel protector film starts from Lower-right corner to Top-left

Don't:
- Remove panel protector Film parallel X-direction

Don't :
- Touch or Press PCBA Area.