INNOLUX 群創光電

PRODUCT SPECIFICATION

Doc. Number:

☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

MODEL NO.: N140ACA
SUFFIX: GT1 Rev.C1
(SD11L87672)

Customer: Lenovo

APPROVED BY **SIGNATURE**

Name / Title
Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
簡豪慶	李軒誠	蔡琇伃

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REVISION HISTORY

Version	Date	Page	Description
1.0	25 May. 2023	All	Tentative Specification Ver. 1.0 was first issued.
2.0	13 Jul. 2023	All	Preliminary Specification Ver. 2.0 was first issued.
3.0	18 Aug. 2023	All	Approval Specification Ver. 3.0 was first issued.
3.1	24 Nov. 2023	P5	Update 1.2 General spec

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N140ACA-GT1 is a 14.0” (14.0” diagonal) TFT Liquid Crystal Display NB module with LED Backlight unit and 40 pins eDP interface. This module supports 2240 x 1400 AAS mode and can display 16,777,216 colors.

1.2 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Screen Size	14.0 diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	2240 x R.G.B. x 1400	pixel	
Pixel Pitch	0.13464 (H) x 0.13464 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	Color	-
Color depth	Real 8bits		
Interface	eDP1.4 (4 lane / 2.7G)		
Transmissive Mode	Normally Black	-	-
Surface Treatment	3H, Anti-Glare	-	-
Luminance, White	300	cd/m2	
Color Gamut	100%	SRGB	
Power Consumption	Total 4.2 W (Max.) @ cell 0.7 W (Max.), BL 3.5 W (Max.)		(1)
Special Function	Item	Support	Note
	Free-sync	Yes	
	PSR (Panel Self Refresh)	PSR2	
	DPST (Display power saving Technology)	Yes	
	Adaptive sync	Yes	
	LRR (Low refresh rate)	Yes	LRR 2.5
	VRR (Variable Refresh Rate)	Yes	
	DMRRS	Yes	

Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, fv = 60 Hz, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 ºC, whereas **Mosaic** pattern is displayed.

Note (2) Display port interface signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2 (eDP1.4). There are many optional items described in eDP1.4. If some optional item is requested, please contact us.

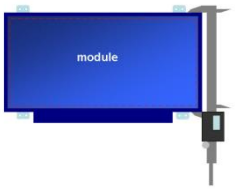
2. . MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	306.29	306.59	306.89	mm	(1)(2)(3)
	Vertical (V) (w/o PCB)	196.70	197.00	197.30	mm	
	Thickness (T) (w/o PCB)	-	-	2.4	mm	
	Thickness (T) (with PCB)	-	-	4.4		
Active Area	Horizontal	301.49	301.59	301.69	mm	
	Vertical	188.40	188.50	188.60	mm	
Weight		-	-	230	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Dimensions are measured by caliper.

(3) Panel thickness is measured with calipers clamping mylar or tape tightly



2.1 CONNECTOR TYPE

Please refer appendix outline drawing for detail design.

Connector Part No.: **MSAK24025P40MB**

User's connector Part No: IPEX-20453-040T-03

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

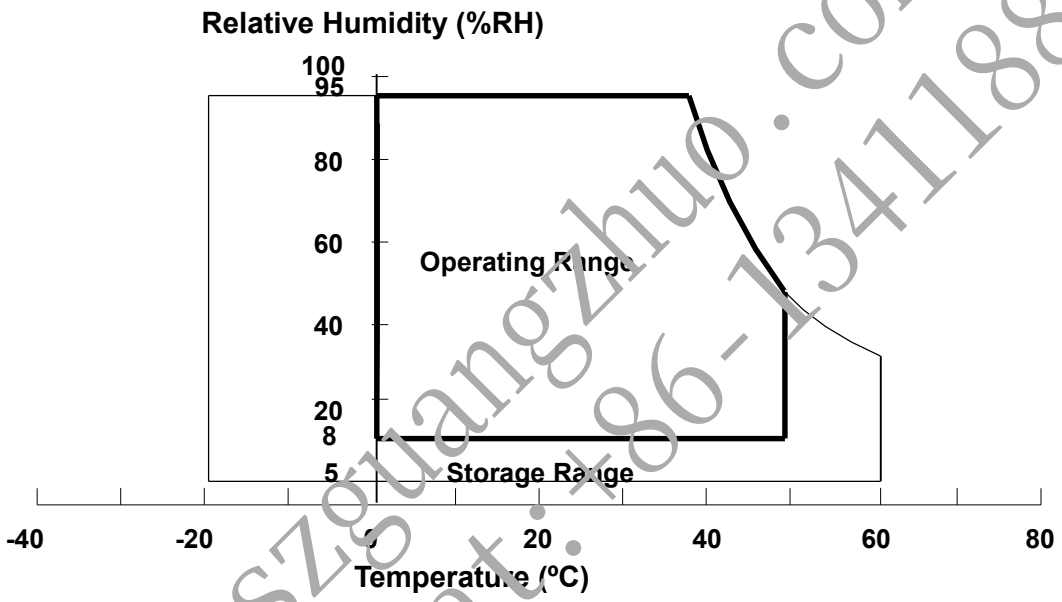
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)

Note (1) (a) 95 %RH Max. (Ta < 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max.

(c) No condensation.

Note (2) The temperature of panel surface should be 0 ºC min. and 60 ºC max.



3.2 ELECTRICAL ABSOLUTE RATINGS

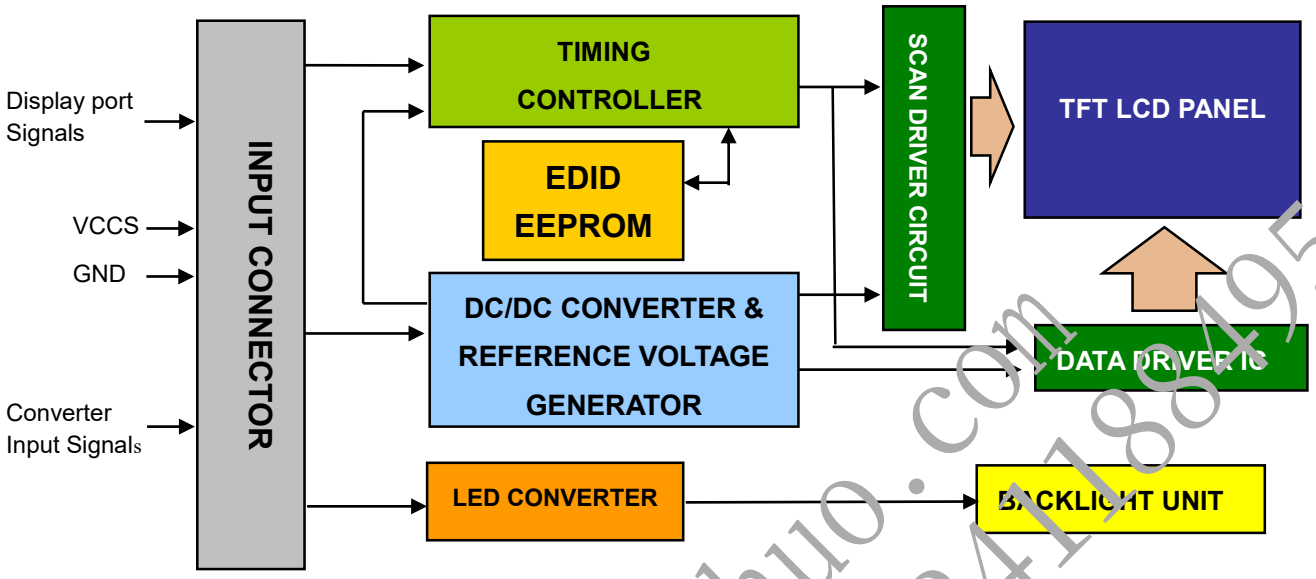
3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	VCCS+0.3	V	
Converter Input Voltage	LED_VCCS	-0.3	26	V	(1)
Converter Control Signal Voltage	LED_PWM,	-0.3	3.6	V	(1)
Converter Control Signal Voltage	LED_EN	-0.3	3.6	V	(1)

Note (1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “ELECTRICAL CHARACTERISTICS”.

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



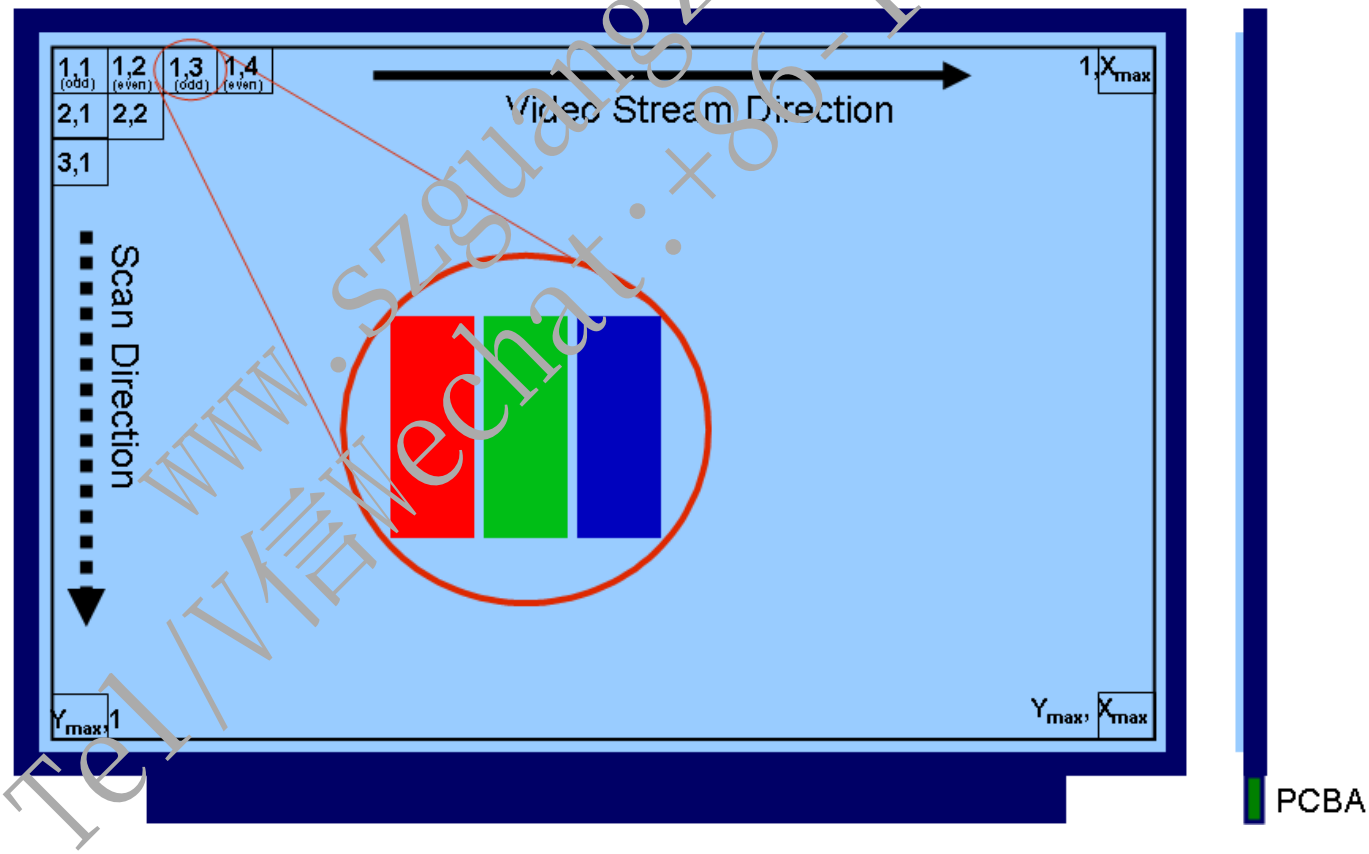
4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserved for LCD test)	
2	H_GND	High Speed Ground	
3	ML3-	Complement Signal-Lane 3	
4	ML3+	True Signal-Main Lane 3	
5	H_GND	High Speed Ground	
6	ML2-	Complement Signal-Lane 2	
7	ML2+	True Signal-Main Lane 2	
8	H_GND	High Speed Ground	
9	ML1-	Complement Signal-Lane 1	
10	ML1+	True Signal-Main Lane 1	
11	H_GND	High Speed Ground	
12	ML0-	Complement Signal-Lane 0	
13	ML0+	True Signal-Main Lane 0	
14	H_GND	High Speed Ground	
15	AUX+	True Signal-Auxiliary Channel	
16	AUX-	Complement Signal-Auxiliary Channel	
17	H_GND	High Speed Ground	
18	VCCS	Power Supply +3.3 V (typical)	
19	VCCS	Power Supply +3.3 V (typical)	
20	VCCS	Power Supply +3.3 V (typical)	
21	VCCS	Power Supply +3.3 V (typical)	
22	BIST_EN	Panel Built In Self Test Enable	Note (2)
23	GND	Ground	
24	GND	Ground	

25	GND	Ground	
26	GND	Ground	
27	HPD	Hot Plug Detect	
28	BL_GND	BL Ground	
29	BL_GND	BL Ground	
30	BL_GND	BL Ground	
31	BL_GND	BL Ground	
32	LED_EN	BL_Enable Signal of LED Converter	
33	LED_PWM	PWM Dimming Control Signal of LED Converter	
34	NC	No Connection (Reserved for LCD test)	
35	NC	No Connection (Reserved for LCD test)	
36	LED_VCCS	BL Power	
37	LED_VCCS	BL Power	
38	LED_VCCS	BL Power	
39	LED_VCCS	BL Power	
40	NC	No Connection (Reserved for LCD test)	

Note (1) The first pixel is odd as shown in the following figure.



Note (2) The setting of BIST function are as follows.

Pin	Enable	Disable
BIST_EN	High Level	Low Level or Open

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

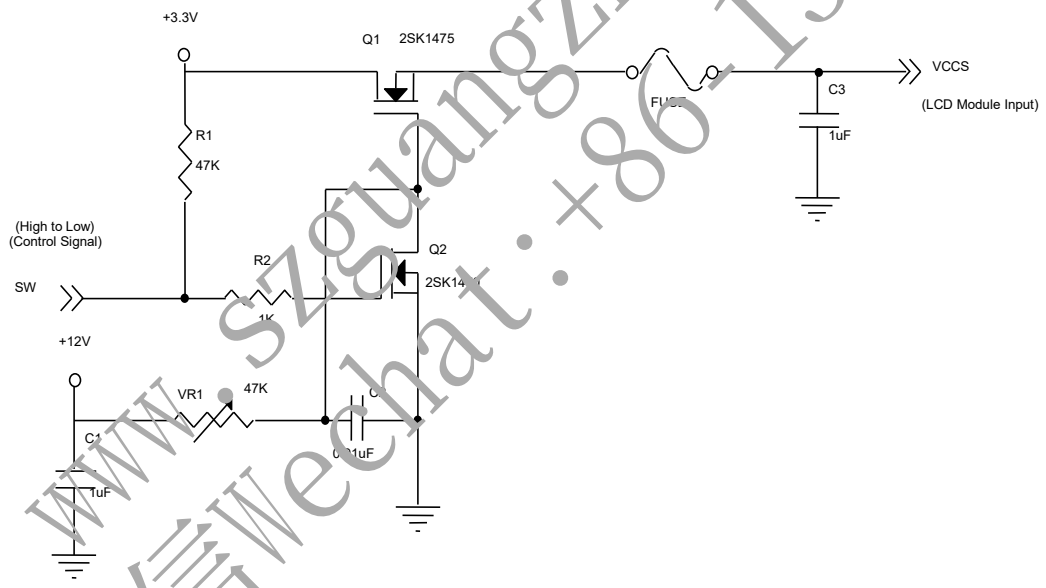
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)
Ripple Voltage		V_{RP}	-	-	100	mV	(1)
Inrush Current		I_{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Mosaic	Icc	-	-	212	mA	(3)a
	Black		-	-	212	mA	(3)
	(Solid Pattern)		-	-	776	mA	(3)b
HPD Impedance		R_{HPD}	30K			ohm	(4)
HPD	High Level		2.25	-	2.75	V	(5)
	Low Level		0	-	0.4	V	(5)
BIST_EN	High Level		3.0	-	3.6	V	
	Low Level		0	-	0.6	V	

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

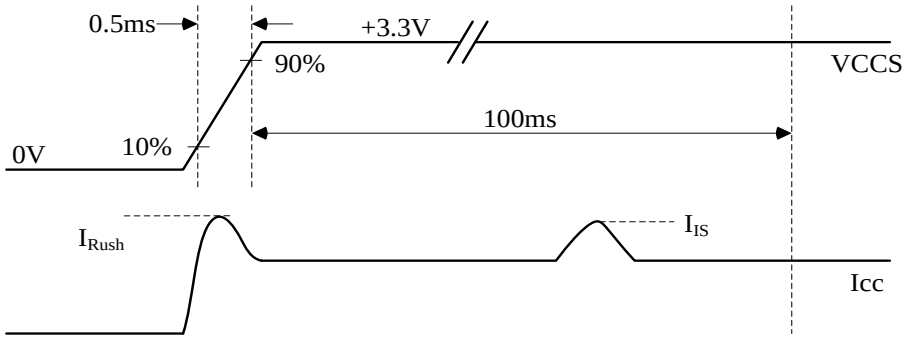
Note (2) I_{RUSH}: the maximum current when VCCS is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.

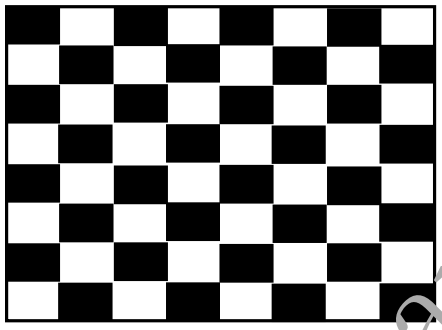


VCCS rising time is 0.5ms



Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 °C, DC Current and f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern



Active Area

b. The Solid Pattern is the largest one of R/G/B pattern

Note (3) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. Please refer to Note (4) of 4.3.2 LED CONVERTER SPECIFICATION to obtain more information.

Note (4) When a source detects a low-going HPD pulse, it must be regarded as a HPD event. Thus, the source must read the link / sink status field or receiver capability field of the DPCD and take corrective action.

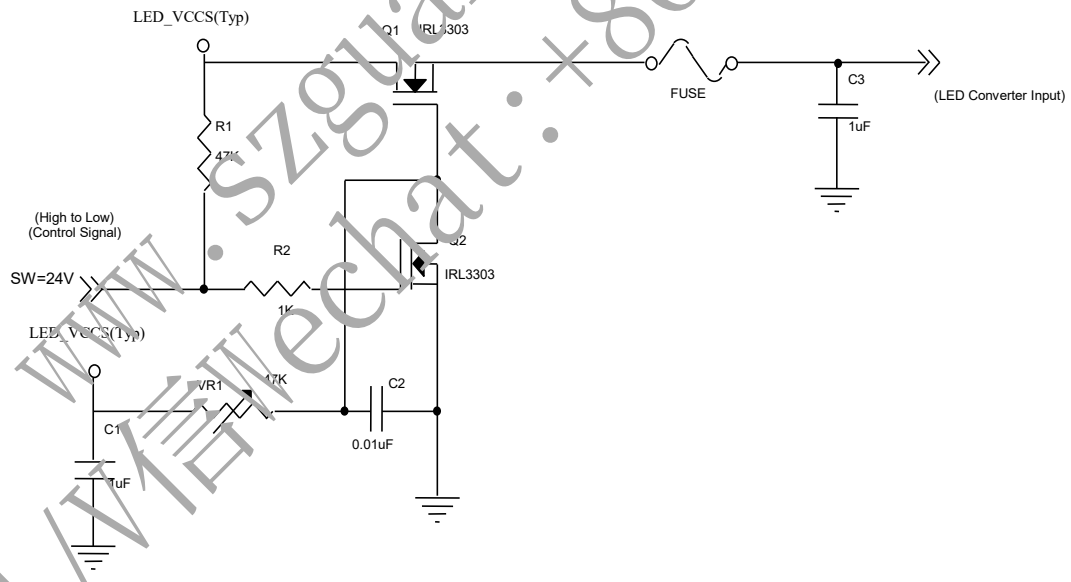
4.3.2 LED CONVERTER SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input Power Supply Voltage		LED_Vccs	5.0	12.0	21.0	V	
Converter Inrush Current		$I_{LEDRUSH}$	-	-	1.5	A	(1)
LED_EN Control Level	Backlight On		2.2	-	3.6	V	(4)
	Backlight Off		0	-	0.6	V	(4)
LED_EN Impedance		R_{LED_EN}	30K	-	-	ohm	(4)
PWM Control Level	PWM High Level		2.2	-	3.6	V	(4)
	PWM Low Level		0	-	0.6	V	(4)
PWM Impedance		R_{PWM}	30K	-	-	ohm	(4)
PWM Control Duty Ratio			1	-	100	%	(5)
PWM Control Permissive Ripple Voltage		V_{PWM_pp}	-	-	100	mV	
PWM Control Frequency		f_{PWM}	190	-	2K	Hz	(2)
LED Power Current	LED_VCCS =Typ.	ILED	174	270	291	mA	(3)
LED dimming control method by LED controller			DC Mode				

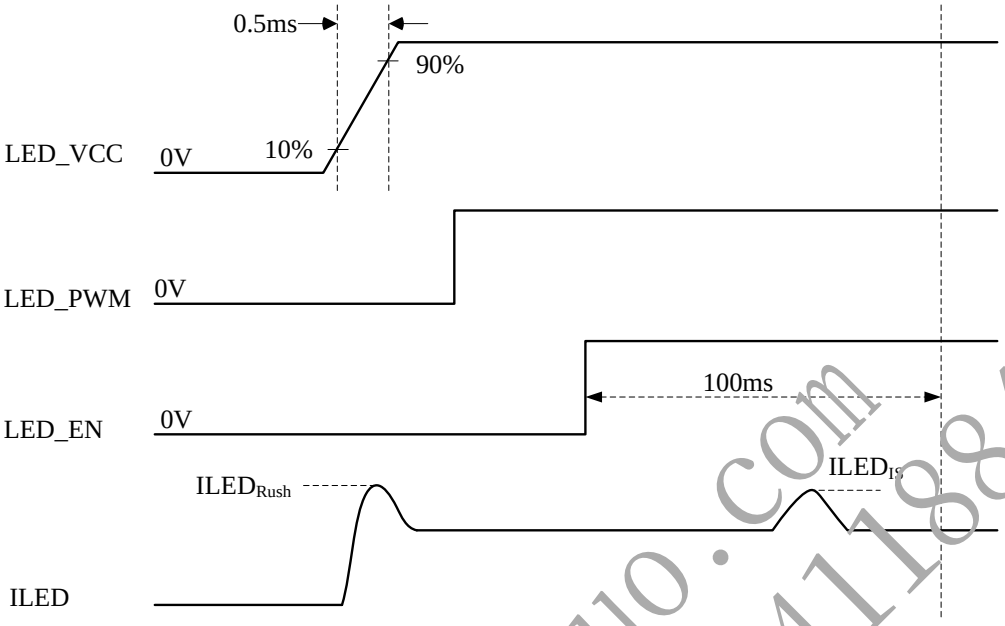
Note (1) ILEDRUSH: the maximum current when LED_VCCS is rising,

$I_{LED_{IS}}$: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.



VLED rising time is 0.5ms



Note (2) If PWM control frequency is applied in the range less than 1KHz, the "waterfall" phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

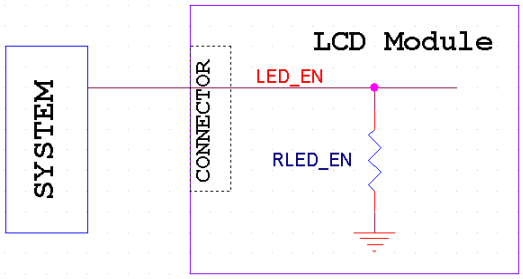
$$(N+0.33)*f \leq f_{PWM} \leq (N+0.66)*f$$

N : Integer ($N \geq 3$)

f : Frame rate

Note (3) The specified LED power supply current is under the conditions at "LED_VCCS = Typ.", Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.

Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. For example, the figure below describes the equivalent pull down impedance of LED_EN (If it exists). The rest pull down impedances of other signals (eg. HPD, PWM …) are in the same concept.



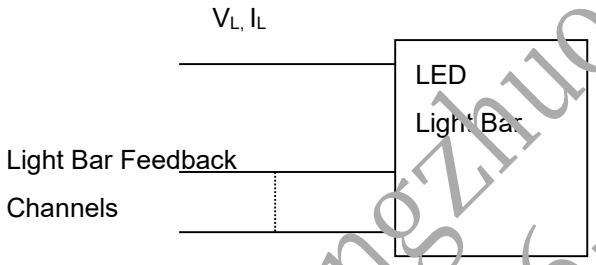
Note (5) If the cycle-to-cycle difference of PWM duty exceeds 0.1%, especially when the PWM duty is low, slight brightness change might be observed.

4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	32.4	34.8	36	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L	--	82.2	--	mA	
Power Consumption	P_L		2.86	2.96	W	(3)
LED Life Time	L_{BL}	15000	-	-	Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 ºC and I_L = (13.7) mA(Per EA) until the brightness becomes □ 50% of its original value.

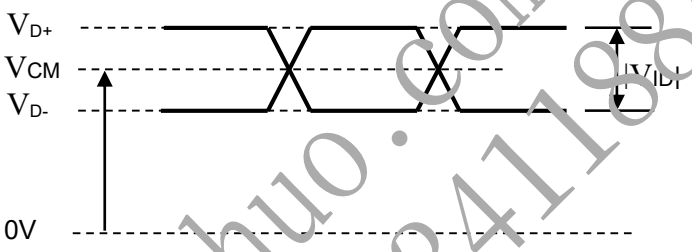
4.4 DISPLAY PORT INPUT SIGNAL TIMING SPECIFICATIONS

4.4.1 ELECTRICAL SPECIFICATIONS

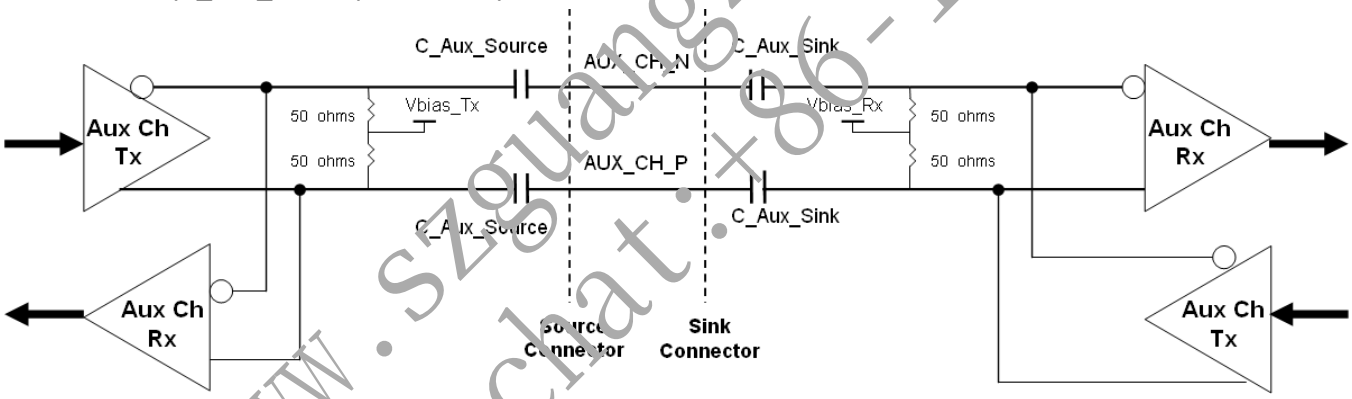
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Signal Common Mode Voltage(MainLink and AUX)	VCM	0		2	V	(1)(4)
AUX AC Coupling Capacitor	C_Aux_Source	75		200	nF	(2)
Main Link AC Coupling Capacitor	C_ML_Source	75		200	nF	(3)

Note (1)Display port interface related AC coupled signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2. There are many optional items described in eDP1.2. If some optional item is requested, please contact us.

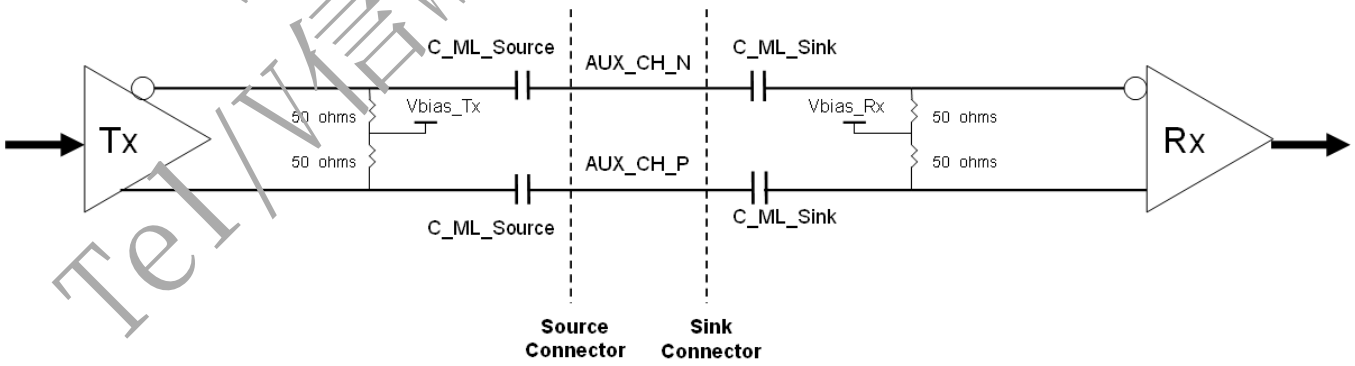
Single Ended



(2) Recommended eDP AUX Channel topology is as below and the AUX AC Coupling Capacitor (C_Aux_Source) should be placed on the source device.



(3) Recommended Main Link Channel topology is as below and the Main Link AC Coupling Capacitor (C_ML_Source) should be placed on the source device.



(4) The source device should pass the test criteria described in DisplayPortCompliance Test Specification (CTS) 1.1

4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Refresh rate 60Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	196.99	207.36	217.73	MHz	-
DE	Vertical Total Time	TV	1433	1440	1447	TH	-
	Vertical Active Display Period	TVD	1400	1400	1400	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	40	TV-TVD	TH	-
	Horizontal Total Time	TH	2388	2400	2412	Tc	-
	Horizontal Active Display Period	THD	2240	2240	2240	Tc	-
	Horizontal Active Blanking Period	THB	TH-THB	160	TH-THB	Tc	-

Refresh rate 50Hz

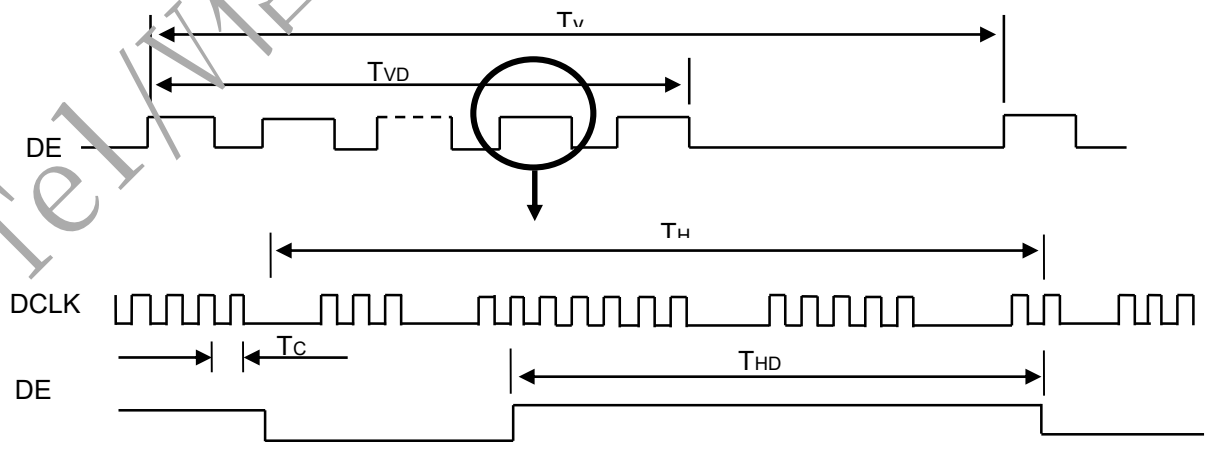
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	164.16	172.8	181.44	MHz	-
DE	Vertical Total Time	TV	1433	1440	1447	TH	-
	Vertical Active Display Period	TVD	1400	1400	1400	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	40	TV-TVD	TH	-
	Horizontal Total Time	TH	2388	2400	2412	Tc	-
	Horizontal Active Display Period	THD	2240	2240	2240	Tc	-
	Horizontal Active Blanking Period	THB	TH-THB	160	TH-THB	Tc	-

Refresh rate 48Hz

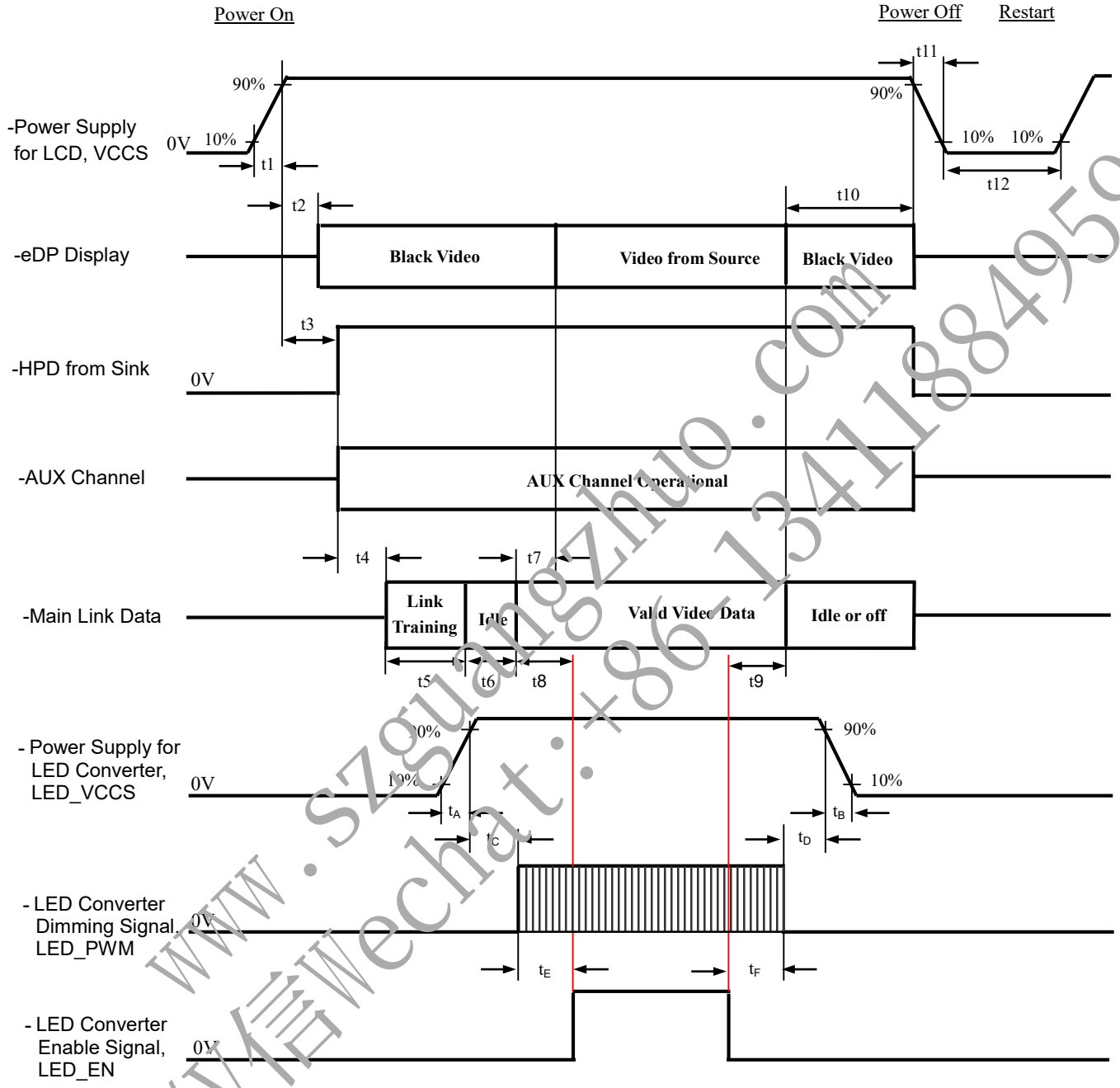
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	157.59	165.89	174.18	MHz	-
DE	Vertical Total Time	TV	1433	1440	1447	TH	-
	Vertical Active Display Period	TVD	1400	1400	1400	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	40	TV-TVD	TH	-
	Horizontal Total Time	TH	2388	2400	2412	Tc	-
	Horizontal Active Display Period	THD	2240	2240	2240	Tc	-
	Horizontal Active Blanking Period	THB	TH-THB	160	TH-THB	Tc	-

Note (1) The panel can operate at 60Hz normal mode and power saving mode, respectively. All reliability tests are based on specific timing of 60Hz refresh rate. We can only assure the panel's electrical function at power saving mode.

INPUT SIGNAL TIMING DIAGRAM



4.6 POWER ON/OFF SEQUENCE



Timing Specifications

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	VCCS Power rail rise time, 10% to 90%	Source	0.5	10	ms	See Note 5 below-
t2	Delay from VCCS to black video generation	Sink	0	80	ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source (see Notes:2 and 3 below)
t3	Delay from VCCS to HPD high	Sink	0	80	ms	Sink AUX Channel must be operational upon HPD high (see Note:4 below)
t4	Delay from HPD high to link training initialization	Source	0	-	ms	Allows for Source to read Link capability and initialize
t5	Link training duration	Source	0	-	ms	Dependant on Source link training protocol
t6	Link idle	Source	0	-	ms	Min Accounts for required BS-Idle pattern. Max allows for Source frame synchronization
t7	Delay from valid video data from Source to video on display	Sink	0	50	ms	Max value allows for Sink to validate video data and timing. At the end of T7, Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and Sink will no longer generate automatic Black Video
t8	Delay from valid video data from Source to backlight on	Source	80	-	ms	Source must assure display video is stable *: Recommended by INX. To avoid garbage image.
t9	Delay from backlight off to end of valid video data	Source	0	-	ms	Source must assure backlight is no longer illuminated. At the end of T9, Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and Sink will automatically display Black Video. (See Notes: 2 and 3 below) *: Recommended by INX. To avoid garbage image.
t10	Delay from end of valid video data from Source to power off	Source	0	500	ms	Black video will be displayed after receiving idle or off signals from Source
t11	VCCS power rail fall time, 90%	Source	0.5	10	ms	See Note 5 below-

	to 10%					
t12	VCCS Power off time	Source	500	-	ms	-
t_A	LED power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t_B	LED power rail fall time, 90% to 10%	Source	0	10	ms	-
t_C	Delay from LED power rising to LED dimming signal	Source	1	-	ms	-
t_D	Delay from LED dimming signal to LED power falling	Source	1	-	ms	-
t_E	Delay from LED dimming signal to LED enable signal	Source	0	-	ms	-
t_F	Delay from LED enable signal to LED dimming signal	Source	0	-	ms	-

Note (1) Please don't plug or unplug the interface cable when system is turned on.

Note (2) The Sink must include the ability to automatically generate Black Video autonomously. The Sink must automatically enable Black Video under the following conditions:

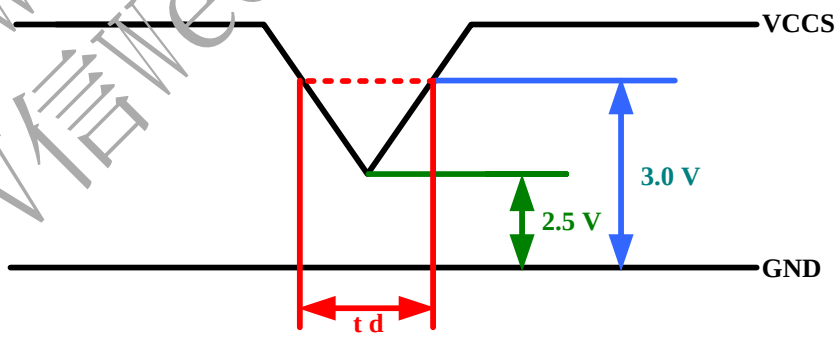
- Upon VCC power-on (within T2 max)
- When the "NoVideoStream_Flag" (VB-ID Bit 3) is received from the Source (at the end of T9)

Note (3) The Sink may implement the ability to disable the automatic Black Video function, as described in Note (2), above, for system development and debugging purposes.

Note (4) The Sink must support AUX Channel polling by the Source immediately following LCDVCC power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to response to an AUX Channel transaction with the time specified within T3 max.

Note (5) The VCCS power rail is recommended to rise and fall linearly. If not, please contact us to conduct risk assessment

4.7 MOMENTARY VOLTAGE DROPS



(1) When 2.5V □ Vcc ＜3.0V and td□10ms , the unit must work normally when VCC return to 3.0V.

(2) When Vcc < 2.5V, momentary voltage shall conform to the input voltage sequence.

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

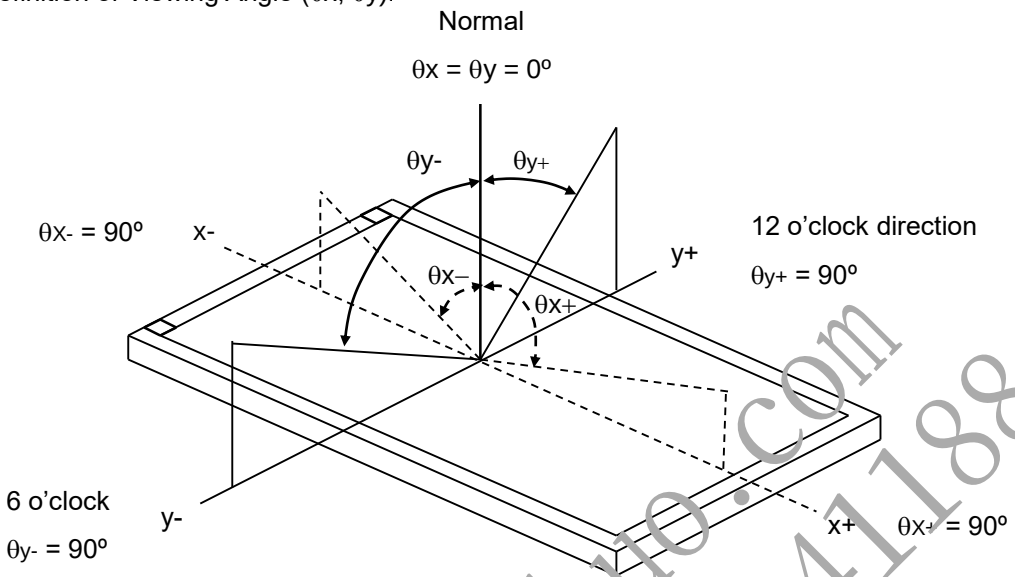
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	82.2	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	1000	1200	-	-	(2), (5),(7)
Response Time		T_R		-	11	14	ms	(3),(7)
		T_F		-	9	11	ms	
Average Luminance of White		L_{AVE}		255	300	345	cd/m²	(4), (6),(7)
Color Chromaticity	Red	Rx		Typ – 0.025	0.640	Typ + 0.025	-	(1),(7)
		Ry			0.330		-	
	Green	Gx			0.300		-	
		Gy			0.600		-	
	Blue	Bx			0.150		-	
		By			0.060		-	
	White	Wx			0.313		-	
		Wy			0.329		-	
Color gamut (sRGB)		sRGB		98	100		%	(8)
Viewing Angle	Horizontal	θ_x+	CR≥10	80	89		Deg.	(1),(5), (7)
		θ_x-		80	89	-		
	Vertical	θ_Y+		80	89	-		
		θ_Y-		80	89	-		
White Variation		δW_{5p}	θ_x=0°, θ_Y =0°	-	1.10	1.25	%	(5),(6), (7)
		δW_{13p}	θ_x=0°, θ_Y =0°	-	1.33	1.50	%	
Free sync	White	FS_W	θ_x=0°, θ_Y =0°	-	-	0.03	Nits/Hz	(1),(5), (7),(9)
	Gray(50%)	FS_G		-	-	0.04		
Low Blue Light		BLR	θ_x=0°, θ_Y =0°	-	-	50	%	(1), (5),(7), (10)
		CCT		5500	-	7000	K	

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

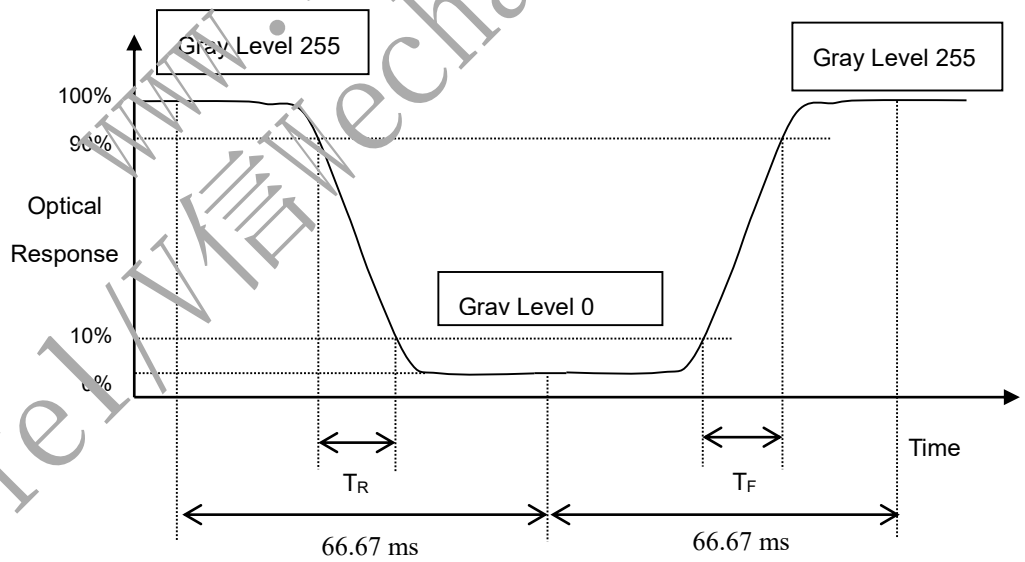
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

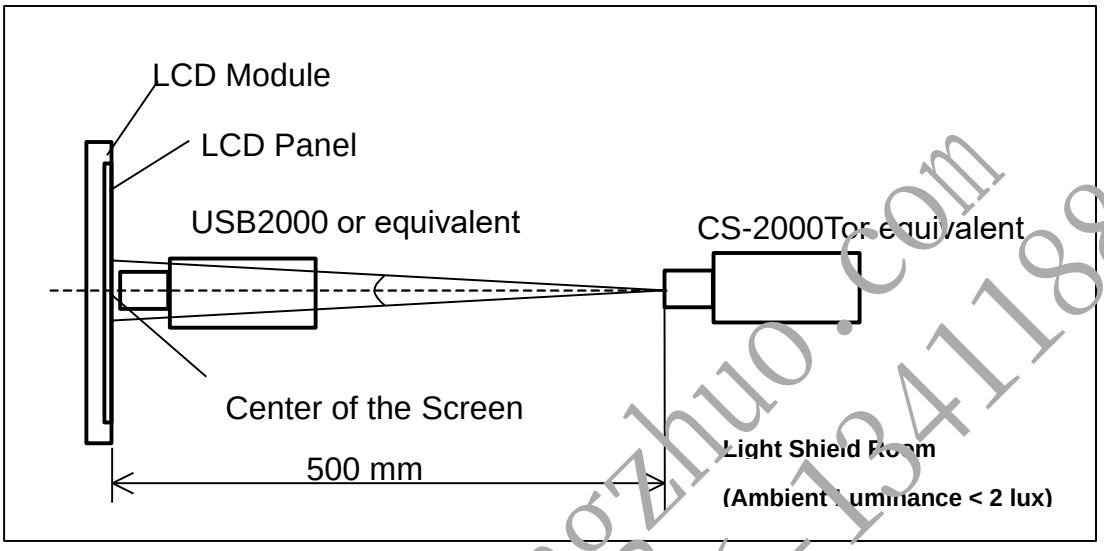
Measure the luminance of gray level 255 at 5 points

L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

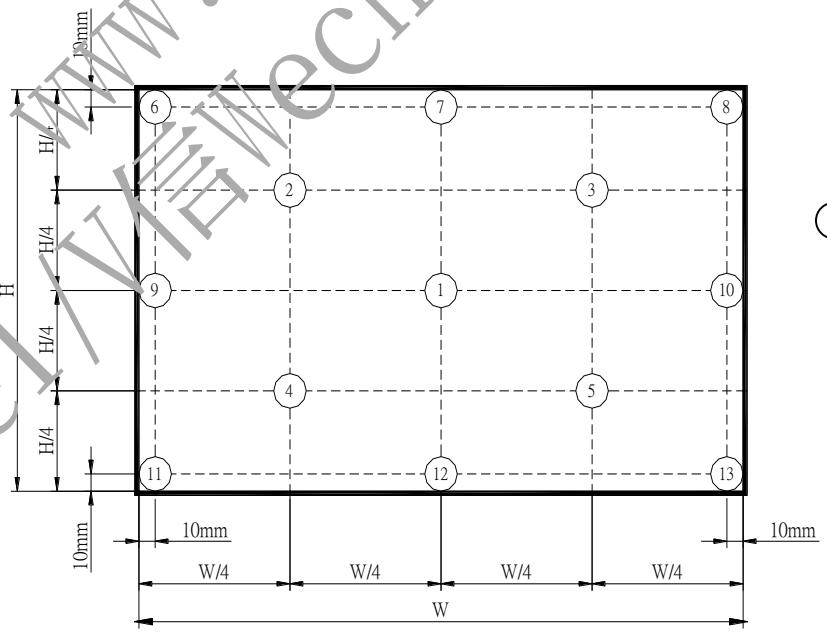


Note (6) Definition of White Variation (δW)

Measure the luminance of gray level 63 at 5 points

δW_{5p} = { Maximum [L (1)~ L (5)] / Minimum [L (1)~ L (5)]}*100%

δW_{13p} = { Maximum [L (1)~ L (13)] / Minimum [L (1)~ L (13)]}*100%



X : Test Point

X=1 to 13

Active area

Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

Note (8) Definition of color gamut (C.G%):

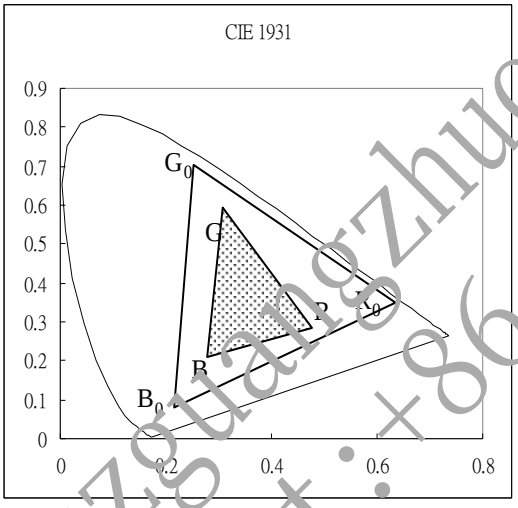
C.G%= □R G B /□R_0 G_0 B_0,*100%

R_0, G_0, B_0 : color coordinates of red, green, and blue defined by sRGB, respectively.

R, G, B : color coordinates of module on 63 gray levels of red, green, and blue, respectively.

R_0 G_0 B_0 : area of triangle defined by R_0, G_0, B_0

R G B: area of triangle defined by R, G, B



Note(9) Free Sync (FS):

FS= | L(60)-L(40) | / (F(60)-F(40))

L(x): Luminance of x Hz

F(x): x Hz frame rate

Note (10) Definition of Low Blue Light (LBL)

Measure the luminance of gray level 255 at center points

$$Blue\ Light\ Ratio(BLR) = \left[\frac{\text{Range (415~455 nm)}}{\text{Range (400~500 nm)}}\right] \text{ x } 100\%$$

Range (415~455 nm): Light intensity between 415 nm and 455 nm

Range (400~500 nm): Light intensity between 400 nm and 500 nm

LBL = LBL (1)

LBL (X) is corresponding to the Low Blue Light of the point X at Figure in Note (6)

6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60ºC, 240 hours	(1) (2)
Low Temperature Storage Test	-20ºC, 240 hours	
Thermal Shock Storage Test	-20ºC, 0.5hour←→60℃, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	50ºC, 240 hours	
Low Temperature Operation Test	0ºC, 240 hours	
High Temperature & High Humidity Operation Test	50ºC, RH 80%, 240hours	
ESD Test (Operation)	150pF, 330Ω, 1sec/cycle Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±15KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave,1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect.

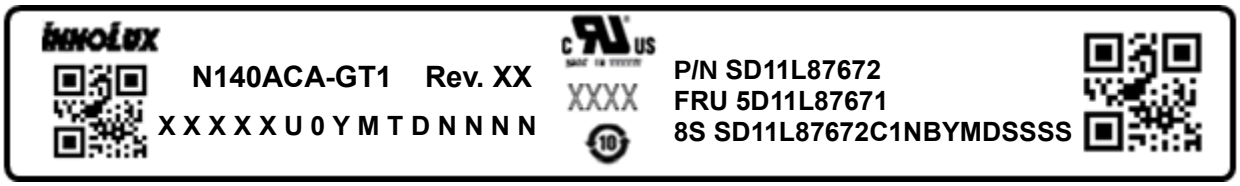
Note (2) Evaluation should be tested after storage at room temperature for more than two hour

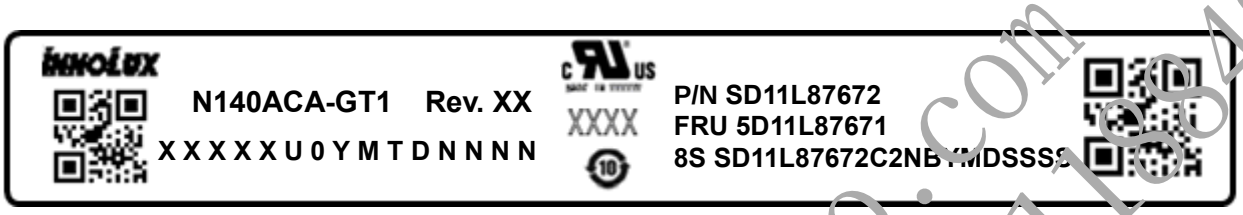
Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

7. PACKING

7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

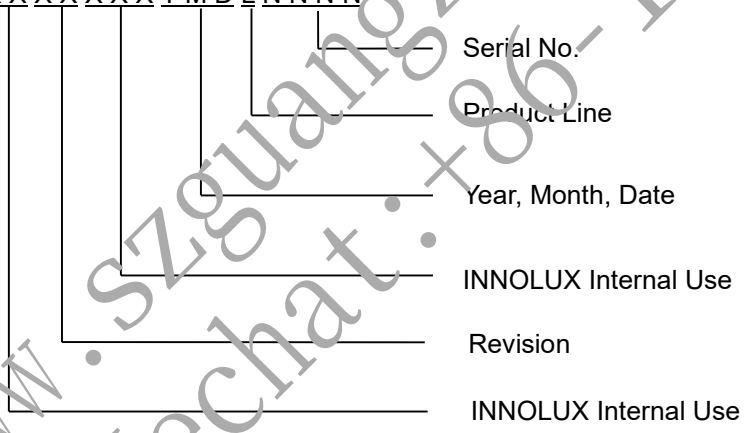




(a) Model Name: N140ACA-GT1

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X X X X X X Y M D L N N N N



(d) Production Location: MADE IN XXXX.

(e) UL logo: XXXX especially stands for panel manufactured by INNOLUX China satisfying UL requirement.

Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2010~2019

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

For barcode content 8S SD11L87672 C1NB YMD SSSS

(a) 8S: Fixed characters.

(b) SD11L87672 : Customer part number SD11L87672, fixed characters.

(c) C: Fixed characters

(d) 1: Revision History, 1~9, A~Z, exclude I , O , Q and U.

(e) XX: Fixed characters.

(f) YMD: Production date: Year: 0~9, for 2010~2019

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Z, for 1st to 31st, exclude I , O , Q and U

(g) SSSS: Series number: exclude I , O , Q and U

7.2 CARTON

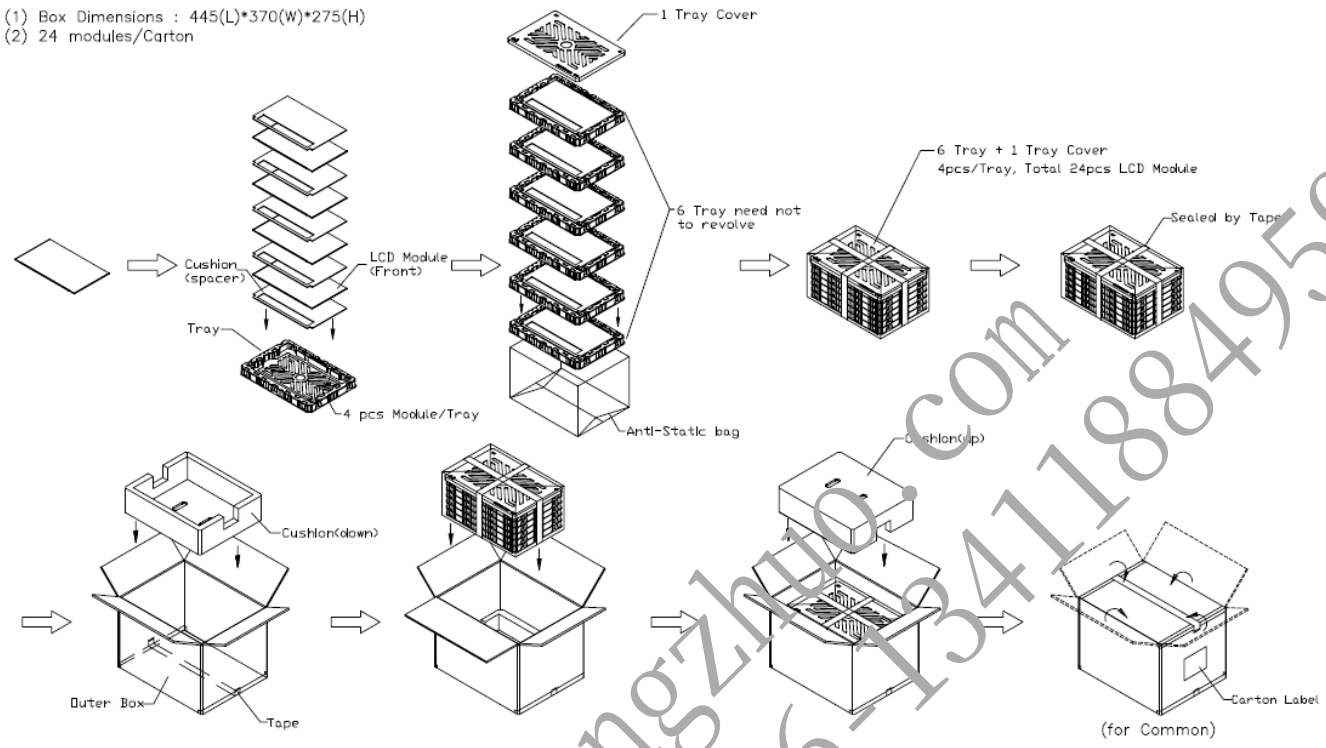


Figure. 7-2 Packing method

7.3 PALLET

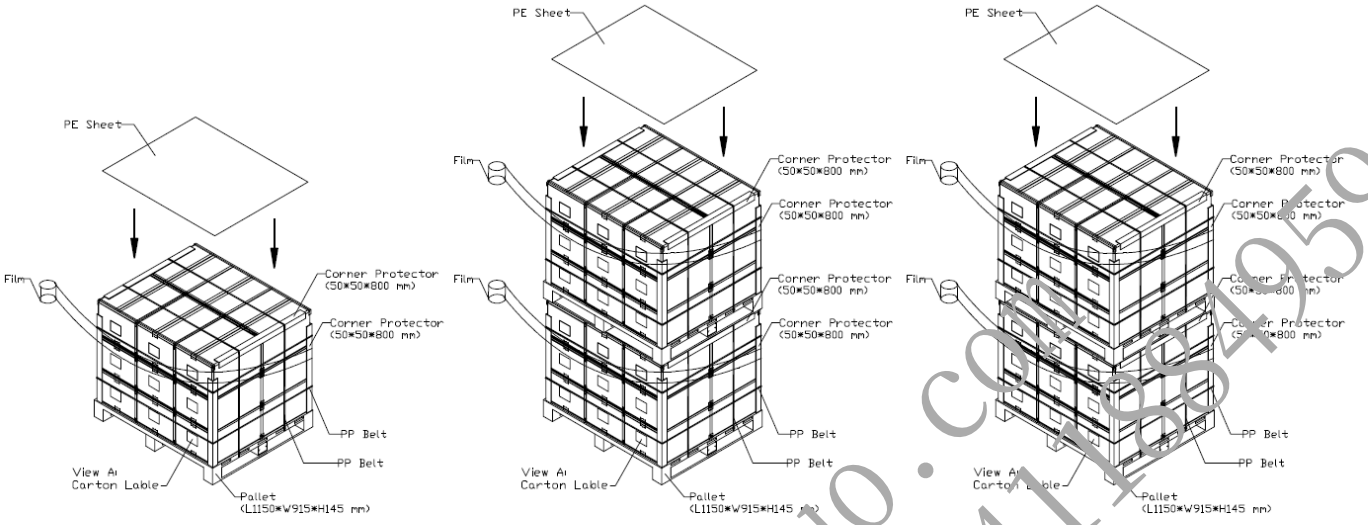


Figure. 7-3 Packing method

7.4 UN-PACKAGING METHOD

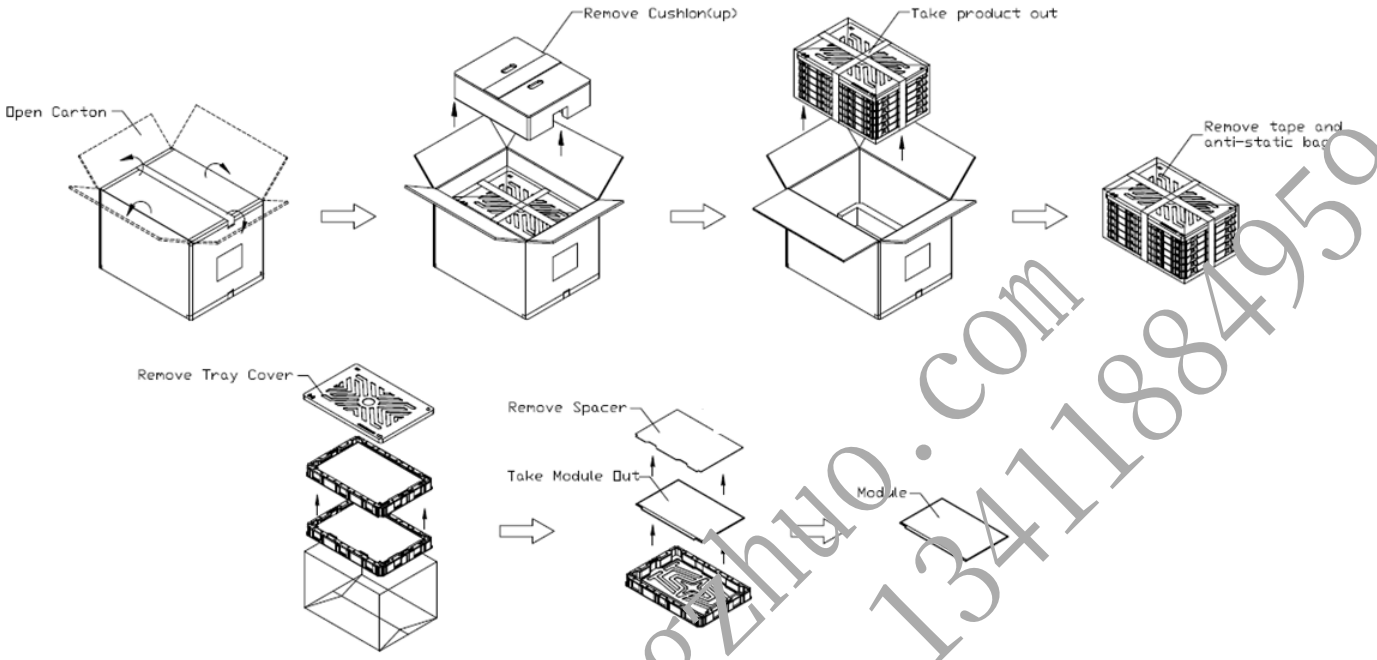


Figure. 7-4 un-packing method

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

Appendix. EDID DATA STRUCTURE

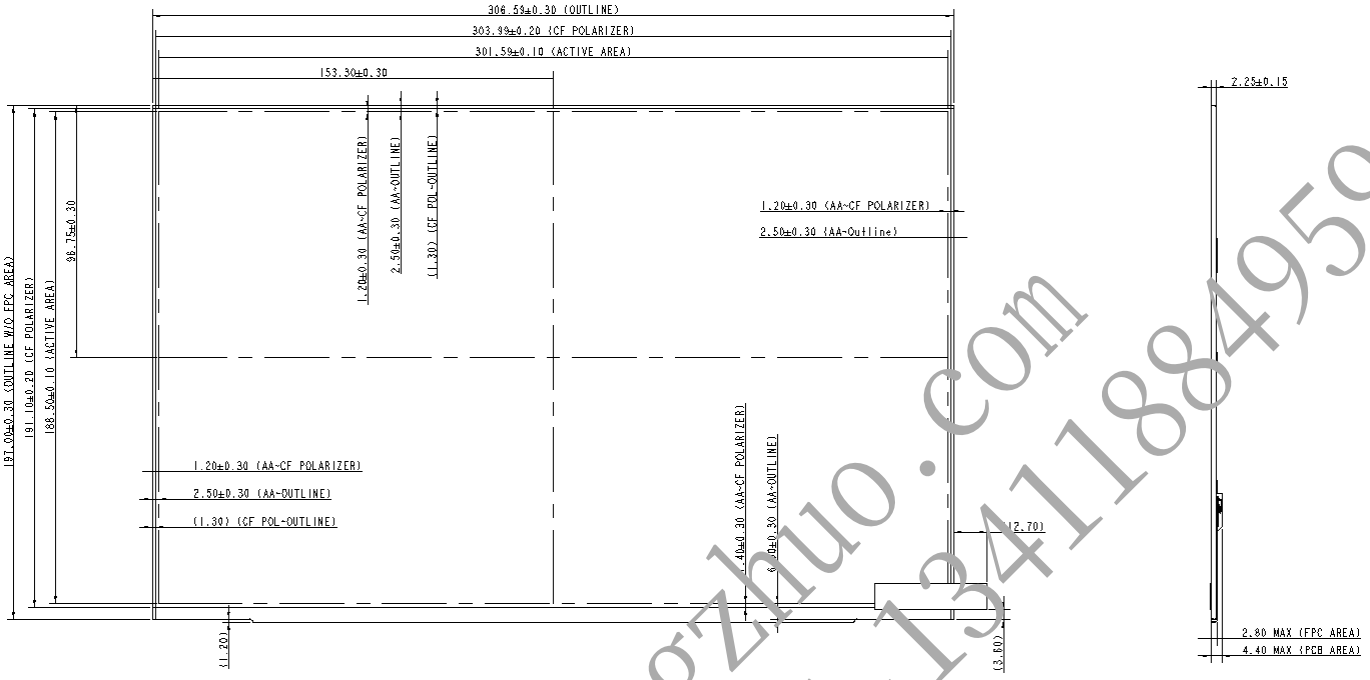
The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

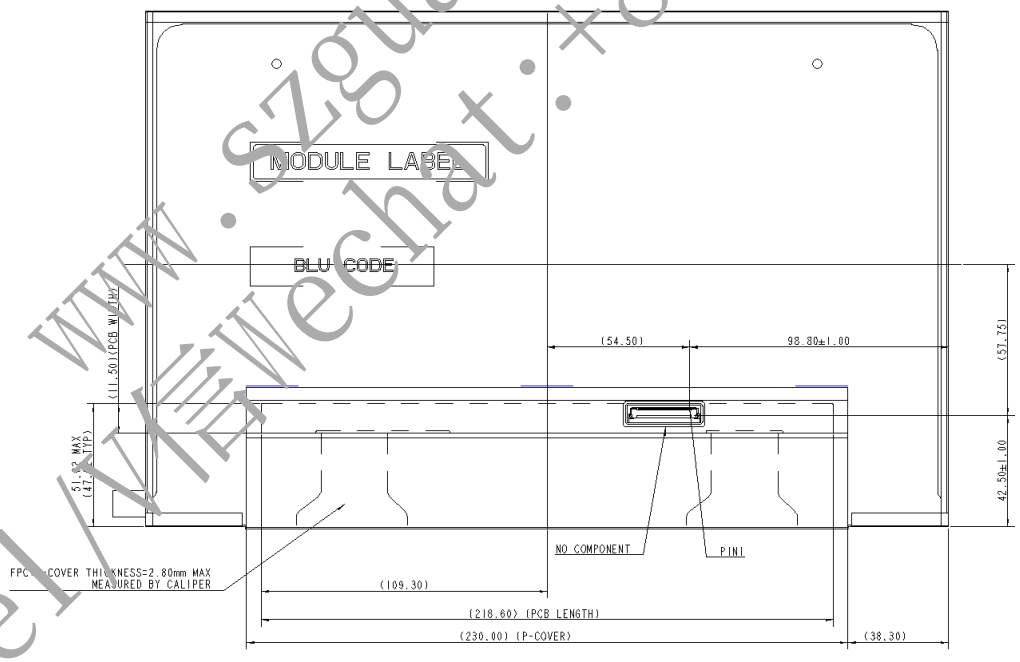
Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	00	Header	00	00000000
1	01	Header	FF	11111111
2	02	Header	FF	11111111
3	03	Header	FF	11111111
4	04	Header	FF	11111111
5	05	Header	FF	11111111
6	06	Header	FF	11111111
7	07	Header	00	00000000
8	08	EISA ID manufacturer name ("CMN")	0D	00001101
9	09	EISA ID manufacturer name	AE	10101110
10	0A	ID product code (LSB)	61	01100001
11	0B	ID product code (MSB)	14	00010100
12	0C	ID S/N (fixed "0")	00	00000000
13	0D	ID S/N (fixed "0")	00	00000000
14	0E	ID S/N (fixed "0")	00	00000000
15	0F	ID S/N (fixed "0")	00	00000000
16	10	Week of manufacture (fixed week code)	0D	00001101
17	11	Year of manufacture (fixed year code)	21	00100001
18	12	EDID structure version ("1")	01	00000001
19	13	EDID revision ("4")	04	00000100
20	14	Video I/P definition ("Digital")	A5	10100101
21	15	Active area horizontal (“30.159cm“)	1E	00011110
22	16	Active area vertical (“19.85cm“)	13	00010011
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("RGB, The native pixel format and preferred refresh rate, Continous frequency")	03	00000011
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	EE	11101110
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	95	10010101
27	1B	Rx=0.64	A3	10100011
28	1C	Ry=0.33	54	01010100
29	1D	Gx=0.3	4C	01001100
30	1E	Gy=0.6	99	10011001
31	1F	Bx=0.15	26	00100110
32	20	By=0.06	0F	00001111
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer's reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001

40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("207.36MHz")	00	00000000
55	37	# 1 Pixel clock (hex LSB first)	51	01010001
56	38	# 1 H active ("2240")	C0	11000000
57	39	# 1 H blank ("160")	A0	10100000
58	3A	# 1 H active : H blank	80	10000000
59	3B	# 1 V active ("1400")	78	01111000
60	3C	# 1 V blank ("40")	28	00101000
61	3D	# 1 V active : V blank	50	01010000
62	3E	# 1 H sync offset ("48")	30	00110000
63	3F	# 1 H sync pulse width ("32")	20	00100000
64	40	# 1 V sync offset : V sync pulse width ("10 : 6")	A6	10100110
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width	00	00000000
66	42	# 1 H image size ("301 mm")	2D	00101101
67	43	# 1 V image size ("188 mm")	BC	10111100
68	44	# 1 H image size : V image size	10	00010000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71	47	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
72	48	Indicates that this 18 byte descriptor is a Display Descriptor	00	00000000
73	49	Indicates that this 18 byte descriptor is a Display Descriptor	00	00000000
74	4A	Set to 00h when 18 byte descriptor is used as a Display Descriptor	00	00000000
75	4B	Tag Number for Display Range Limits Descriptor	FD	11111101
76	4C	Display Range Limits Offset : FLAGs	00	00000000
77	4D	Minimum Vertical Rate ("40Hz")	28	00101000
78	4E	Maximum Vertical Rate ("60Hz")	3C	00111100
79	4F	Minimum Horizontal Rate ("86KHz")	56	01010110
80	50	Maximum Horizontal Rate ("86KHz")	56	01010110
81	51	Maximum Pixel Clock ("207.36MHz")	15	00010101
82	52	Video Timing Support Flags : Bytes 10 --> 17 indicate support for additional video timings	01	00000001
83	53	Line Feed (0Ah if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	0A	00001010
84	54	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If	20	00100000

		Byte 10 = 02h or 04h)		
85	55	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	20	00100000
86	56	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	20	00100000
87	57	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	20	00100000
88	58	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	20	00100000
89	59	Space (20h if Byte 10 = 00h or 01h) or Video Timing Data (00h-->FFh If Byte 10 = 02h or 04h)	20	00100000
90	5A	Detailed timing description # 3	00	00000000
91	5B	# 3 Flag	00	00000000
92	5C	# 3 Reserved	00	00000000
93	5D	# 3 ASCII string Vendor	FE	11111110
94	5E	# 3 Flag	00	00000000
95	5F	# 3 Character of string ("C")	43	01000011
96	60	# 3 Character of string ("M")	4D	01001101
97	61	# 3 Character of string ("N")	4E	01001110
98	62	# 3 New line character indicates end of ASCII string	0A	00001010
99	63	# 3 Padding with "Blank" character	20	00100000
100	64	# 3 Padding with "Blank" character	20	00100000
101	65	# 3 Padding with "Blank" character	20	00100000
102	66	# 3 Padding with "Blank" character	20	00100000
103	67	# 3 Padding with "Blank" character	20	00100000
104	68	# 3 Padding with "Blank" character	20	00100000
105	69	# 3 Padding with "Blank" character	20	00100000
106	6A	# 3 Padding with "Blank" character	20	00100000
107	6B	# 3 Padding with "Blank" character	20	00100000
108	6C	Detailed timing description # 4	00	00000000
109	6D	# 4 Flag	00	00000000
110	6E	# 4 Reserved	00	00000000
111	6F	# 4 ASCII string Model Name	FE	11111110
112	70	# 4 Flag	00	00000000
113	71	# 4 Character of Model name ("N")	4E	01001110
114	72	# 4 Character of Model name ("1")	31	00110001
115	73	# 4 Character of Model name ("4")	34	00110100
116	74	# 4 Character of Model name ("0")	30	00110000
117	75	# 4 Character of Model name ("A")	41	01000001
118	76	# 4 Character of Model name ("C")	43	01000011
119	77	# 4 Character of Model name ("A")	41	01000001
120	78	# 4 Character of Model name ("-")	2D	00101101
121	79	# 4 Character of Model name ("G")	47	01000111
122	7A	# 4 Character of Model name ("T")	54	01010100
123	7B	# 4 Character of Model name ("1")	31	00110001
124	7C	# 4 New line character indicates end of ASCII string	0A	00001010
125	7D	# 4 Padding with "Blank" character	20	00100000
126	7E	Extension flag	00	00000000
127	7F	Checksum	26	00100110

Appendix. OUTLINE DRAWING

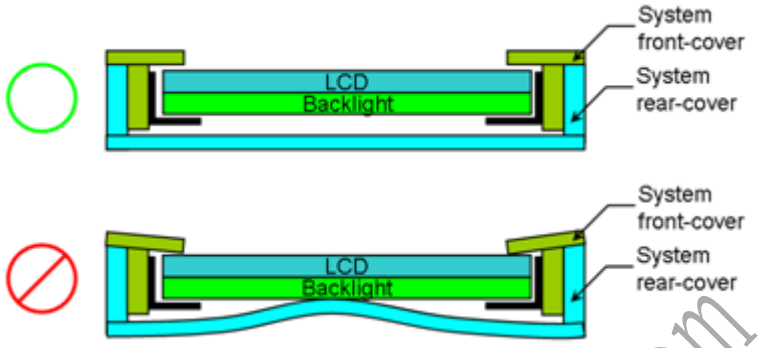
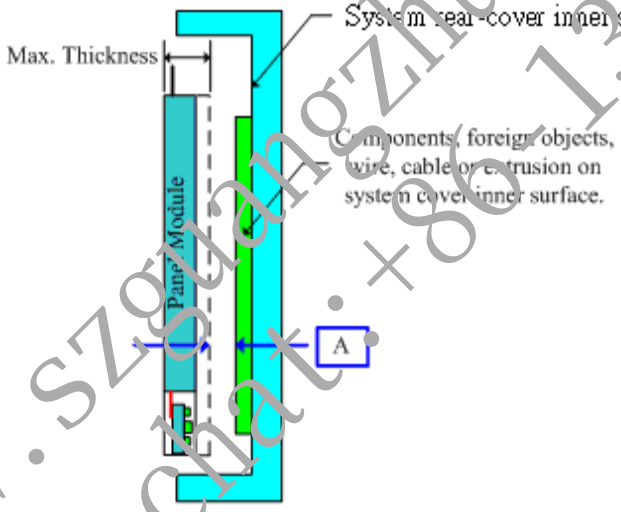


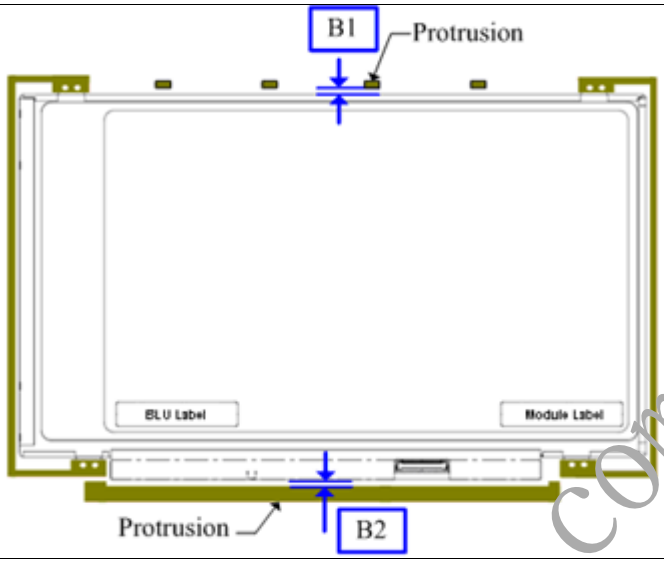


Note. Dimensions measuring instruments as below,

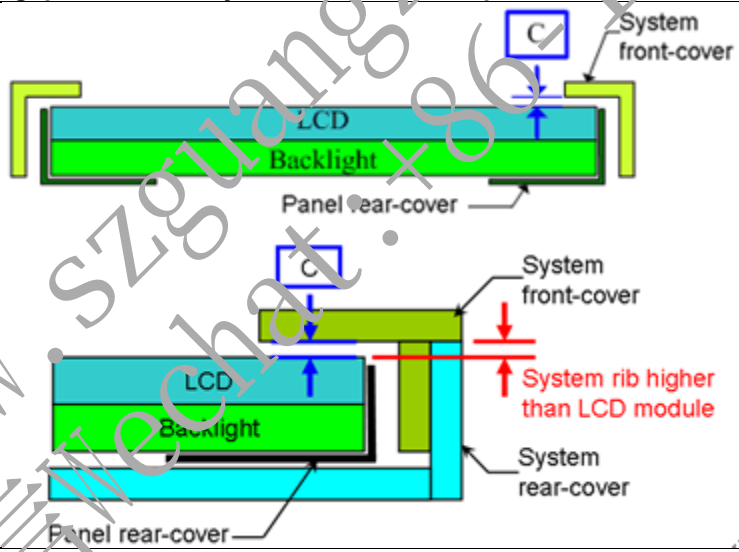
1. Length/ Width/Thickness : Caliper
2. Height : Height gauge

Appendix. SYSTEM COVER DESIGN GUIDANCE

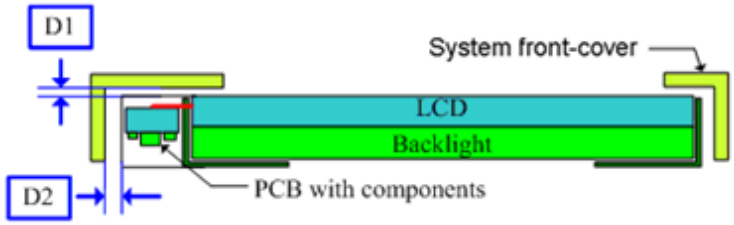
0.	**Permanent deformation of system cover after reliability test**
	
Definition	System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
1.	**Design gap A between panel & any components on system rear-cover**
	
Definition	Gap between panel's maximum thickness boundary & system's inner surface components such as wire, cable, extrusion is needed for preventing from backpack or pogo test fail. Because zero gap or interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur. Maximum flatness of panel and system rear-cover should be taken into account for gap design. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
2	**Design gap B1 & B2 between panel & protrusions**



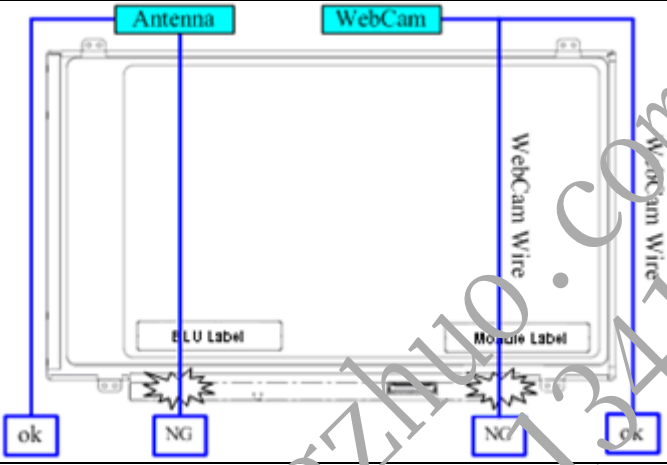
Definition	Gap between panel & protrusions is needed to prevent shock test failure. Because protrusions with small gap may hit panel during the test. Issue such as cell crack, abnormal display may occur. The gap should be large enough to absorb the maximum displacement during the test. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
3	**Design gap C between system front-cover & panel surface.**



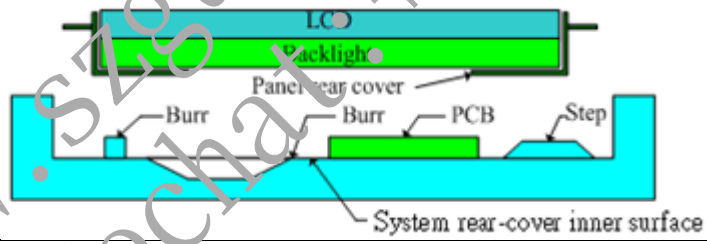
Definition	Gap between system front-cover & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system font-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test, or during pooling inspection procedure. To remain sufficient gap, design with system rib higher than maximum panel thickness is recommended. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
4	**Design gap D1 & D2 between system front-cover & PCB Assembly.**



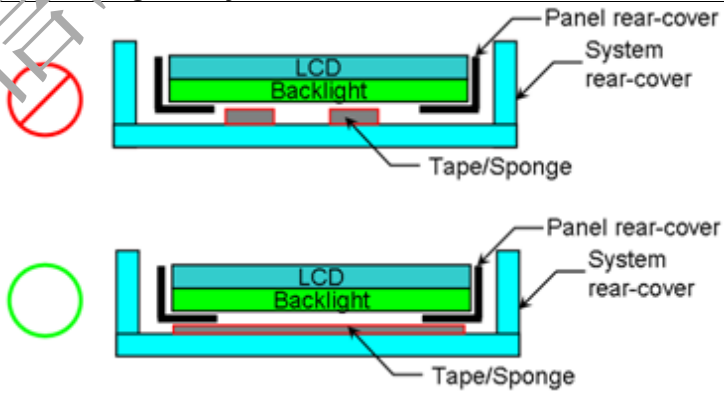
Definition	Same as point 2 and 3, but focus on PCBA side.
5	**Interference examination of antenna cable and WebCam wire**



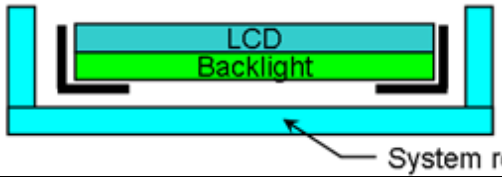
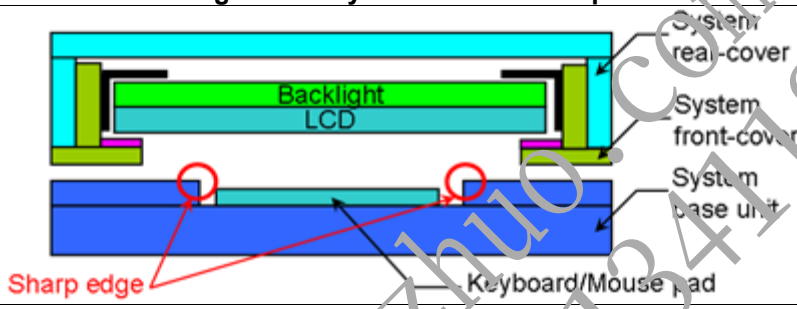
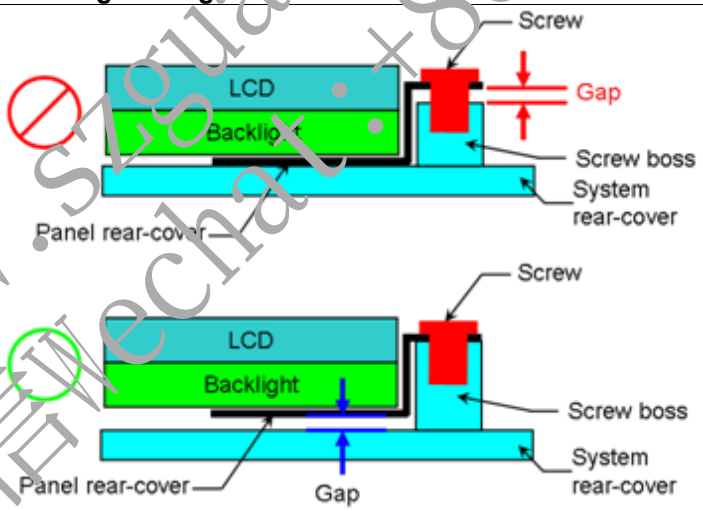
Definition	Antenna cable or WebCam wire should not overlap with panel outline. Because issue such as abnormal display & white spot after backpack test, hinge test, twist test or pogo test may occur. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
6	**System rear-cover inner surface examination**

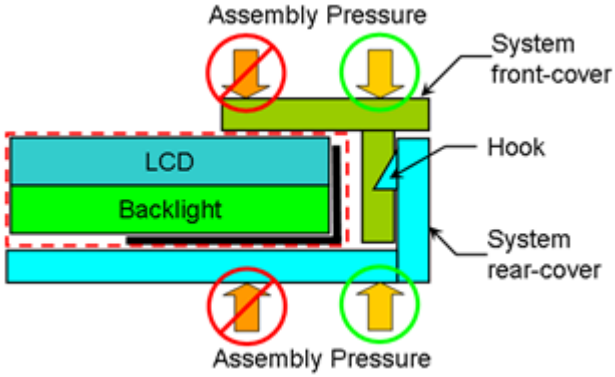


Definition	Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.
7	**Tape/sponge design on system inner surface**

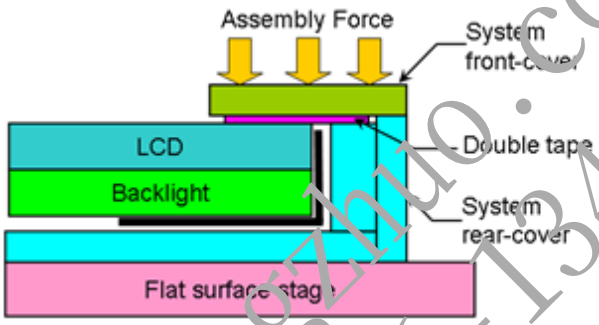


Definition	To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, tape/sponge should be well covered under panel rear-cover. Because tape/sponge in separate location may act as pressure concentration location.

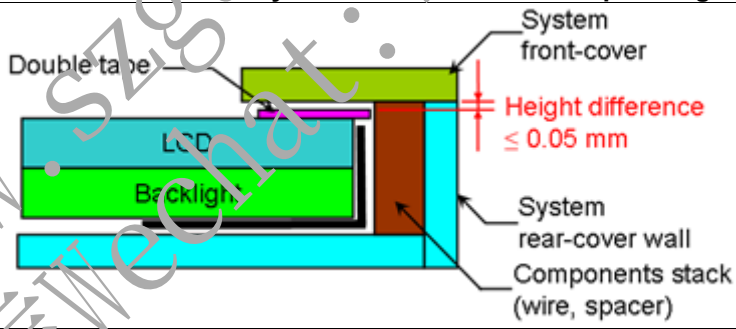
8	**Material used for system rear-cover**
	
Definition	System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw's boss positioning for module's bracket are deformed during open-close test. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.
9	**System base unit design near keyboard and mouse pad**
	
Definition	To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, sharp edge design in keyboard surface may damage panel during the test. We suggest to use slope edge design, or to reduce the thickness difference of keyboard/mouse pad from the nearby surface.
10	**Screw boss height design**
	
Definition	Screw boss height should be designed with respect to the height of bracket bottom surface to panel bottom surface + flatness change of panel itself. Because gap will exist between screw boss and bracket, if the screw boss height is smaller. As result while fastening screw, bracket will deformed and pooling issue may occur.
11	**Assembly SOP examination for system front-cover with Hook design**



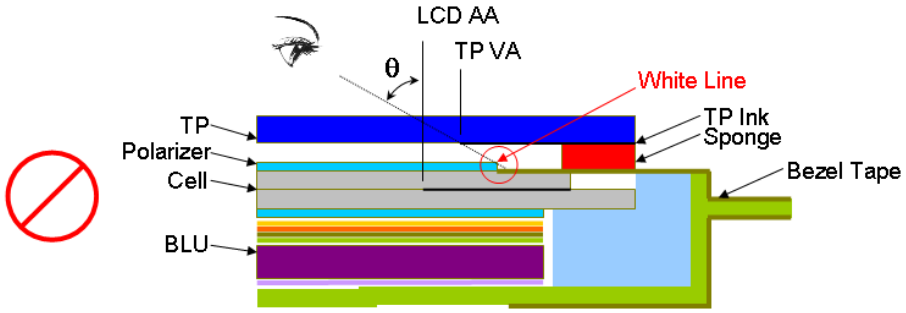
Definition	To prevent panel crack during system front-cover assembly process with hook design, it is not recommended to press panel or any location that related directly to the panel.
12	**Assembly SOP examination for system front-cover with Double tape design**

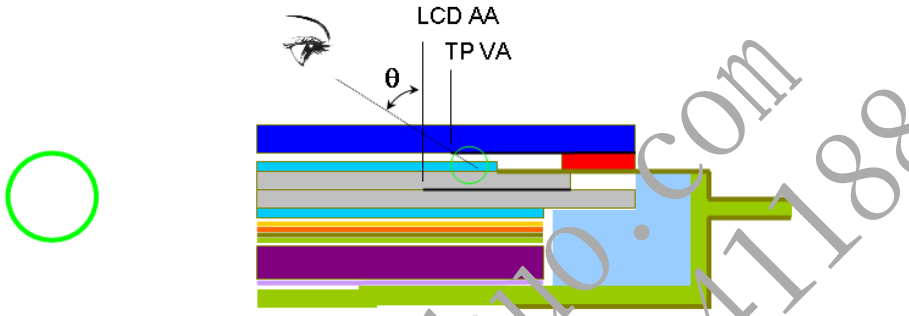


Definition	To prevent panel crack during system front-cover assembly process with double tape design, it is only allowed to give slight pressure (MAX 3 Kgf/50mm2) with large contact area. This can help to distribute the stress and prevent stress concentration. We also suggest putting the system on a flat surface stage to prevent unequal stress distribution during the assembly.
13	**System front-cover assembly reference with Double tape design**



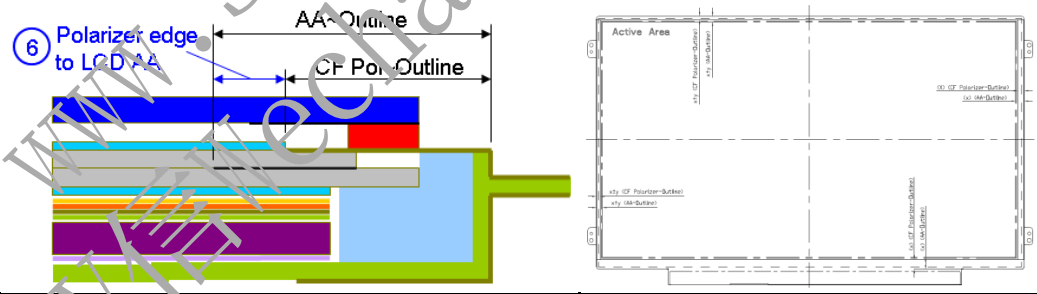
Definition	To prevent system front-cover peeling at double tape contact area, Height difference between system front-cover assembly reference such as wall or components stack (wire, spacer) and double tape top surface must be less than 0.05mm.
14	**Touch Application : TP and LCD Module Combination for White Line Prevention**



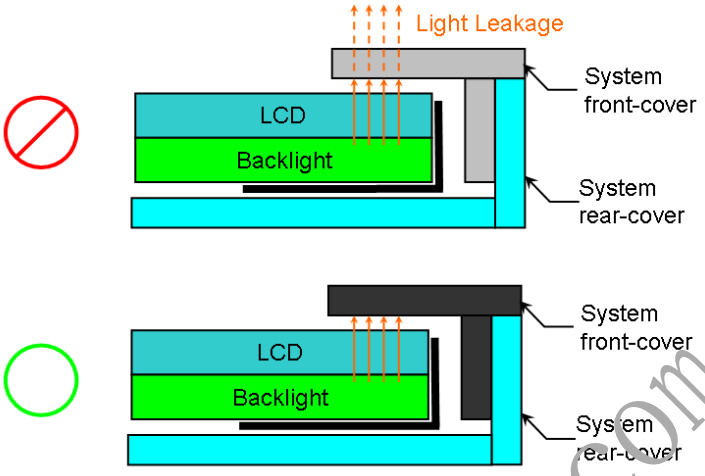
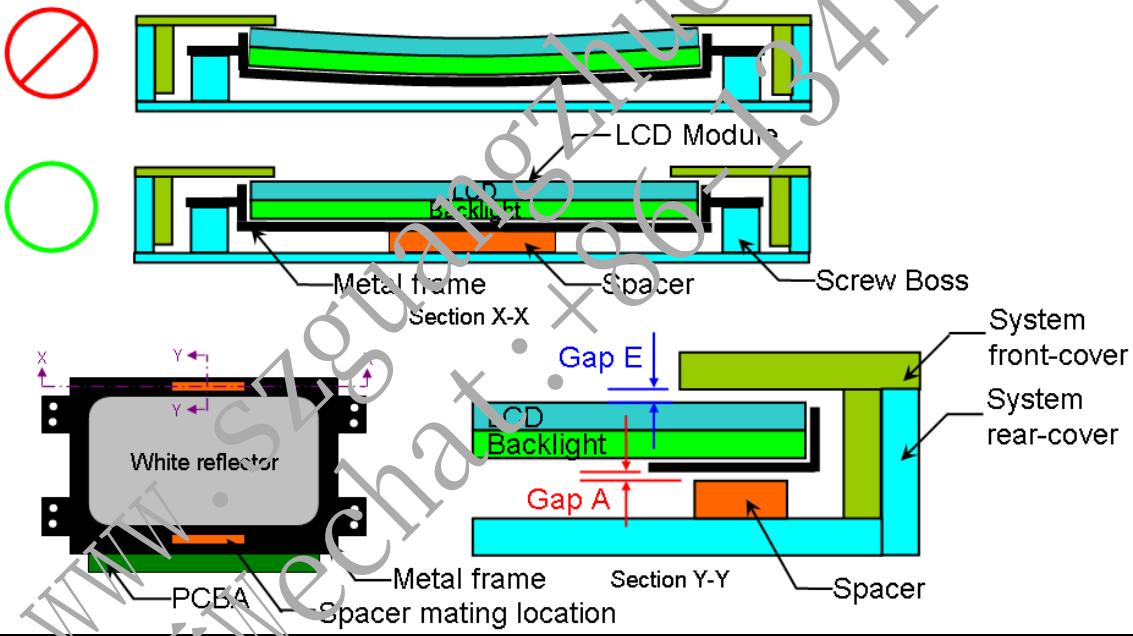


Parameter consideration for White Line Issue :	
1	TP VA to LCD AA distance
2	TP Assembly tolerance
3	TP Ink Printing tolerance
4	Sponge thickness and tolerance
5	Inspection/Viewing Angle specification
6	Polarizer edge to LCD AA distance and tolerance

Polarizer edge to LCD AA distance can be derived by “AA~Outline” – “CF Pol~Outline” with respect to INX 2D Outline Drawing on each side.



Definition	For using in Touch Application: to prevent White Line appears between TP and LCD module combination, the maximum inspection angle location must not fall onto LCD polarizer edge, otherwise light line near edge of polarizer will be appear. Parameters such as TP VA to LCD AA distance, TP assembly tolerance, TP Ink printing tolerance, Sponge thickness and tolerance, and Maximum Inspection/Viewing Angle, must be considered with respect to LCD module’s Polarizer edge location and tolerance. This consideration must be taken at all four edges separately. The goal is to find parameters combination that allow maximum inspection angle falls inside polarizer black margin area. Note: Information for Polarizer edge location and its tolerance can be derived from INX 2D Outline Drawing (“AA ~Outline“ - “CF Pol~Outline”). Note: Please feel free to contact INX FAE Engineer. By providing value of parameters above on each side, we can help to verify and pass the white line risk assessment for customer reference.

15	**Color of system front-cover material**
	
Definition	To prevent light leakage is seen at system front-cover due to material transparency, we suggest using dark color material (black) for system front-cover design.
16	**Inspection spec of gap E between system front-cover to LCD module surface**
	
Definition	To maintain gap E (gap of system front-cover to LCD module) in its inspection spec, especially at location with maximum LCD deformation (center of LCD length), we recommend adding spacer with design gap A smaller or equal to gap E. The allowable spacer mating location is on module metal frame outside LCD Active-Area. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.

Appendix. LCD MODULE HANDLING MANUAL

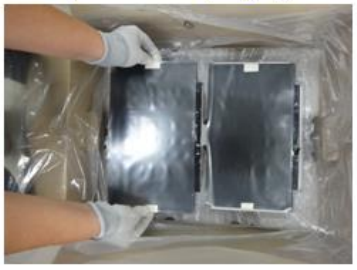
Purpose	• **This SOP is prepared to prevent panel dysfunction possibility through incorrect handling procedure.** • **This manual provides guide in unpacking and handling steps.** • **Any person which may contact / related with panel, should follow guide stated in this manual to prevent panel loss.**
1.	**Unpacking**

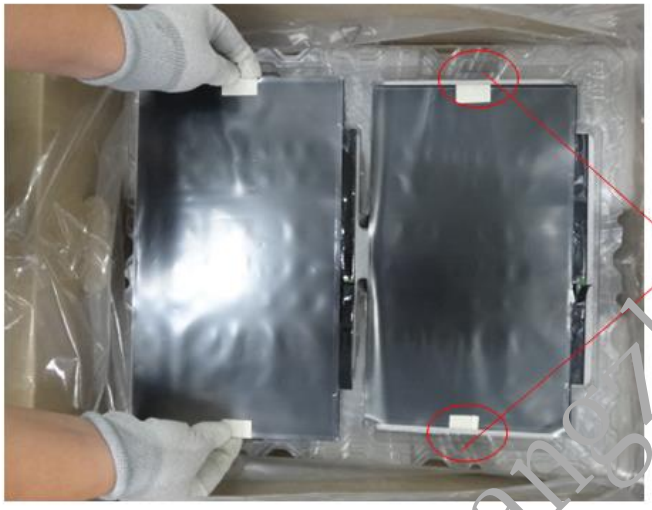
2.	**Panel Lifting**

Remove PET Cover

Remove PE Foam

Handle with care
(see next page)





Finger Slot

Use slots at both sides for finger insertion.
Handle panel upward with care.

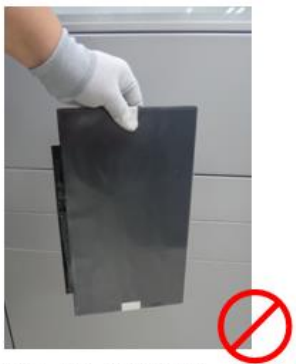
3.	Do and Don't

Do :

- Handle with both hands
- Handle panel at left and right edge

Don't :

- Lifting with one hand.



- Handle at PCBA side.

Don't :

- Stack panels.

- Press panel.

Don't :

- Put foreign stuff onto panel

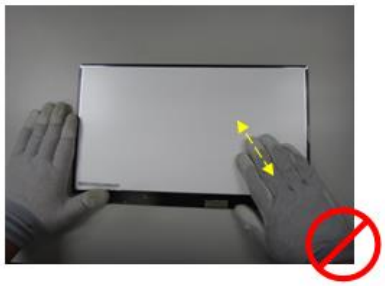
- Put foreign stuff under panel

Don't :

- Paste any material unto white reflector sheet

Don't :

- Pull / Push white reflector sheet



Don't :

- Hold at panel corner.

Don't :

- Twist panel.

Do :

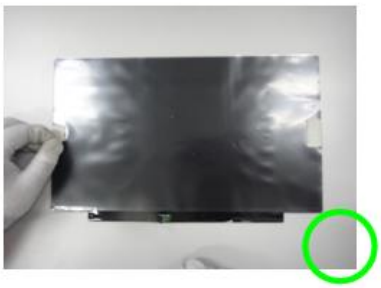
- Hold panel at top edge while inserting connector.

Don't :

- Press white reflector sheet while inserting connector.

Do :

- Remove panel protector film starts from side tape.



Don't :

- Remove panel protector film from film corner directly before side tape is removed.