SPECIFICATION
FOR
APPROVAL

(◆) **Preliminary Specification**
( ) **Final Specification**

Title	13.3” WQXGA TFT LCD

Customer	
MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	LP133WQ1
Suffix	SPH2

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

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Contents

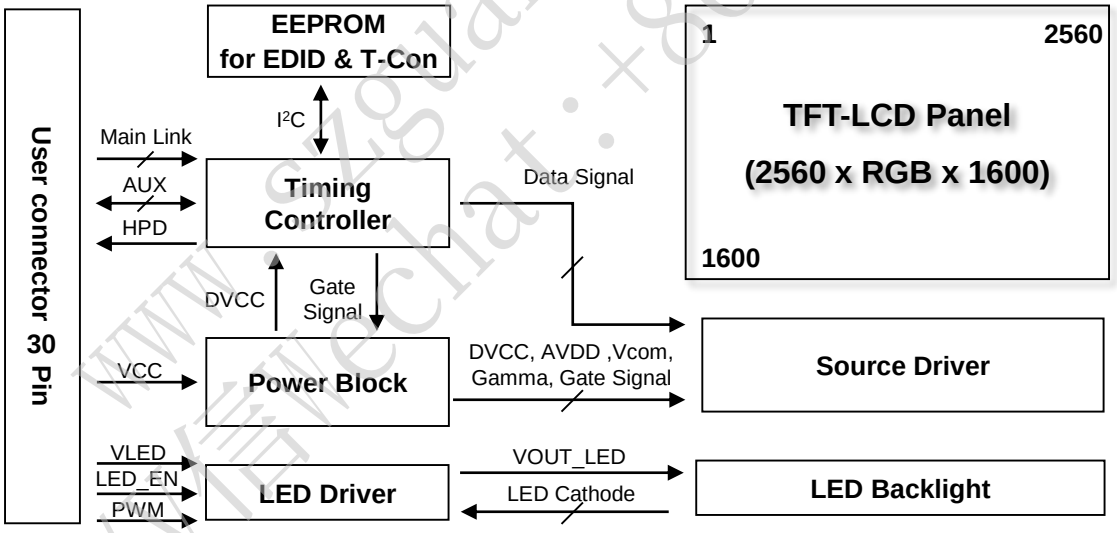
Record of Revisions

Revision No	Revision Date	Page	Before	After	EDID version
0.1	Jun. 08. 2022	All	First Draft (Preliminary Specification)	-	

1. General Description

1-1. Introduction

The LP133WQ1 is a Color Active Matrix Liquid Crystal Display with an integral LED backlight system. The matrix employs Oxide Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. This TFT-LCD has 13.3 inches diagonally measured active display area with WQXGA resolution (2560 horizontal by 1600 vertical pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 8-bit gray scale signal for each dot, thus, presenting a palette of more than 16,777,216 colors. The LP133WQ1 has been designed to apply the interface method that enables low power, high speed, low EMI. The LP133WQ1 is intended to support applications where thin thickness, low power are critical factors and graphic displays are important. In combination with the vertical arrangement of the sub-pixels, the LP133WQ1 characteristics provide an excellent flat display for office automation products such as Notebook PC.



1-2. General Feature

Active Screen Size		13.3 inches diagonal
Outline Dimension		291.08(H, Typ.) × 194.40(V, Typ. With PCB) × 2.00(D, Max. LCM Body) [mm]
Pixel Pitch		0.11175 mm x 0.11175 mm
Pixel Format		2560 horiz. by 1600 vert. Pixels RGB strip arrangement
Color Depth		8-bit, 16,777,216 colors
Luminance, White		400 cd/m^2(Typ.)
Power Consumption		Total : 3.52W (Typ.) Logic : 0.55W (Typ. @ Mosaic), B/L : 2.97W (Typ.)
Weight		175g (Max.)
Display Operating Mode		Normally black
Surface Treatment		Anti Glare treatment (3H) of the front Polarizer
Color Gamut		sRGB
LED Dimming Control mode		DC Dimming
RoHS Compliance		Yes
BFR / PVC / As Free		Yes for all
eDP version(Tcon)		eDP1.4
DPCD version		Ver1.3
Function	PSR	PSR2 + LRR2.5
	sDRRS	Not support
	DMRRS	Not support
	Adaptive sync	Freesync support
	NVSR	Not support
	SSC	Not support

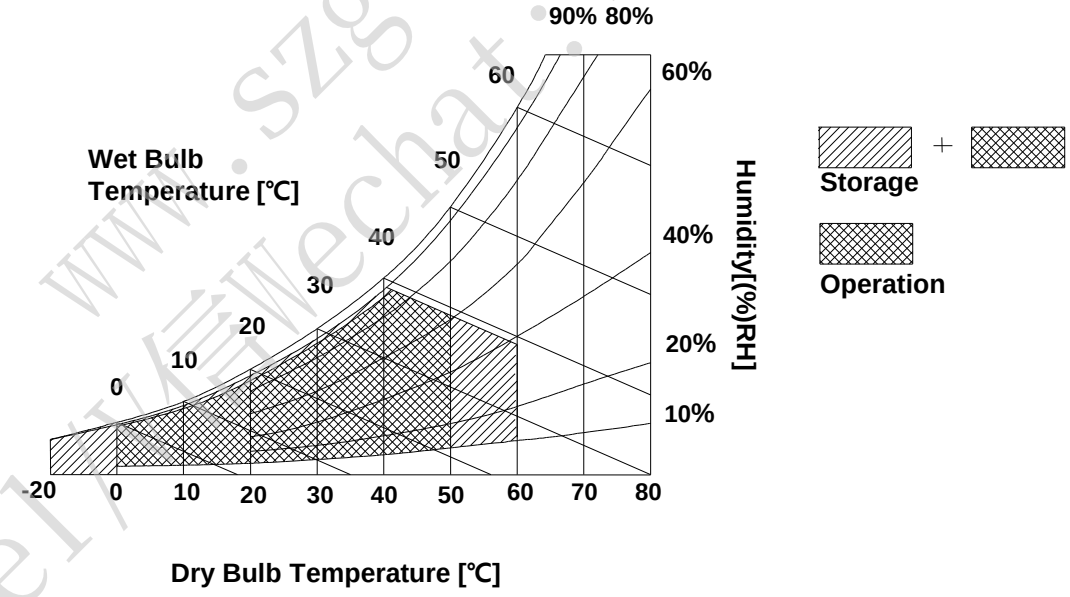
2. Absolute Maximum Ratings

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Values		Units	Notes
		Min	Max		
Power Input Voltage	VCC	-0.3	4.0	V_{DC}	at 25 ± 2°C
Operating Temperature	TOP	0	50	°C	1
Storage Temperature	TST	-20	60	°C	1,2
Operating Ambient Humidity	HOP	10	90	%RH	1
Storage Humidity	HST	10	90	%RH	1,2

Note : 1. Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39°C Max, and no condensation of water.
Note : 2. Storage Condition is guaranteed under packing condition.
Note : 3. Operating and storage conditions are guaranteed with 5~ 95% at Wet Bulb Temp 23~27 ℃



3. Electrical Specifications

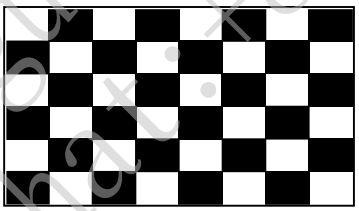
3-1. LCD Electrical Characteristics

Table 2. LCD ELECTRICAL CHARACTERISTICS

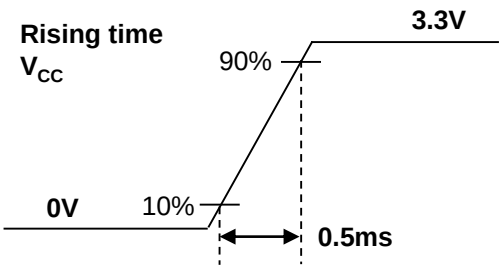
Parameter		Symbol	Values			Unit	Notes
			Min	Typ	Max		
Power Supply Input Voltage		V_{CC}	3.0	3.3	3.6	V	1
Permissive Power Supply Input Ripple		V_{CCrp}	-	-	100	mV_{p-p}	
Power Supply Input Current	Mosaic	I_{CC}	-	167	185	mA	2
Power Consumption		P_{CC}	-	0.55	0.61	W	
Power Supply Inrush Current		I_{CC_P}	-	-	1.5	A	3
Differential Impedance		Z_{eDP}	90	100	110	Ω	

Note)

1. The measuring position is the connector of LCM and the test conditions are under 25℃, fv = 60Hz
2. The specified I_{CC} current and power consumption are under the V_{CC} = 3.3V , 25℃, fv = 60Hz condition and Mosaic pattern.



3. The V_{CC} rising time is same as the minimum of T1 at Power on sequence.



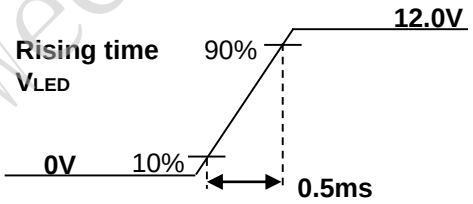
3-2. LED Backlight Electrical Characteristics

Table 3. LED B/L ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Values			Unit	Notes
			Min	Typ	Max		
LED Power Input Voltage		V_{LED}	5.0	12.0	21.0	V	1
LED Power Input Current		I_{LED}	-	247	255	mA	2
LED Power Consumption		P_{LED}	-	2.97	3.07	W	
LED Power Inrush Current		I_{LED_P}	-	-	1.5	A	3
PWM Duty Ratio			1	-	100	%	4
PWM Resolution			10			Bit	5
PWM Jitter			0	-	0.05	%	6
PWM Frequency		F_{PWM}	200	-	2000	Hz	7
PWM	High Level Voltage	V_{PWM_H}	2.5	-	3.6	V	
	Low Level Voltage	V_{PWM_L}	0	-	0.3	V	
	Rising Time	Tr_{PWM}	-	-	500	ns	
	Falling Time	Tf_{PWM}	-	-	500	ns	
LED_EN	High Voltage	$V_{LED\_EN\_H}$	2.5	-	3.6	V	
	Low Voltage	$V_{LED\_EN\_L}$	0	-	0.3	V	
Life Time			15,000	-	-	Hrs	8

Note)

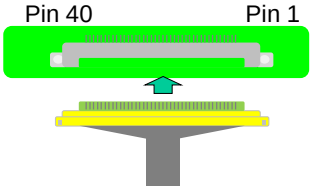
1. The measuring position is the connector of LCM and the test conditions are under 25℃.
2. The current and power consumption with LED Driver are under the V_{LED} = 12.0V , 25℃, PWM Duty 100% and White pattern with the normal frame frequency operated(60Hz).
3. The V_{LED} rising time is same as the minimum of T13 at Power on sequence.



4. The operation of LED Driver below minimum dimming ratio may cause flickering or reliability issue.
5. 10bit resolution means it's possible to change PWM duty by 0.1% step. (8bit operated by 0.4% step)
6. If Jitter of PWM is bigger than maximum, it may induce flickering.
7. This Spec. is not effective at 100% dimming ratio as an exception because it has DC level equivalent to 0Hz. In spite of acceptable range as defined, the PWM Frequency should be fixed and stable for more consistent brightness control at any specific level desired.
8. The life time is determined as the time at which brightness of LCD is 50% compare to that of minimum value specified in table 7. under general user condition.

3-3. Interface Connections

Table 4. MODULE CONNECTOR PIN CONFIGURATION (CN1)

Pin	Symbol	Description	Notes
1	NC Reserved	Reserved for LCD manufacturer's use	
2	GND	High Speed Ground	
3	Lane3_N	Complement Signal Link Lane 3	
4	Lane3_P	True Signal Link Lane 3	
5	GND	High Speed Ground	
6	Lane2_N	Complement Signal Link Lane 2	
7	Lane2_P	True Signal Link Lane 2	
8	GND	High Speed Ground	
9	Lane1_N	Complement Signal Link Lane 1	
10	Lane1_P	True Signal Link Lane 1	
11	GND	High Speed Ground	
12	Lane0_N	Complement Signal Link Lane 0	[Connector]
13	Lane0_P	True Signal Link Lane 0	LSC, GT05Q-40S-H10
14	GND	High Speed Ground	(40pin , 0.5pitch) or equivalent
15	AUX_CH_P	True Signal Auxiliary Channel	
16	AUX_CH_N	Complement Signal Auxiliary Channel	
17	GND	High Speed Ground	
18	VCC	LCD logic and driver power	[Connector pin arrangement]
19	VCC	LCD logic and driver power	Pin 40 Pin 1
20	VCC	LCD logic and driver power	
21	VCC	LCD logic and driver power	
22	LCD Self Test or NC	LCD Panel Self Test Enable (Optional)	
23	GND	LCD logic and driver ground	
24	GND	LCD logic and driver ground	
25	GND	LCD logic and driver ground	
26	GND	LCD logic and driver ground	
27	HPD	HPD signal pin	[LGD P-Vcom using information]
28	BL_GND	LED Backlight ground	1. Pin for P-Vcom : #34, #35
29	BL_GND	LED Backlight ground	2. P-Vcom Address : 0x9E
30	BL_GND	LED Backlight ground	
31	BL_GND	LED Backlight ground	
32	BL ENABLE	LED Backlight control on/off control	
33	BL PWM	System PWM signal input for dimming	
34	NC Reserved	Reserved for LCD manufacture's use	
35	NC Reserved	Reserved for LCD manufacture's use	
36	VLED	LED Backlight power (12V Typical)	
37	VLED	LED Backlight power (12V Typical)	
38	VLED	LED Backlight power (12V Typical)	
39	VLED	LED Backlight power (12V Typical)	
40	NC Reserved	Reserved for LCD manufacture's use	

3-3-1. Input/output signal circuit

Figure1.HPD Output circuit is as below

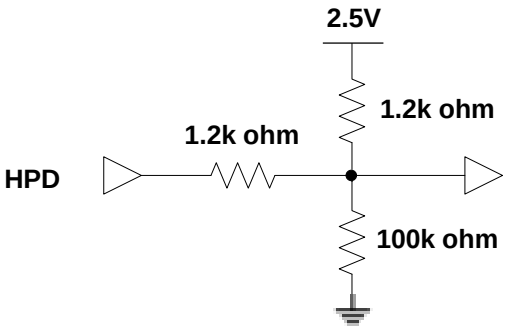


Figure2.BL PWM input circuit is as below

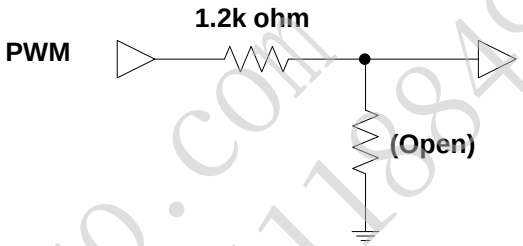


Figure3.BL Enable input circuit is as below

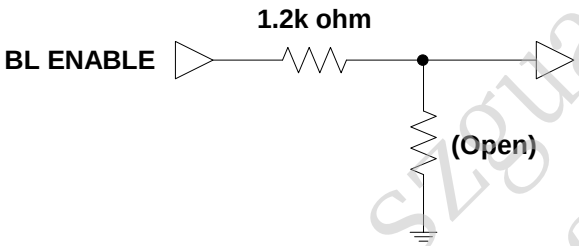


Figure4.BIST input circuit is as below

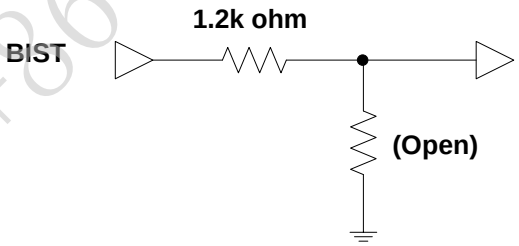
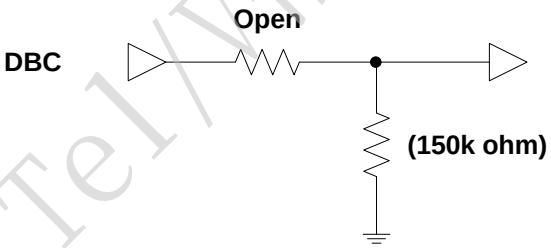
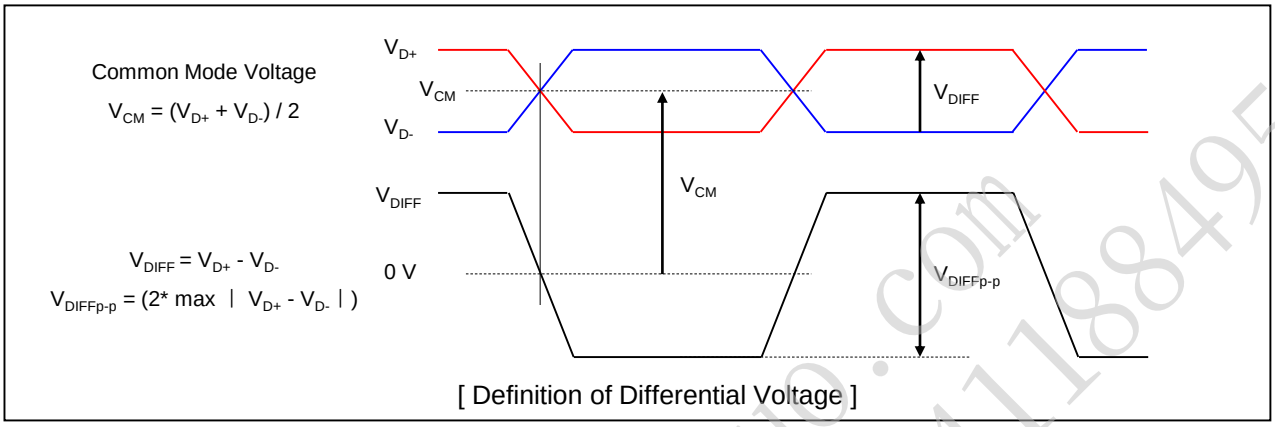


Figure5.DBC input circuit is as below



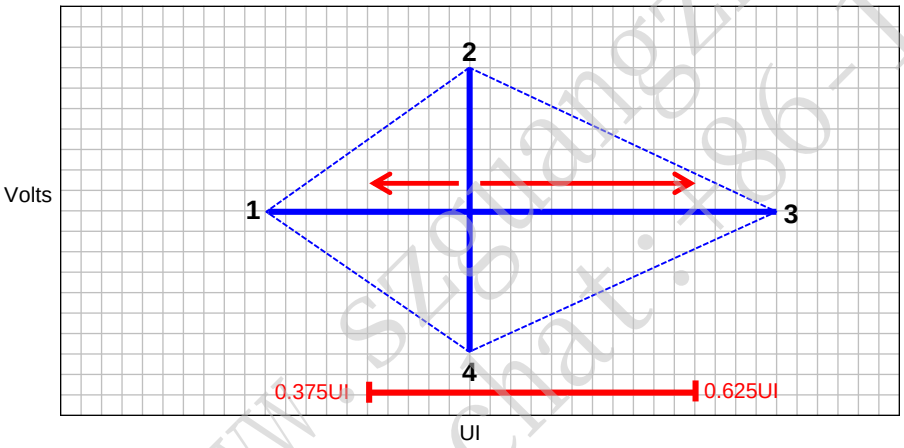
3-4. eDP Signal Timing Specifications

3-4-1. Definition of Differential Voltage



[Definition of Differential Voltage]

3-4-2. Main Link EYE Diagram



[EYE Mask at TP3_EQ/RX_EQ]

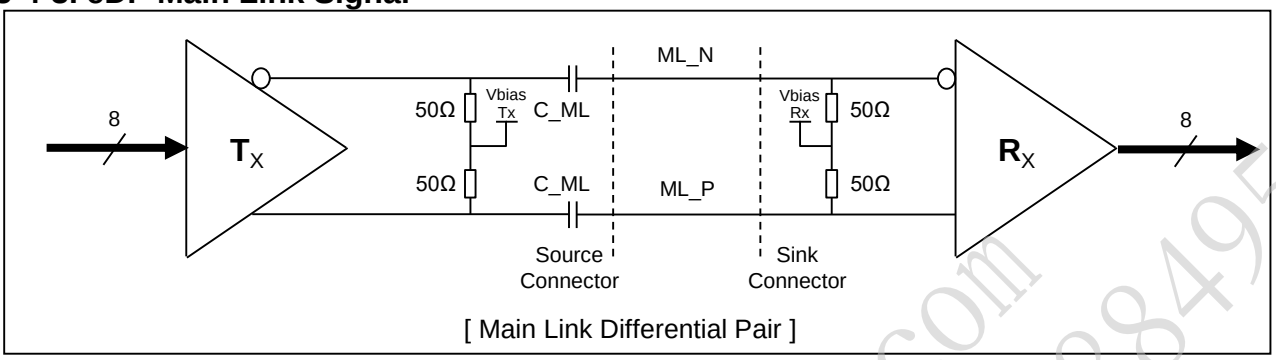
Point	Time(UI)	Voltage(V)
1	Any UI location (0mV)	0.000
2	0.375<point2<0.625	0.0375
3	Point1 + 0.5UI	0.000
4	0.375<point4<0.625	-0.0375

[eDP TP3_EQ EYE Mask Vertices]

Point	Time(UI)	Voltage(V)
1	Any UI location (0mV)	0.000
2	0.375<point2<0.625	0.035
3	Point1 + 0.45UI	0.000
4	0.375<point2<0.625	-0.035

[eDP RX_EQ EYE Mask Vertices]

3-4-3. eDP Main Link Signal

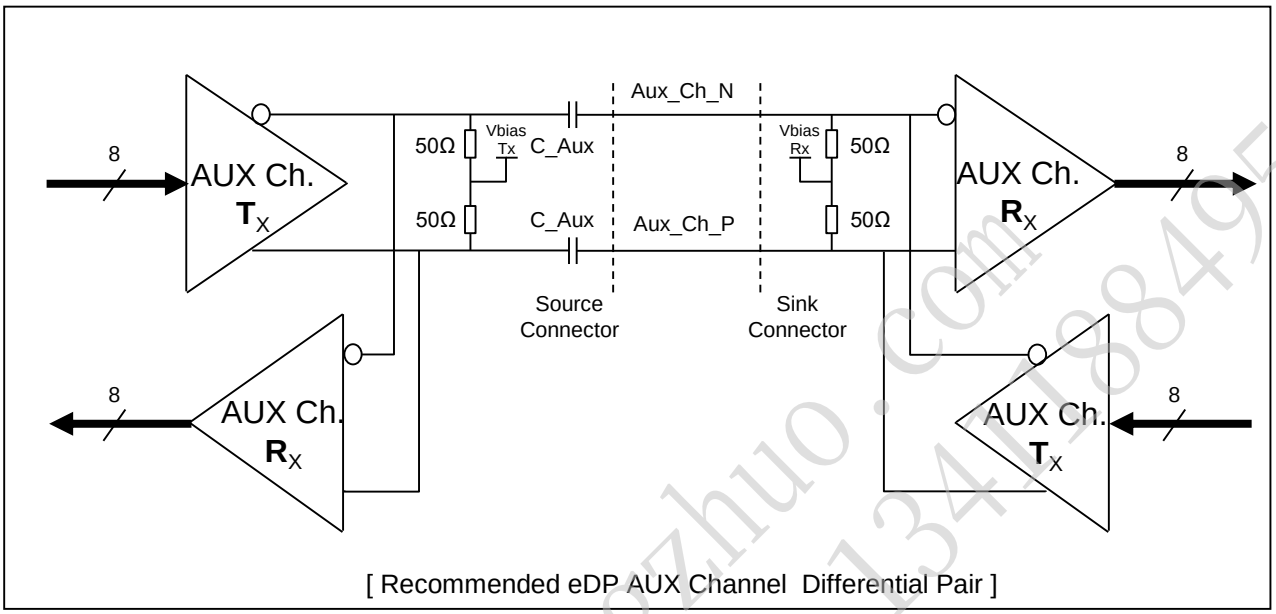


[Main Link Differential Pair]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval for high bit rate2 (5.4Gbps / lane)	UI_HBR2	-	185	-	ps	
Unit Interval for high bit rate (2.7Gbps / lane)	UI_HBR	-	370	-	ps	
Unit Interval for reduced bit rate (1.62Gbps / lane)	UI_RBR	-	617	-	ps	
Link Clock Down Spreading	Amplitude	0	-	0.5	%	
	Frequency	30		33	kHz	
Differential peak-to-peak voltage at Source side connector	$V_{TX-DIFFp-p}$	90	-	-	mV	For HBR2(5.4Gbps)
		350	-	-		For HBR(2.7Gbps)
		400	-	-		For RBR(1.62Gbps)
EYE width at Source side connector	$T_{TX-EYE-CONN}$	0.38			UI	For HBR(5.4Gbps)
		0.58	-	-		For HBR(2.7Gbps)
		0.75	-	-		For RBR(1.62Gbps)
Differential peak-to-peak voltage at Sink side connector	$V_{RX-DIFFp-p}$	70			mV	For HBR(5.4Gbps)
		150	-	-		For HBR(2.7Gbps)
		136	-	-		For RBR(1.62Gbps)
EYE width at Sink side connector	$T_{RX-EYE-CONN}$	0.38			UI	For HBR(5.4Gbps)
		0.51	-	-		For HBR(2.7Gbps)
		0.46	-	-		For RBR(1.62Gbps)
Rx DC common mode voltage	$V_{RX\ CM}$	0	-	1.0	V	
AC Coupling Capacitor	C_{SOURCE_ML}	75		200	nF	Source side

Note)
1. Termination resistor is typically integrated into the transmitter and receiver implementations.
2. AC Coupling Capacitor is not placed at the sink side.
3. In cabled embedded system, it is recommended the system designer ensure that EYE width and voltage are met at the sink side connector pins.

3-4-4. eDP AUX Channel Signal

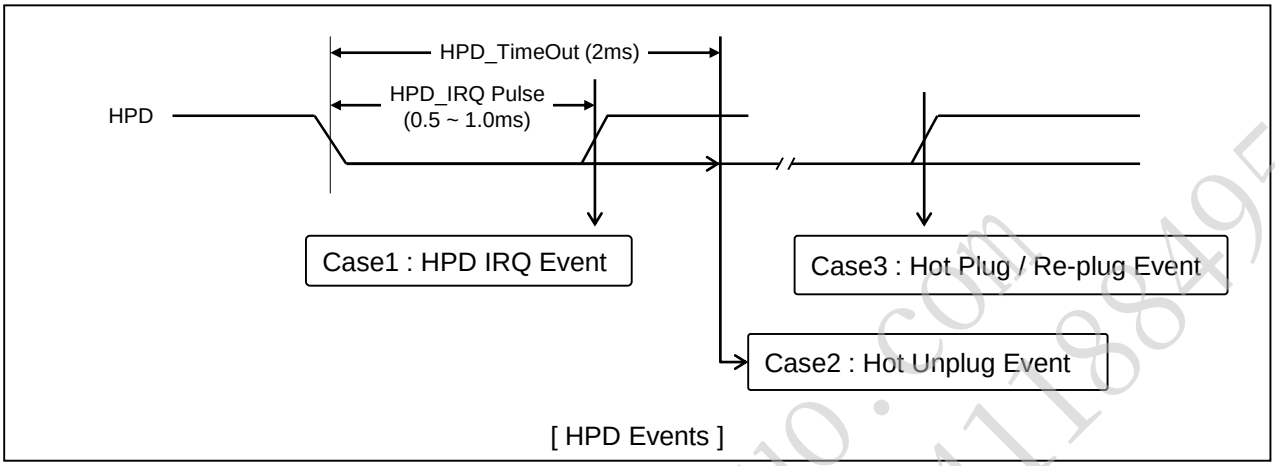


[Recommended eDP AUX Channel Differential Pair]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
AUX Unit Interval	UI	0.4	-	0.6	us	
AUX Jitter at Tx IC Package Pins	T_{jitter}	-	-	0.04	UI	Equal to 24ns
AUX Jitter at Rx IC Package Pins		-	-	0.05	UI	Equal to 30ns
AUX Peak-to-peak voltage at TX package pins (TP1)	$V_{AUX-DIFFp-p}$	0.18	0.20	1.38	V	
AUX Peak-to-peak voltage at TP3		0.14	-	1.36	V	
AUX EYE width at Connector Pins of Tx and Rx		0.98	-	-	UI	
AUX DC common mode voltage	V_{AUX-CM}	0	-	1.0	V	
AUX AC Coupling Capacitor	$C_{SOURCE-AUX}$	75		200	nF	Source side

Note)
1. Termination resistor is typically integrated into the transmitter and receiver implementations.
2. AC Coupling Capacitor is not placed at the sink side.
3. $V_{AUX-DIFFp-p}$ = 2* | V_{AUXP}-V_{AUXN} |

3-4-5. eDP HPD Signal



[HPD Events]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
HPD Voltage	HPD	2.25	-	3.6	V	Sink side Driving
Hot Plug Detection Threshold		2.0	-	-	V	Source side Detecting
Hot Unplug Detection Threshold		-	-	0.8	V	
HPD_IRQ Pulse Width	HPD_IRQ	0.5	-	1.0	ms	
HPD_TimeOut		2.0	-	-	ms	HPD Unplug Event

Note)
1. HPD IRQ : Sink device wants to notify the Source device that Sink's status has changed so it toggles HPD line, forcing the Source device to read its Link / Sink Receiver DPCD field via the AUX-CH
2. HPD Unplug : The Sink device is no longer attached to the Source device and the Source device may then disable its Main Link as a power saving mode
3. Plug / Re-plug : The Sink device is now attached to the Source device, forcing the Source device to read its Receiver capabilities and Link / Sink status Receiver DPCD fields via the AUX-CH

3-5. Signal Timing Specifications

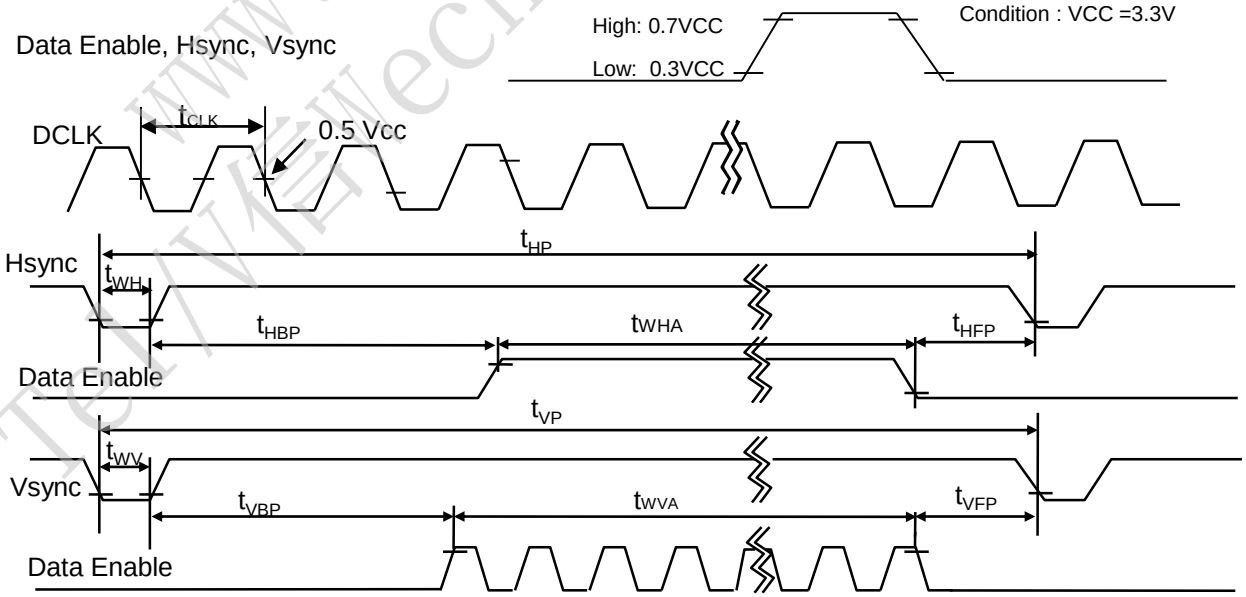
This is the signal timing required at the input of the User connector. All of the interface signal timing should be satisfied with the following specifications and specifications of eDP Tx/Rx for its proper operation.

Table 4. TIMING TABLE

ITEM	Symbol		Min	Typ	Max	Unit	Note
DCLK	Frequency	f_{CLK}	-	268.6	-	MHz	
Hsync	Period	t_{HP}	2712	2720	2728	t_{CLK}	
	Width	t_{WH}	28	32	36		
	Width-Active	t_{WHA}		2560			
Vsync	Period	t_{VP}	1645	1646	1647	t_{HP}	
	Width	t_{WV}	6	6	6		
	Width-Active	t_{WVA}		1600			
Data Enable	Horizontal back porch	t_{HBP}	78	80	82	t_{CLK}	
	Horizontal front porch	t_{HFP}	46	48	50		
	Vertical back porch	t_{VBP}	36	37	38	t_{HP}	
	Vertical front porch	t_{VFP}	3	3	3		

Notice. all reliabilities are specified for timing specification based on refresh rate of 60Hz. However, LP133WQ1 has a good actual performance even at lower refresh rate (e.g. 40Hz or 50Hz) for power saving Mode, whereas LP133WQ1 is secured only for function under lower refresh rate. 60Hz at Normal mode, 50Hz, 40Hz at Power save mode. Don't care Flicker level (Power save mode).

3-6. Signal Timing Waveforms



3-7. Color Input Data Reference

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color ; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Table 5. COLOR DATA REFERENCE

Color		Input Color Data																							
		RED								GREEN								BLUE							
		MSB							LSB	MSB							LSB	MSB							LSB
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED (0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	…				…								…								…				
	RED (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN (0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	...				...								...								...				
	GREEN (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	GREEN (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
BLUE	BLUE (0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	…				…								…								…				
	BLUE (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	BLUE (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

3-8. Power Sequence

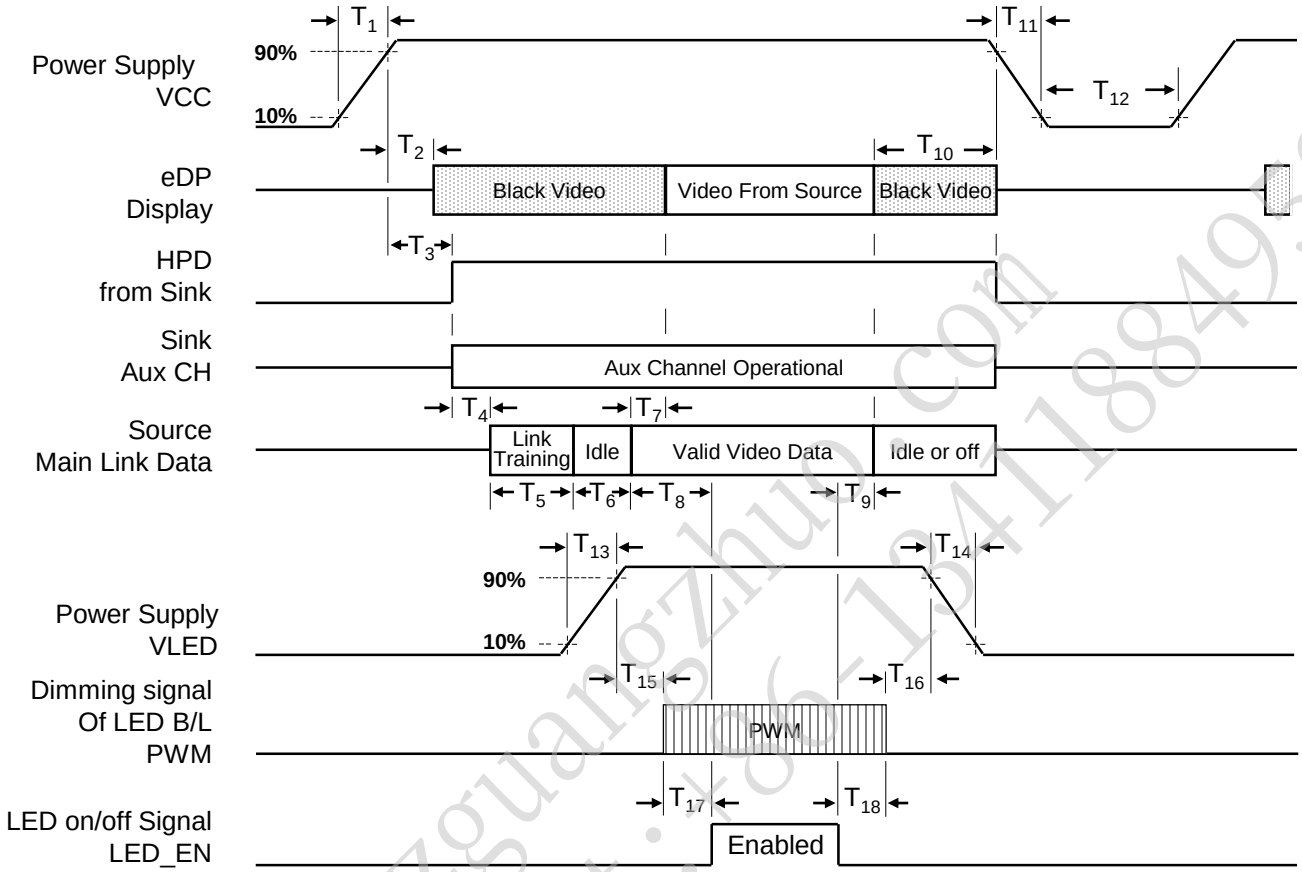


Table 6. POWER SEQUENCE TABLE

Symbol	Required By	Limits		Units	Notes	Symbol	Required By	Limits		Units	Notes
		Min	Max					Min	Max		
T_1	Source	0.5	10	ms	-	T_{10}	Source	0	500	ms	7
T_2	Sink	0	200	ms	-	T_{11}	Source	-	10	ms	-
T_3	Sink	0	200	ms	-	T_{12}	Source	500	-	ms	
T_4	Source	-	-	ms	-	T_{13}	Source	0.5	10	ms	-
T_5	Source	-	-	ms	-	T_{14}	Source	0.5	10	ms	-
T_6	Source	-	-	ms	-	T_{15}	Source	10	-	ms	-
T_7	Sink	0	50	ms	-	T_{16}	Source	10	-	ms	-
T_8	Source	-	-	ms	5	T_{17}	Source	0	-	ms	-
T_9	Source	-	-	ms	6	T_{18}	Source	0	-	ms	-

Note) 1. Do not insert the mating cable when system turn on.
2. Valid Data have to meet "3-3. eDP Signal Timing Specifications"
3. Video Signal, LED_EN and PWM need to be on pull-down condition on invalid status.
4. LGD recommend the rising sequence of VLED after the Vcc and valid status of Video Signal turn on.
5. Driving signal of B/L must be "On" after normal video signal (Normal operating data from source) input.
6. When VCC off, LED EN must be dropped to low level within black video data.(LGD recommend **-50 ~-100ms**)
7. For stable operation of BL, Black video data have to meet min **-100ms**.

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 20 minutes in a dark environment at 25°C. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of and θ equal to 0°.
FIG. 1 presents additional information concerning the measurement equipment and method.

FIG. 1 Optical Characteristic Measurement Equipment and Method

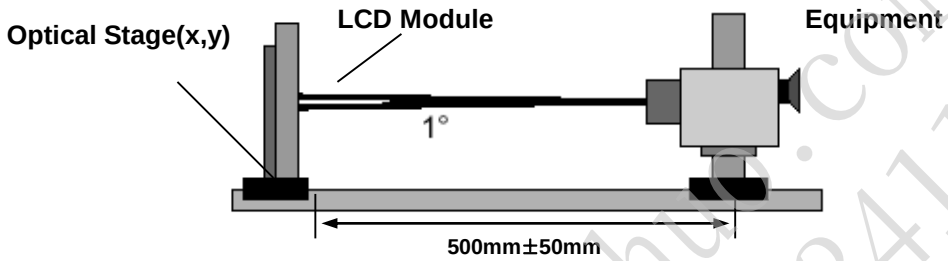


Table 7. OPTICAL CHARACTERISTICS

Ta=25°C, VCC=3.3V, fv=60Hz

Parameter		Symbol	Values			Units	Notes
			Min	Typ	Max		
Contrast Ratio		CR	1000	1300	-		1
Surface Luminance, white		L_{WH}	340	400	460	cd/m²	2
Luminance Variation		$\delta_{WHITE(5P)}$	80	-	-	%	3
		$\delta_{WHITE(13P)}$	60	70	-		
Response Time		Tr + Tf	-	30	35	ms	4
Color Gamut		sRGB	95%	100%	-		CIE 1931
Color Coordinates	RED	Rx	Typical - 0.025	0.650	Typical + 0.025	-	5
		Ry		0.330			
	GREEN	Gx		0.295			
		Gy		0.605			
	BLUE	Bx		0.145			
		By		0.055			
	WHITE	Wx		0.313			
		Wy		0.329			
Viewing Angle	x axis, right(Φ=0°)	θ_R	-	85	-	Degree	6
	x axis, left (Φ=180°)	θ_L	-	85	-		
	y axis, top (Φ=90°)	θ_T	-	85	-		
	y axis, bottom (Φ=270°)	θ_B	-	85	-		
Gray Scale							7

Note)

1. It should be measured in the center of screen(*P1*). Contrast Ratio(*CR*) is defined mathematically as

$$CR = \frac{Surface\ Luminance\ at\ Full\ White\ condition(P1)}{Surface\ Luminance\ at\ Full\ Black\ condition(P1)}$$

2. Surface luminance(L_{WH}) is the average of 5 point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see FIG 2.

$$L_{WH} = average\ luminance(P1, P2, P3, P4, P5)$$

3. The variation in surface luminance , The panel total variation (δ_{WHITE}) is determined by measuring at each test point 1 through 13 and then defined as following numerical formula. For more information see FIG 2.

$$\delta_{WHITE(5P)} = \frac{Minimum\ Luminance(P1, P2, P3, P4, P5)}{Maximum\ Luminance(P1, P2, P3, P4, P5)} \times 100$$

$$\delta_{WHITE(13P)} = \frac{Minimum\ Luminance(P1, P2, \cdots, P12, P13)}{Maximum\ Luminance(P1, P2, \cdots, P12, P13)} \times 100$$

4. Response time is the time required for the display to transition from black to white (rise time, Tr) and from white to black (falling time, Tf). For additional information see FIG 3.

5. It should be measured in the center of screen (*P1*).
Color coordinates must be measured with the equipment which has optical wavelength resolution of under 2㎚. (ex. PR-670, PR-680, CS-2000/2000A….)

6. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 4.

7. Gray scale specification

Gray Level	Luminance [%] (Typ)
L0	0.06
L31	1.03
L63	4.67
L95	11.22
L127	21.68
L159	35.71
L191	52.64
L223	74.54
L255	100

FIG. 2 Luminance

< Luminance & Luminance Variation Measuring Point >

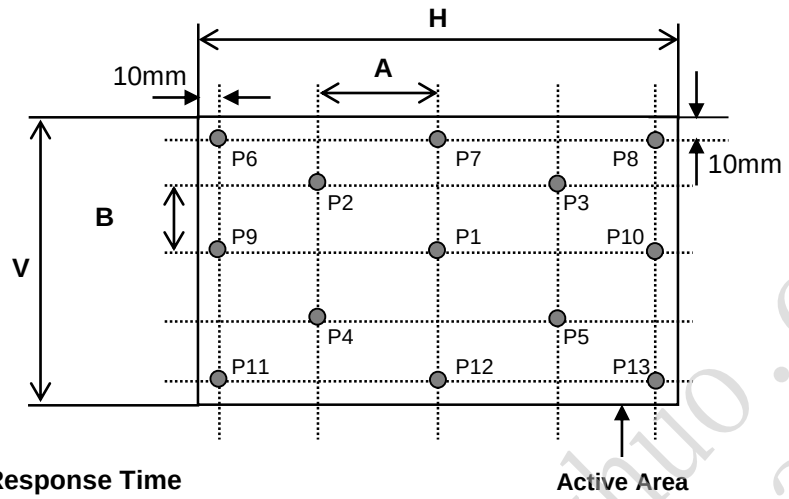


FIG. 3 Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white”.

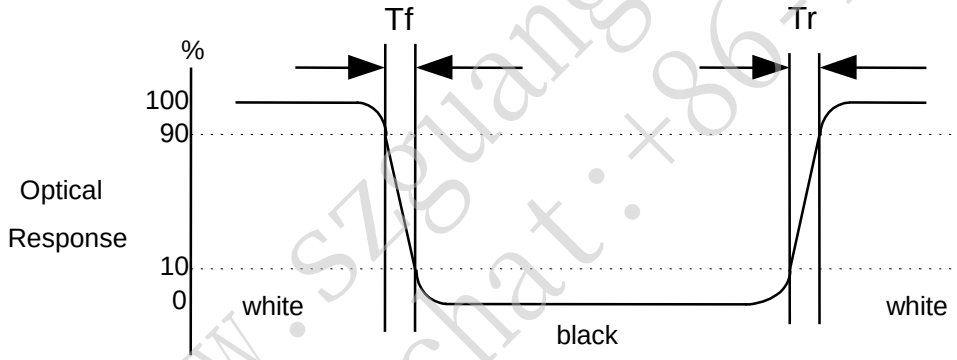
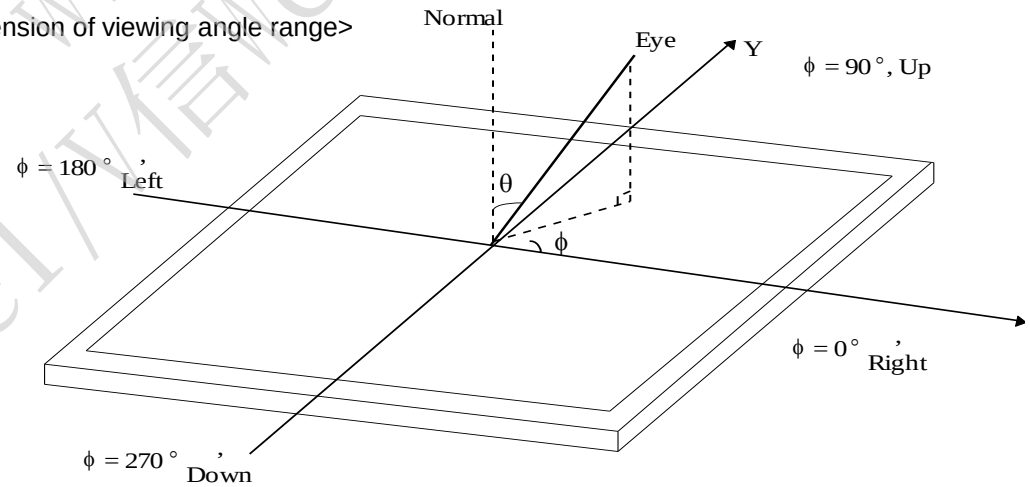


FIG. 4 Viewing angle

<Dimension of viewing angle range>



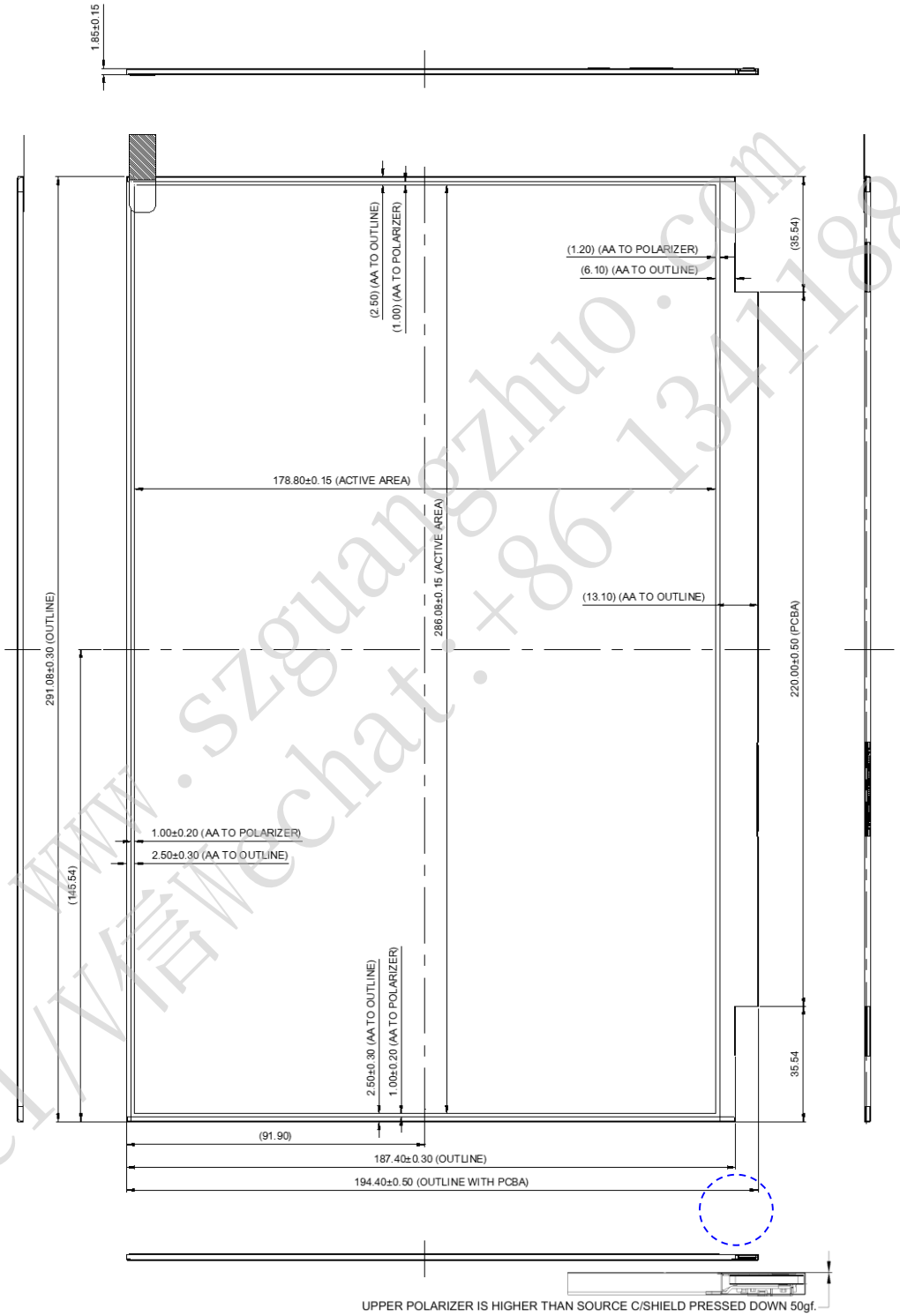
5. Mechanical Characteristics

The contents provide general mechanical characteristics for the model LP133WQ1. In addition the figures in the next page are detailed mechanical drawing of the LCD.

Outline Dimension	Horizontal	291.08 ± 0.3 mm
	Vertical	194.40 ± 0.5 mm (with PCB)
	Thickness	2.00 Max
Upper Polarizer Dimension	Horizontal	288.08 ± 0.2 mm
	Vertical	181.00 ± 0.2 mm
Active Display Area	Horizontal	286.08 mm ± 0.15mm
	Vertical	178.80 mm ± 0.15mm
Weight	175g (Max.)	
Surface Treatment	Anti Glare treatment(3H) of the front polarizer	

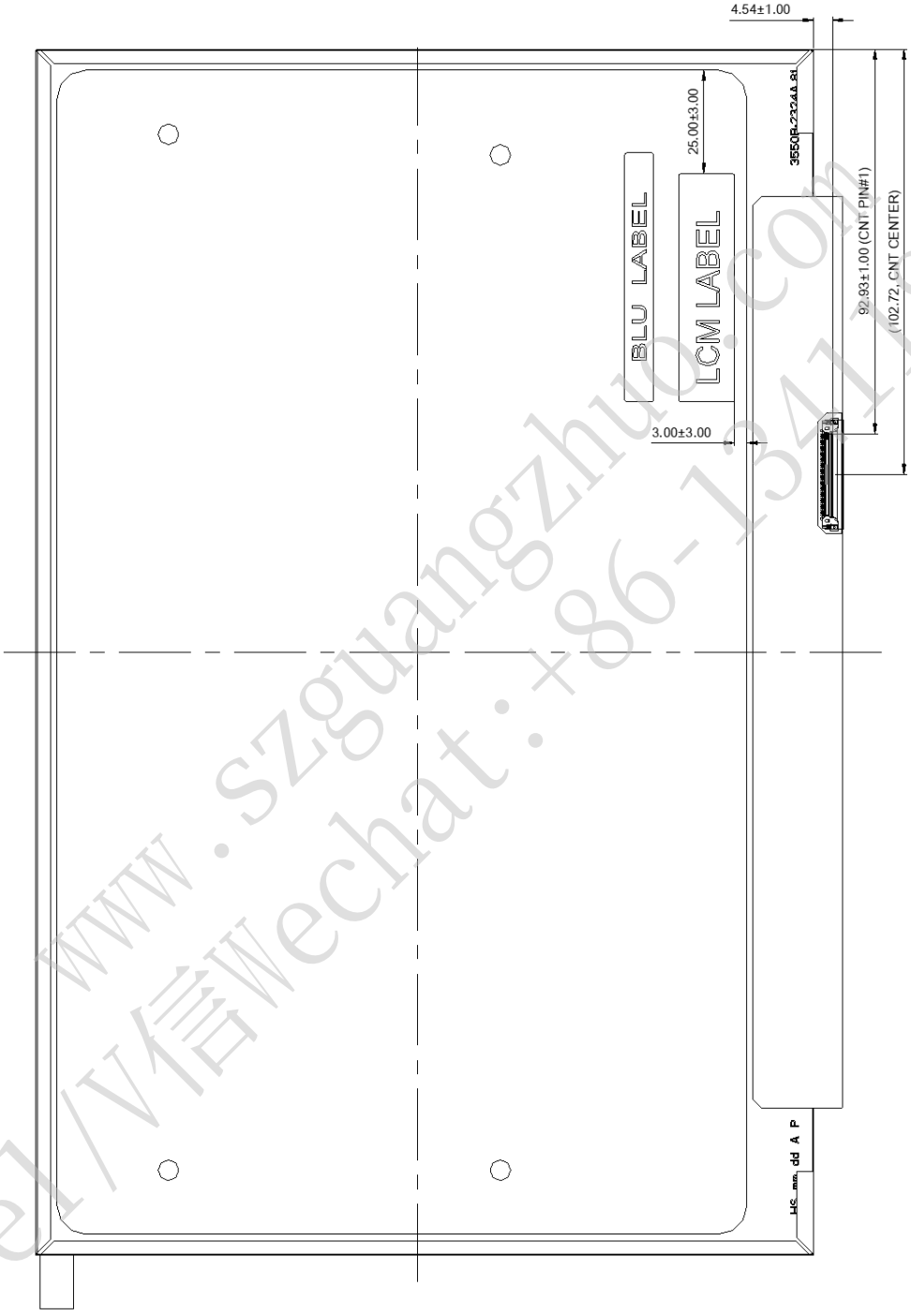
<FRONT VIEW>

Notes (Measurement method refer to the Appendix D)
1) Unit[mm], General tolerance : ± 0.5mm
2) All components except cover shield of LCM is under upper POL.
3) Warpage Spec : Max ±0.5mm



<REAR VIEW>

Notes
1) Unit[mm], General tolerance : ± 0.5mm
2) LCM Label Information refer to the page 25.



6. Reliability

Environment test condition

No.	Test Item	Conditions
1	High temperature storage test	Ta= 60°C, 240h
2	Low temperature storage test	Ta= -20°C, 240h
3	High temperature operation test	Ta= 50°C, 50%RH, 240h
4	Low temperature operation test	Ta= 0°C, 240h
5	Vibration test (non-operating)	Random, 1.0Grms, 10 ~ 300Hz(PSD 0.0035) 3 axis, 30min/axis
6	Shock test (non-operating)	- No functional or cosmetic defects following a shock to all 6 sides delivering at least 180 G in a half sine pulse no longer than 2 ms to the display module - No functional defects following a shock delivering at least 200 g in a half sine pulse no longer than 2 ms to each of 6 sides. Each of the 6 sides will be shock tested with one each display, for a total of 6 displays
7	Altitude operating storage / shipment	0 ~ 10,000 feet (3,048m) 24Hr 0 ~ 40,000 feet (12,192m) 24Hr
8	ESD	± 8kV for contact discharge ± 15kV for air discharge

[Result Evaluation Criteria]

1. Comparing the initial functional FOS status, there should be no major change which might affect the practical display function when the display reliability test is conducted.

2. After conduct reliability tests, LGD guarantees only functional FOS quality.

3. In the Reliability Test, Confirm performance after leaving in room temp.

4. In the standard condition, there shall be no practical problems that may affect the display function 24 hours later after reliability test. After the reliability test, we can guarantee the product only when the corrosion is causing its malfunction. The corrosion causing no functional defect can not be guaranteed.

7. International Standards

7-1. Safety

a) UL 60950-1, Underwriters Laboratories Inc.
Information Technology Equipment - Safety - Part 1 : General Requirements.
b) CAN/CSA-C22.2 No. 60950-1-07, Canadian Standards Association.
Information Technology Equipment - Safety - Part 1 : General Requirements.
c) EN 60950-1, European Committee for Electro technical Standardization (CENELEC).
Information Technology Equipment - Safety - Part 1 : General Requirements.
d) IEC 60950-1, The International Electro technical Commission (IEC).
Information Technology Equipment - Safety - Part 1 : General Requirements

7-2. Environment

a) RoHS, Directive 2011/65/EU of the European Parliament and of the council of 8 June 2011

8. Packing

8-1. Designation of Lot Mark

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M

A,B,C : SIZE(INCH)
D : YEAR
E : MONTH
F ~ M : SERIAL NO.

TBD

Note

1. YEAR

Year	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029
Mark	K	L	M	N	P	R	S	T	U	V

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

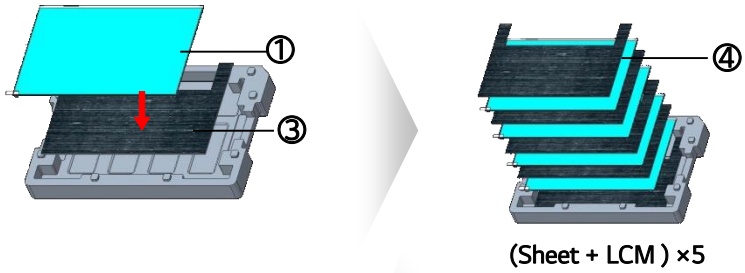
Serial No. is printed on the label. The label is attached to the backside of the LCD module.
This is subject to change without prior notice.

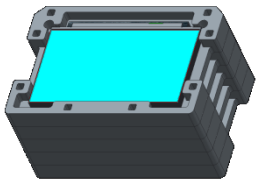
8-2. Packing Form

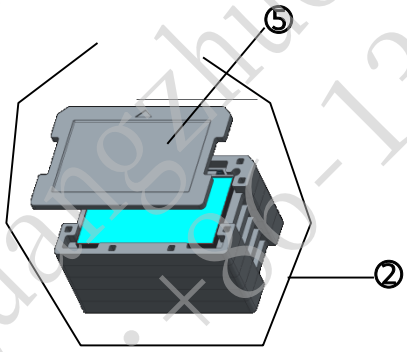
a) Package quantity in one box : 35 pcs

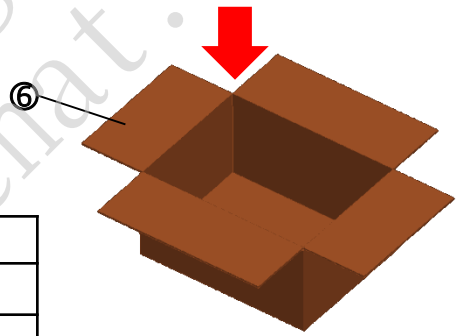
b) Box Size : 410*278*328

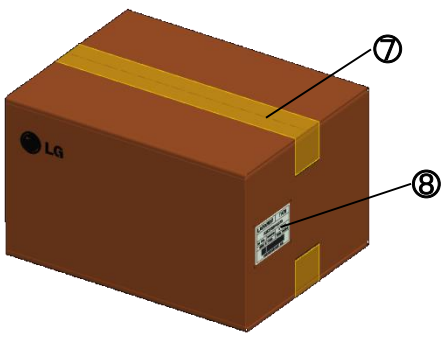
8-3. Packing Assembly











5 LCM / Tray

7 Tray / Bpx

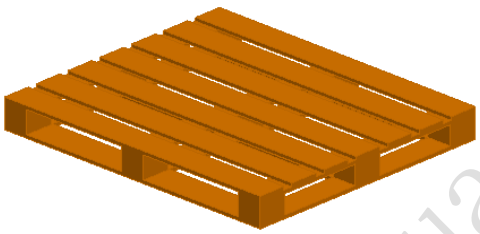
35LCM/Box

2EA Desiccant in the box

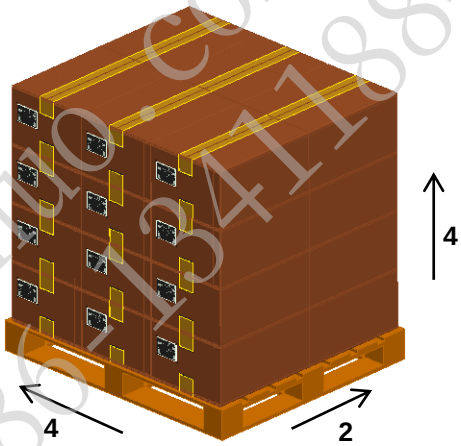
NO.	DESCRIPTION	MATERIAL
1	LCD Module	
2	BAG	AL
3	Cushion	PE
4	Bottom Tray	EPO
5	Top Tray	EPO
6	BOX	SWR4
7	TAPE	OPP 70MMX300M
8	LABEL	ART 100X70

8-4 Pallet Assembly

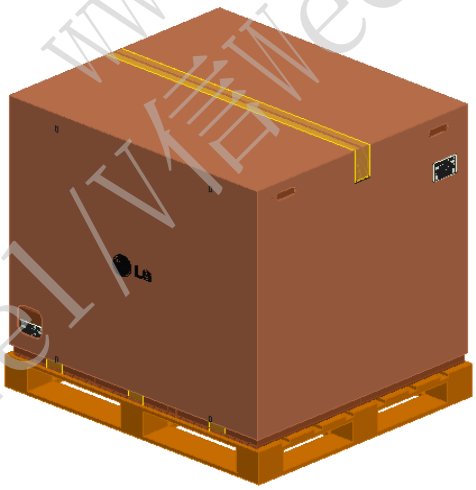
1. Pallet Ready



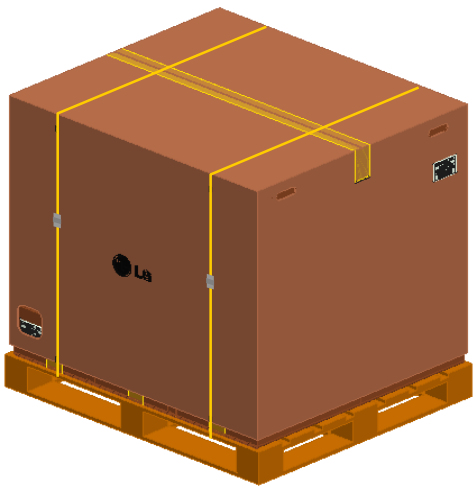
2. 4 x 2 x 4 Box Pattern



3. Angle Packing & Taping

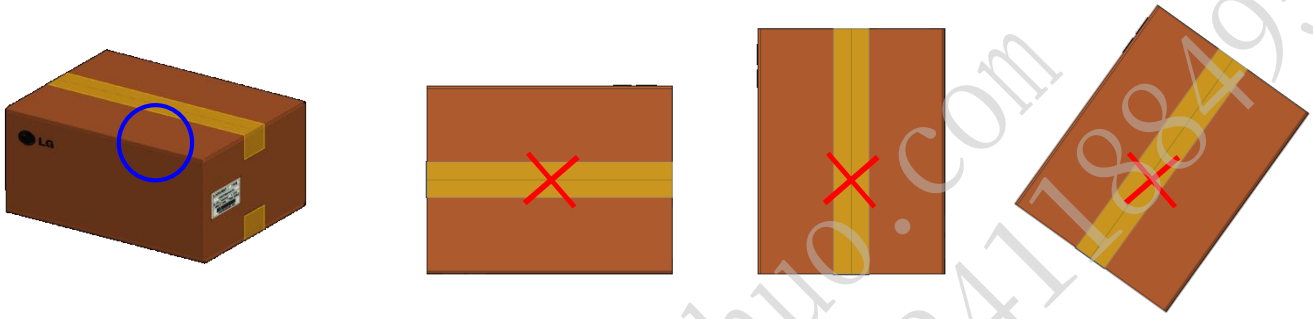


4. Banding

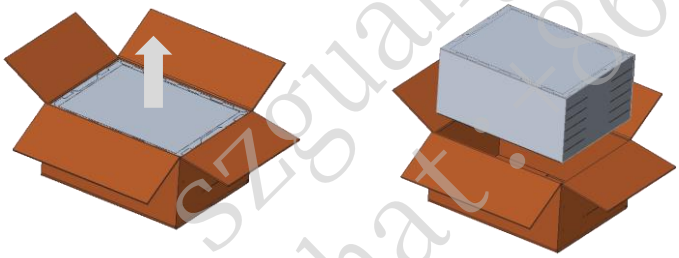


8-4. Precautions for unpacking the Box

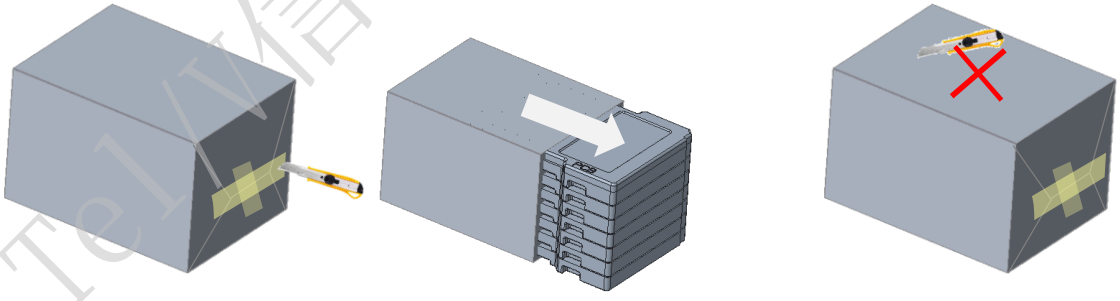
a.) Don't throw or tilt the box and put it on a flat surface.



b.) Place the box on a flat floor and Take out the AL bag vertically.



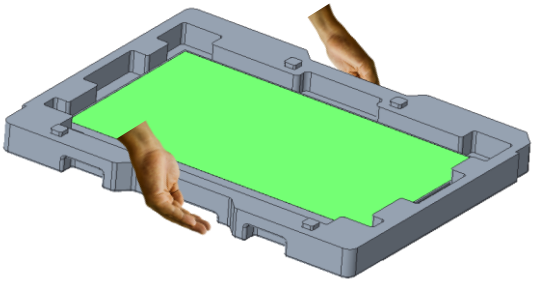
c.) Cut the tape on the side of the bag with a knife and Take out the tray horizontally.

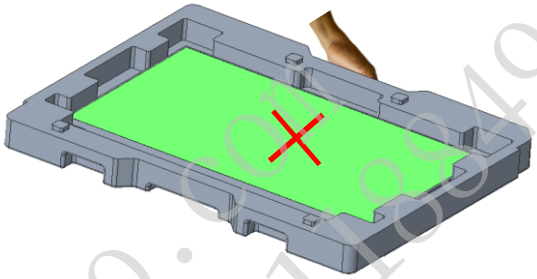


Caution : Do not cut the top of the bag with a knife.
(The Knife can damage product)

8-5. Precautions for Handling tray

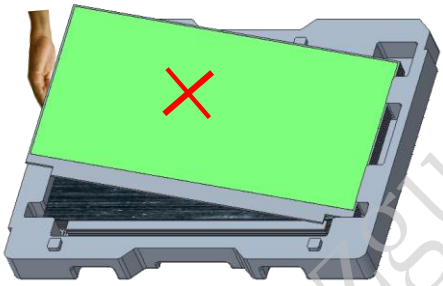
a.) Hold center of short or long side of the tray with both hands when handling one or more trays.

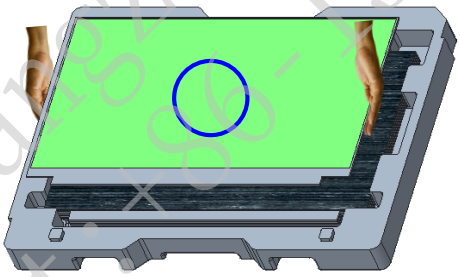




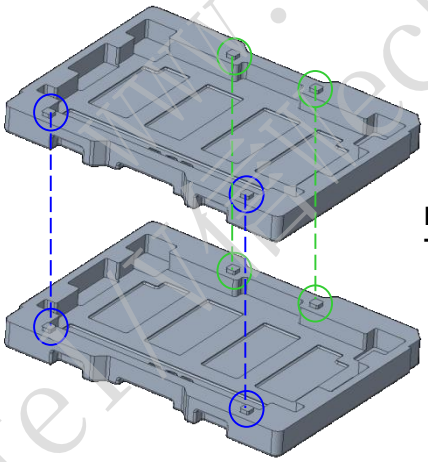
Caution : Do not handle with only one hand.

b.) Always place tray on flat surface and Don't tilt with one hand to take out.





c.) When stacking trays, Please align same position of the protrusion of each tray.



If not Aligned,
The tray may slip without being loaded.

d.) The maximum stacking quantity is equal to the number of loads per box.

- Recommended as above because heavier weight can cause muscular skeletal disease and operator handling errors.

9. PRECAUTIONS

Please pay attention to the followings when you use this TFT LCD module.

9-1. MOUNTING PRECAUTIONS

(1) You must mount a module using holes arranged in four corners or four sides.
(2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(4) You should adopt radiation structure to satisfy the temperature specification.
(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(9) Do not open the case because inside circuits do not have sufficient strength.
(10) When handling the LCD module, it needs to handle with care not to give mechanical stress to the PCB and Mounting Hole area."

9-2. OPERATING PRECAUTIONS

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=± 200mV(Over and under shoot voltage)

(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
(4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.

9-3. ELECTROSTATIC DISCHARGE CONTROL

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-4. PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter.

9-5. STORAGE

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

9-6. HANDLING PRECAUTIONS FOR PROTECTION FILM

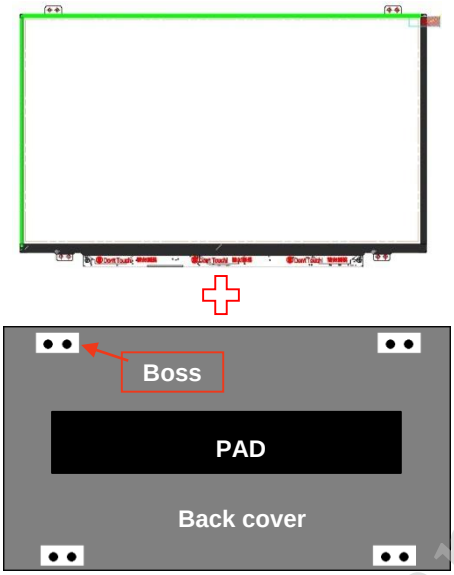
(1) When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) The protection film is attached to the polarizer with a small amount of glue. If some stress is applied to rub the protection film against the polarizer during the time you peel off the film, the glue is apt to remain on the polarizer.
Please carefully peel off the protection film without rubbing it against the polarizer.
(3) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.
(4) You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

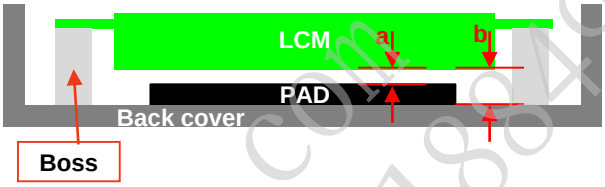
9-7. THE LGD QA RESPONSIBILITY WILL BE AVOIDED IN CASE OF BELOW

(1) When the customer attaches TSM(Touch Sensor Module) on LCM without Supplier's approval.
(2) When the customer attaches cover glass on LCM without Supplier's approval.
(3) When the LCMs were repaired by 3rd party without Supplier's approval.
(4) When the LCMs were treated like Disassemble and Rework by the Customer and/or Customer's representatives without supplier's approval.

APPENDIX A. LGD Proposal for system cover design

1	**Gap check for securing the enough gap between LCM and System back cover.**

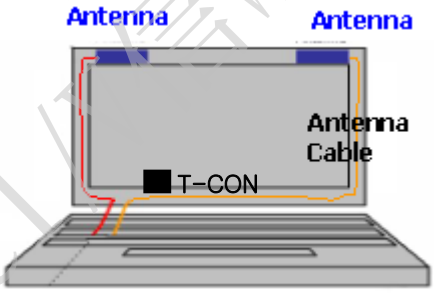




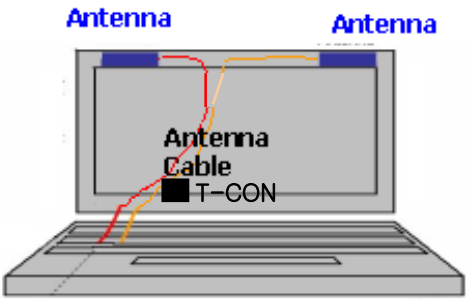
◆ a : min 0mm
◆ b : min 0.3mm, Max 1.0mm

Define	1. Rear side of LCM is sensitive against external stress, and previous check about interference is highly needed.
	2. In case there is something from system cover comes into the boundary above, mechanical interference may cause the FOS defects. (e.g.. Ripple, White spot..)

2	**Check if antenna cable is sufficiently apart from T-CON of LCD Module.**



OK

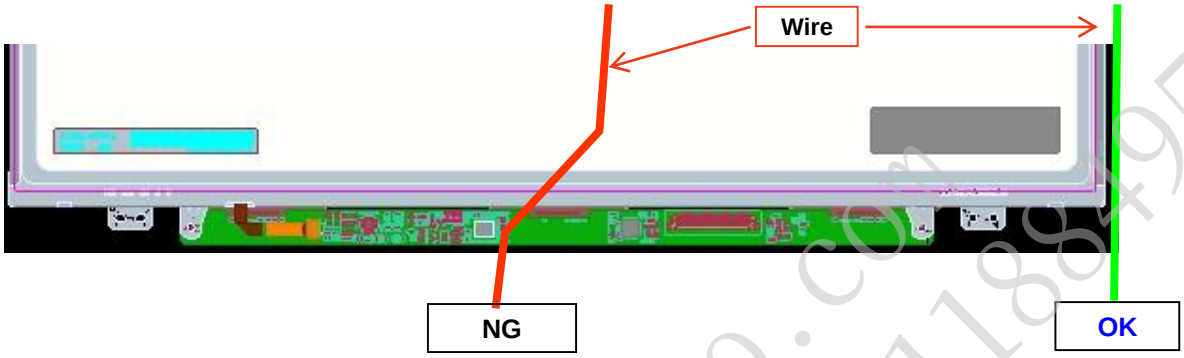


NG

Define	If system antenna is overlapped with T-CON, It might be cause the noise

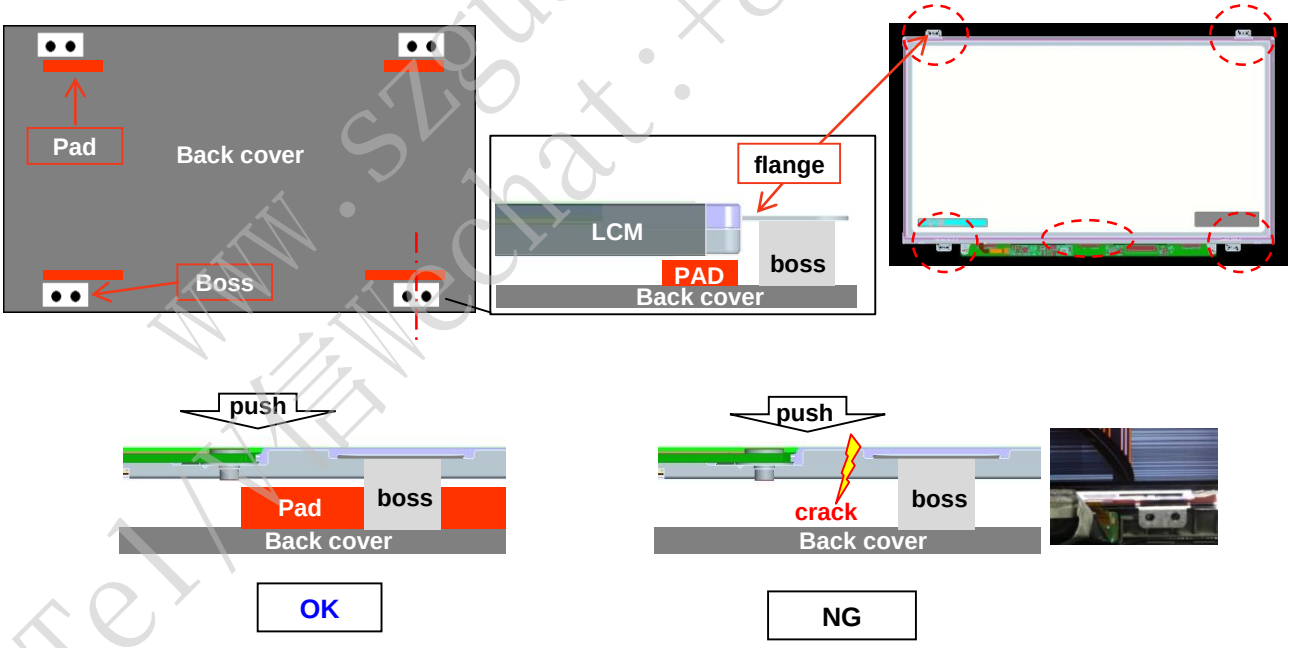
APPENDIX A. LGD Proposal for system cover design

3	Checking the path of the System wire



Define	1. If Wire path overlapped with LCM, it is happened white spot. COF problem, etc.
	2. OK ➔ Wire path design to system side. NG ➔ Wire path overlapped with LCM.

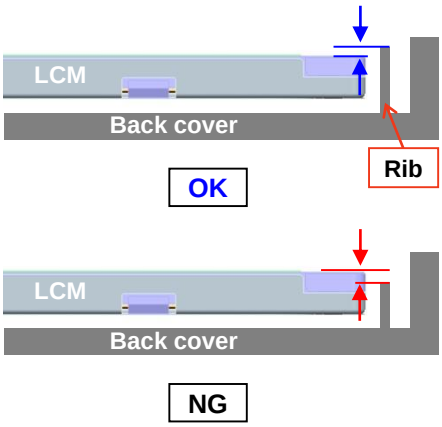
4	Add pad to Prevent panel crack against external load (push)

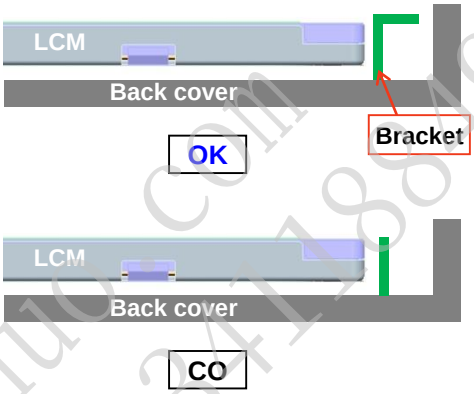


Define	1. At flat type LCM, panel is easily cracked at flange area during push, assemble.
	2. Add pad, it prevent panel crack

APPENDIX A. LGD Proposal for system cover design

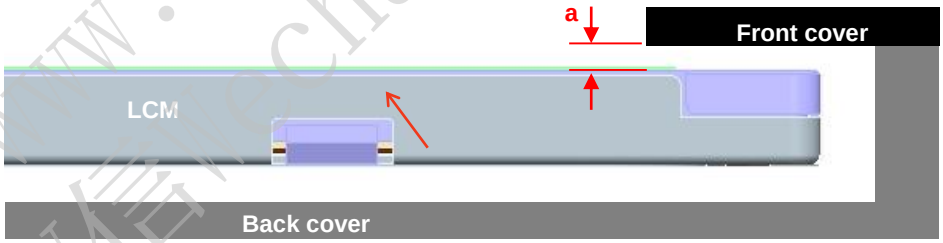
5	Check the rib or Bracket on back cover





Define	1.It is necessary that the height of back cover rib or bracket is higher than LCM height. It can prevent direct compression of panel at LCM edge.
	2.”ㄱ” shape bracket is stronger than “I” shape one.

6	Check the gap between front cover and LCM (glass)

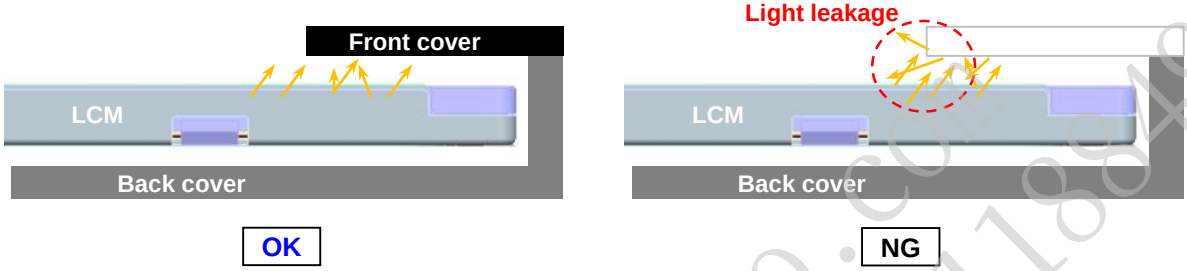


[OK] a ≥ 0.3mm
[CO] 0.3mm ≥ a ≥ 0.1mm
[NG] a ≤ 0.1mm

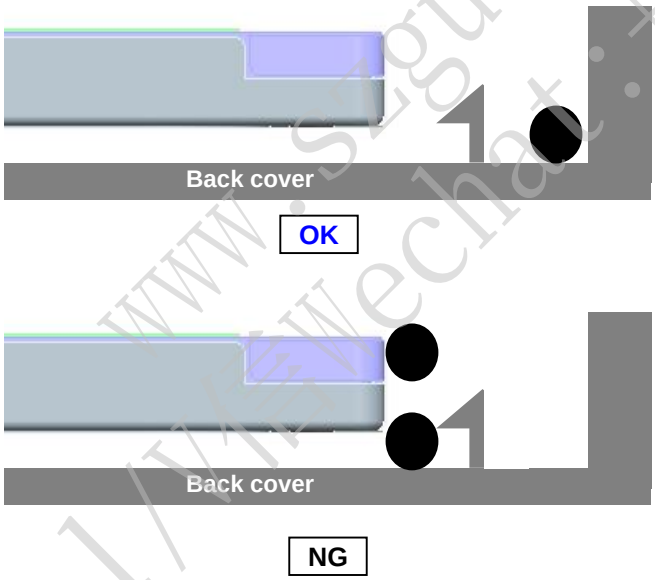
Define	Ripple can be happened by little gap between glass and front cover.

APPENDIX A. LGD Proposal for system cover design

7	**Check the rib or Bracket on back cover**



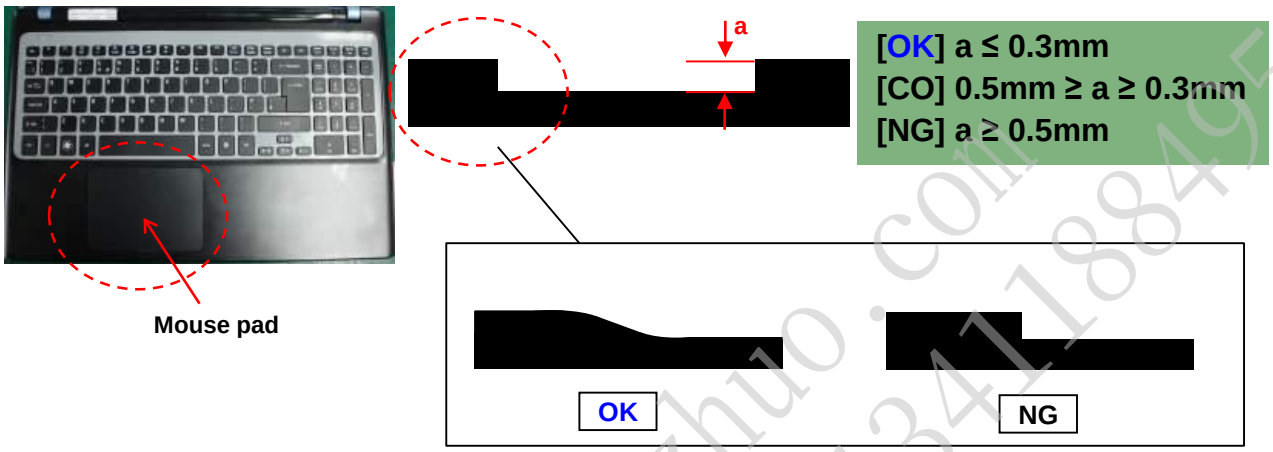
Define	1.If it is possible, shrink to apply front cover of white color.
	2. White color can caused light leakage
8	**Check the wire position(path)**



Define	1. It is necessary that wire is posited out of hook, not posited near hook,.
	2. If wire is posited near hook, it can be happened assemble error and panel crack during assemble front cover

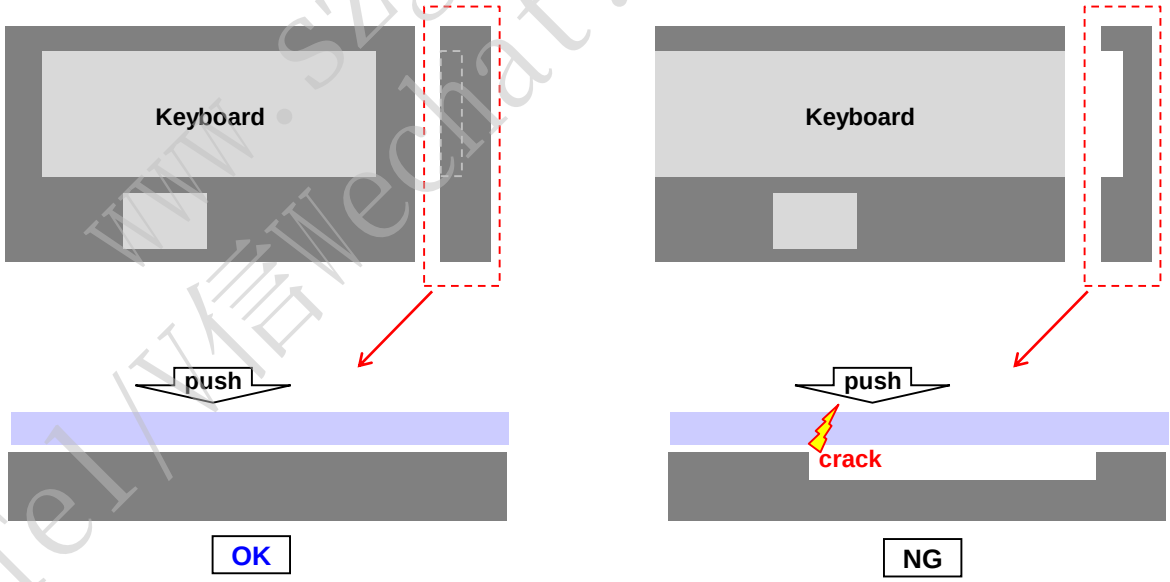
APPENDIX A. LGD Proposal for system cover design

9	Check mouse pad (touch pad) depth and shape of edge



Define	1.Mouse pad step is deep, it is caused panel crack by external load.
	2. The edge shape must be smooth.

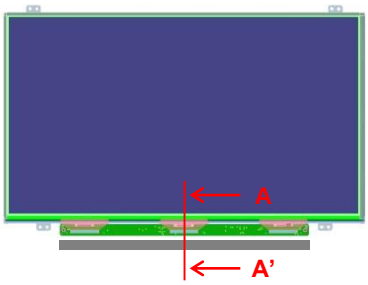
10	Check the step of keyboard area

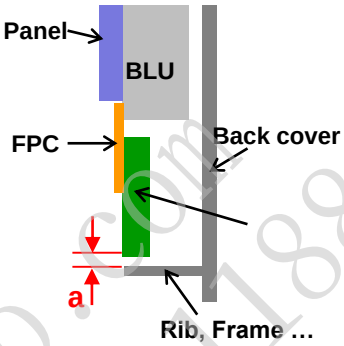


Define	The step of keyboard at the side edge of main body, it is caused panel crack

APPENDIX A. LGD Proposal for system cover design

11	Check the gap [PCB ~ system]

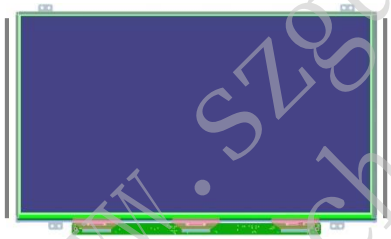




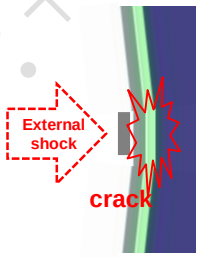
a ≥ 0.5mm [at max dimension of design]
a ≥ 1.0mm [at typical dimension of design]

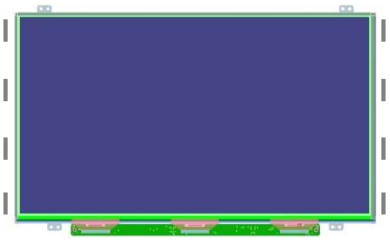
Define	1. Gap is too small, FPC is easily cracked by interference and repetitive bending. (circuit is opened) .
	2. Gap is must be kept more than 0.5mm(max dim.) and 1.0mm(typ dim.) .

12	System rib (on A cover)

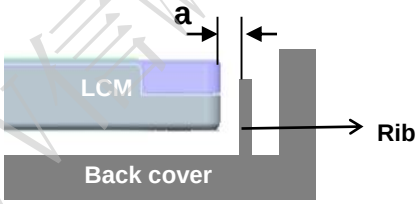


OK





NG

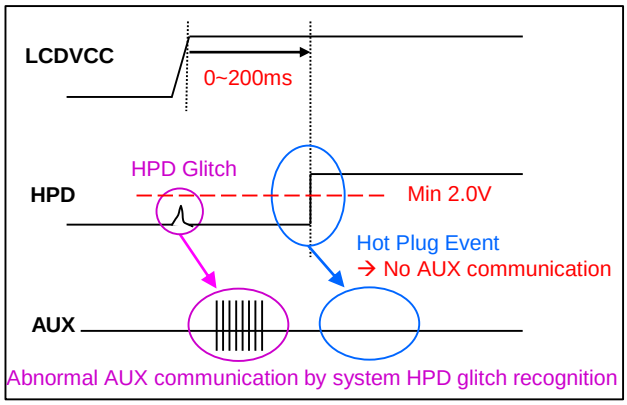


a ≥ 0.5mm [at max dimension of design]
a ≥ 1.0mm [at typical dimension of design]

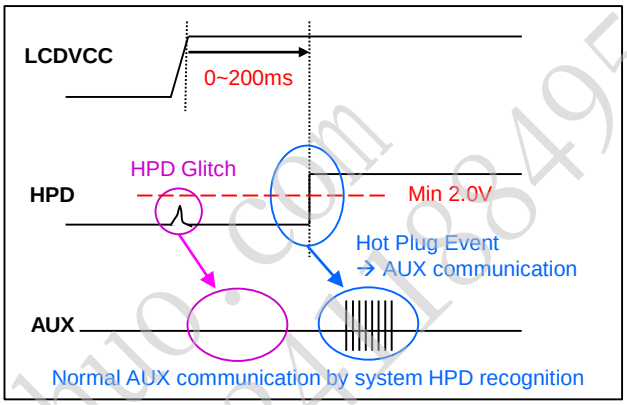
Define	1. Gap is too small and rib is too short, panel is easily cracked by external stress.
	2. Gap is must be kept more than 0.5mm(max dim.) and 1.0mm(typ dim.) .
	3. The figure of rib is continuous or fully long.

APPENDIX B. LGD Proposal for eDP Interface Design Guide

1	HPD Signal recognition



[Abnormal Communication By HPD Glitch]

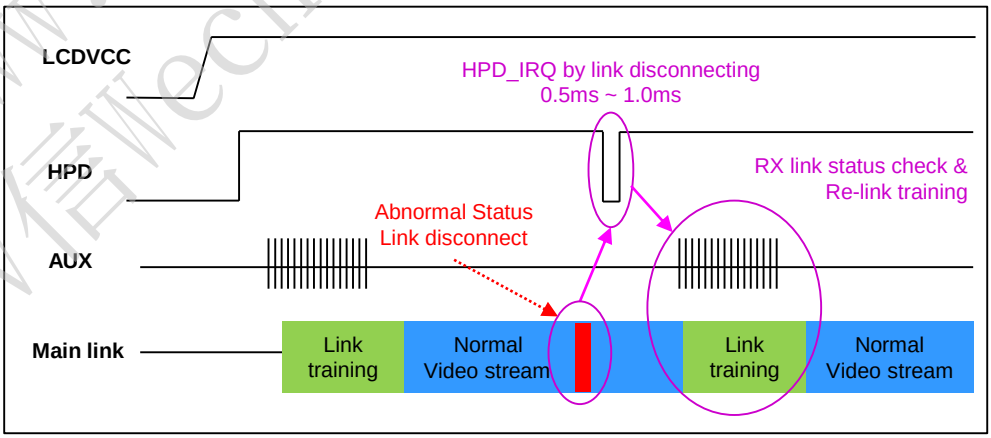


[Normal Communication By HPD Signal]

Define	1. Hot Plug Detection (HPD) Threshold level of Source Device is minimum 2.0V
	2. HPD Unplug : HPD pulse stays low longer than 2ms. DP Tx shall wait for HPD signal to go high again.
	3. “HPD High” is confirmed only after HPD has been asserted continuously for 100msec.

2	IRQ (Interrupt Request) HPD Pulse Definition

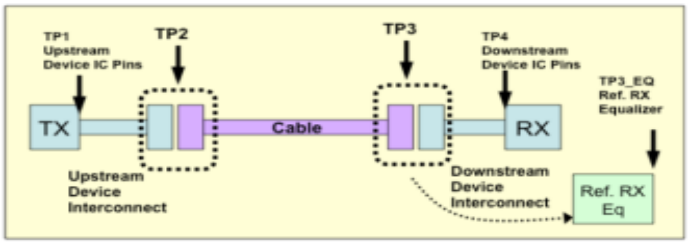
Ex) HPD Pulse



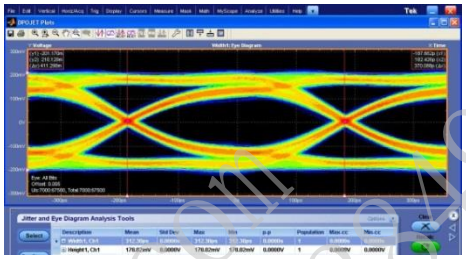
Define	Upon detection this “HPD IRQ Event”(0.5ms ~ 1ms) ,the source device must read the link / sink status field of the DPCD and take corrective action.

APPENDIX B. LGD Proposal for eDP Interface Design Guide

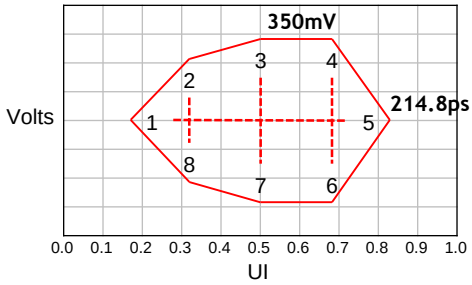
3 Main Link EYE Diagram



*Note : In PCBA side, LGD measured TP3 on LCD connector

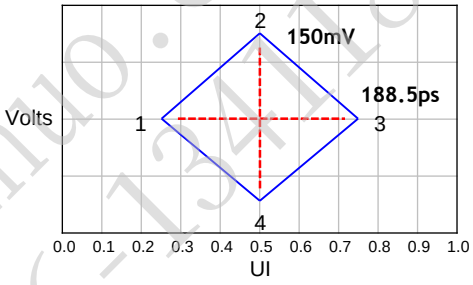


[EYE Diagram]



Point	UI	Voltage (Volts)
1	0.210	0.000
2	0.355	0.140
3	0.500	0.175
4	0.645	0.175
5	0.790	0.000
6	0.645	-0.175
7	0.500	-0.175
8	0.355	-0.140

[EYE Vertices for TP2 at HBR]

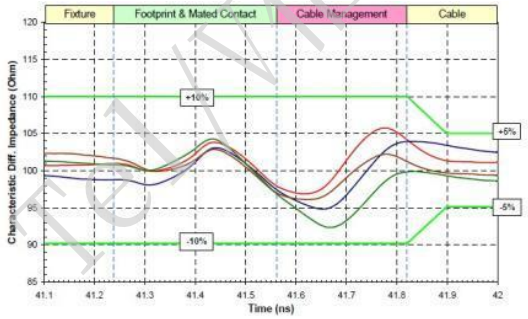


Point	UI	Voltage (Volts)
1	0.246	0.000
2	0.500	0.075
3	0.755	0.000
4	0.500	-0.075

[EYE Vertices for TP3 at HBR]

Define	Main Link EYE Diagram should meet TP2 and TP3 point

4 Cable Impedance management

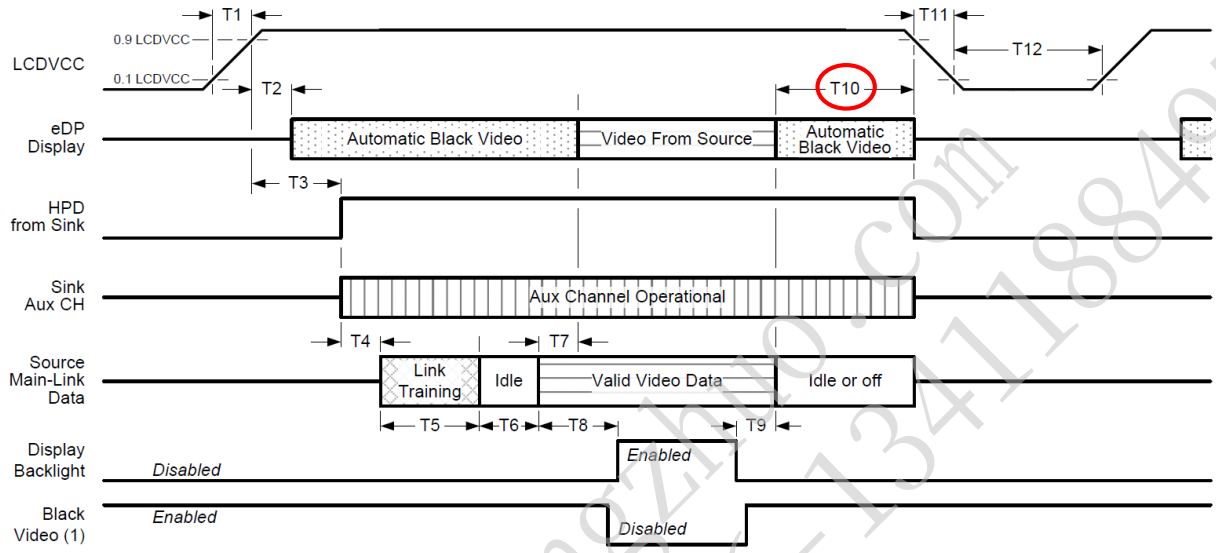


Segment	Differential Impedance	Maximum Tolerance
Fixture	100 Ω	+/- 10%
Connector	100 Ω	
Wire management	100 Ω	
Cable	100 Ω	+/- 5%

Define	Cable Impedance 100 Ω +/- 5% (95Ω ~ 105Ω)

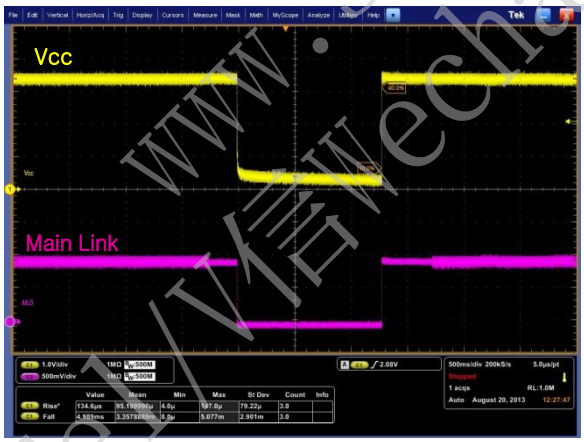
APPENDIX B. LGD Proposal for eDP Interface Design Guide

5 Main Link Off vs. LCD Power Off at Non-PSR

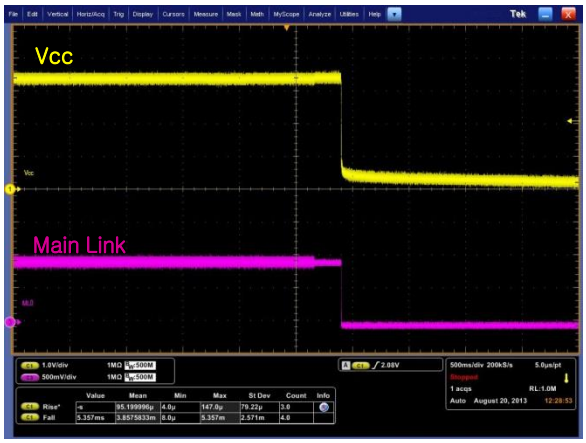


Timing Parameter	Description	Required By	Min	Max
T10	Delay from end of valid video from Source to Power Off	Source	0ms	500ms

* LGD recommend that Source must power off the LCDVCC if Main Link off like below.



[Case1. Resolution Change]

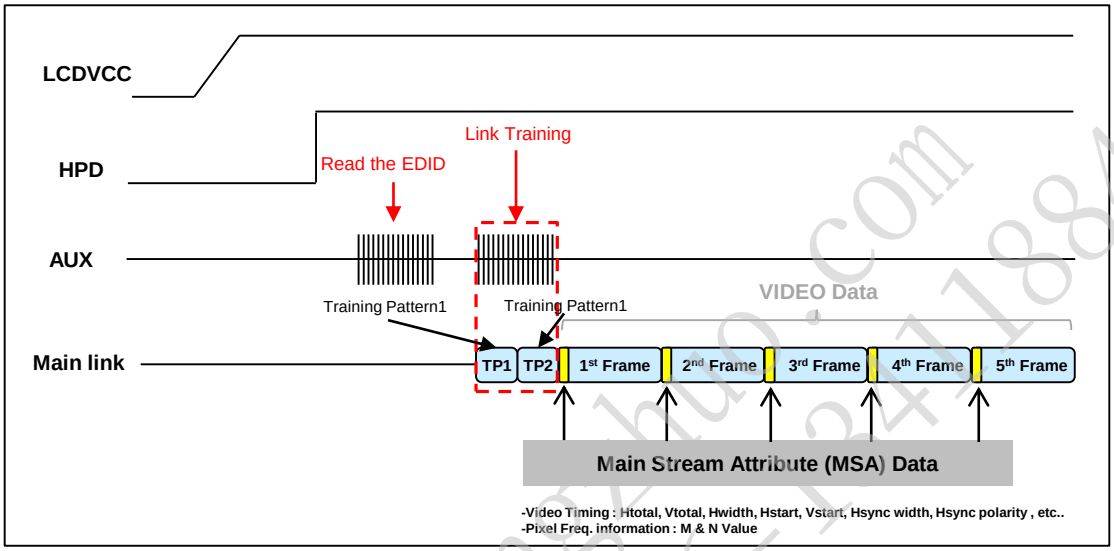


[Case2. Close the Lid]

Define	If Main Link off signal from Source, then LCDVCC must be Power Off within T10 period at Non-PSR mode

APPENDIX B. LGD Proposal for eDP Interface Design Guide

6	Main Link M & N value of MSA data

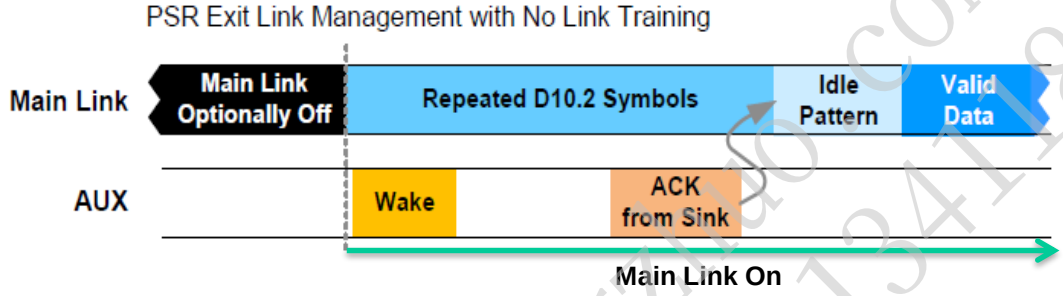


Define	It need to fix M& N value of MSA data output to prevent the initial abnormal M& N Value from incoming after power on.

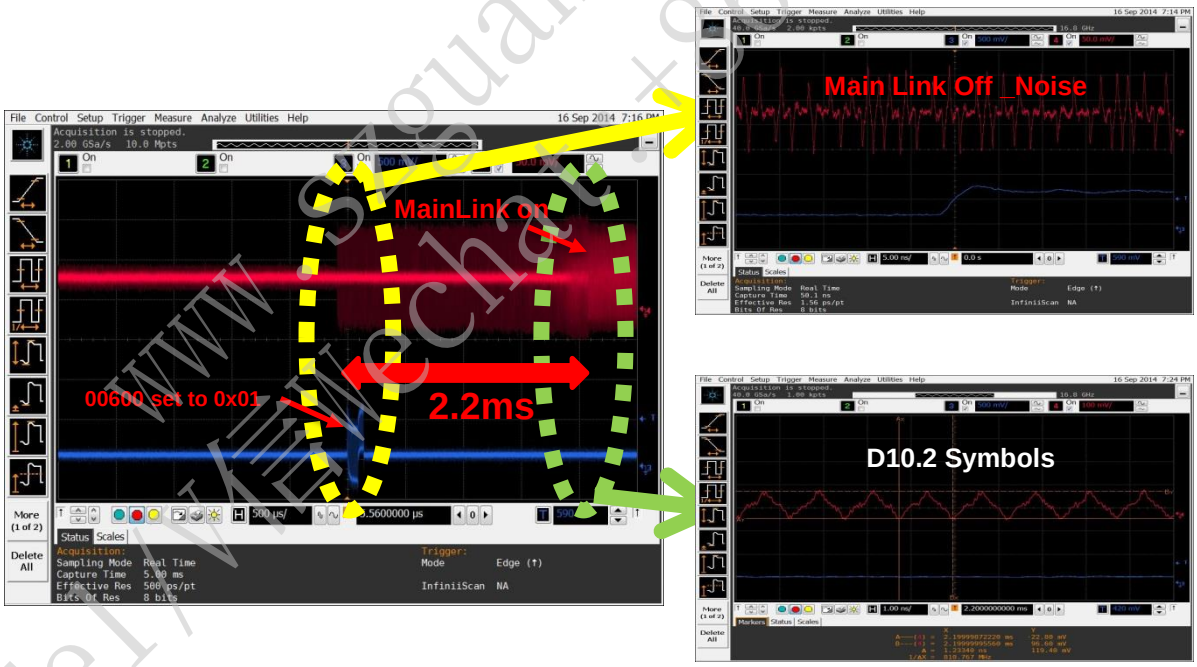
APPENDIX B. LGD Proposal for eDP Interface Design Guide

7	PSR Exit

If link training is not required, the Source must begin transmitting data on the Main Link prior to the wake AUX command which occurs through writing 01h to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h; see *DP v1.2a*), as illustrated in the upper portion of Figure 6-9. This transmitted data must be a repetition of D10.2 symbols (which is the same as Link Training Pattern 1). Note the requirement above to transmit five repeats of the Idle Pattern after receiving ACK from the Sink.



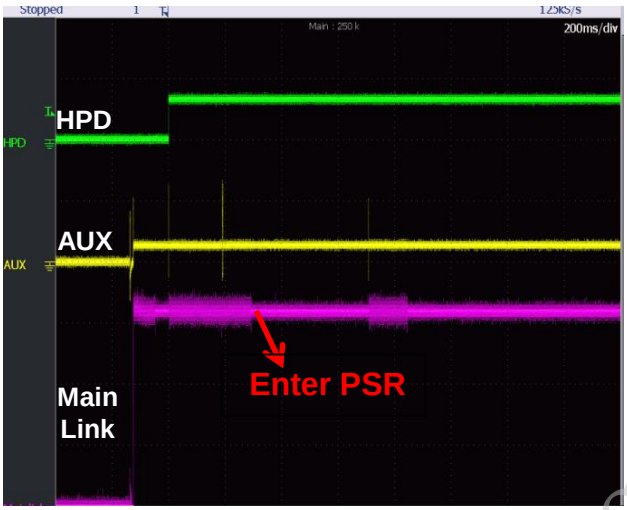
-. The below waveform is the issued case.



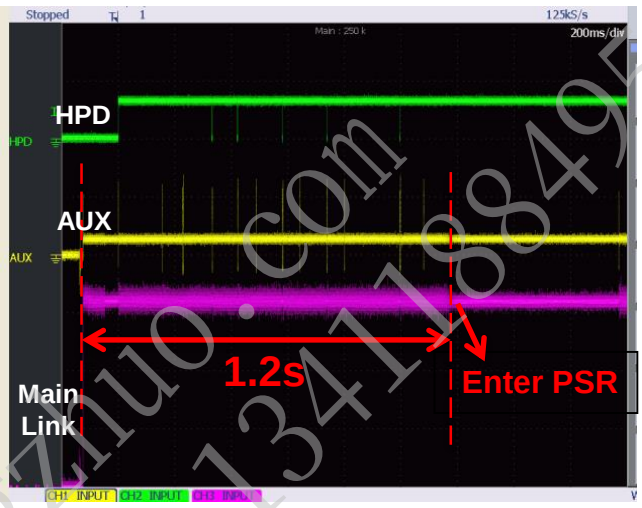
Define	If link training is not required, the source must begin transmitting data on the ML prior to the wake AUX wake-up command.

APPENDIX B. LGD Proposal for eDP Interface Design Guide

8	1st time PSR Entry after Power on



< Issue waveform >



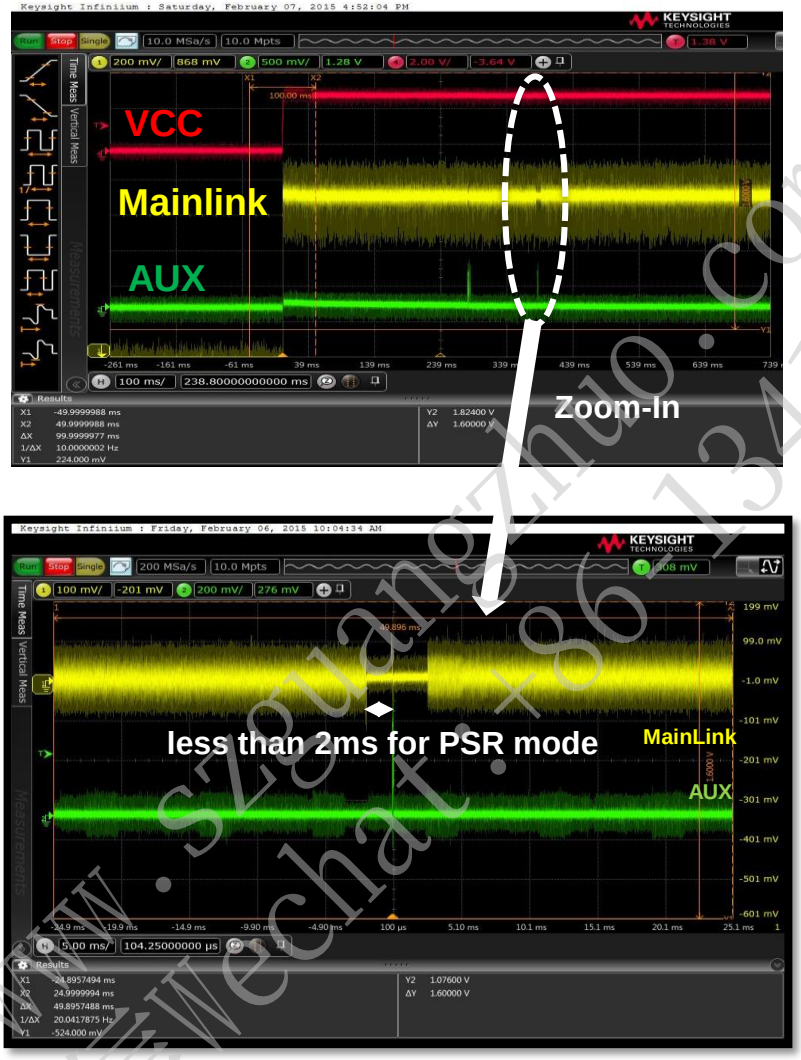
< solution waveform >

1. It is found that with solution , the TCON enter the PSR timing is 1.2s delay from VCC on which avoid TCON capture the wrong data from DP link(poor link quality) and enter the BIST mode + PSR mode(black screen).
2. **According to test, link is stable 800ms after VCC on.**

Define	After power(Vcc) on, the DP link is not stable, so the source try to PSR entry at 800ms after Power(Vcc) on..

APPENDIX B. LGD Proposal for eDP Interface Design Guide

9	PSR Period Issue

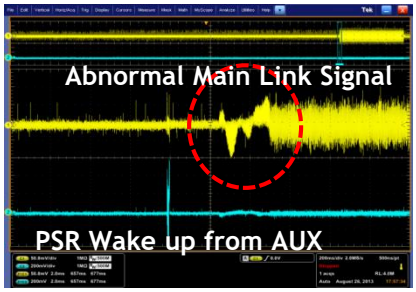


1. When issue is happened, system go to PSR mode for very short time.
2. If PSR active period is shorter than 1frame(16.67ms), T-Con can not go to the standby mode for PSR exit.

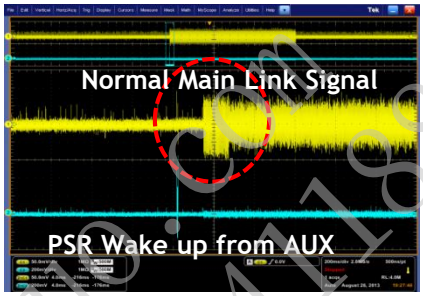
Define	When GPU go to the PSR mode, the source must hold the main link off over than 1frame.

APPENDIX B. LGD Proposal for eDP Interface Design Guide

10	Main Link Noise at PSR Exit



[Abnormal Main Link Noise]



[Normal Main Link Signal]

Define	Main Link Noise at PSR Exit mode can be a cause abnormal display.

APPENDIX C. Enhanced Extended Display Identification Data (EEDID™) 1/3

TBD

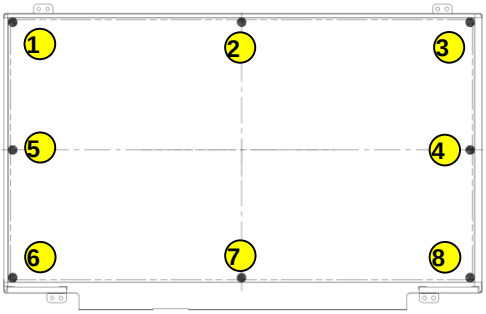
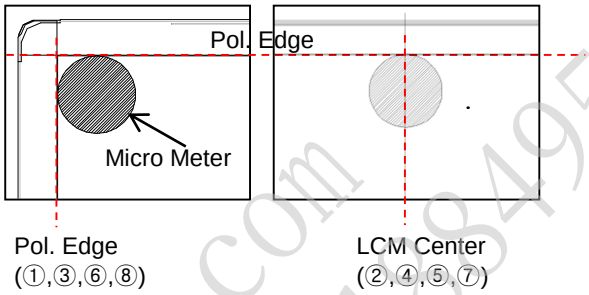
APPENDIX C. Enhanced Extended Display Identification Data (EEDID™) 2/3

TBD

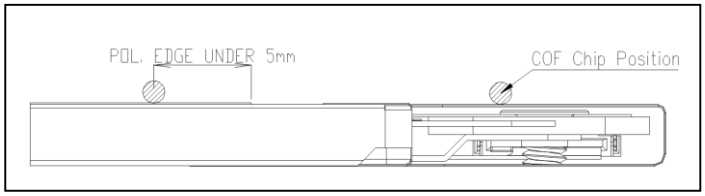
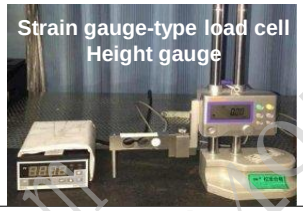
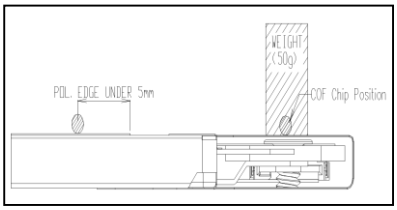
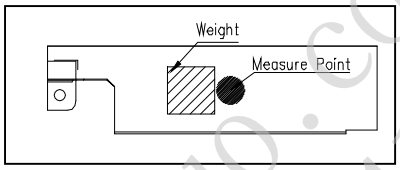
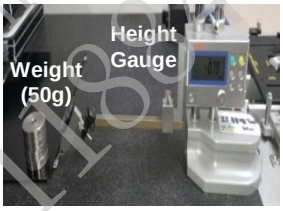
APPENDIX C. Enhanced Extended Display Identification Data (EEDID™) 3/3

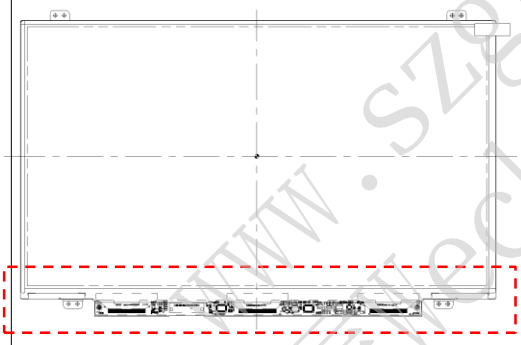
TBD

APPENDIX D. LGD Proposal for Measurement Method

1	LCM Thickness
Point	  Pol. Edge (①,③,⑥,⑧) LCM Center (②,④,⑤,⑦)
Measure Tool	Micro Meter  
Guide	✓ Measure the thickness between Polarizer surface and M-Chassis on the rear of LCM ✓ Subtract Pol. protect film thickness from LCM thickness

APPENDIX D. LGD Proposal for Measurement Method

2	Height of PCB Area
Measure Tool & Point	 
Measure Tool & Point	  
Guide	✓ Measure the height between upper Polarizer surface and C/Shield top surface. ✓ Measure the height include force(50gf) on the C/Shield surface at FPC/COF Center. ✓ The CAS Spec. : All components except cover shield of LCM is under upper POL. Upper polarizer higher than source cover shield pressed down 50g.
Measure condition	Put the LCM on flat ground w/o interference on PCB rear side



※ Measure Point

Item	Description
Measure Tool	Height gauge (with Strain gauge type load-cell or weight)
Measure Point	V-dimension : Pol. Edge ~ 5mm, FPC/COF Center(or Chip) H-dimension : Each FPC/COF Center(or Chip) → Including all of components on PCB