




Product Specification

AU OPTRONICS CORPORATION

() Preliminary Specifications

(✓) Final Specifications

Module	15.6" (15.55") FHD 16:9 Color TFT-LCD with LED Backlight design
Model Name	BI56HAN02.6 (H/W:0A) Dell P/N : GHWIK
Note ()	<i>LED Backlight with driving circuit design</i>

Customer	Date
_____	_____
Checked & Approved by	Date
_____	_____
Note: This Specification is subject to change without notice.	

Approved by	Date
<u><i>Buffy Chen</i></u>	<u><i>2019/02/12</i></u>
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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2018/08/08	All	First edition for customer		
0.2 2018/12/27	6		Update chromaticity coordinates	
	28		Update shipping label format	
	31		Update EDID description	
1.0 2019/02/12	All		Final edition for customer	



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I. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD module, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electronic breakdown.



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2. General Description

BI56HAN02.6 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 FHD, 1920(H) x 1080(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are eDP(Embedded DisplayPort) interface compatible.

BI56HAN02.6 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	394.9			
Active Area	[mm]	344.16 × 193.59			
Pixels H × V		1920 × 3(RGB) × 1080			
Pixel Pitch	[mm]	0.17925 × 0.17925			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black			
White Luminance (ILED= 25mA) (Note: ILED is LED current)	[cd/m²]	300 typ. (5 points average) 255 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		800:1 typ.			
Response Time	[ms]	25 Typ, 35 max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	0.2W			
Weight	[Grams]	380 max			
Physical Size	[mm]		Min.	Typ.	Max.
		Length	350.36	350.66	350.96
		Width (w/o FPC)	204.94	205.24	205.54
Thickness		Thickness	3.2 max (panel side) 5.4 max (PCBA side)		
Electrical Interface		2 Lane eDP 1.3			
Glass Thickness	[mm]	0.4			
Surface Treatment		Anti-Glare			
Support Color		262K colors (RGB 6-bit)			
Temperature Range					
Operating	[°C]	0 to +50			
Storage (Non-Operating)	[°C]	-20 to +60			
RoHS Compliance		RoHS Compliance			



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2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

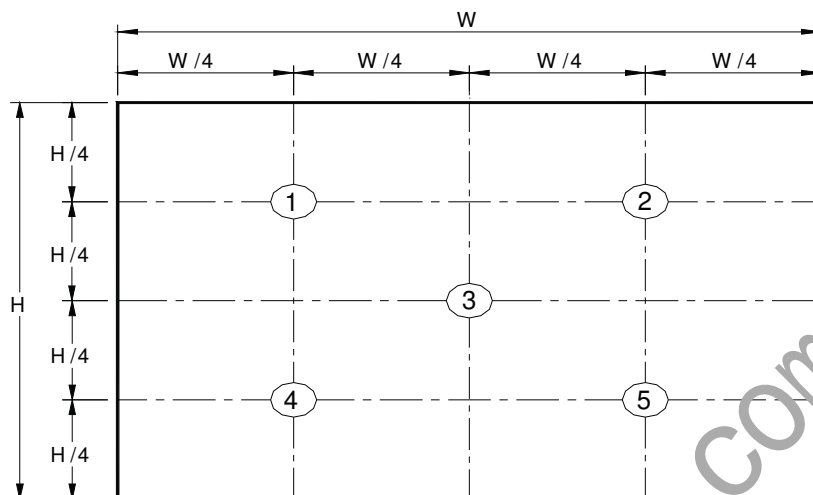
Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note			
White Luminance ILED=25mA			5 points average	255	300	-	cd/m ²	1, 4, 5.			
Viewing Angle		θ_R	Horizontal (Right) CR = 10 (Left)	80	85	-	degree	4, 9			
		θ_L		80	85	-					
		ψ_H	Vertical (Upper) CR = 10 (Lower)	80	85	-					
		ψ_L		80	85	-					
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4			
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.60		2, 3, 4			
Contrast Ratio		CR		-	800	-		4, 6			
Cross talk		%						4, 7			
Response Time		T _{RT}	Rising + Falling		25	35					
Color / Chromaticity Coordinates	Red	R _x	CIE 1931	0.610	0.640	0.670		4			
		R _y		0.306	0.336	0.366					
	Green	G _x		0.231	0.321	0.351					
		G _y		0.589	0.619	0.649					
	Blue	B _x		0.126	0.156	0.186					
		B _y		0.012	0.042	0.072					
	White	W _x		0.283	0.313	0.343					
		W _y		0.299	0.329	0.359					
	NTSC			%					72	-	



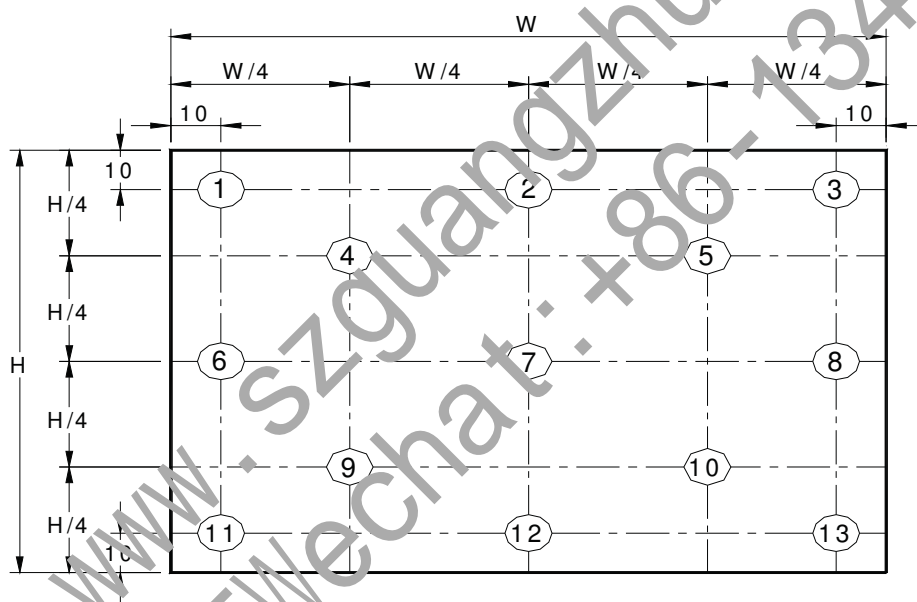
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Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{V5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

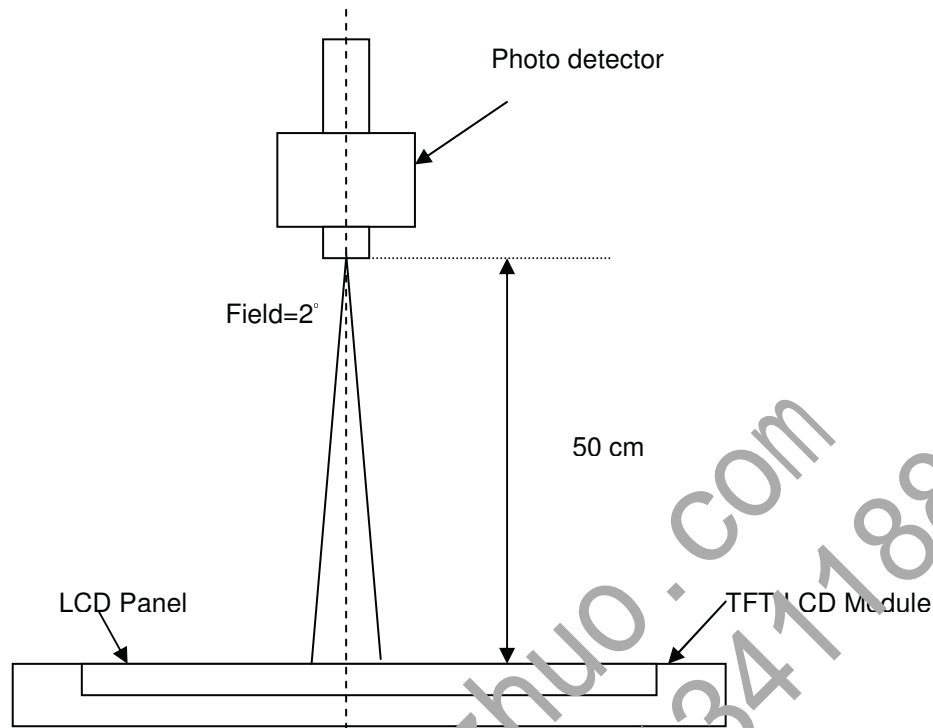
Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



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Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points , $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (1)

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

Note 7 : Definition of Cross Talk (CT)

$$CT = |YB - YA| / YA \times 100 (\%)$$

Where

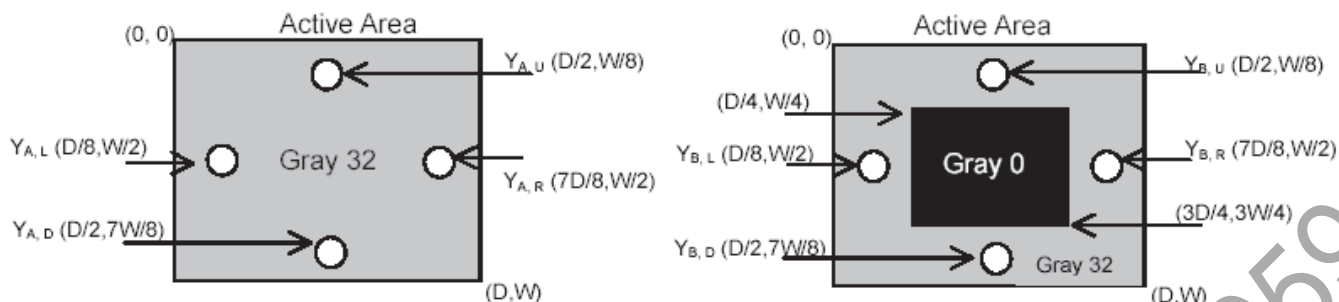
YA = Luminance of measured location without gray level 0 pattern (cd/m²)

YB = Luminance of measured location with gray level 0 pattern (cd/m²)



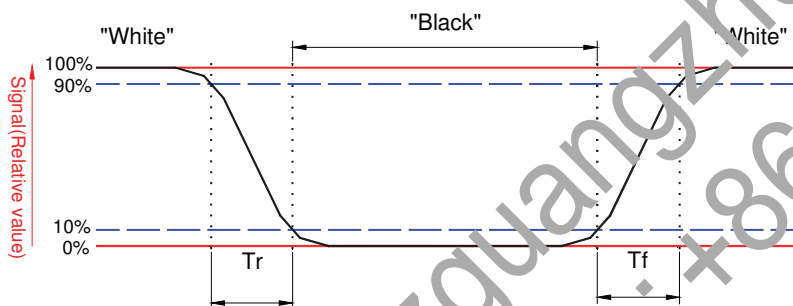
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Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



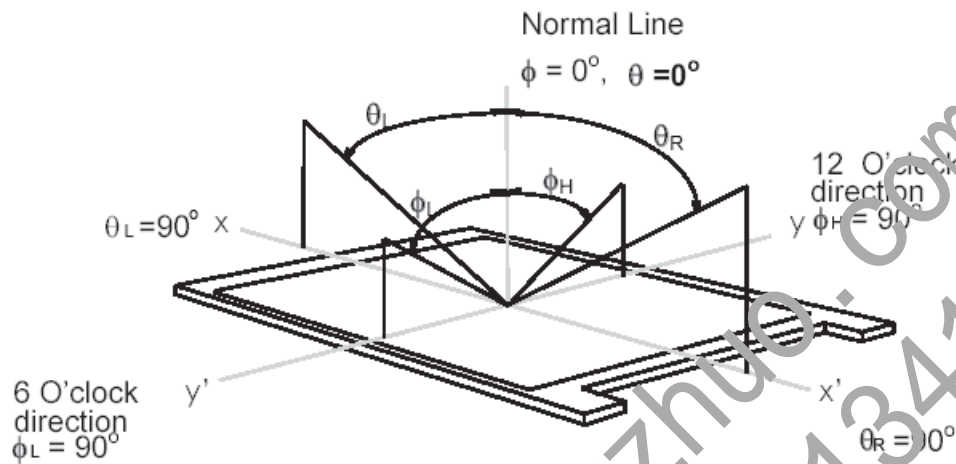


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Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (ϕ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



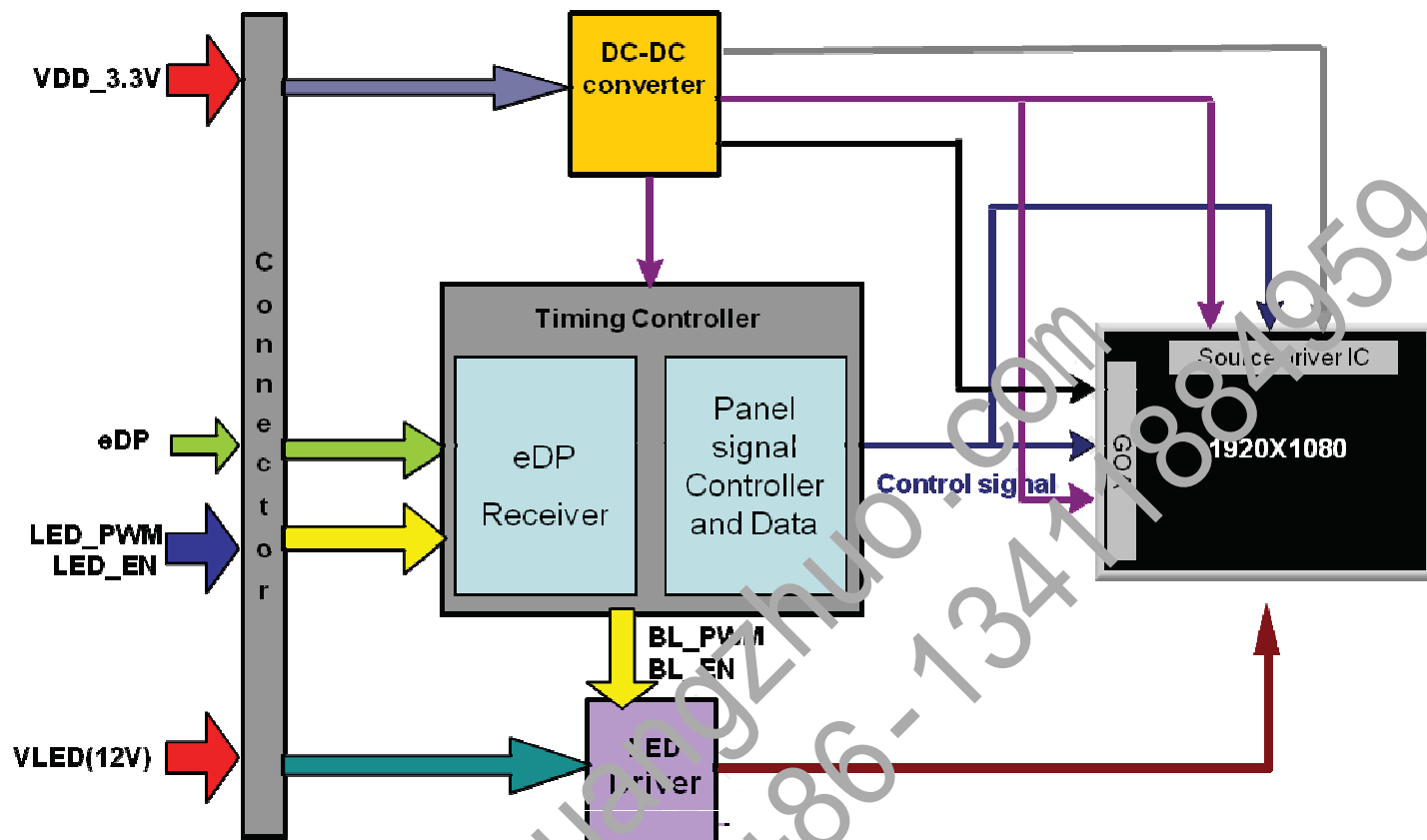


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3. Functional Block Diagram

The following diagram shows the functional block of the 15.6 inches wide Color TFT/LCD 30 Pin (One CH/connector Module)





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4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

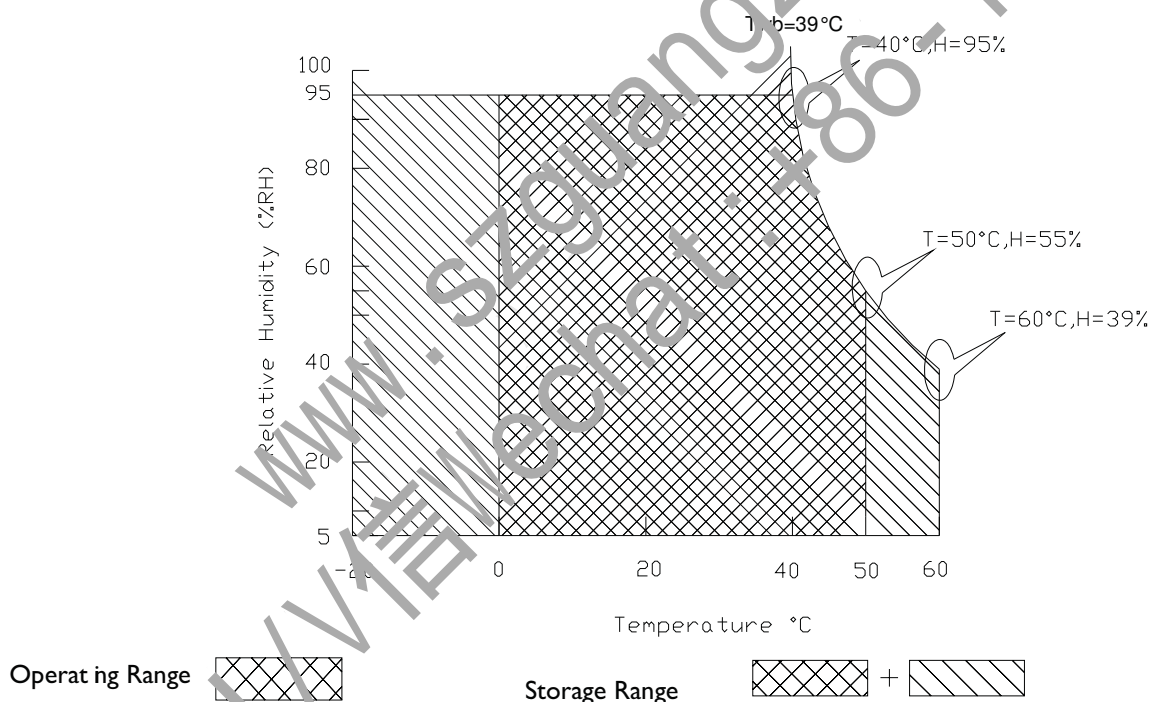
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).





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5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

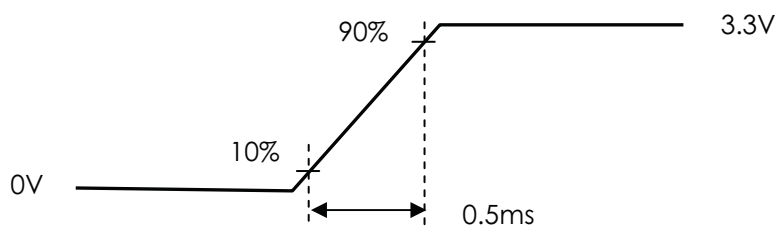
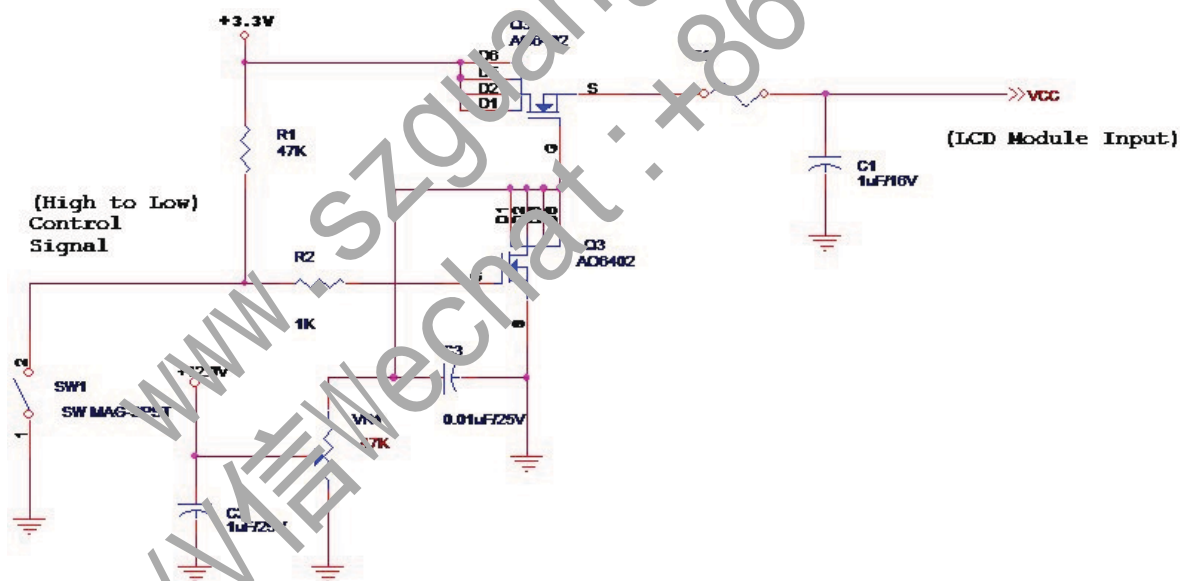
The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	1.2	1.6	[Watt]	Note 1
IDD	IDD Current	-	-	533	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : PDD(typ)@ mosaic pattern Maximum Power ; PDD(Max)@ R/C/B pattern Maximum Power

$$IDD(Max)=PDD(Max) / VDD(Min)$$

Note 2 : Measure Condition



Vin rising time



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5.1.2 Signal Electrical Characteristics

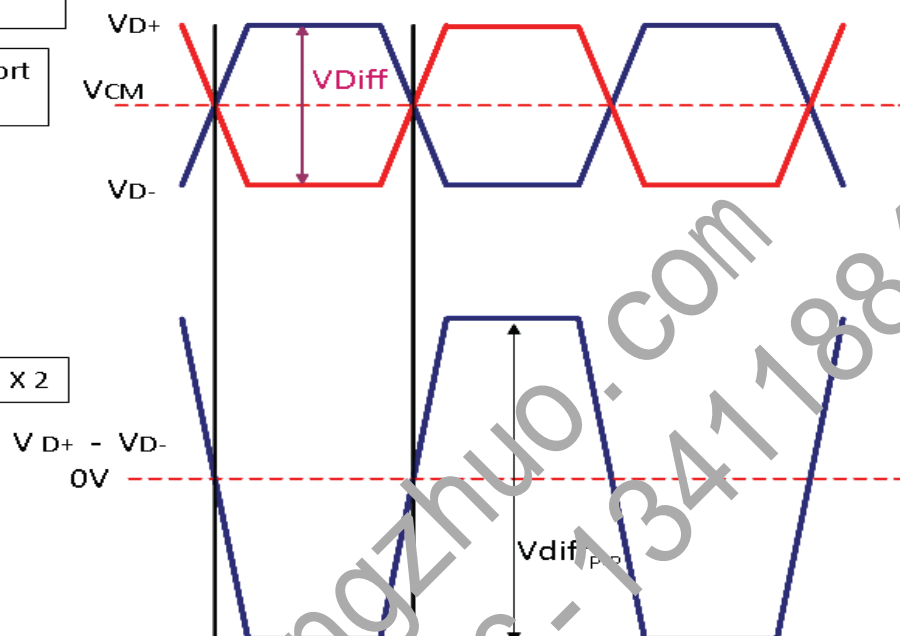
Signal electrical characteristics are as follows;

Display Port main link signal:

Differential pair VD+ , VD-
Which is one Display port
Main link

VCM of Display port
Main link

$$V_{diffP-P} = [(VD+) - (VD-)] \times 2$$

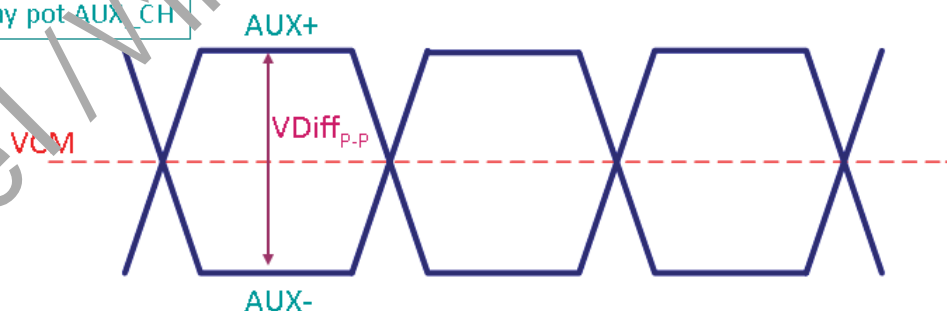


Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
VDiff _{P-P}	Peak-to-peak Voltage at Receiving Device	150		1320	mV

Follow as VESA display port standard V1.1a

Display Port AUX_CH signal:

Differential AUX+ , AUX-
Which is Display port AUX_CH





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Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff _{p,p}	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

Follow as VESA display port standard VI.1a.

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25	-	3.0	V

Follow as VESA display port standard VI.1a.



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5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	4.6	[Watt]	(Ta=25°C), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25°C), Note 2 If=21 mA

Note 1: Calculator value for reference $P_{LED} = V_F$ (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	5.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25°C)
LED Enable Input High Level	VLED_EN	2.0	-	5.5	[Volt]	
LED Enable Input Low Level	*Note 1	-	-	0.5	[Volt]	
PWM Logic Input High Level	V_PWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level	*Note 1	-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

Note 1: Recommend system pull up/down resistor no bigger than 10kohm



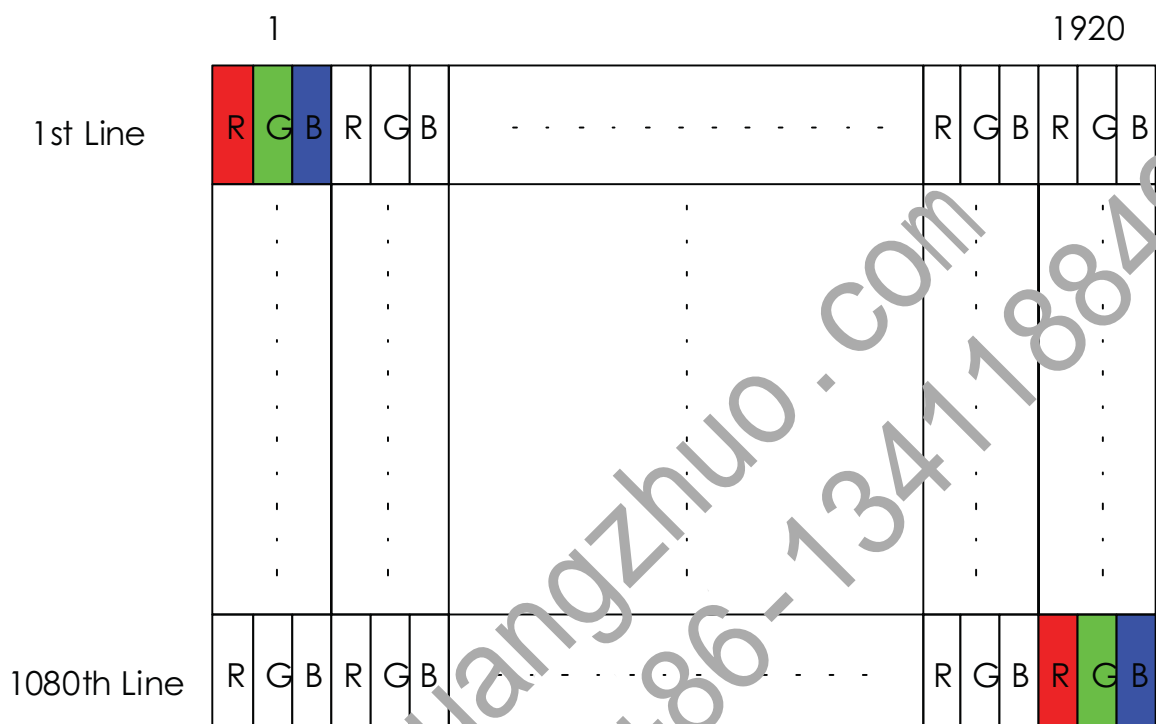
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6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.





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6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX
Type / Part Number	IPEX 20765-030E-11A or compatible
Mating Housing/Part Number	IPEX 20453-230T-11 or compatible



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6.2.2 Pin Assignment

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN#	Symbol	Function
1	DCR_EN	DCR_EN
2	H_GND	High Speed Ground
3	LaneI_N	Comp Signal Lane I
4	LaneI_P	True Signal Link Lane I
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	LCD_Self_Test or NC	LCD Panel Self Test Enable (Optional)
15	LCD_GND	LCD logic and driver ground
16	LCD_GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	BL_GND	Backlight_ground
19	BL_GND	Backlight_ground
20	BL_GND	Backlight_ground
21	BL_GND	Backlight_ground
22	BL_Enable	Backlight On / Off
23	BL_PWM_DIM	System PWM signal Input
24	NC	No Connect (Reserved)
25	NC	No connect (Reserved)
26	BL_PWR	Backlight power (5V~21V)
27	BL_PWR	Backlight power (5V~21V)
28	BL_PWR	Backlight power (5V~21V)
29	BL_PWR	Backlight power (5V~21V)
30	NC	No Connect (Reserved)

Note1 : start from right side

Note2 : Input signals shall be low or High-impedance state when VDD is off.



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6.3 Interface Timing

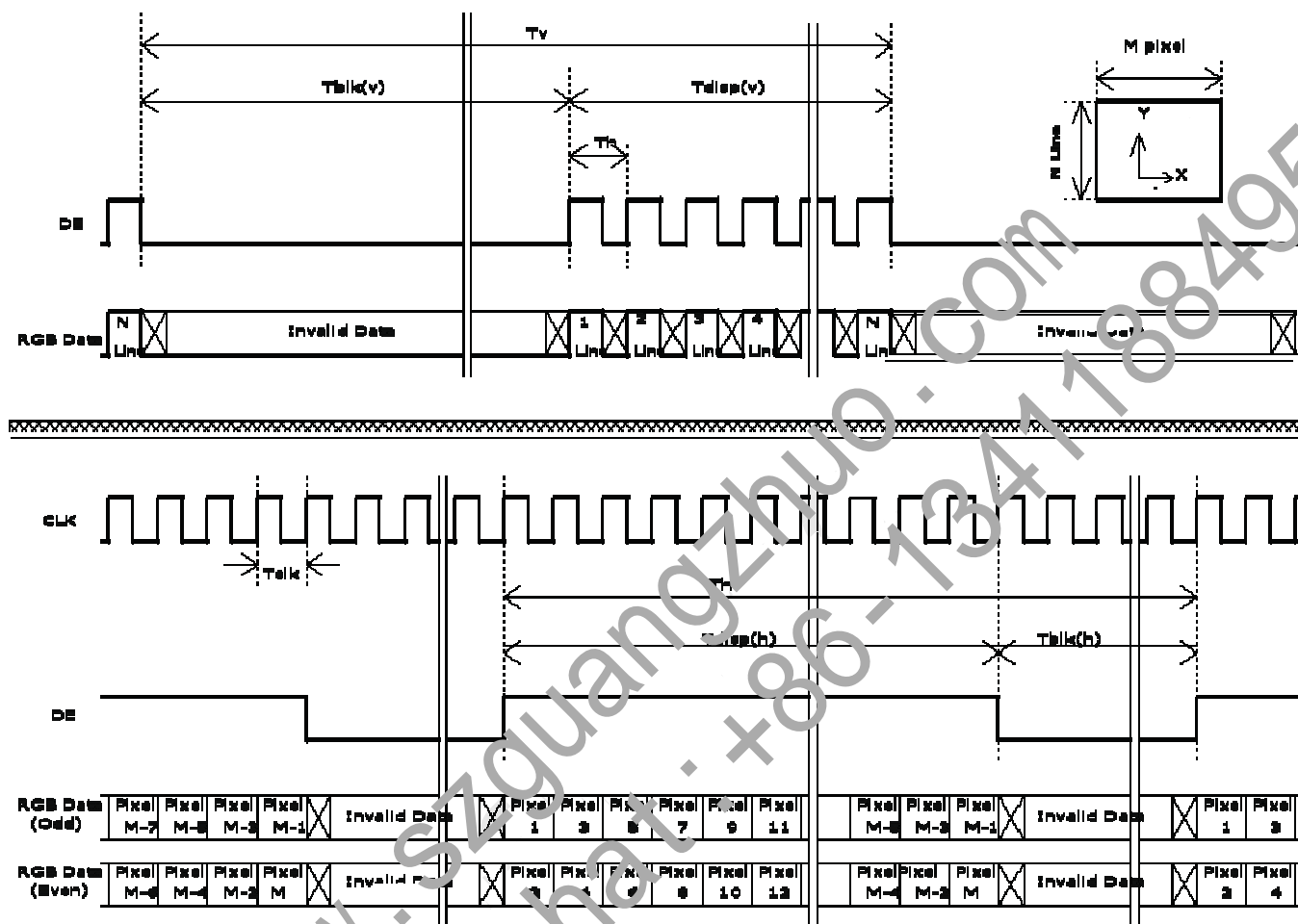
Basically, interface timings should match the 1920x1080 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		I/ T _{Clock}	-	141	-	MHz
Vertical Section	Period	T _V	1084	1118	1080+B	T _{Line}
	Active	T _{VD}	1080			
	Blanking	T _{VB}	4	38	A	
Horizontal Section	Period	T _H	2000	2100	1920+B	T _{Clock}
	Active	T _{HD}	1920			
	Blanking	T _{HB}	80	180	B	

Note : 1. DE mode only

2. The maximum clock frequency = $(1920+B) \times (1080+A) \times 60 < 149.1 \text{ MHz}$

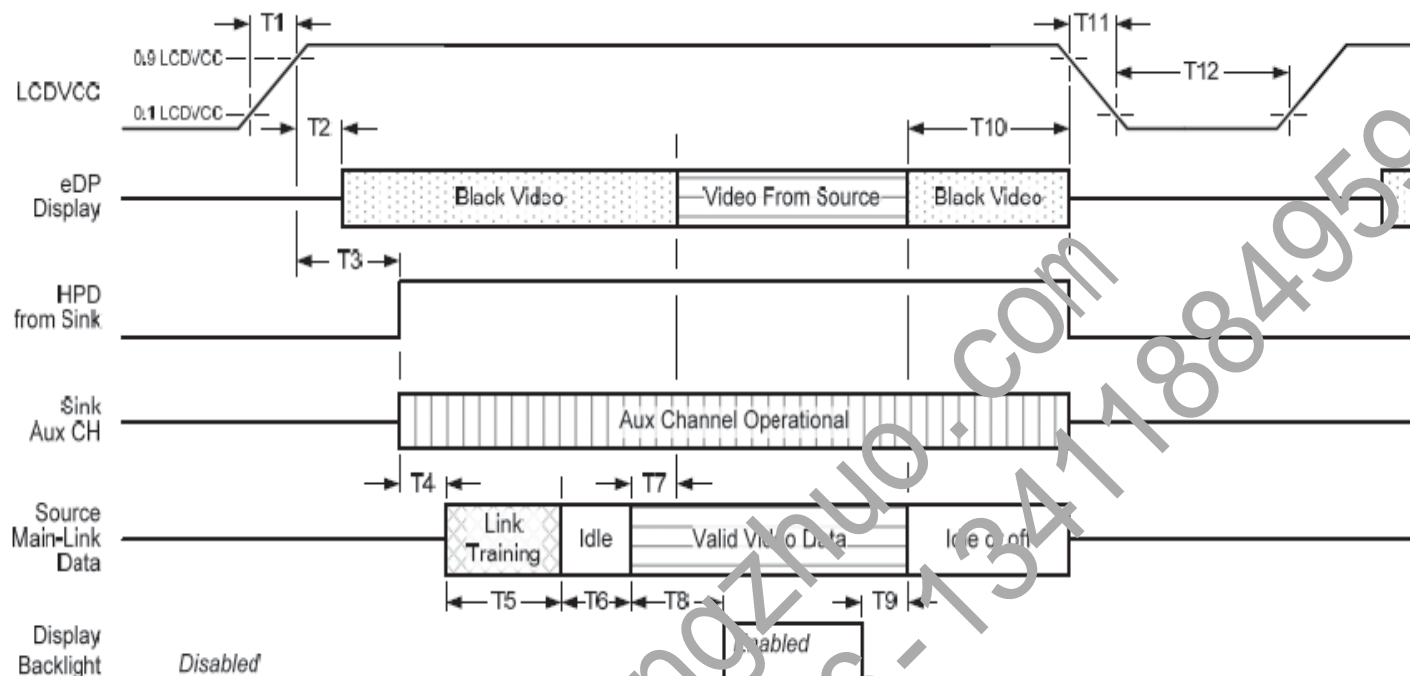
6.3.2 Timing diagram



6.4 Power ON/OFF Sequence

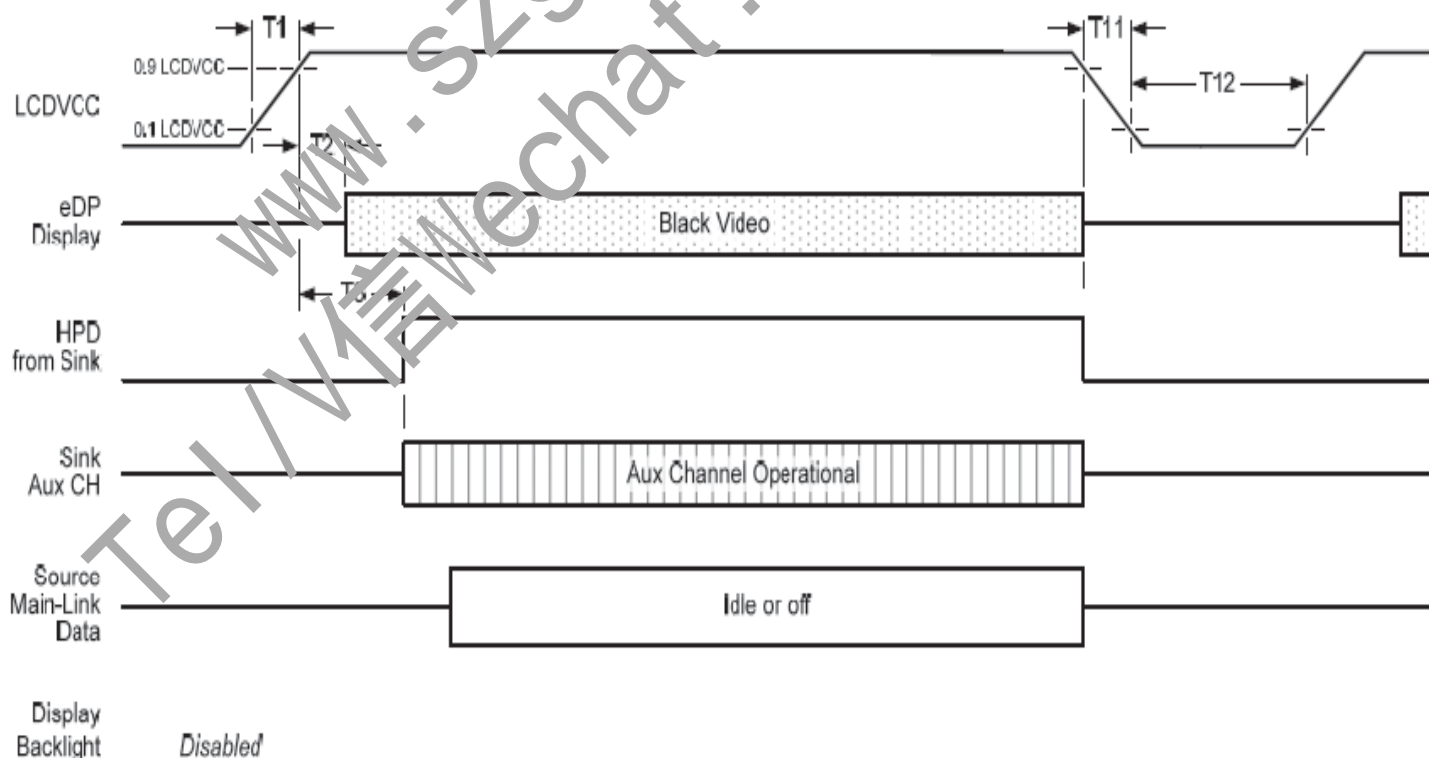
Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:



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Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to sink training protocol.
T6	link idle	source				Min allows for required PS-link pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		64ms	max allows sink to date video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	50ms		500ms	
T11	power rail fall time, 90% to 10%	source			1ms	
T12	power off time	source	500ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:

-upon LCDVDD power on (with in T1 max) when the "No video stream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).

-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

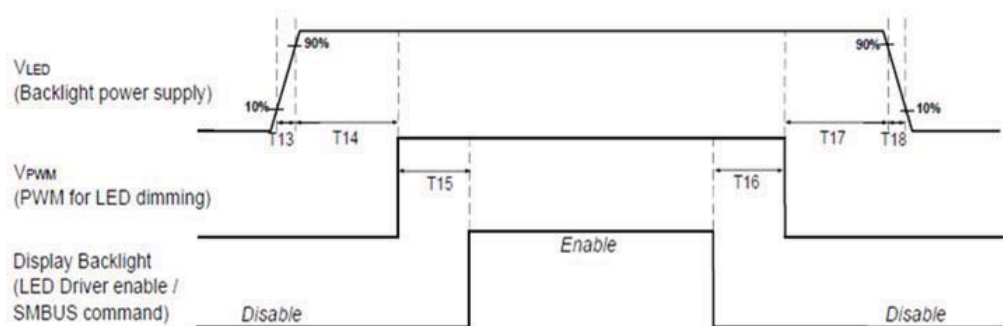
Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can verify if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.



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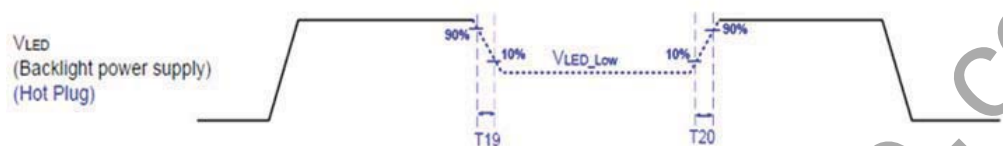
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Display Port panel B/L power sequence timing parameter:



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



Seamless change: $T19, T20 = 5 \times T_{PWM}^*$

* $T_{PWM} = 1 / \text{PWM Frequency}$



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7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C, 90%RH, 300h	
High Temperature Operation	Ta= 50°C, Dry, 300h	
Low Temperature Operation	Ta=0°C, 300h	
High Temperature Storage	Ta= 60°C, 300h	
Low Temperature Storage	Ta= -20°C, 250h	
Thermal Shock Test	Ta=-20°C (30min) ~ 60°C (30min), 100cycles condition.	
ESD	Contact : ±8 kV Air : ±5 kV	Note I

Note I: According to EN 1000 4-2, ESD class B: Some performance degradation allowed. No data lost
Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%



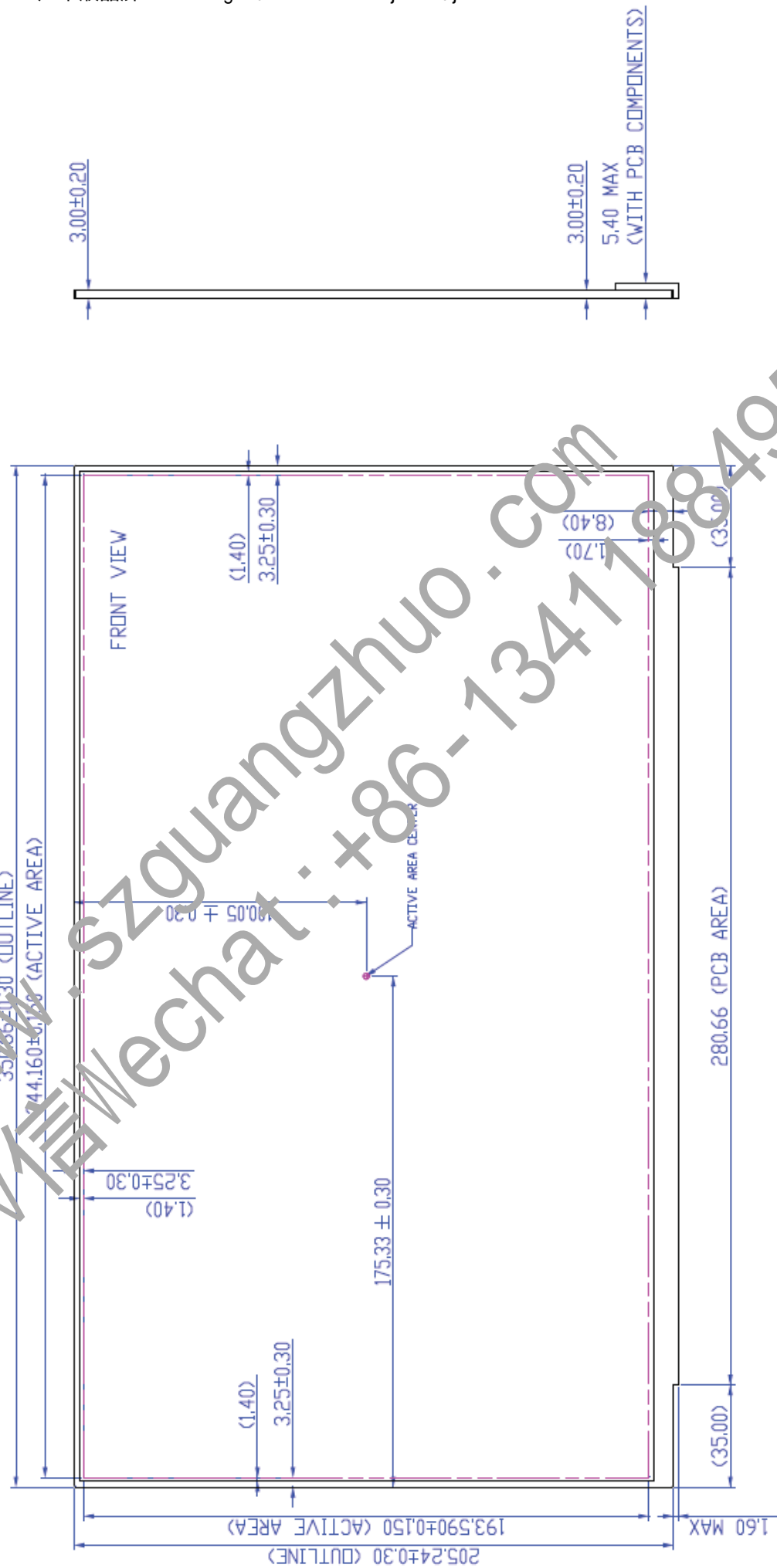
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8. Mechanical Characteristics

8.1 LCM Outline Dimension

8.1.1 Standard Front View

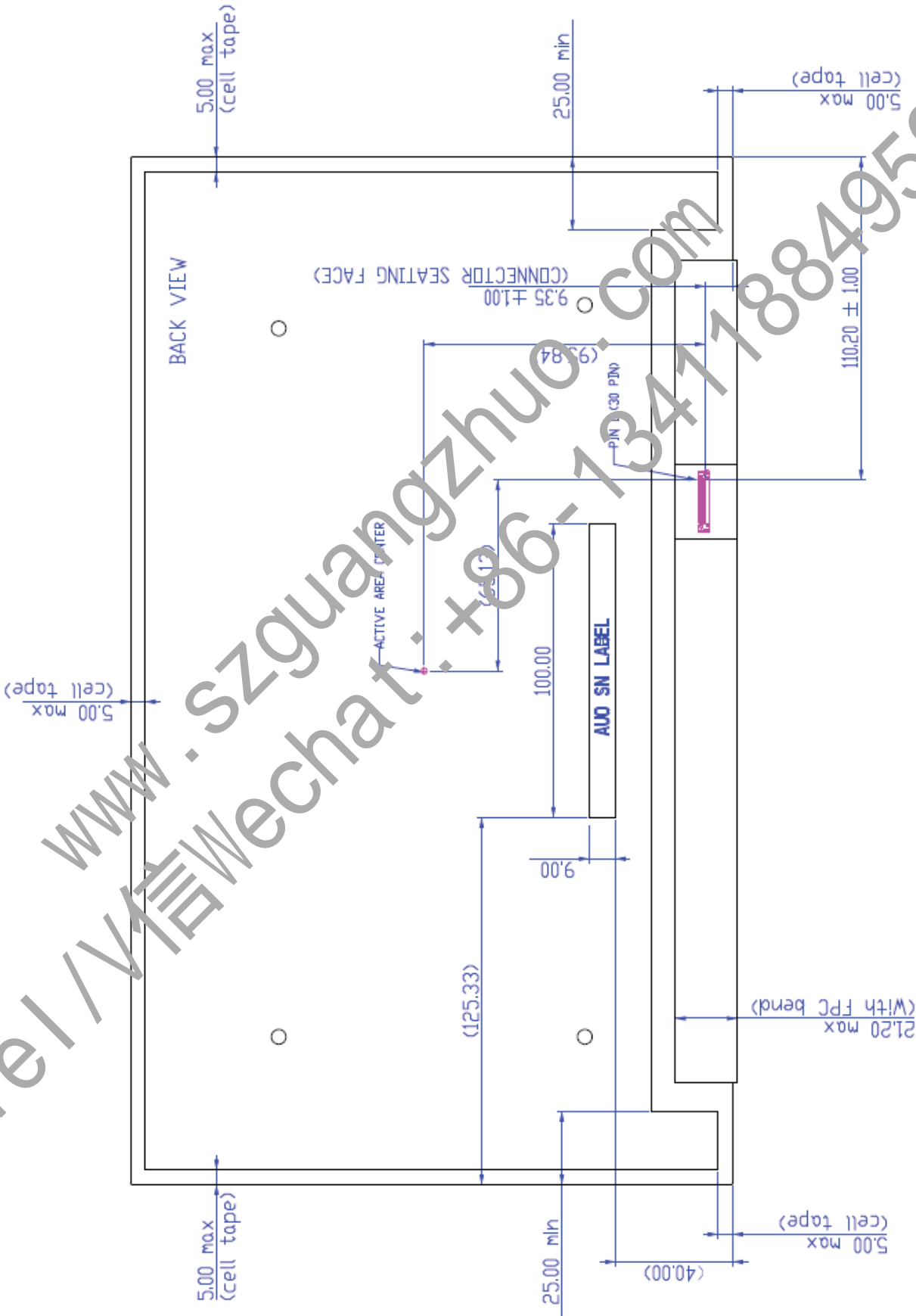


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8.1.2 Standard Rear View






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9. Shipping and Package

9.1 Shipping Label Format

 *XXXXXXXXXX-XXXXXX* H/W : 0A	Manufactured MM/WW Model No: B156HAN02.6 AU Optronics F/W:1 MADE IN CHINA(30B)	 CN-0GHW1K-DQSAU- XXX-XXXX-A00 Made In China DP/N 0GHW1K	  
---	---	---	---

9.2 Definition of customer PPID Label and Revision Code

Please refer to the Dell Part Identification Label Specification, Number:13196

Build Name(s):	PPID Revision Code(s):
Sub System Test (SST) Working Sample (WS) ENG 2	X00, X01, X02, ..., X0n
Product Test (PT) Engineering Sample (ES) ENG 3	X10, X11, X12, ..., X1n
System Test (ST) Customer Sample (CS) ENG 4	X20, X21, X22, ..., X2n
X-Build (XB) Mass Production (MP) ENG 5	A00, A01, A02, ... A0n



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9.3 Carton Package

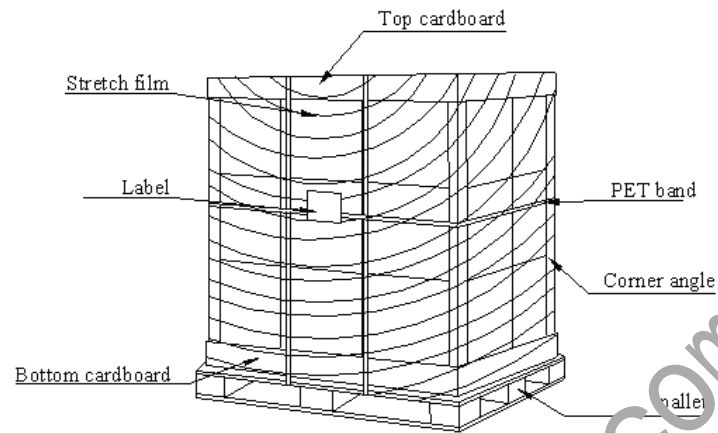




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9.4 Shipping Package of Palletizing Sequence



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10. Appendix: EDID Description

	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)	Value (DEC)
Header	0	Header	00	00000000	0
	1	Header	FF	11111111	255
	2	Header	FF	11111111	255
	3	Header	FF	11111111	255
	4	Header	FF	11111111	255
	5	Header	FF	11111111	255
	6	Header	FF	11111111	255
	7	Header	00	00000000	0
Vendor / Product EDID Version	8	EISA manufacture code = 3 Character ID	06	00000110	6
	9	EISA manufacture code (Compressed ASCII)	AF	10101111	175
	0A	Panel Supplier Reserved – Product Code	ED	11101101	237
	0B	Panel Supplier Reserved – Product Code	20	00100110	38
	0C	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
	0D	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
	0E	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
	0F	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
	10	Week of manufacture	00	00000000	0
	11	Year of manufacture	1C	00011100	28
	12	EDID structure version # = 1	01	00000001	1
	13	EDID revision # = 4	04	00000100	4
Display Parameters	14	Video I/P definition	A5	10100101	165
	15	Max H image size = ?? cm(Rounded to cm)	22	00100010	34
	16	Max V image size = ?? cm(Rounded to cm)	13	00010011	19
	17	Display gamma = (gamma × 100)-100 = Example: (2.2×100) – 100 = 120	78	01111000	120
	18	Feature support	02	00000010	2
Panel Color Coordinates	19	Red/Green Low bit (RxLy/GxGy)	C6	11000110	198
	1A	Blue/White Low bit (BxBY/WxWy)	35	00110101	53
	1B	Red X Rx = 0.???	A3	10100011	163
	1C	Red Y Ry = 0.???	56	01010110	86
	1D	Green X Rx = 0.???	52	01010010	82
	1E	Green Y Ry = 0.???	9E	10011110	158
	1F	Blue X Rx = 0.???	28	00101000	40
	20	Blue Y Ry = 0.???	0A	00001010	10
	21	White X Rx = 0.???	50	01010000	80
	22	White Y Ry = 0.???	54	01010100	84
Establish ed Timings	23	Established timings 1 (00h if not used)	00	00000000	0
	24	Established timings 2 (00h if not used)	00	00000000	0
	25	Manufacturer's timings (00h if not used)	00	00000000	0
Standard Timing ID	26	Standard timing ID1 (01h if not used)	01	00000001	1
	27	Standard timing ID1 (01h if not used)	01	00000001	1
	28	Standard timing ID2 (01h if not used)	01	00000001	1
	29	Standard timing ID2 (01h if not used)	01	00000001	1
	2A	Standard timing ID3 (01h if not used)	01	00000001	1
	2B	Standard timing ID3 (01h if not used)	01	00000001	1
	2C	Standard timing ID4 (01h if not used)	01	00000001	1
	2D	Standard timing ID4 (01h if not used)	01	00000001	1
	2E	Standard timing ID5 (01h if not used)	01	00000001	1



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	2F	Standard timing ID5 (01h if not used)	01	00000001	1
	30	Standard timing ID6 (01h if not used)	01	00000001	1
	31	Standard timing ID6 (01h if not used)	01	00000001	1
	32	Standard timing ID7 (01h if not used)	01	00000001	1
	33	Standard timing ID7 (01h if not used)	01	00000001	1
	34	Standard timing ID8 (01h if not used)	01	00000001	1
	35	Standard timing ID8 (01h if not used)	01	00000001	1
Timing Descriptor #1	36	Pixel Clock/10,000 (LSB)	14	00010100	26
	37	Pixel Clock/10,000 (MSB)	37	00110111	55
	38	Horizontal Active = ??? pixels (lower 8 bits)	80	10000000	128
	39	Horizontal Blanking (Thbp) = 320 pixels (lower 8 bits)	B4	10110100	180
	3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	70	01110000	112
	3B	Vertical Active = ??? lines	38	00111000	56
	3C	Vertical Blanking (Tvbp) = ?? lines (DE Blanking typ. for DE only panels)	26	00100110	38
	3D	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	40	01000000	64
	3E	Horizontal Sync, Offset (Thfp) = ?? pixels	6C	01101100	108
	3F	Horizontal Sync, Pulse Width = ??? pixels	30	00110000	48
	40	Vertical Sync, Offset (Tvfp) = ? lines Sync Width = ? lines	AA	10101010	170
	41	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0
	42	Horizontal Image Size = ??? mm	58	01011000	88
	43	Vertical image Size = ??? mm	C2	11000010	194
	44	Horizontal Image Size / Vertical image size	10	00010000	16
	45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0
	46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0
	47	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, 01: Stereo, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bit 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3 ==> fix=1A	1A	00011010	26
Timing Descriptor #2 (=Timing Descriptor #1)	48	Pixel Clock/10,000 (LSB)	10	00010000	16
	49	Pixel Clock/10,000	2C	00101100	44
	4A	Horizontal Active = xxxx pixels (lower 8 bits)	80	10000000	128
	4B	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)	B4	10110100	180
	4C	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	70	01110000	112
	4D	Vertical Active = xxxx lines	38	00111000	56
	4E	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels)	26	00100110	38
	4F	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	40	01000000	64
	50	Horizontal Sync, Offset (Thfp) = xxxx pixels	6C	01101100	108
	51	Horizontal Sync, Pulse Width = xxxx pixels	30	00110000	48
	52	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	AA	10101010	170
	53	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0
	54	Horizontal Image Size = xxx mm	58	01011000	88
	55	Vertical image Size = xxx mm	C2	11000010	194
	56	Horizontal Image Size / Vertical image size	10	00010000	16



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	57	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0
	58	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0
		Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no stereo, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3			
	59	==> fix=1A	1A	00011010	26
Timing Descriptor #3 Dell specific information	5A	Flag	00	00000000	0
	5B	Flag	00	00000000	0
	5C	Flag	00	00000000	0
	5D	Data Type Tag: Alphanumeric Data String (ASCII) ==> fix=FE	FE	11111110	254
	5E	Flag	00	00000000	0
	5F	Dell P/N 1 st Character	47	01000111	71
	60	Dell P/N 2 nd Character	48	01001000	72
	61	Dell P/N 3 rd Character	57	01010111	87
	62	Dell P/N 4 th Character	31	00110001	49
	63	Dell P/N 5 th Character	4B	01001011	75
	64	EDID Revision Bit[6:0] See charts below Bit[7] 0: X-rev, 1: A-rev	80	10000000	128
	65	Manufacturer P/N	42	01000010	66
	66	Manufacturer P/N	31	00110001	49
	67	Manufacturer P/N	35	00110101	53
	68	Manufacturer P/N	36	00110110	54
	69	Manufacturer P/N	48	01001000	72
	6A	Manufacturer P/N	41	01000001	65
	6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	4E	01001110	78
Timing Descriptor #4	6C	Flag	00	00000000	0
	6D	Flag	00	00000000	0
	6E	Flag	00	00000000	0
	6F	Data Type Tag: Manufacturer Specified Data 00 ==> fix=00	00	00000000	0
	70	Flag	00	00000000	0
	71	Color Management	03	00000011	3
	72	Panel Structure	41	01000001	65
	73	Frame Rate	02	00000010	2
	74	Light Controller Interface and Luminance	9E	10011110	158
	75	Outdoor Features	00	00000000	0
	76	Multi-Media Features	10	00010000	16
	77	Multi-Media Features	00	00000000	0
	78	Special Features #1	00	00000000	0
	79	Special Features #2	0A	00001010	10
	7A	Special Features #3	01	00000001	1
	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010	10
	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
Checksum	7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00	00000000	0
	7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	02	00000010	2



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10.2 Notes

DPCD Ver.	sDRRS	DCR	DMRRS	PSR	MBO	VESA DSC	MSO	Free-Sync	HDR	Dimming
1.3	On	On	Off	On	Off	Off	Off	Off	No	PWM

- 1) Any other PCB component is lower than top polarizer.
- 2) The vernier caliper is used to measure the X,Y,Z outline dimension and other dimensions are measured by 3D measuring instrument. For the flatness is measured by the thick gauge.
- 3) Attached cell tape is naturally floating, and need to be compressed while measuring.