Product Specification

AU OPTRONICS CORPORATION

( ) Preliminary Specifications
(✓) Final Specifications

Module	14.0" WUXGA 16:10 Color TFT-LCD with LED Backlight design
Model Name	B140UAN02.2
H/W	1A
Note ( )	*LED Backlight with driving circuit design*

Customer	Date	Approved by	Date
		Grace Hung	07/11/2022
Checked & Approved by	Date	Prepared by	Date
		WanChiao Hu	07/11/2022
Note: This Specification is subject to change without notice.		MPBU Marketing Division AU Optronics corporation	

Contents

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Record of Revision

Version and Date	Page	Old description	New Description	Remark
1.0 2022/07/11	All	First Edition for Customer create PN		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module.The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B140UAN02.2 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:10 WUXGA, 1920(H)x1200(V) screen and 16.7M colors (RGB 8-bits data driver) with LED backlight driving circuit. All input signals are eDP(Embedded DisplayPort) interface compatible.

B140UAN02.2 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

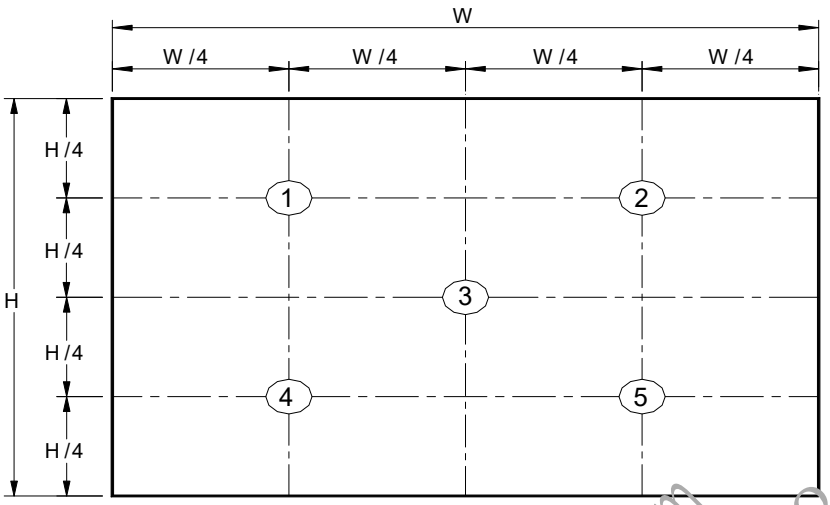
Items	Unit	Specifications			
Screen Diagonal	[mm]	355.6			
Active Area	[mm]	301.59 X 188.50			
Pixels H x V		1920x3(RGB) x 1200			
Pixel Pitch	[mm]	0.15708 X 0.15708			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black (AHVA)			
White Luminance (I_{LED}=8.0mA) **(Note: ILED is LED current)**	[cd/m^2]	400 typ. (5 points average) 340 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		1200 typ / 1000 min			
Response Time	[ms]	30 typ / 35 max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	2.16 W			
Weight	[Grams]	210 max.			
Physical Size	[mm]		Min.	Typ.	Max.
		Length	306.29	306.59	306.89
		Width	197.15	197.45	198.45
		Thickness	-	-	2.1/3.9
Electrical Interface		eDP1.4			
Glass Thickness	[mm]	0.2			
Surface Treatment		Anti-Glare, Hardness 3H			
Support Color		16.7M colors (RGB –8bits)			
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60			
RoHS Compliance		RoHS Compliance			

2.2 Optical Characteristics

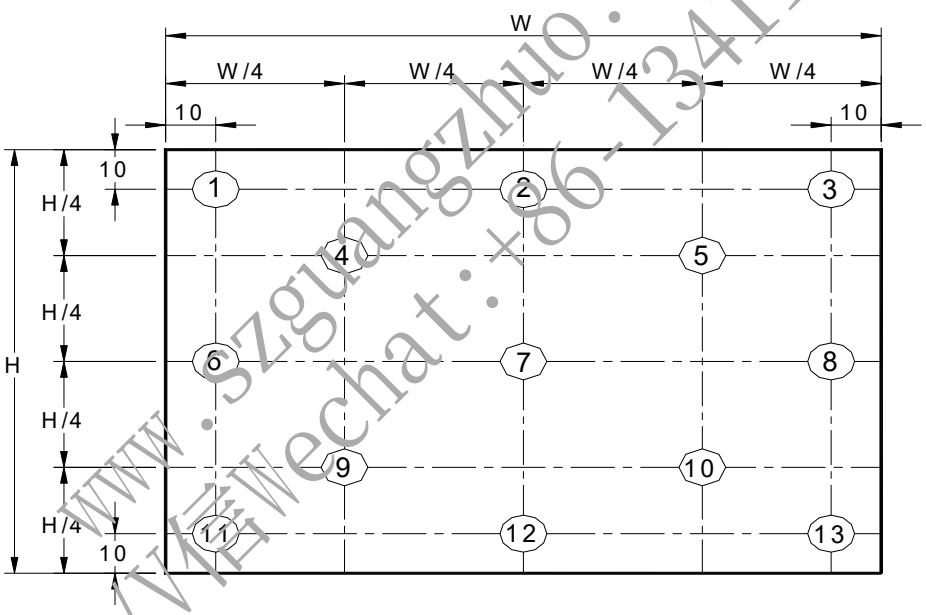
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=8.0mA			5 points average	340	400		cd/m²	1, 4, 5.
Viewing Angle		θ_R	Horizontal (Right)	-	85	-	degree	4, 9
		θ_L	CR = 10 (Left)	-	85	-		
		ψ_H	Vertical (Upper)	-	85	-	degree	
		ψ_L	CR = 10 (Lower)	-	85	-		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.6		2, 3, 4
Contrast Ratio		CR		1000	1200	-		4, 6
Cross talk		%			4			4, 7
Response Time		T_{RT}	Rising + Falling	-	30	35	msec	4, 8
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.626	0.656	0.686		4
		Ry		0.302	0.332	0.362		
	Green	Gx		0.255	0.285	0.315		
		Gy		0.591	0.621	0.651		
	Blue	Bx		0.115	0.145	0.175		
		By		0.027	0.057	0.087		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
sRGB		%		95	100	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



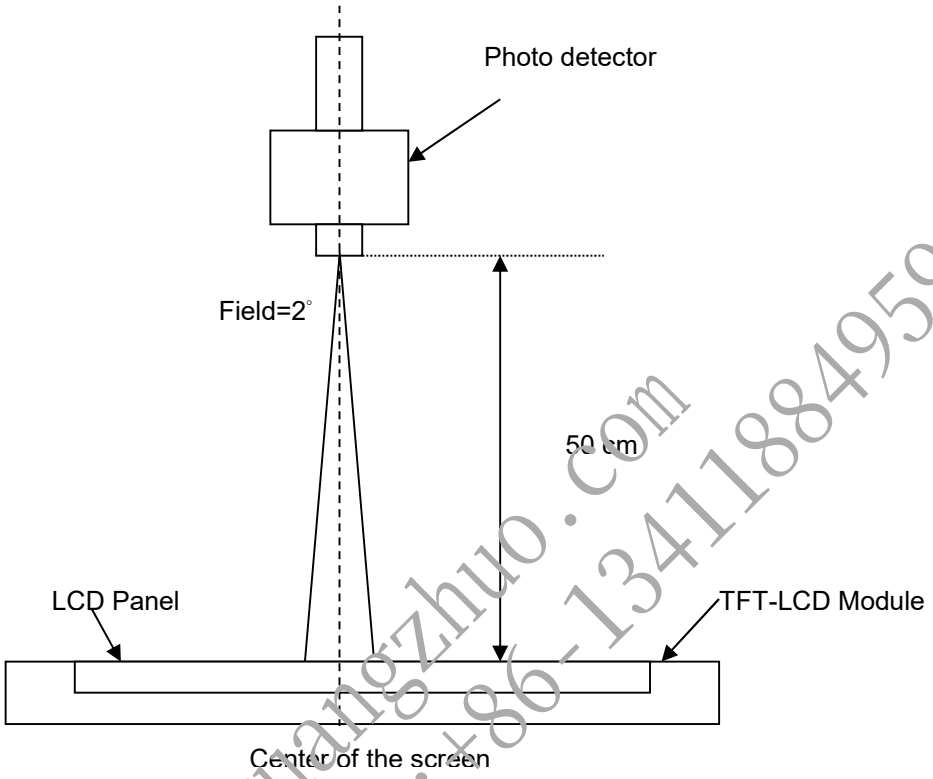
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

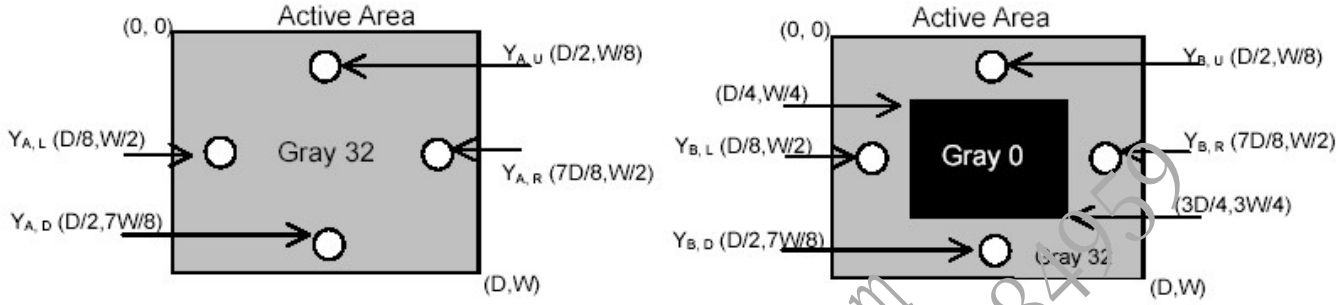
Note 7： Definition of Cross Talk (CT)

CT = | Y_B – Y_A | / Y_A × 100 (%)

Where

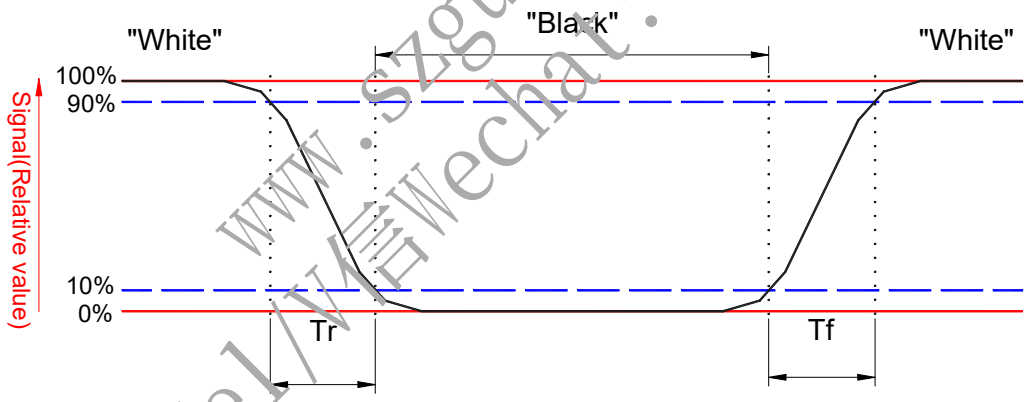
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



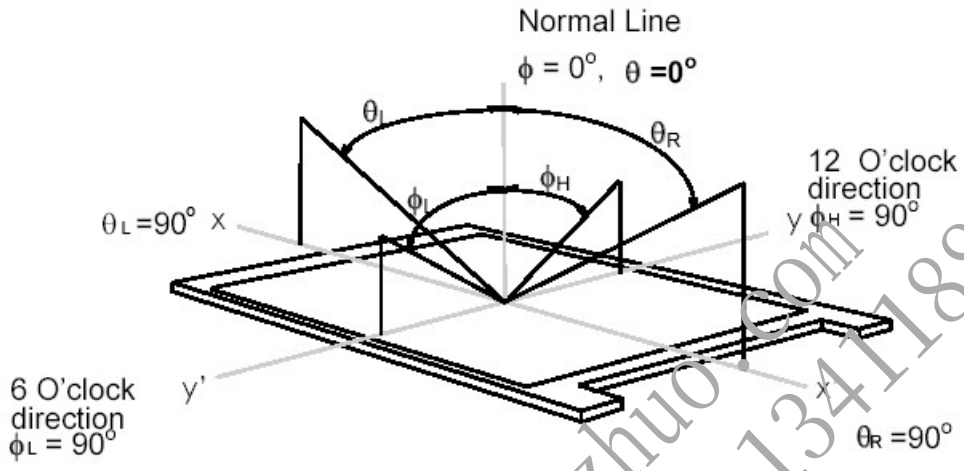
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



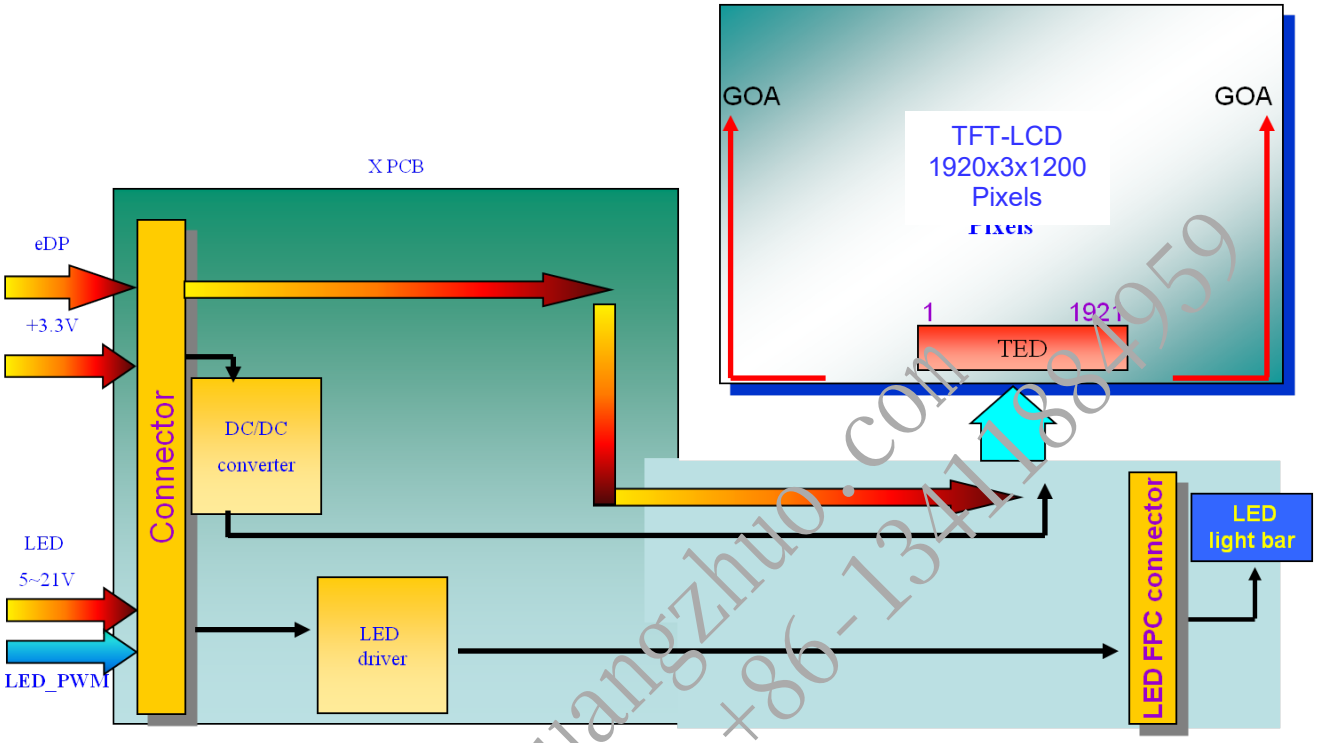
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 14.0 inches wide Color TFT/LCD 30 Pin



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	90	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	90	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

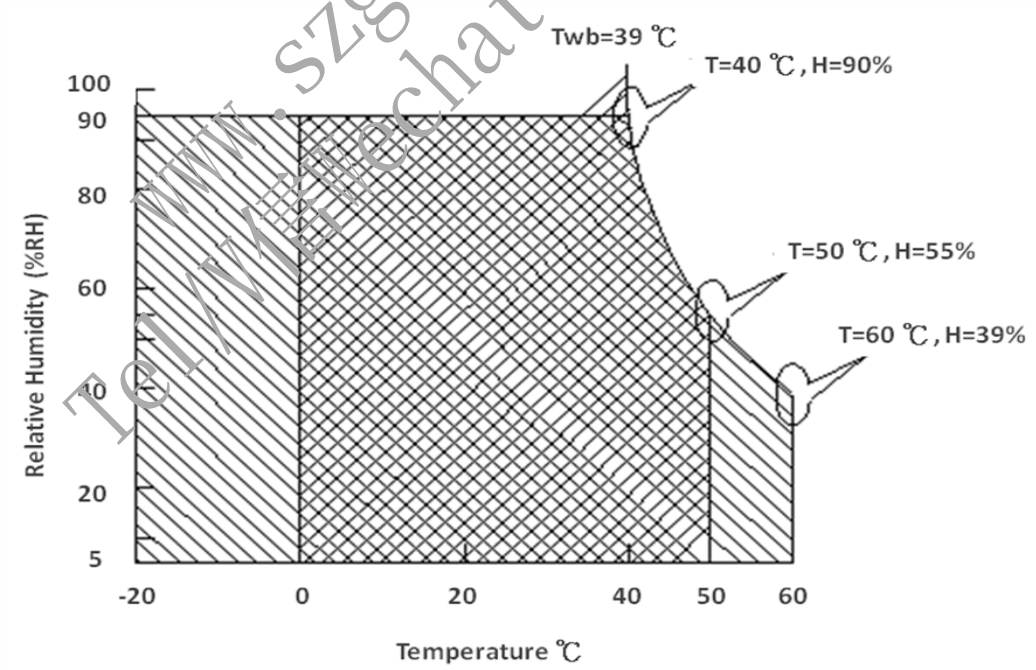
Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard)

Note 5: The packing material of system forbid to involve ammonium component

Note 6: The reliability test conditions of system do not exceed the verified conditions of TFT module

Note 7: Be sure the panel test condition do not exceed the component limitation of TFT module(TN Liquid crystal , for example)



Operating Range

Storage Range

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

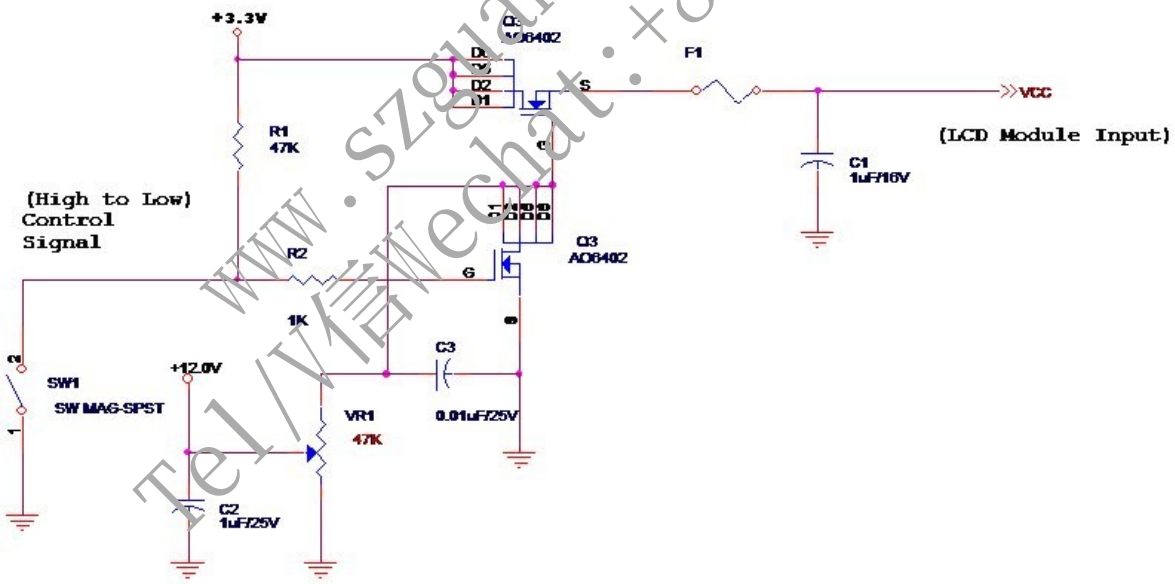
The power specification are measured under 25℃ and frame frenquency under 60Hz

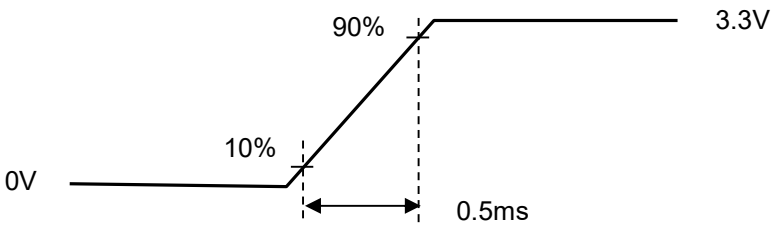
Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	0.36	1.0	[Watt]	Note 1
IDD	IDD Current	-		333	[mA]	Note 1
IRush	Inrush Current	-		2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-		100	[mV] p-p	

Note 1 : PDD(typ)@ mosaic pattern Maximum Power; PDD(Max)@ R/G/B pattern Maximum Power

IDD(Max)=PDD(Max) / VDD(Min)

Note 2：Measure Condition





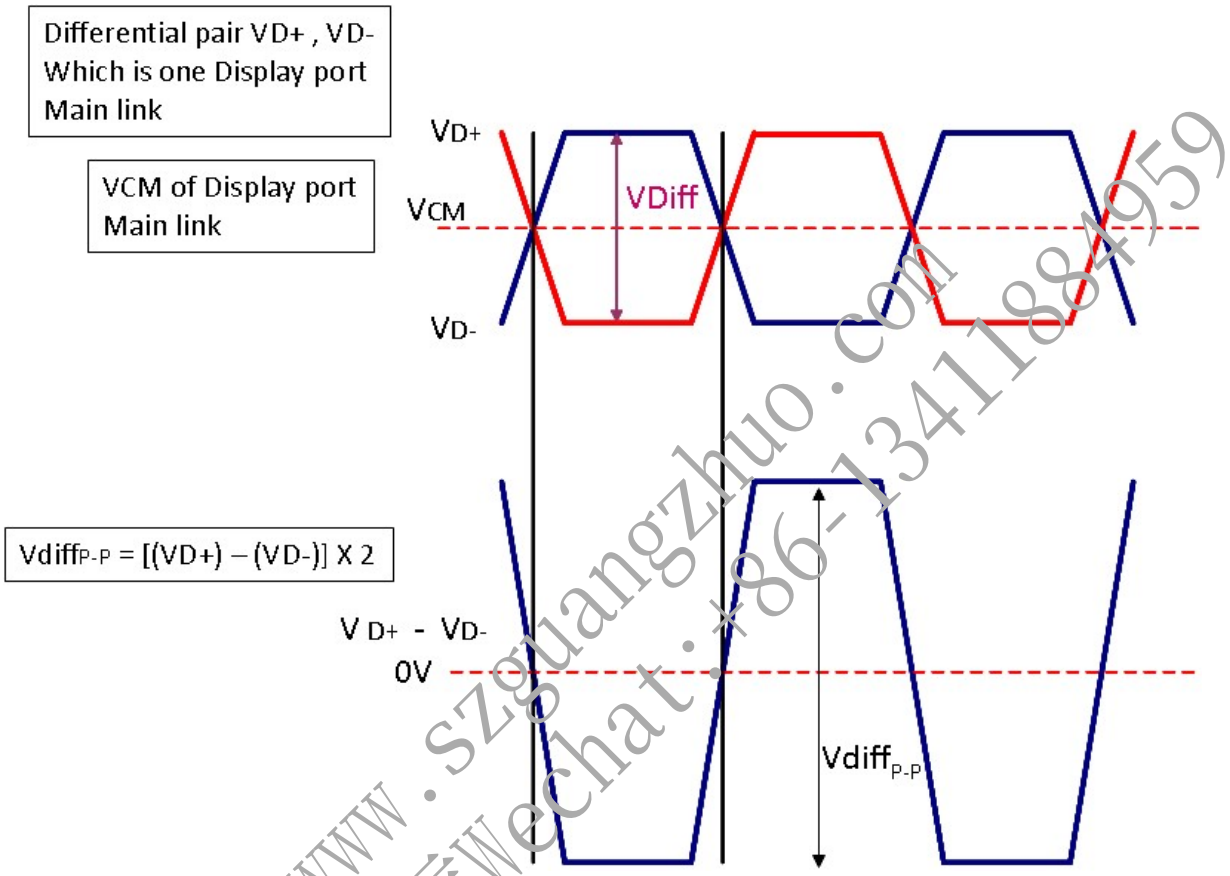
Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

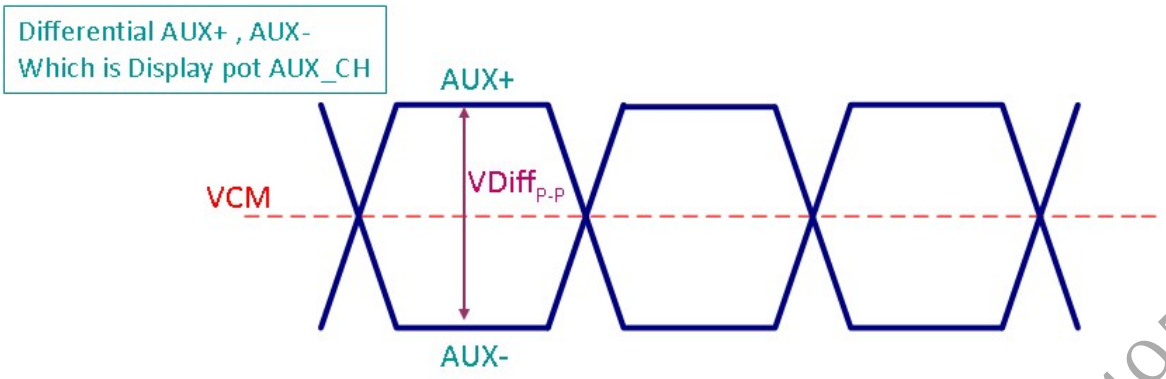
Display Port main link signal:



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	HBR:150		1320	mV

Fallow as VESA display port standard V1.3

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
$VDiff_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	400		800	mV

Fallow as VESA display port standard V1.3.

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25		3.6	V

Fallow as VESA display port standard V1.3.

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	1.8	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25℃), Note 2 I_F=9.5 mA

Note 1: Calculator value for reference P_{LED} = VF (Normal Distribution) * IF (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

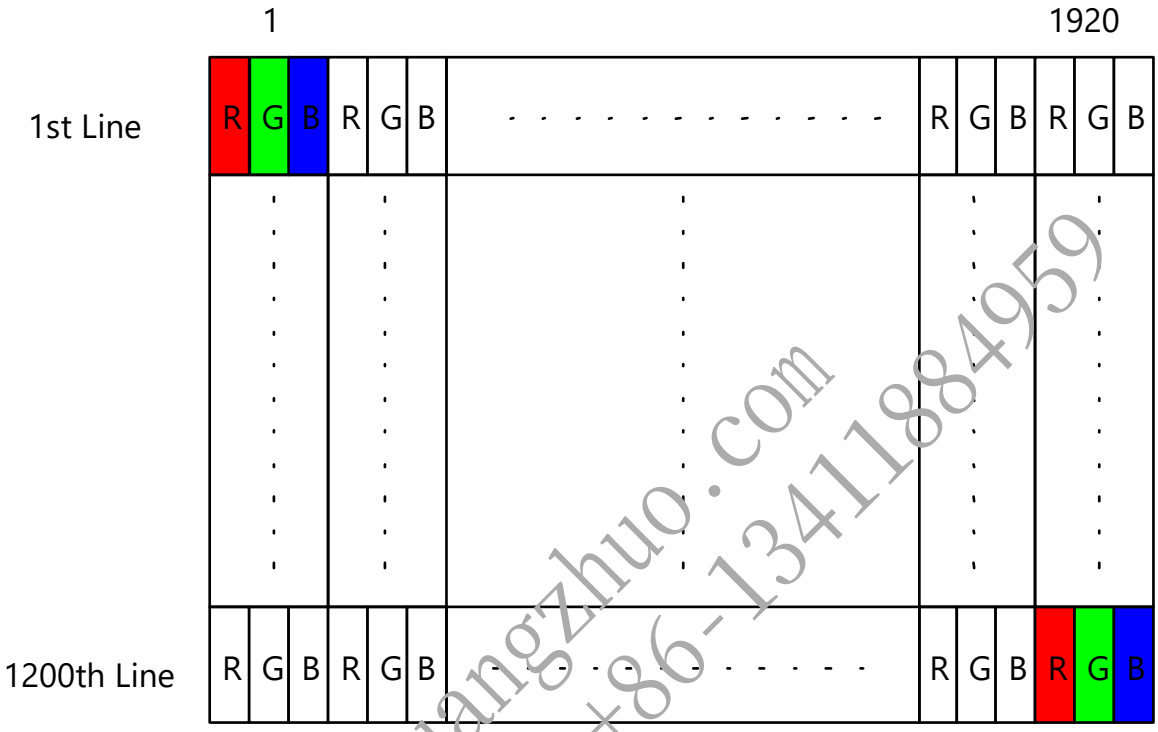
Parameter	Symbol	Min.	Typ	Max	Units	Remark
LED Power Supply	VLED	5.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2.2	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.2	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	-	2K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

Note 1 : Recommend system pull up/down resistor no bigger than 10kohm

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

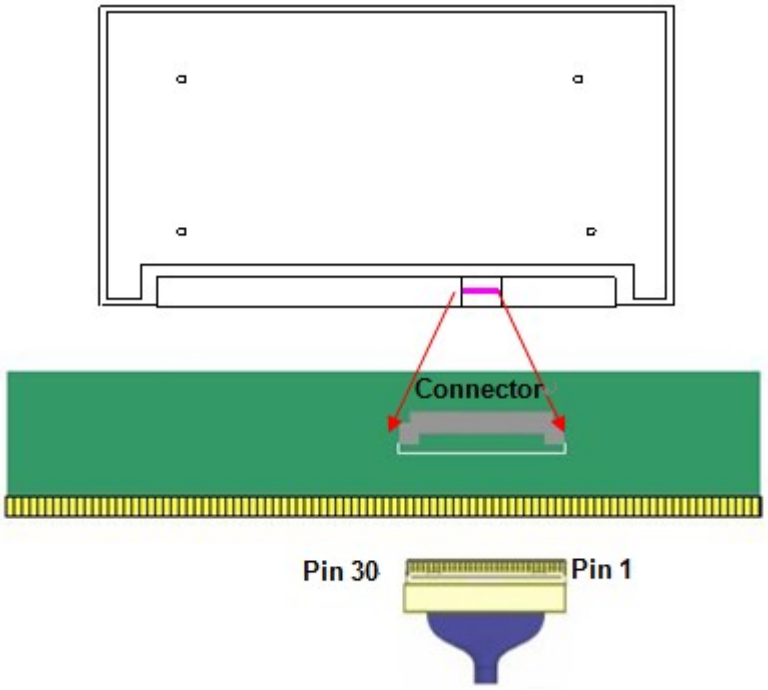
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX
Type / Part Number	IPEX 20765-030E-11A or compatible
Mating Housing/Part Number	I-PEX 20704-030T-13

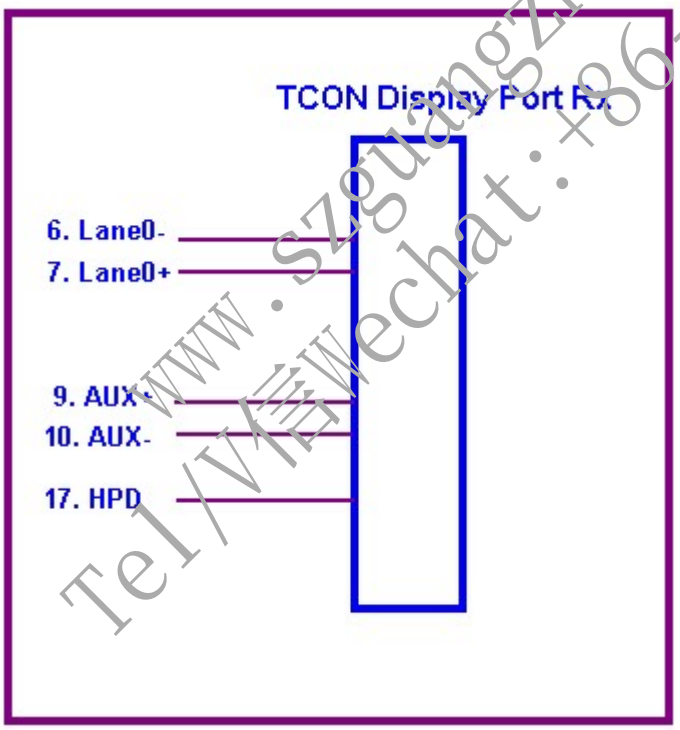
6.2.2 Pin Assignment (2 Lane)

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO	Symbol	Function
1	NC	No Connect
2	H_GND	High Speed Ground
3	Lane1_N	Comp Signal Lane 1
4	Lane1_P	True Signal Link Lane 1
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	LCD_Self_Test	LCD Panel Self Test Enable
15	LCD GND	LCD logic and driver ground
16	LCD GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	BL_GND	Backlight_ground
19	BL_GND	Backlight_ground
20	BL_GND	Backlight_ground
21	BL_GND	Backlight_ground
22	BL_Enable	Backlight On / Off
23	BL PWM DIM	System PWM signal Input
24	AUO use only	AUO use only
25	AUO use only	AUO use only
26	BL_PWR	Backlight power (5V~21V)
27	BL_PWR	Backlight power (5V~21V)
28	BL_PWR	Backlight power (5V~21V)
29	BL_PWR	Backlight power (5V~21V)
30	NC	No Connect



Note1: Start from right side.
Note2: Input signals shall be low or High-impedance state when VDD is off.
Internal circuit of **eDP inputs** are as following.



6.3 Interface Timing

6.3.1 Timing Characteristics

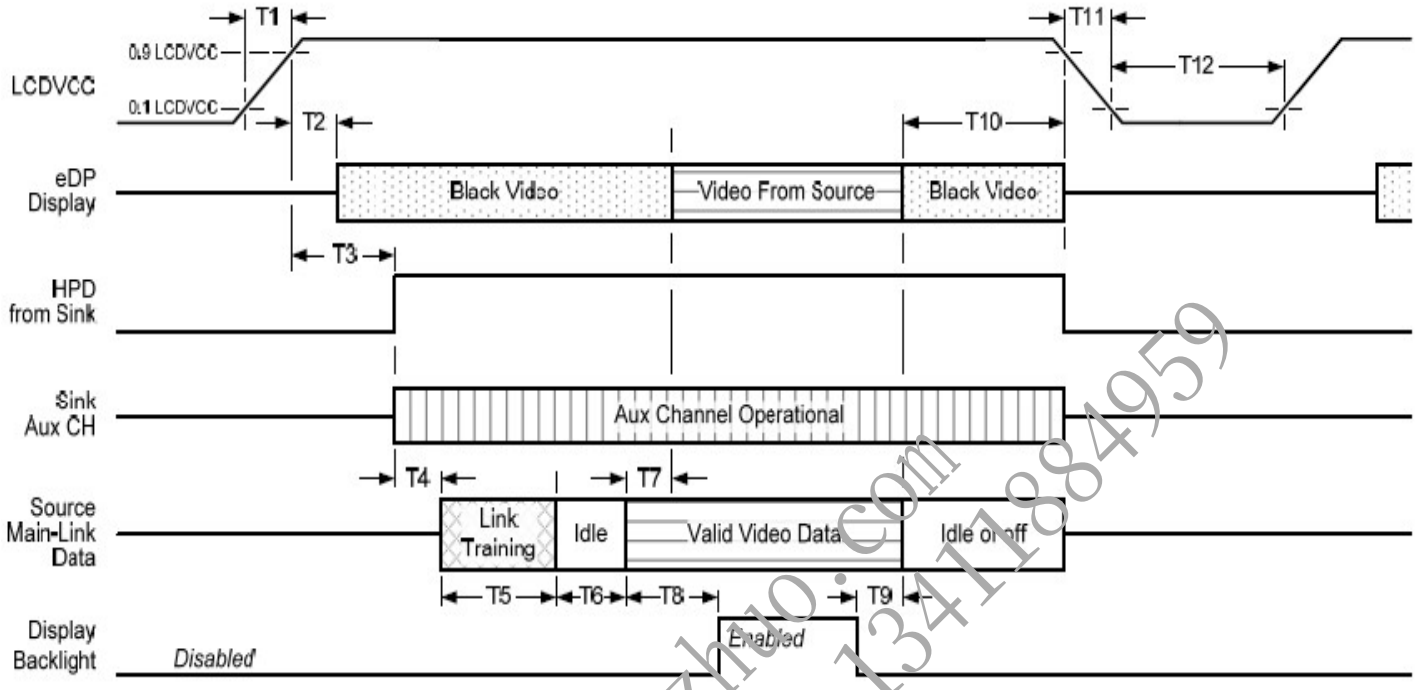
Basically, interface timings should match the 1920x1200 / 60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	48	60	-	Hz
Clock frequency		1/ T_{Clock}	124.88	156.1	-	MHz
Vertical Section	Period	T_V	1236	1236	1200+A	Vertical Section
	Active	T_{VD}	1200			
	Blanking	T_{VB}	36	36	A	
Horizontal Section	Period	T_H	2104	2104	1920+B	Horizontal Section
	Active	T_{HD}	1920			
	Blanking	T_{HB}	184	184	B	

Note 1 : The above is as optimized setting
Note 2 : The maximum clock frequency = (1920+B)*(1200+A)*60<156.1MHz

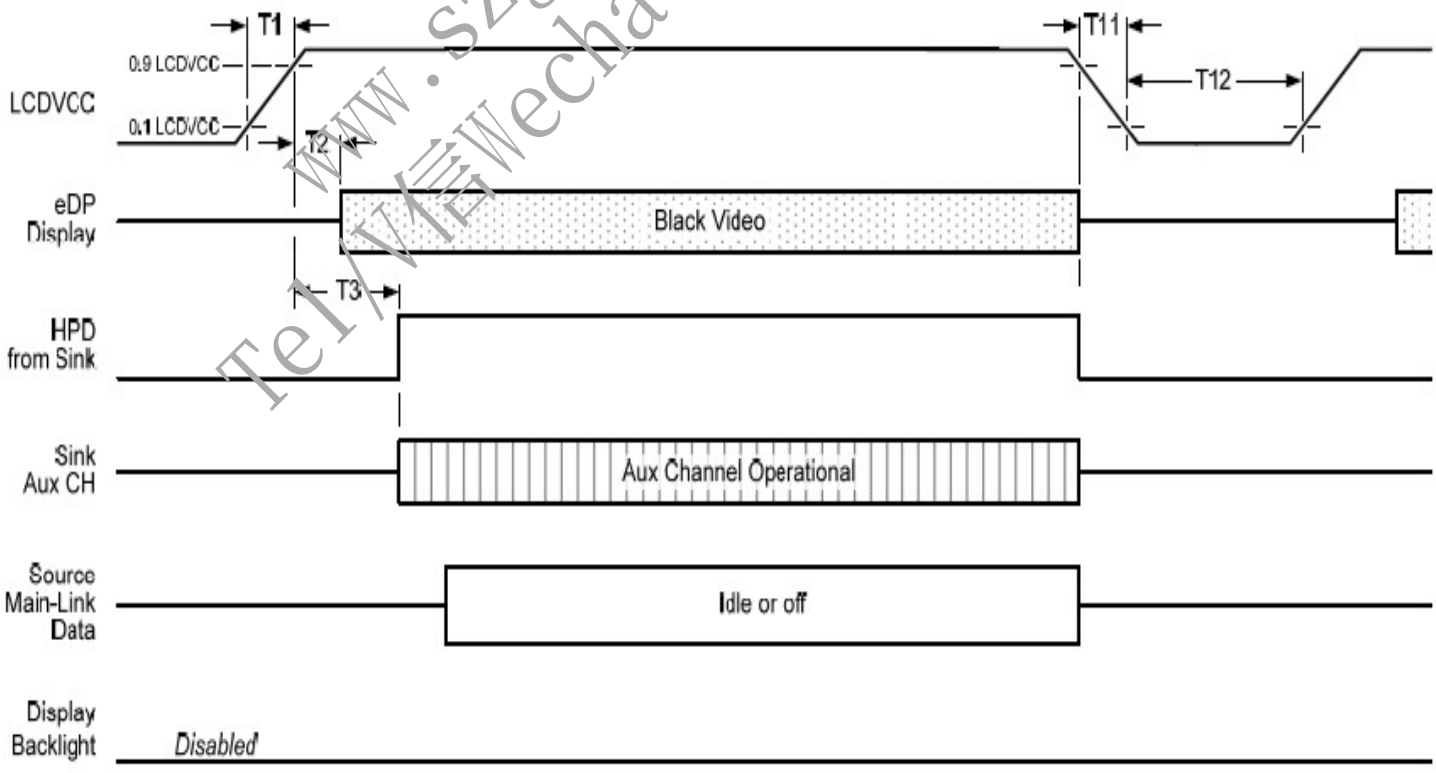
6.4 Power ON/OFF Sequence

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	50ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:

-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).

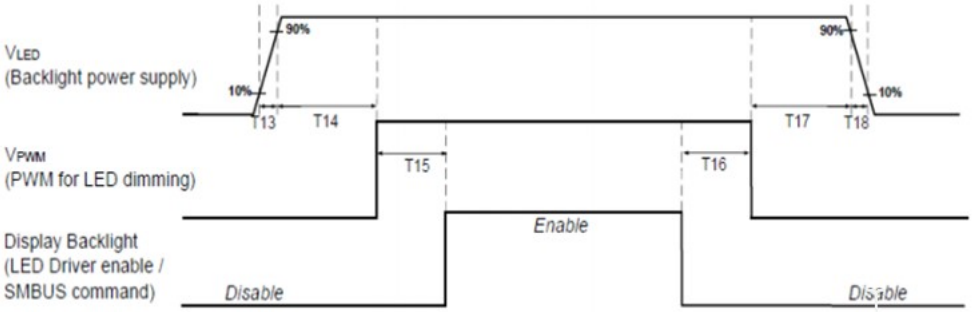
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Note 4: T8>T7

Display Port panel B/L power sequence timing parameter:

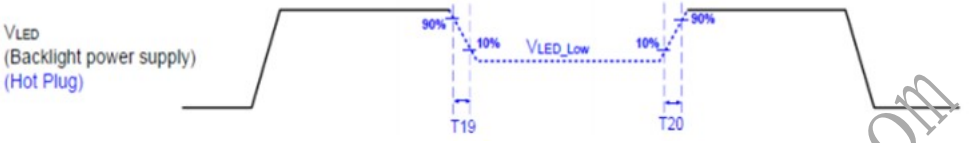


	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	0	-
T16	0	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM}= 1/PWM Frequency

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

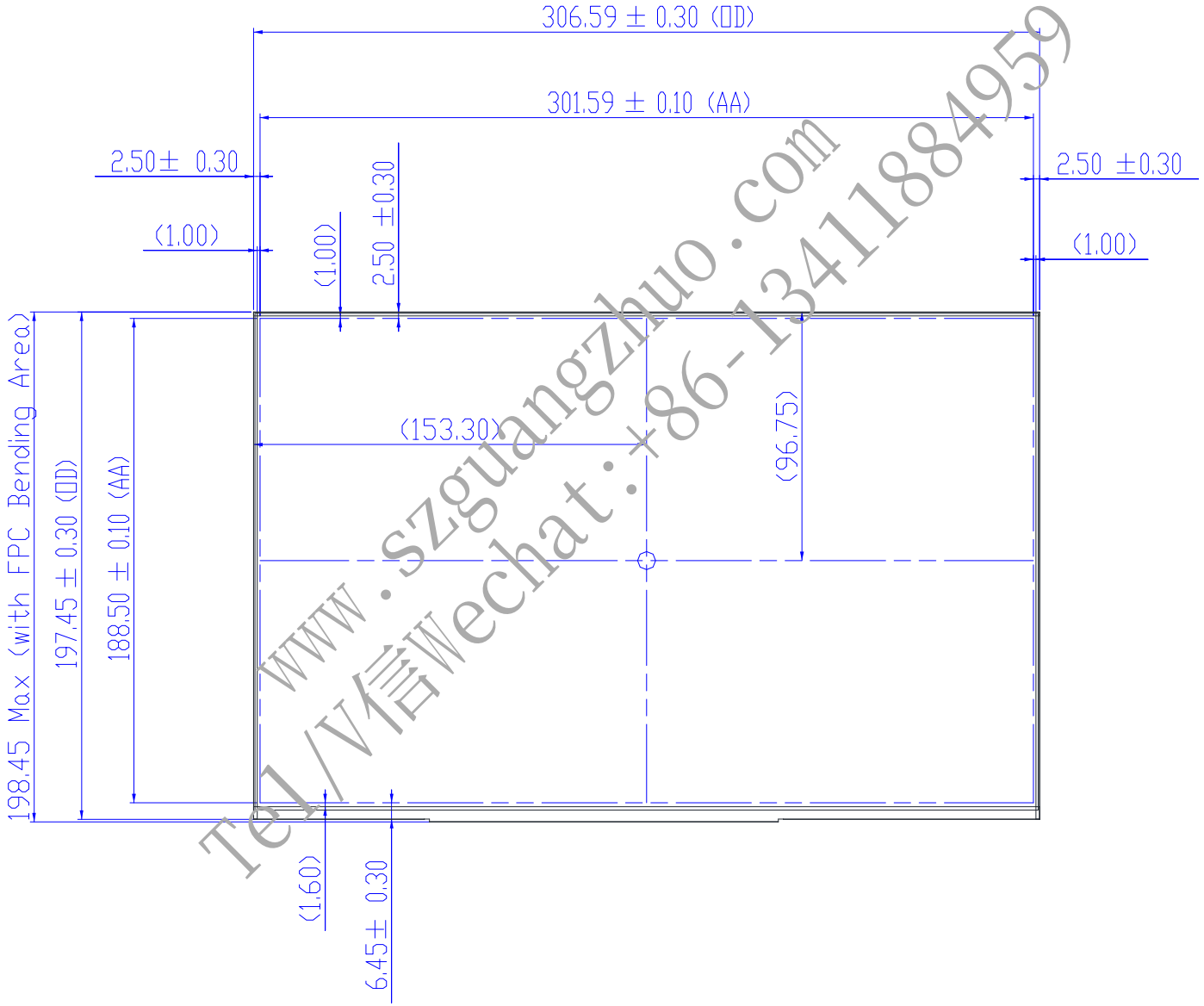
Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 35%RH, 300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 250h	
Thermal Shock Test	Ta=-20℃to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable. No data lost, No hardware failures.

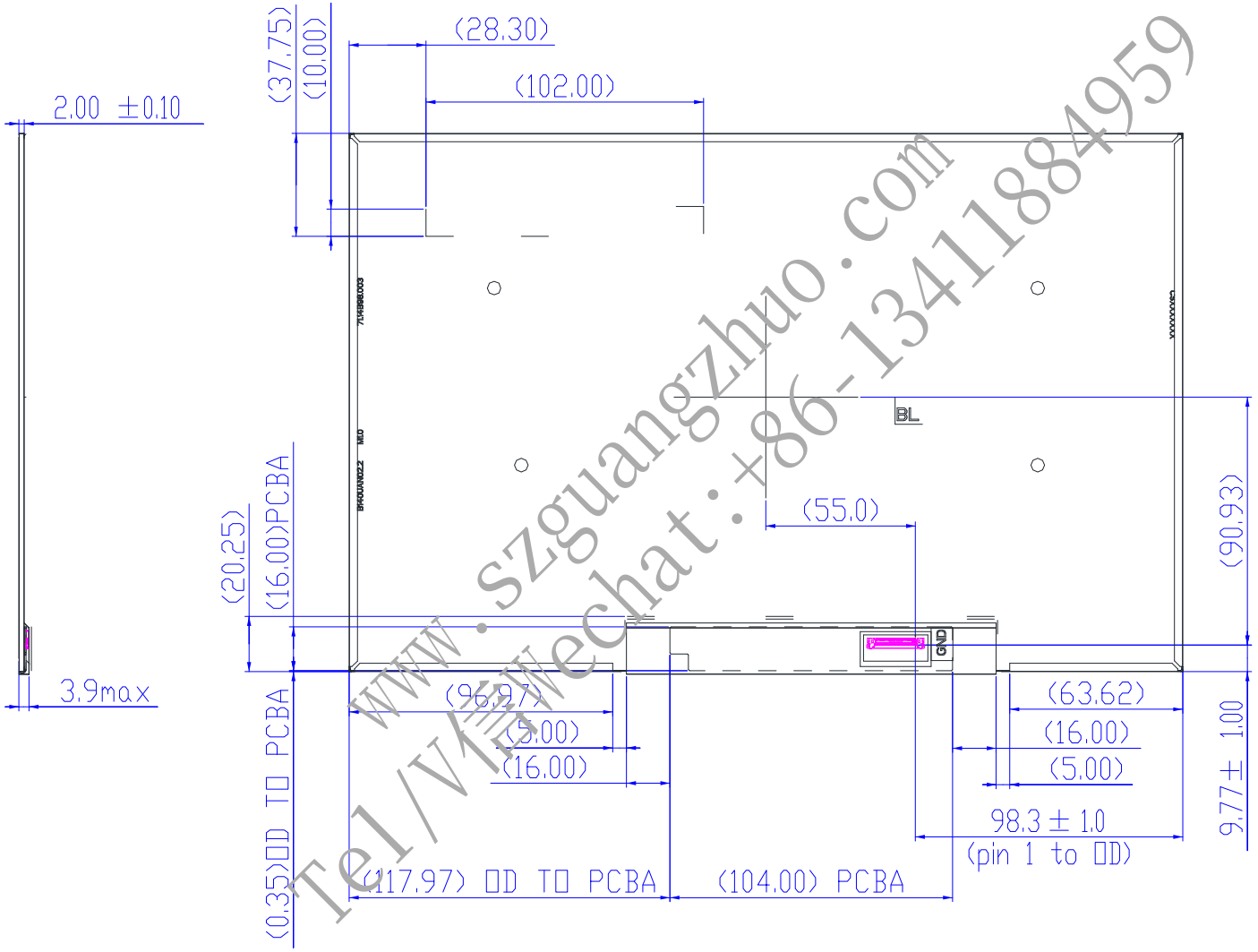
Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

8.1 LCM Outline Dimension



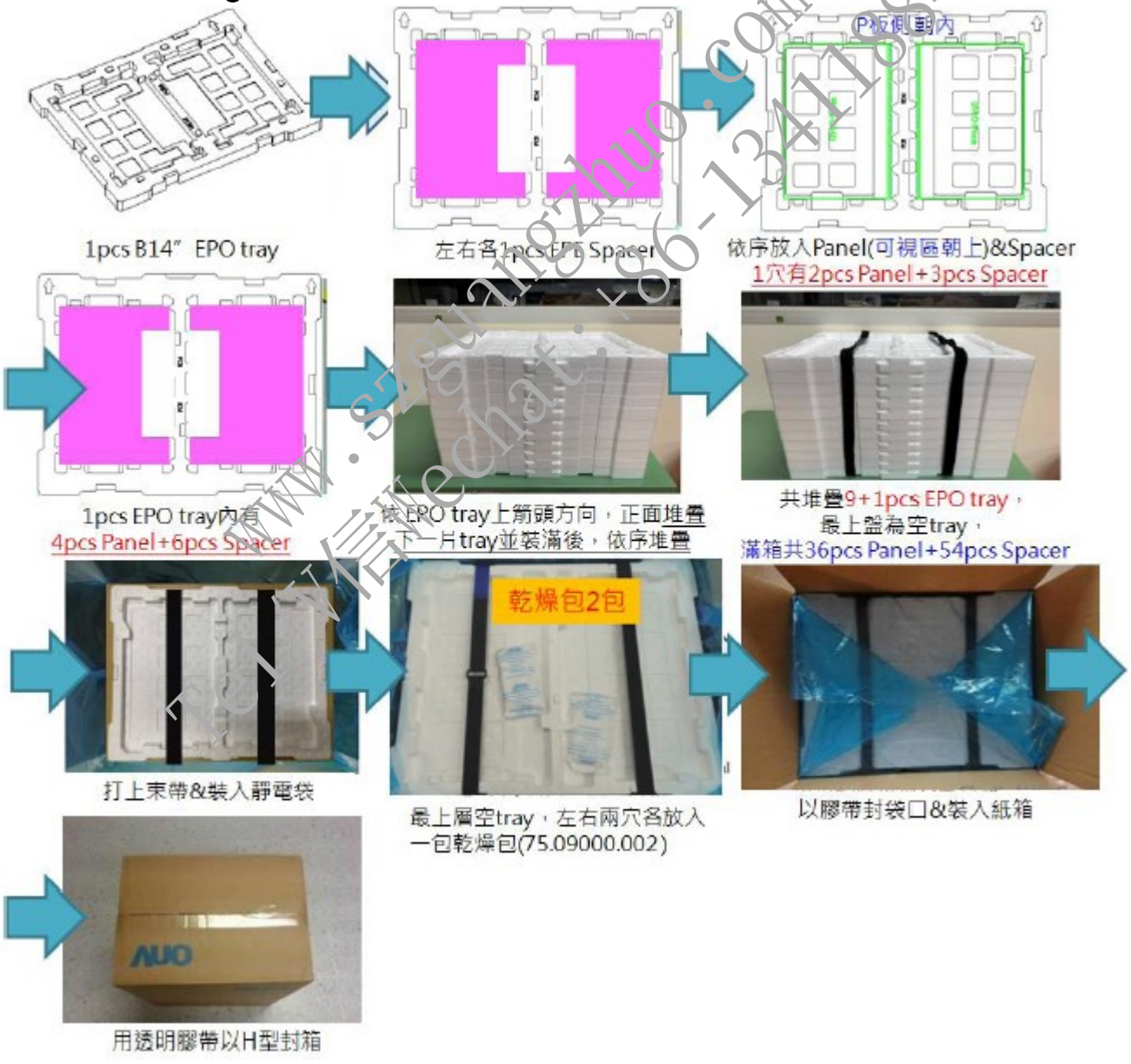
AU OPTRONICS CORPORATION



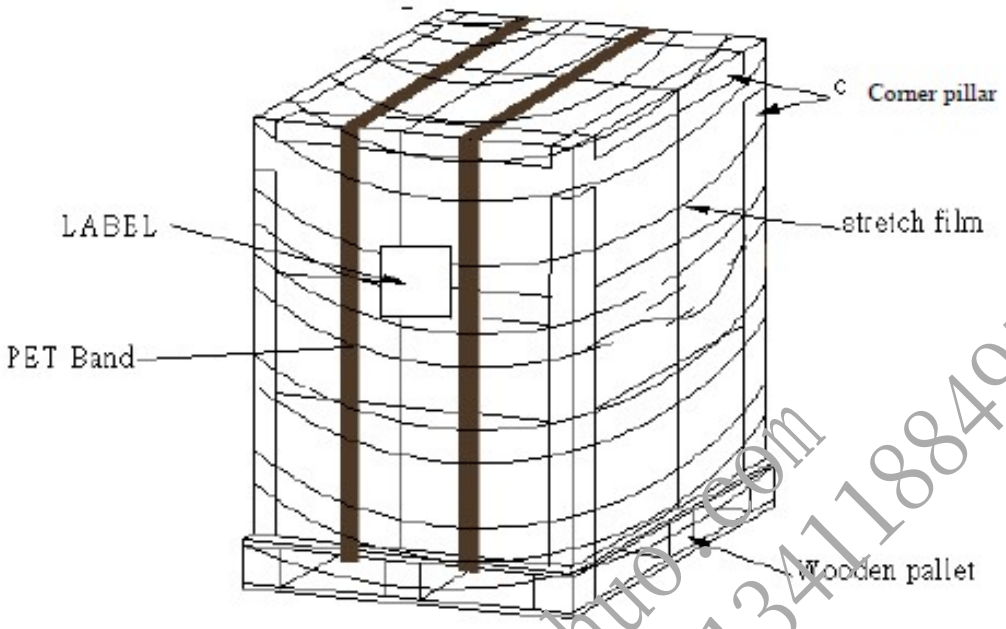
9. Shipping and Package

9.1 Shipping Label Format

9.2 Carton Package



9.3 Shipping Package of Palletizing Sequence



單層 pallet 打棧示意圖
One pallet illustration

10. Appendix: EDID Description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01	Header	FF	11111111	255	
02	Header	FF	11111111	255	
03	Header	FF	11111111	255	
04	Header	FF	11111111	255	
05	Header	FF	11111111	255	
06	Header	FF	11111111	255	
07	Header	00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	A0	10100000	160	
0B	Product Code	72	01110010	114	
0C	32-bit ser #	00	00000000	0	
0D	ID S/N - option	00	00000000	0	
0E	ID S/N - option	00	00000000	0	
0F	ID S/N - option	00	00000000	0	
10	Week of manufacture	1E	00011110	30	
11	Year of manufacture	1F	00011111	31	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	04	00000100	4	
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	A5	10100101	165	
15	**Max H image size** *(rounded to cm)*	1E	00011110	30	
16	**Max V image size** *(rounded to cm)*	13	00010011	19	
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120	
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	03	00000011	3	
19	Red/green low bits **(Lower 2:2:2:2 bits)**	00	00000000	0	
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	25	00100101	37	
1B	Red x **(Upper 8 bits)**	A8	10101000	168	
1C	Red y/ highER 8 bits	55	01010101	85	
1D	Green x	49	01001001	73	
1E	Green y	9F	10011111	159	
1F	Blue x	25	00100101	37	
20	Blue y	0E	00001110	14	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27	Standard timing #1	01	00000001	1	
28	Standard timing #2	01	00000001	1	
29	Standard timing #2	01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B	Standard timing #3	01	00000001	1	

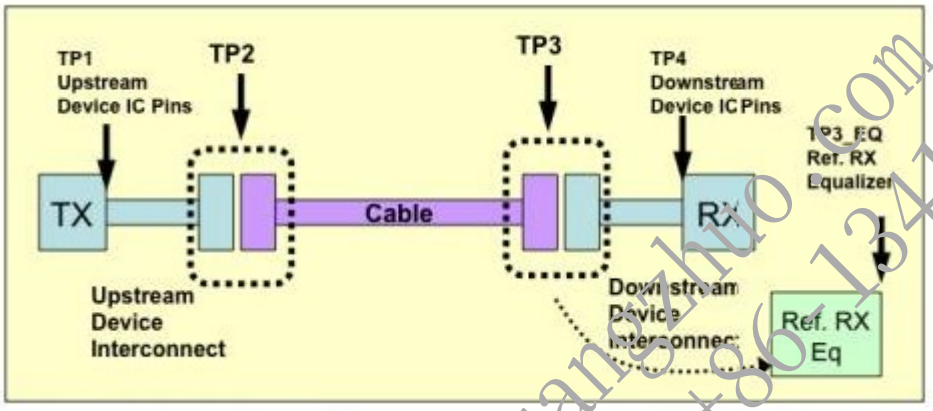
2C	Standard timing #4	01	00000001	1	
2D	Standard timing #4	01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F	Standard timing #5	01	00000001	1	
30	Standard timing #6	01	00000001	1	
31	Standard timing #6	01	00000001	1	
32	Standard timing #7	01	00000001	1	
33	Standard timing #7	01	00000001	1	
34	Standard timing #8	01	00000001	1	
35	Standard timing #8	01	00000001	1	
36	Pixel Clock/10000 LSB	FA	11111010	250	
37	Pixel Clock/10000 USB	3C	00111100	60	
38	Horz active **Lower 8bits**	80	10000000	128	
39	Horz blanking **Lower 8bits**	B8	10111000	184	
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	70	01110000	112	
3B	Vertical Active **Lower 8bits**	B0	10110000	176	
3C	Vertical Blanking **Lower 8bits**	24	00100100	36	
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	40	01000000	64	
3E	HorzSync. Offset	10	00010000	16	
3F	HorzSync.Width	10	00010000	16	
40	VertSync.Offset : VertSync.Width	3E	00111110	62	
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0	
42	Horizontal Image Size **Lower 8bits**	2D	00101101	45	
43	Vertical Image Size **Lower 8bits**	BC	10111100	188	
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	10	00010000	16	
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0	
46	Vertical Border *(zero for internal LCD)*	00	00000000	0	
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24	
48	Pixel Clock/10000 LSB	C8	11001000	200	
49	Pixel Clock/10000 USB	30	00110000	48	
4A	Horz active **Lower 8bits**	80	10000000	128	
4B	Horz blanking **Lower 8bits**	B8	10111000	184	
4C	HorzAct:HorzBlnk **Upper 4:4 bits**	70	01110000	112	
4D	Vertical Active **Lower 8bits**	B0	10110000	176	
4E	Vertical Blanking **Lower 8bits**	24	00100100	36	
4F	Vert Act : Vertical Blanking **(upper 4:4 bit)**	40	01000000	64	
50	HorzSync. Offset	10	00010000	16	
51	HorzSync.Width	10	00010000	16	
52	VertSync.Offset : VertSync.Width	3E	00111110	62	
53	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0	
54	Horizontal Image Size **Lower 8bits**	2D	00101101	45	
55	Vertical Image Size **Lower 8bits**	BC	10111100	188	
56	Horizontal & Vertical Image Size **(upper 4:4 bits)**	10	00010000	16	
57	Horizontal Border *(zero for internal LCD)*	00	00000000	0	
58	Vertical Border *(zero for internal LCD)*	00	00000000	0	
59	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24	
5A	descriptor #3	00	00000000	0	

5B	Reserved for definition	00	00000000	0	
5C	Reserved for definition	00	00000000	0	
5D	ASCII String	FD	11111101	253	
5E	Reserved for definition	00	00000000	0	
5F	Manufacture	30	00110000	48	0
60	Manufacture	3C	00111100	60	<
61	Manufacture	4B	01001011	75	K
62	Reserved for definition	4B	01001011	75	K
63	Reserved for definition	10	00010000	16	
64	Reserved for definition	01	00000001	1	
65	Reserved for definition	0A	00001010	10	
66	Reserved for definition	20	00100000	32	
67	Reserved for definition	20	00100000	32	
68	Reserved for definition	20	00100000	32	
69	Reserved for definition	20	00100000	32	
6A	Reserved for definition	20	00100000	32	
6B	Reserved for definition	20	00100000	32	
6C	Reserved for definition	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E	Reserved for definition	00	00000000	0	
6F	Reserved for definition	FE	11111110	254	
70	Reserved for definition	00	00000000	0	
71	Manufacture P/N	42	01000010	66	B
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	34	00110100	52	4
74	Manufacture P/N	30	00110000	48	0
75	Manufacture P/N	55	01010101	85	U
76	Manufacture P/N	41	01000001	65	A
77	Manufacture P/N	4E	01001110	78	N
78	Manufacture P/N	30	00110000	48	0
79	Manufacture P/N	32	00110010	50	2
7A	Manufacture P/N	2E	00101110	46	.
7B	Manufacture P/N	32	00110010	50	2
7C	Reserved for definition	20	00100000	32	
7D	Reserved for definition	0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	B8	10111000	184	

10.2 Notes

DPCD Ver.	sDRRS	DCR	DMRRS	PSR	LRR	MBO	VESA DSC	MSO	Free-Sync	HDR	Dimming
1.4	Off	Off	Off	PSR2	On LRR2.5	Off	Off	Off	Off	Off	PWM

1) The height of cell tape no higher than top polarizer 3.0mm
2) LED Driving Solution: Minimum change scale duty of the PWM is 0.1% @PWM frequency 200Hz.
3) When twisting or pressing LCD module, it may cause unexpected acoustic noises or sounds.
4) Maximum value of "Peak current" is as same as "Inrush current" in Electrical Characteristics (Power Specification)
5) $VDiff_{P-P}$ (Peak-to-peak Voltage at a receiving Device) follow as VESA display port standard (test point, TP3, is on panel's PCBa)



6) Suggest ODMs do not use any parts that contain the ingredient of related Ammonium > 5ppb, and other ingredients, if any.
7) Suggest ODMs do not interfere with panel after system assembly in order to avoid possible mura, yellow spot, light leakage, water ripple or side defects by mechanical stress test.