Product Specification

AU OPTRONICS CORPORATION

( ) Preliminary Specifications
(✓) Final Specifications

Module	14.0"(13.97") FHD 16:9 Color TFT-LCD with LED Backlight design
Model Name	B140HAN03.L
HW	1A
Note ( )	*oTP Display*

Customer	Date	Approved by	Date
		Grace Hung	04/17/2023
Checked & Approved by	Date	Prepared by	Date
		Hung-Wei Chen	04/17/2023
Note: This Specification is subject to change without notice.		AU Optronics corporation	

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
1.0 2023/04/17	All	First Edition for Customer		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
10) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
11) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
12) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B140HAN03.L is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 FHD, 1920(H) x1080(V) screen and 16.7M colors (RGB 6-bits with FRC) with LED backlight driving circuit. All input signals are eDP (Embedded DisplayPort) interface compatible.

B140HAN03.L is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

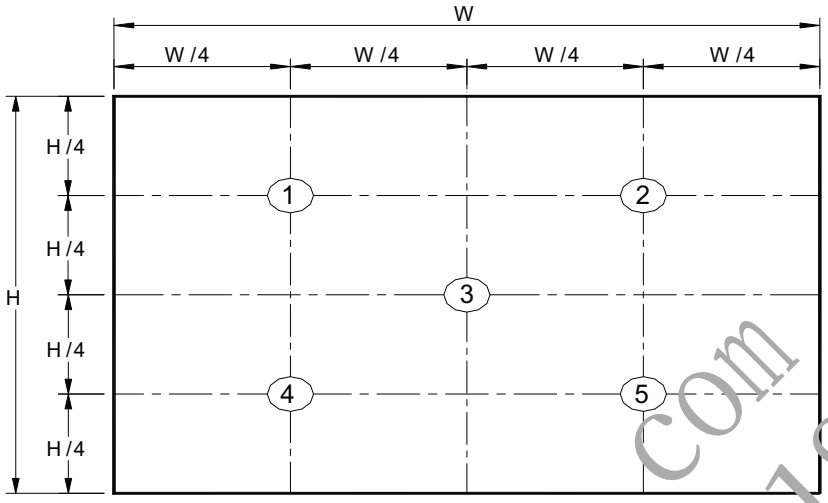
Items	Unit	Specifications			
Screen Diagonal	[mm]	354.95			
Active Area	[mm]	309.37 X 174.02			
Pixels H x V		1920x3(RGB) x 1080			
Pixel Pitch	[mm]	0.161 x 0.161			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black (AHVA)			
White Luminance (ILED=15.5 mA) (Note: ILED is LED current)	[cd/m²]	375 Max. (5 points average) 300 typ. (5 points average) 255 min. (5 points average)			
Luminance Uniformity		1.25 max (5 points)			
Contrast Ratio		1200 typ.			
Response Time	[ms]	20			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	3.6W (Include Logic and Blu power)			
Weight	[Grams]	290 g max			
Physical Size(Touch module)	[mm]		Min.	Typ.	Max.
		Length	315.57	315.87	316.17
		Width	195.08	195.58	196.08
		Thickness	-	-	3.0
Electrical Interface		2 Lane eDP 1.2			
Glass Thickness	[mm]	0.4			
Surface Treatment		Anti-Glare,Hardness 3H			
Support Color		16.7M colors (RGB 6-bits with FRC)			
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60			
RoHS Compliance		RoHS Compliance			

2.3 Optical Characteristics

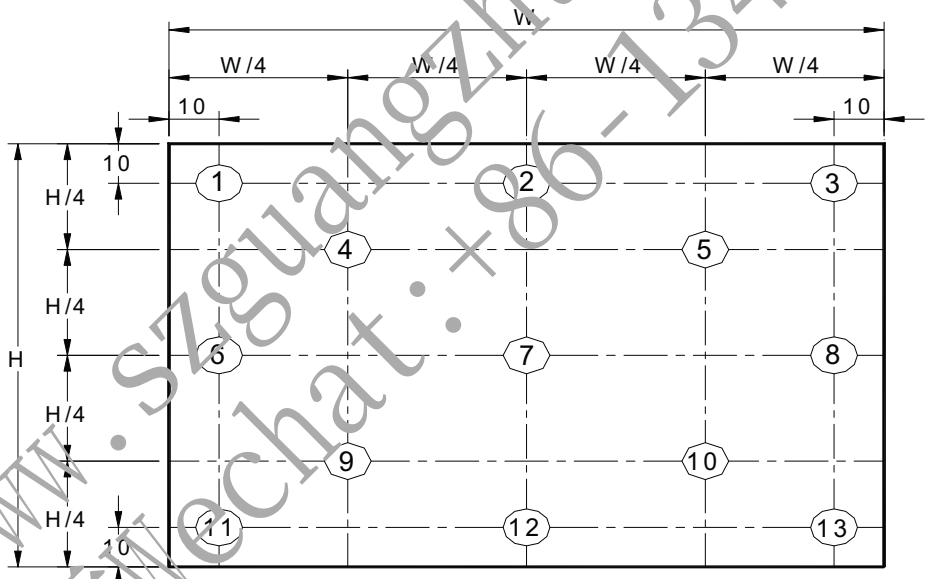
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance ILED=15.5mA (Base Panel Only)			5 points average	255	300	375	cd/m2	1, 4, 5
Viewing Angle		θR θL	Horizontal (Right) CR = 10 (Left)	80 80	89 89	- -	degree	4, 9
		ψH ψL	Vertical (Upper) CR = 10 (Lower)	80 80	89 89	- -		
Luminance Uniformity		δ5P	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ13P	13 Points	-	-	1.6		2, 3, 4
Contrast Ratio		CR		1000	1200	-		4, 6
Cross talk		%				4		4, 7
Response Time		TRT	Rising + Falling	-	20	25		
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.634	0.664	0.694	-	4
		Ry		0.295	0.325	0.355		
	Green	Gx		0.254	0.284	0.314		
		Gy		0.592	0.622	0.652		
	Blue	Bx		0.113	0.143	0.173		
		By		0.027	0.057	0.087		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
sRGB		%		-	100	-		
Low Blue Light		K	CCT	5500	-	7000		
		%	TUV	TUV-method 2				10

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

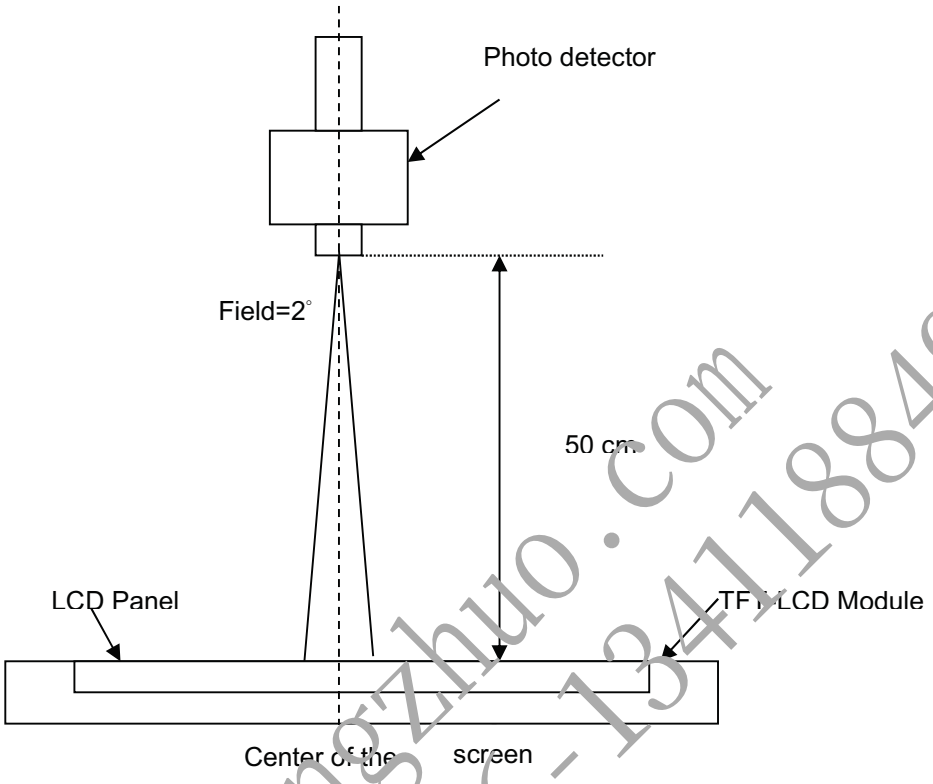
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30

minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points, Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

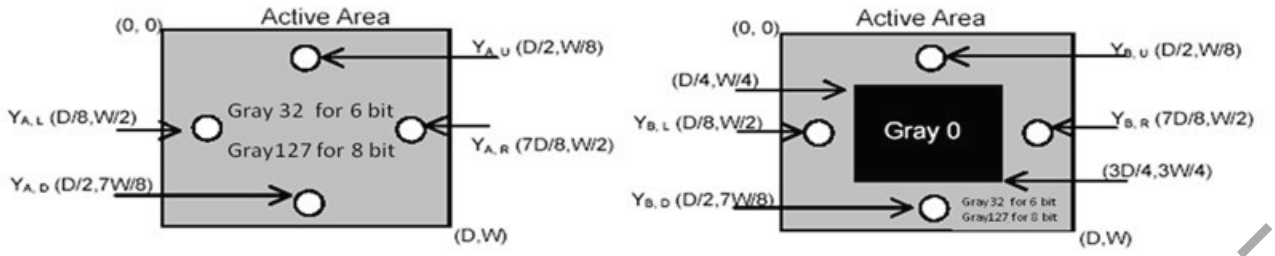
Note 7 : Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100\ (\%)$

Where

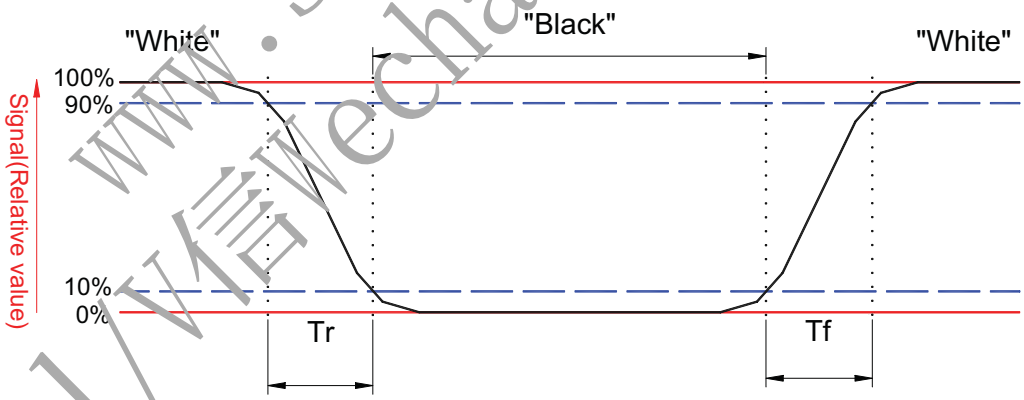
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



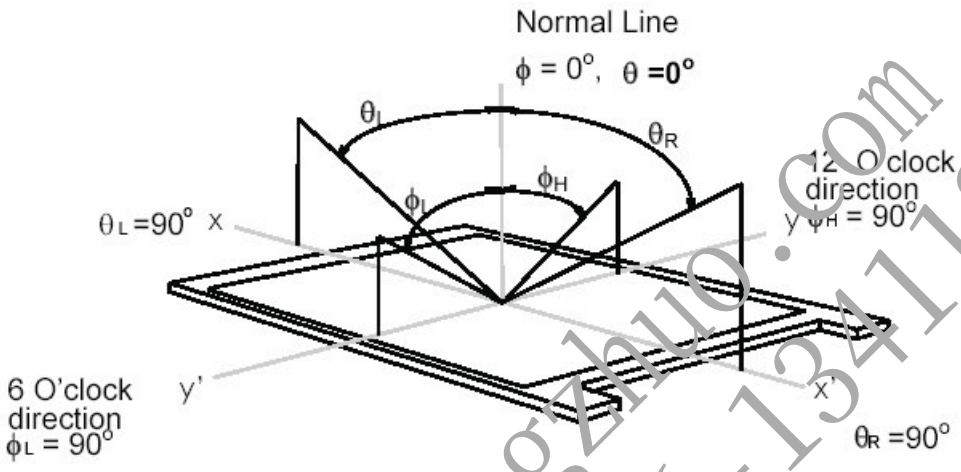
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.

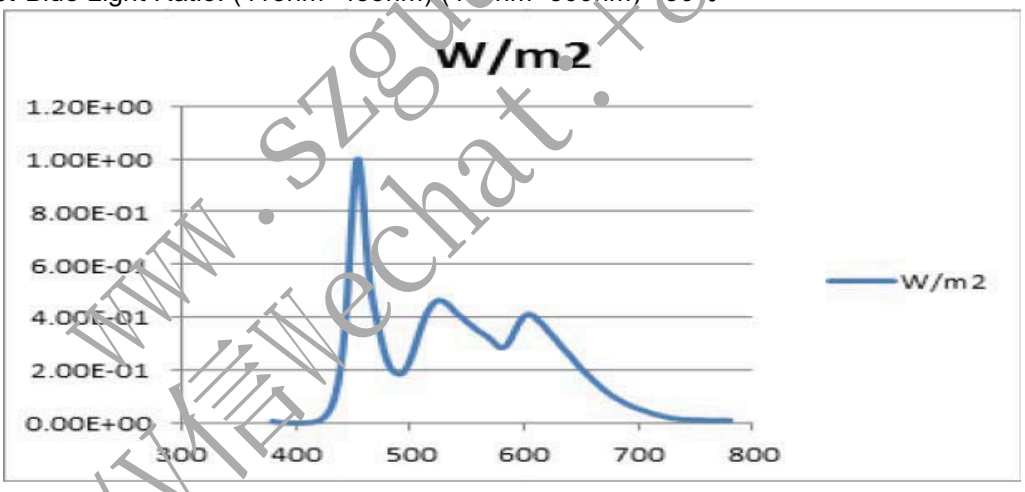


Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.

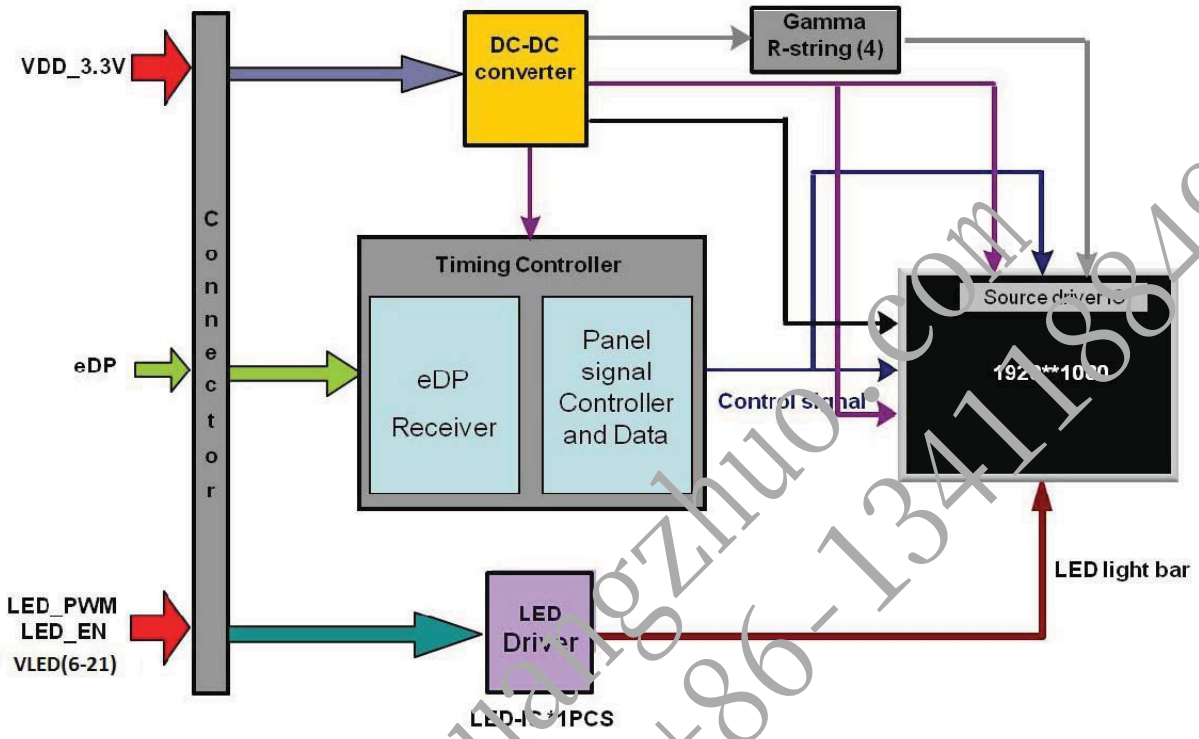


Note 10: Blue Light Ratio: (415nm~455nm)/(400nm~500nm) <50 %



3. Functional Block Diagram

The following diagram shows the functional block of the 14.0 inches wide Color TFT/LCD 40 Pin



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

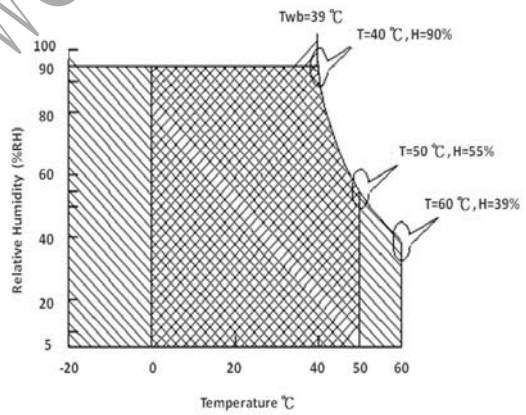
4.2 Absolute Ratings of Touch Sensor Module

Item	Symbol	Min	Max	Unit	Conditions
Touch Sensor Module Power Voltage	VTSP	-0.3	+3.6	[Volt]	
Touch Sensor Module Reset Signal	RST	-0.3	+3.6	[Volt]	
Touch Sensor Module enable Signal	TP_EN	-0.3	+3.6	[Volt]	

4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)
Note 2: Permanent damage to the device may occur if exceed maximum values
Note 3: LED specification refer to section 5.2
Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).
Note 5: The packing material of system forbid to involve ammonium component
Note 6: The reliability test conditions of system do not exceed the verified conditions of TFT module
Note 7: Be sure the panel test condition do not exceed the component limitation of TFT module(TN Liquid crystal , for example)



Operating Range Storage Range

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

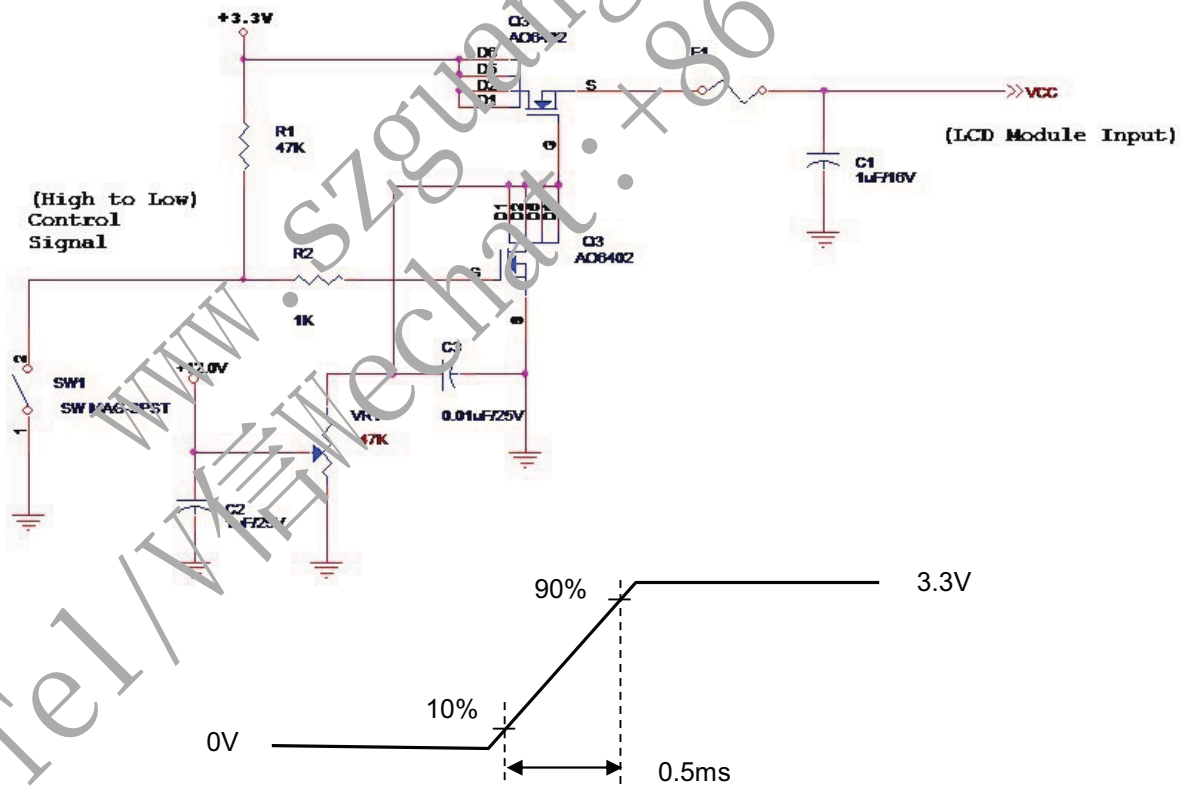
Input power specifications are as follows;

The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	0.8	1.8	[Watt]	Note 1
IDD	IDD Current(RMS)	-	-	267	[mA]	Note 1
IRush	Inrush Current	-	-	1500	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : PDD(typ)@ mosaic pattern Maximum Power; PDD(Max)@ R/G/B pattern Maximum Power

IDD(Max)=PDD(Max) / VDD(Min)



Vin rising time

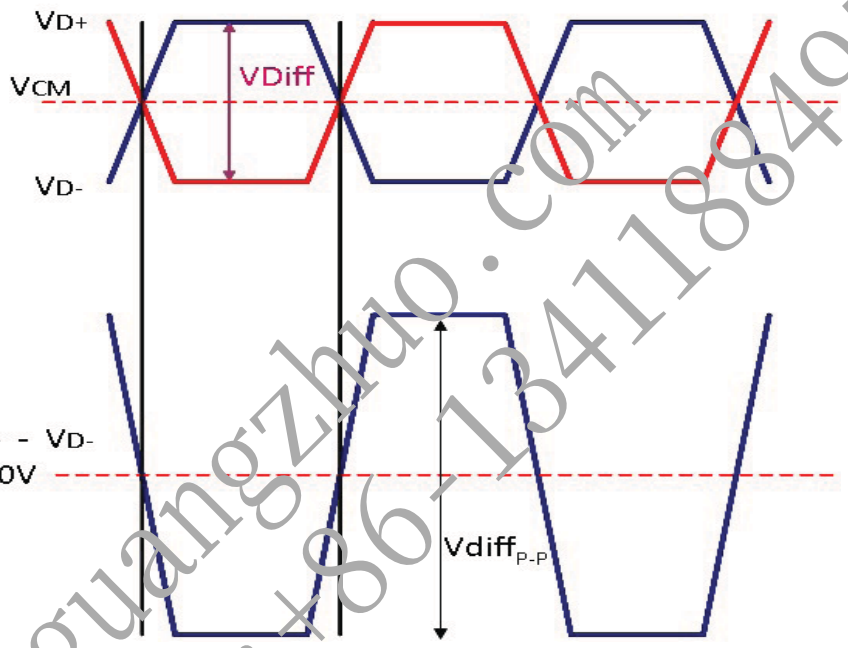
5.1.2 Signal Electrical Characteristics

Signal electrical characteristics are as follows;

Display Port main link signal:

Differential pair VD+ , VD-
Which is one Display port
Main link

VCM of Display port
Main link



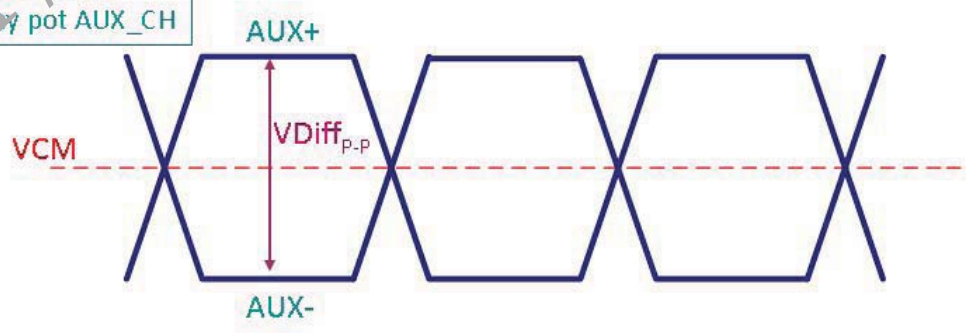
$Vdiff_{P-P} = [(VD+) - (VD-)] \times 2$

Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	HBR:150		1320	mV

Follow as VESA display port standard V1.4

Display Port AUX_CH signal:

Differential AUX+ , AUX-
Which is Display pot AUX_CH



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
$VDiff_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	270		800	mV

Follow as VESA display port standard V1.3

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25		3.6	V

Follow as VESA display port standard V1.3

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	2.5	[Watt]	(Ta=25℃), Note 1
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25℃), Note 2 I_F=15.5 mA
Inrush Current	VLED	-	-	2000	mA	VLED : 12V/White pattern, Note3

Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

Note 3: VDD measured rising timing @ 0.5ms / VLED input 12V / test pattern: White pattern / 1000nit

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED (Note 1)	6.0 (Note 2)	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.5	[Volt]	
PWM Logic Input High Level	PWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	1 *Note2	--	100	%	

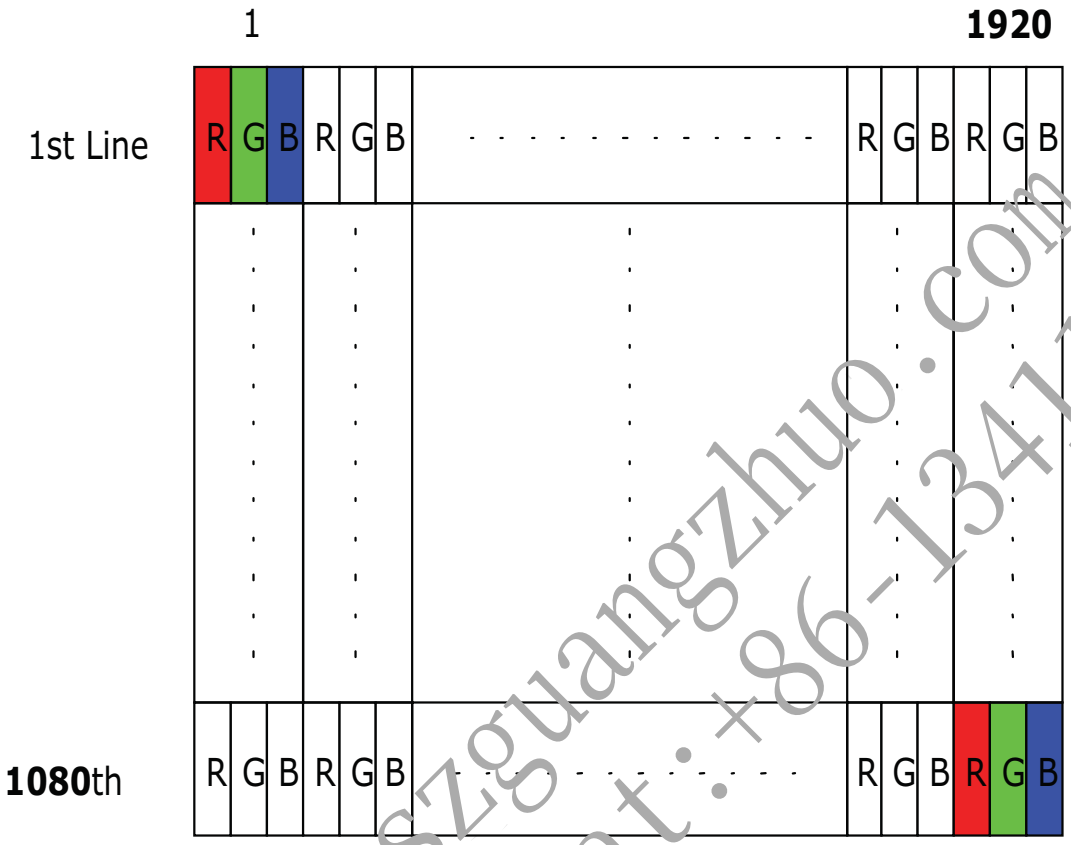
Note 1: Recommend system pull up/down resistor no bigger than 10kohm

Note 2 : If the PWM duty ratio(min) is set between 5% to 1%，the PWM input frequency should be set below 1KHz . The brightness-duty characteristic might not be able to keep in it's linearity if the dimming control is operated in 1% to 5% range.

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

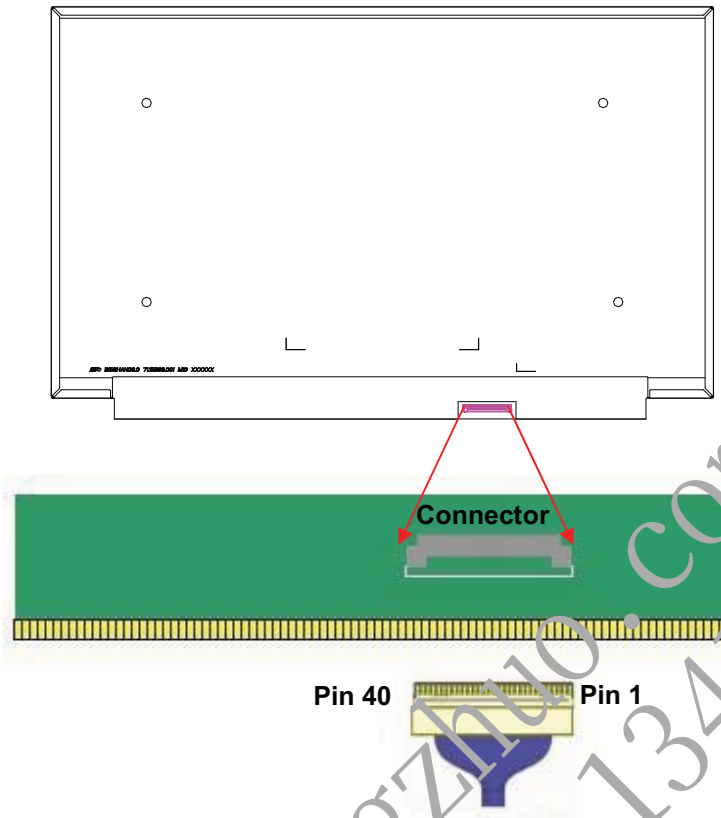
Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or Compatible
Type / Part Number	20738-040E-02 or Compatible
Mating Housing/Part Number	20736-040T-01S or Compatible

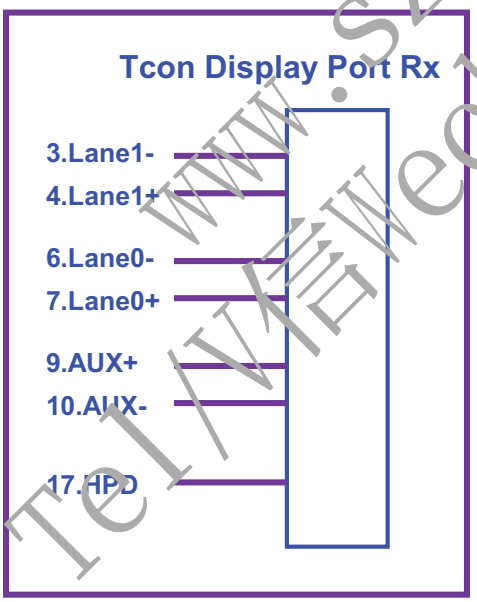
6.2.2 Pin Assignment (with Touch Sensor Pin Assignment)

Pin	Signal	Description
1	NC	NC
2	H_GND	High Speed Ground
3	Lane1_N	Comp Signal Link Lane1
4	Lane1_P	True Signal Link Lane1
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane0
7	Lane0_P	True Signal Link Lane0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch
10	AUX_CH_N	Comp Signal Auxiliary Ch
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	LCD_Self_Test	LCD Panel Self Test Enable
15	LCD_GND	LCD logic and driver ground
16	LCD_GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	BL_GND	Backlight_ground
19	BL_GND	Backlight_ground
20	BL_GND	Backlight_ground
21	BL_GND	Backlight_ground
22	BL_Enable	Backlight On/Off enable
23	BL_PWM_DIM	Backlight PWM Signal Input
24	NC(SDA)	I2C for AUO RD rework
25	NC(SCL)	I2C for AUO RD rework
26	BL_PWR	Backlight Power
27	BL_PWR	Backlight Power
28	BL_PWR	Backlight Power
29	BL_PWR	Backlight Power
30	NC	NC
31	NC	NC
32	NC	NC
33	NC	NC
34	NC	NC
35	NC	NC
36	NC	NC
37	NC	NC
38	NC	NC
39	NC	NC
40	NC	NC



Note1: Start from right side.

Note2: Input signals shall be low or High-impedance state when VDD is off.
Internal circuit of **eDP inputs** are as following.



6.3 Interface Timing

6.3.1 Timing Characteristics

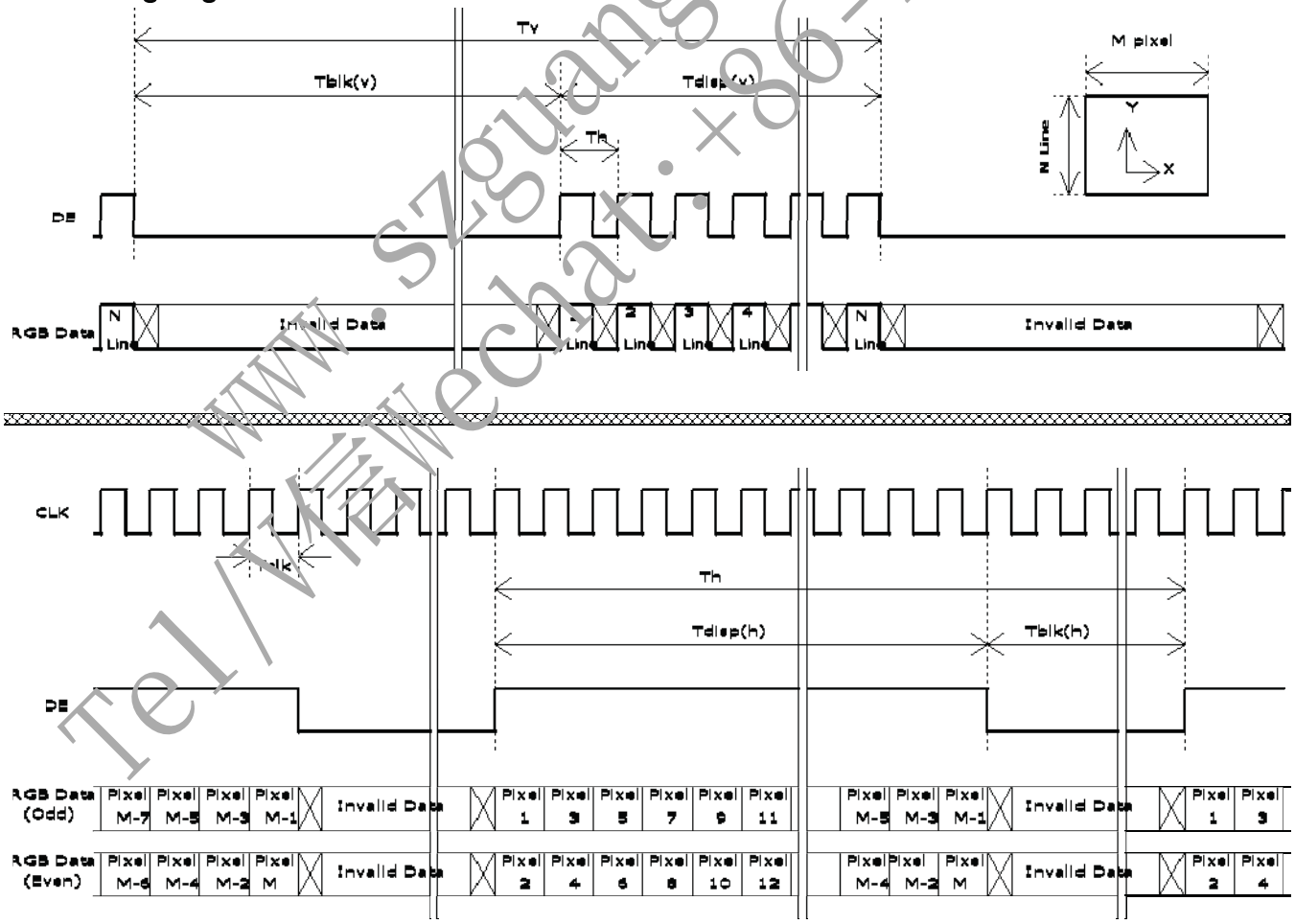
For normal display, interface timings should match the 1920x1080 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		1/ T_{Clock}	138.8	141	165	MHz
Vertical Section	Period	T_V	1090	1116	1080+A	Vertical Section
	Active	T_{VD}	1080			
	Blanking	T_{VB}	10	36	A	
Horizontal Section	Period	T_H	2000	2104	1920+B	Horizontal Section
	Active	T_{HD}	1920			
	Blanking	T_{HB}	80	184	400	

Note 1 : The above is as optimized setting

Note 2 : The maximum clock frequency = (1920+B)*(1080+A)*60<165MHz

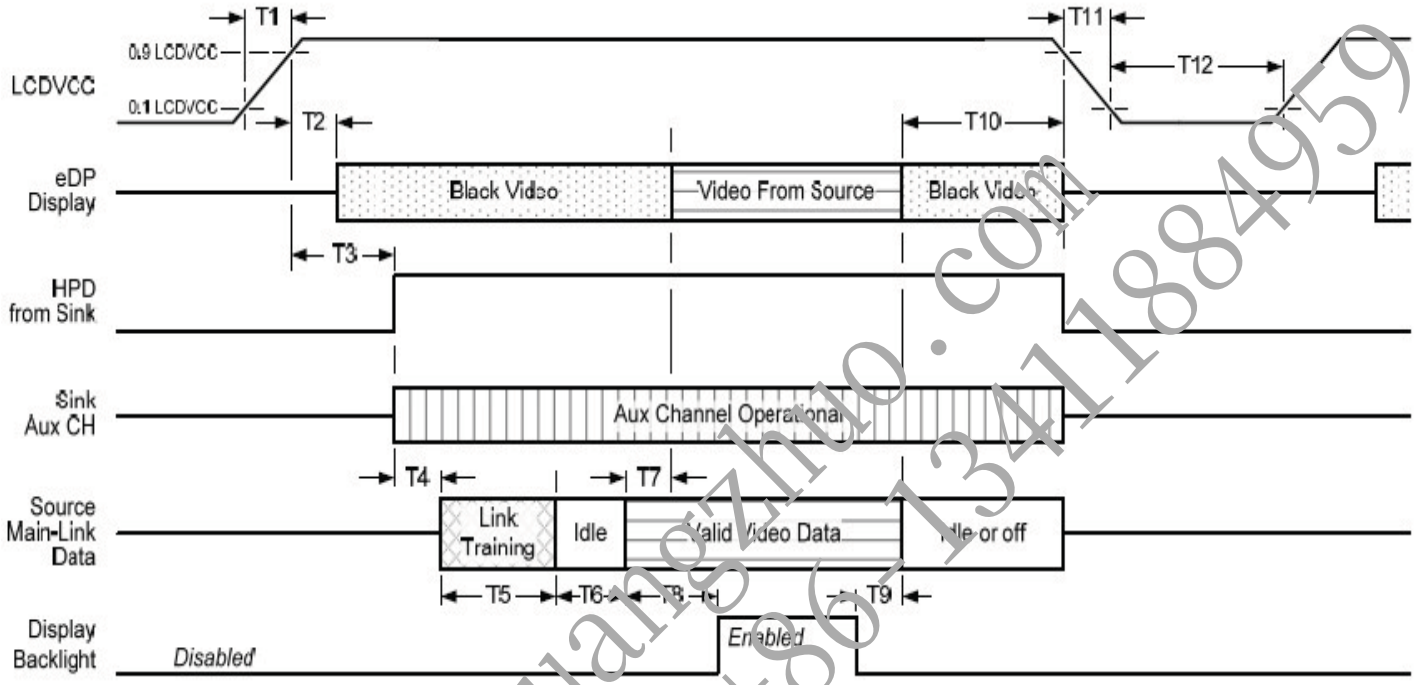
6.3.2 Timing diagram



6.4 Power ON/OFF Sequence

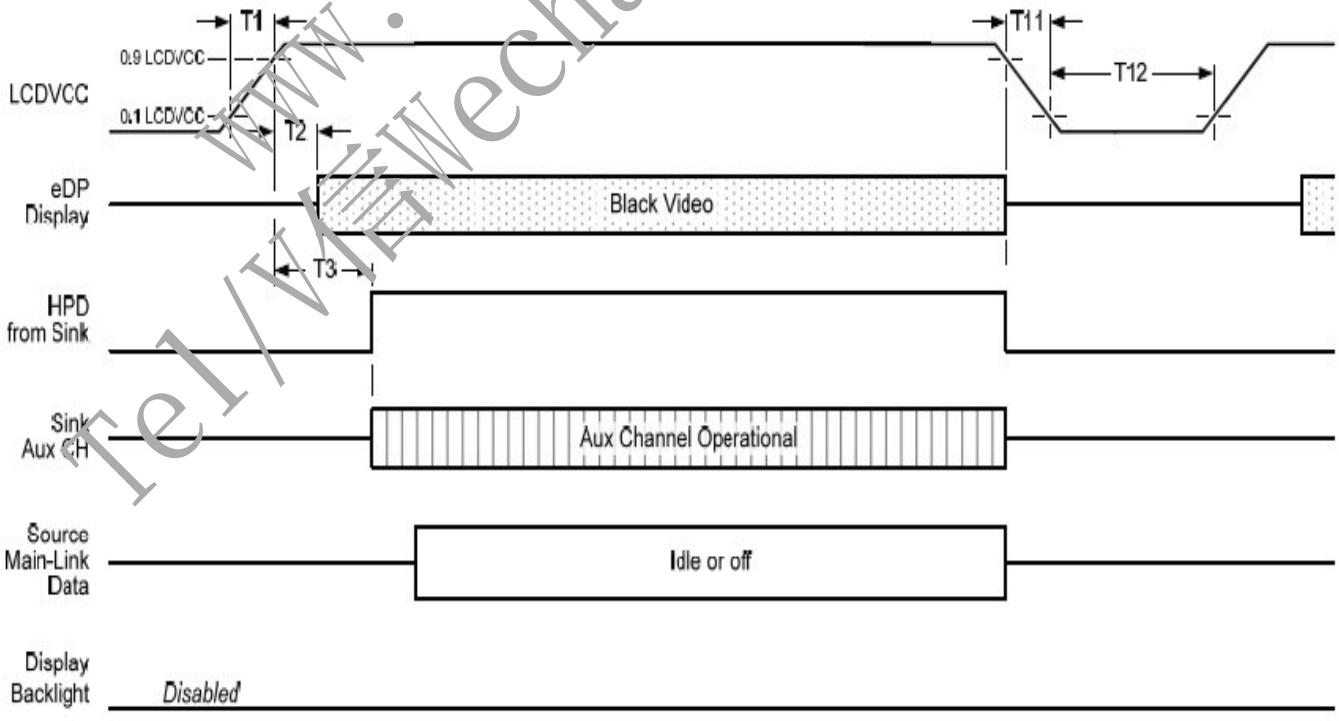
Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 90% to 10%	source			10ms	
T12	power off time	source	500ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:

-upon LCDVDD power on (with in T2 max)- when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).

-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

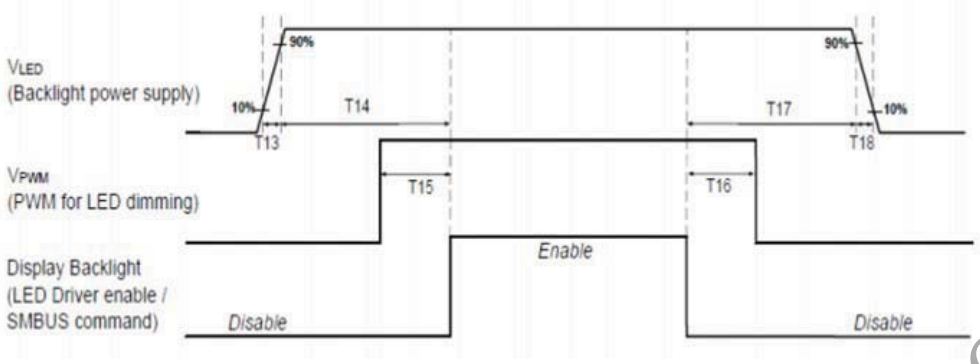
Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Note 4:T8>T7

Display Port panel B/L power sequence timing parameter:

Note: When the adapter is hot plugged, the backlight power supply sequence is shown as below



	Min (ms)	Max (ms)
T13	0.2	-
T14	0	-
T15	-	-
T16	-	-
T17	0	-
T18	0	-
T19	1*	
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM} = 1/PWM Frequency

Note : If T19,T20 < 5xTPWM* , This flash display may occur.We sUGGEST T19,T20≧5xTPWM* to realize seamless change display.

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 240h	
High Temperature Operation	Ta= 60℃, Dry, 240h	
Low Temperature Operation	Ta=0℃, 240h	
High Temperature Storage	Ta= 60℃, 240h	
Low Temperature Storage	Ta= -20℃, 240h	
Thermal Shock Test	Ta=-20℃(30min) ~60℃(30min), 20cycles condition.	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

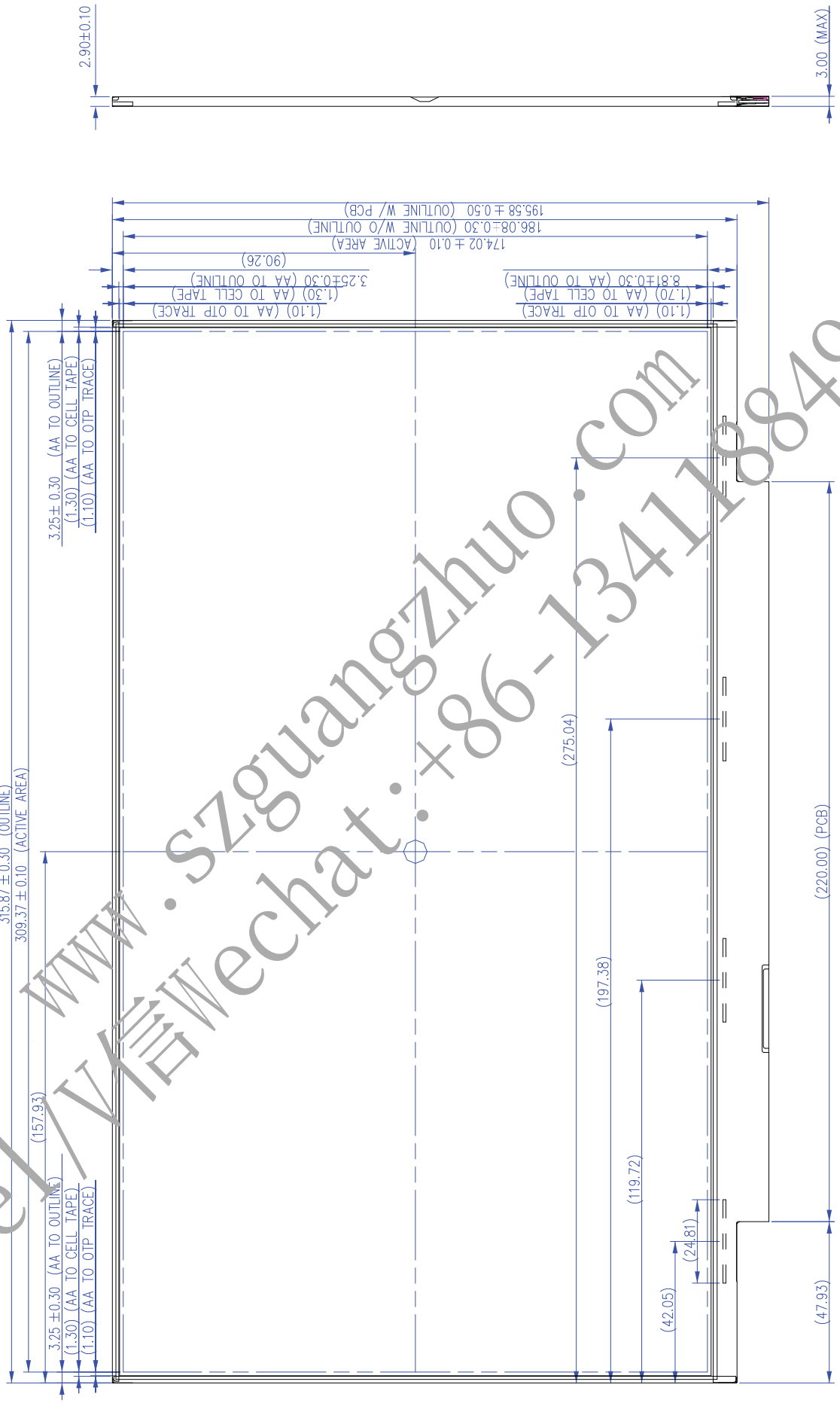
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

. Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

8.1 Total Solution Outline Dimension



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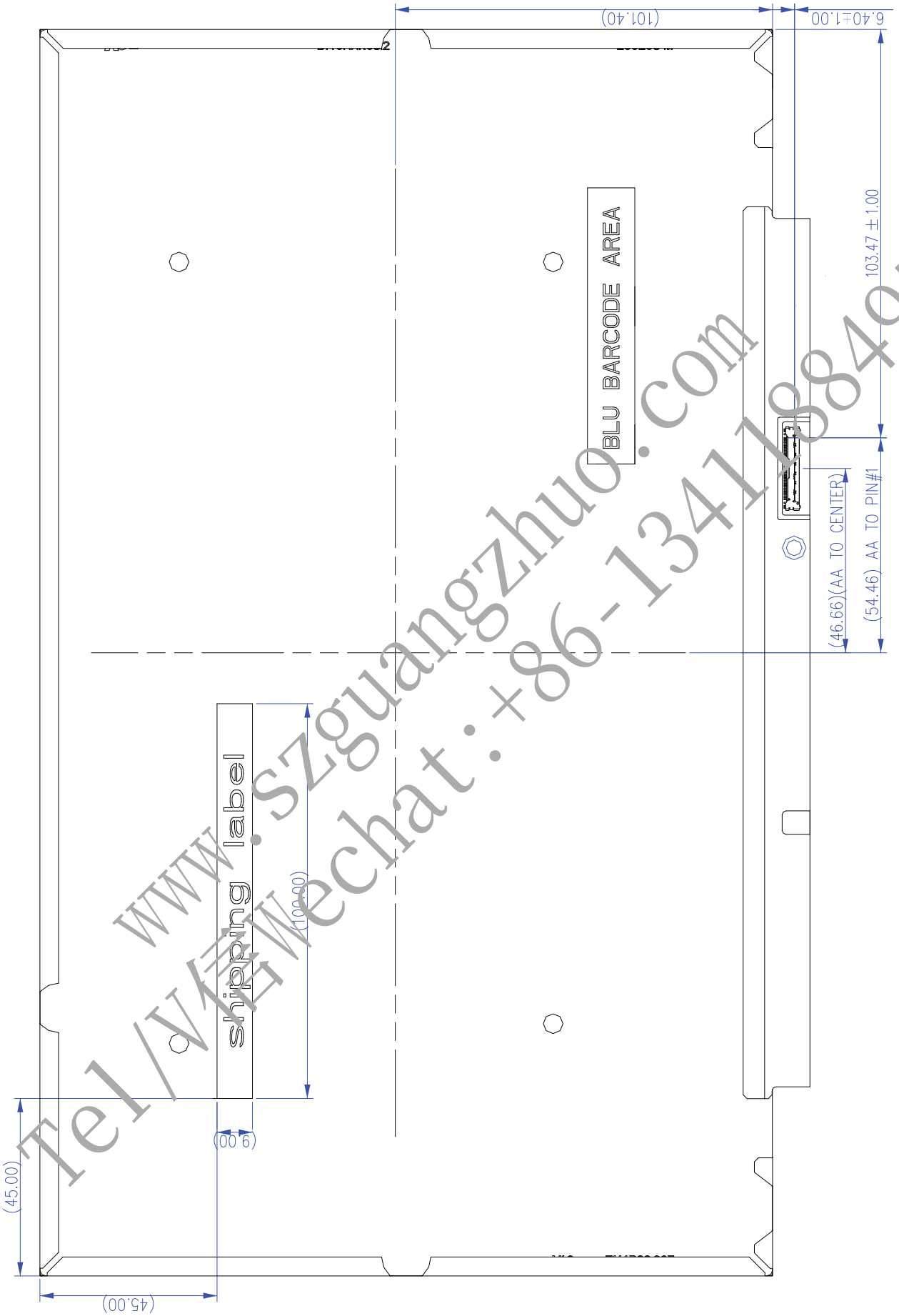
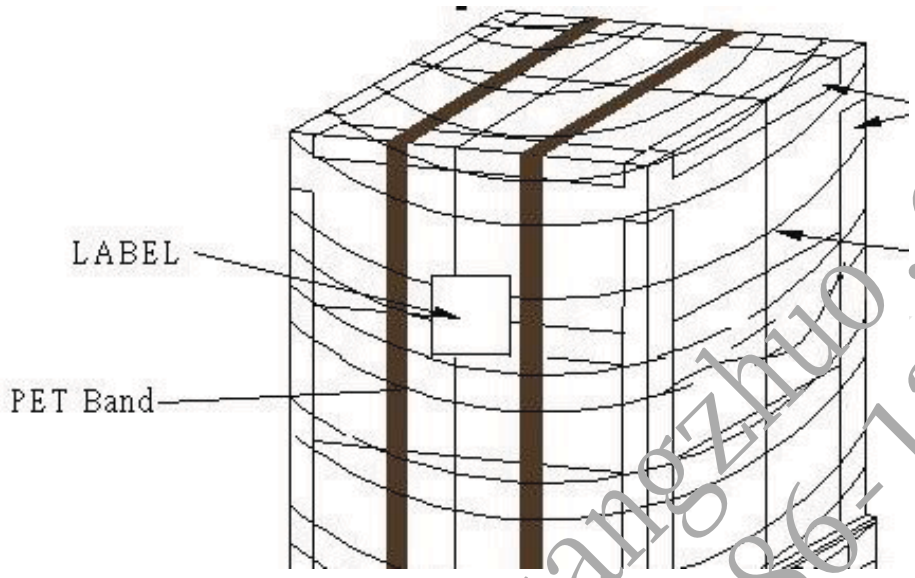


9. Shipping and Package

9.1 Shipping Label Format

9.2 Shipping Package of Palletizing Sequence



10. Appendix:

10.1 EDID Description

Address	FUNCTION	Value	Value	Value
HEX		HEX	BIN	DEC
00	Header	00	00000000	0
01	Header	FF	11111111	255
02	Header	FF	11111111	255
03	Header	FF	11111111	255
04	Header	FF	11111111	255
05	Header	FF	11111111	255
06	Header	FF	11111111	255
07	Header	00	00000000	0
08	EISA Manuf. Code LSB	06	00000110	6
09	Compressed ASCII	AF	10101111	175
0A	Product Code	A6	10100110	166
0B	Product Code	B8	10111000	184
0C	32-bit ser #	00	00000000	0
0D	ID S/N - option	00	00000000	0
0E	ID S/N - option	00	00000000	0
0F	ID S/N - option	00	00000000	0
10	Week of manufacture	00	00000000	0
11	Year of manufacture	20	00100000	32
12	EDID Structure Ver.	01	00000001	1
13	EDID revision #	04	00000100	4
14	Video input def. (digital I/P non-TMDS, CRGB)	A5	10100101	165
15	Max H image size (rounded to cm)	1F	00011111	31
16	Max V image size (rounded to cm)	11	00010001	17
17	Display Gamma (=(gamma*100)-100)	78	01111000	120
18	Feature support (no DPMS, Active OFF, RGB, tmg Blk#1)	02	00000010	2
19	Red/green low bits (Lower 2:2:2:2 bits)	1D	00011101	29
1A	Blue/white low bits (Lower 2:2:2:2 bits)	A5	10100101	165
1B	Red x (Upper 8 bits)	AA	10101010	170
1C	Red y/ highER 8 bits	53	01010011	83
1D	Green x	48	01001000	72
1E	Green y	9F	10011111	159
1F	Blue x	24	00100100	36
20	Blue y	0E	00001110	14
21	White x	50	01010000	80
22	White y	54	01010100	84
23	Established timing 1	00	00000000	0
24	Established timing 2	00	00000000	0
25	Established timing 3	00	00000000	0
26	Standard timing #1	01	00000001	1
27	Standard timing #1	01	00000001	1
28	Standard timing #2	01	00000001	1
29	Standard timing #2	01	00000001	1
2A	Standard timing #3	01	00000001	1
2B	Standard timing #3	01	00000001	1
2C	Standard timing #4	01	00000001	1
2D	Standard timing #4	01	00000001	1
2E	Standard timing #5	01	00000001	1
2F	Standard timing #5	01	00000001	1
30	Standard timing #6	01	00000001	1
31	Standard timing #6	01	00000001	1
32	Standard timing #7	01	00000001	1

33	Standard timing #7	01	00000001	1
34	Standard timing #8	01	00000001	1
35	Standard timing #8	01	00000001	1
36	Pixel Clock/10000 LSB	14	00010100	20
37	Pixel Clock/10000 USB	37	00110111	55
38	Horz active Lower 8bits	80	10000000	128
39	Horz blanking Lower 8bits	B8	10111000	184
3A	HorzAct:HorzBlnk Upper 4:4 bits	70	01110000	112
3B	Vertical Active Lower 8bits	38	00111000	56
3C	Vertical Blanking Lower 8bits	24	00100100	36
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	40	01000000	64
3E	HorzSync. Offset	10	00010000	16
3F	HorzSync.Width	10	00010000	16
40	VertSync.Offset : VertSync.Width	3E	00111110	62
41	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0
42	Horizontal Image Size Lower 8bits	35	00110101	53
43	Vertical Image Size Lower 8bits	AE	10101110	174
44	Horizontal & Vertical Image Size (upper 4:4 bits)	10	00010000	16
45	Horizontal Border (zero for internal LCD)	00	00000000	0
46	Vertical Border (zero for internal LCD)	00	00000000	0
47	Signal (non-intr, norm, no stero, sep sync, neg pol)	18	00011000	24
48	Pixel Clock/10000 LSB	00	00000000	0
49	Pixel Clock/10000 USB	00	00000000	0
4A	Horz active Lower 8bits	00	00000000	0
4B	Horz blanking Lower 8bits	0F	00001111	15
4C	HorzAct:HorzBlnk Upper 4:4 bits	00	00000000	0
4D	Vertical Active Lower 8bits	00	00000000	0
4E	Vertical Blanking Lower 8bits	00	00000000	0
4F	Vert Act : Vertical Blanking (upper 4:4 bit)	00	00000000	0
50	HorzSync. Offset	00	00000000	0
51	HorzSync.Width	00	00000000	0
52	VertSync.Offset : VertSync.Width	00	00000000	0
53	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0
54	Horizontal Image Size Lower 8bits	00	00000000	0
55	Vertical Image Size Lower 8bits	00	00000000	0
56	Horizontal & Vertical Image Size (upper 4:4 bits)	00	00000000	0
57	Horizontal Border (zero for internal LCD)	00	00000000	0
58	Vertical Border (zero for internal LCD)	00	00000000	0
59	Signal (non-intr, norm, no stero, sep sync, neg pol)	20	00100000	32
5A	descriptor #3	00	00000000	0
5B	Reserved for definition	00	00000000	0
5C	Reserved for definition	00	00000000	0
5D	ASCII String	FE	11111110	254
5E	Reserved for definition	00	00000000	0
5F	Manufacture	41	01000001	65
60	Manufacture	55	01010101	85
61	Manufacture	4F	01001111	79
62	Reserved for definition	0A	00001010	10
63	Reserved for definition	20	00100000	32
64	Reserved for definition	20	00100000	32
65	Reserved for definition	20	00100000	32
66	Reserved for definition	20	00100000	32
67	Reserved for definition	20	00100000	32
68	Reserved for definition	20	00100000	32
69	Reserved for definition	20	00100000	32
6A	Reserved for definition	20	00100000	32

6B	Reserved for definition	20	00100000	32
6C	Reserved for definition	00	00000000	0
6D	descriptor #4	00	00000000	0
6E	Reserved for definition	00	00000000	0
6F	Reserved for definition	FE	11111110	254
70	Reserved for definition	00	00000000	0
71	Manufacture P/N	42	01000010	66
72	Manufacture P/N	31	00110001	49
73	Manufacture P/N	34	00110100	52
74	Manufacture P/N	30	00110000	48
75	Manufacture P/N	48	01001000	72
76	Manufacture P/N	41	01000001	65
77	Manufacture P/N	4E	01001110	78
78	Manufacture P/N	30	00110000	48
79	Manufacture P/N	33	00110011	51
7A	Manufacture P/N	2E	00101110	46
7B	Manufacture P/N	4C	01001100	76
7C	Reserved for definition	20	00100000	32
7D	Reserved for definition	0A	00001010	10
7E	Extension Flag	00	00000000	0
7F	Checksum	0C	00001100	12

10.2 Notes

DPCD Ver.	sDRRS	DCR	DMRRS	PSR	LRR	LRR Frame rate	MBO	VESA DSC
1.1	OFF (EDID no support)	N/A	OFF (EDID no support)	N/A	N/A	N/A	N/A	N/A

MSO	G-Sync	Free-Sync	Adaptive-Sync	HDR Tier	HDR Ver.	System Input
N/A	On	On	On	N/A	N/A	PWM