



Product Specification

AUO CORPORATION

(V) Preliminary Specifications

() Final Specifications

Module	13.3" FHD+(WUXGA) 16:10 Color TFT-LCD with LED Backlight design
Model Name	B133UAN04.2
H/W	0A
Note ()	LED Backlight with driving circuit design

Customer Date	Approved by <u>Jo CY Cheng</u> <u>4/2/2024</u>
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Note: This Specification is subject to change without notice.	
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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2024/04/02	All	First Edition for Customer		



1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC62368-1 or UL62368-1), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.



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2. General Description

B133UAN04.2 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:10 WUXGA,1920(H) x1200(V)screen and 16.2M colors (RGB 6-bits+2FRC) with LED backlight driving circuit. All input signals are eDP(Embedded DisplayPort) interface compatible.

B133UAN04.2 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[in]	13.3			
Active Area	[mm]	286.042 x 178.776			
Pixels H x V		1920x3(RGB) x 1200			
Pixel Pitch	[mm]	0.14898x0.14898			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black (AHVA)			
White Luminance (ILED=17.8mA) (Note: ILED is LED current)	[cd/m ²]	300 typ. (5 points average) 255 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		1000 typ			
Response Time	[ms]	25 typ / 35 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	3.9 max. (Include Logic and Blu power)			
Weight	[Grams]	280 max.			
Physical Size	[mm]		Min.	Typ.	Max.
		Length	291.44	291.74	292.04
		Width	189.23	189.53	189.83
		Thickness	-	-	3.0 (Panel side) 4.8 (PCBA Side)
Electrical Interface		2 Lane eDP 1.2			
Glass Thickness	[mm]	0.4			
Surface Treatment		Anti-Glare			



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Support Color		16.2M colors (RGB 6-bits+2FRC)
Temperature Range		
Operating	[°C]	0 to +50
Storage (Non-Operating)	[°C]	-20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

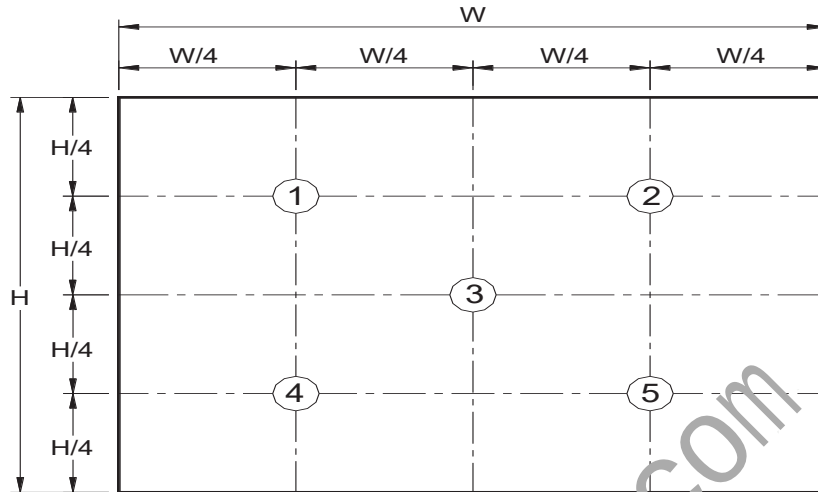
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance $I_{LED}=22mA$	Y_L	5 points average	255	300	-	cd/m ²	1, 4, 5.
Viewing Angle	θ_R	Horizontal (Right)	80	85	-	degree	4, 9
	θ_L	CR = 10 (Left)	80	85	-		
	ϕ_H	Vertical (Upper)	80	85	-		
	ϕ_L	CR = 10 (Lower)	80	85	-		
Luminance Uniformity	δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity	δ_{13P}	13 Points	-	-	1.60		2, 3, 4
Contrast Ratio	CR		-	1000	-		4, 6
Cross talk	%				4		4, 7
Response Time	T_{RT}	Rising + Falling	-	25	35	msec	4, 8
Color / Chromaticity Coordinates	Red	R_x	0.544	0.574	0.604		4
		R_y	0.312	0.342	0.372		
	Green	G_x	0.328	0.358	0.388		
		G_y	0.539	0.569	0.599		
	Blue	B_x	0.132	0.162	0.192		
		B_y	0.084	0.114	0.144		
	White	W_x	0.283	0.313	0.343		
		W_y	0.299	0.329	0.359		
NTSC	%		-	45	-		



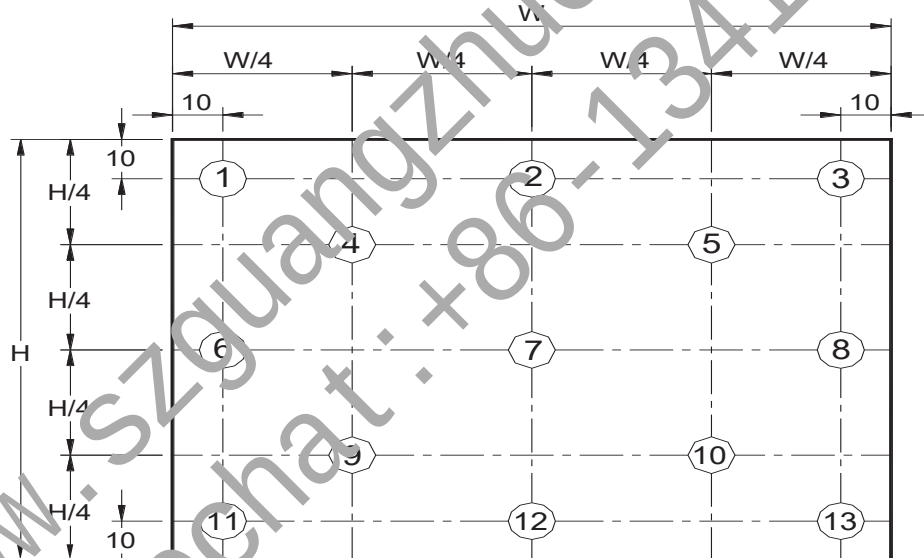
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Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{V5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

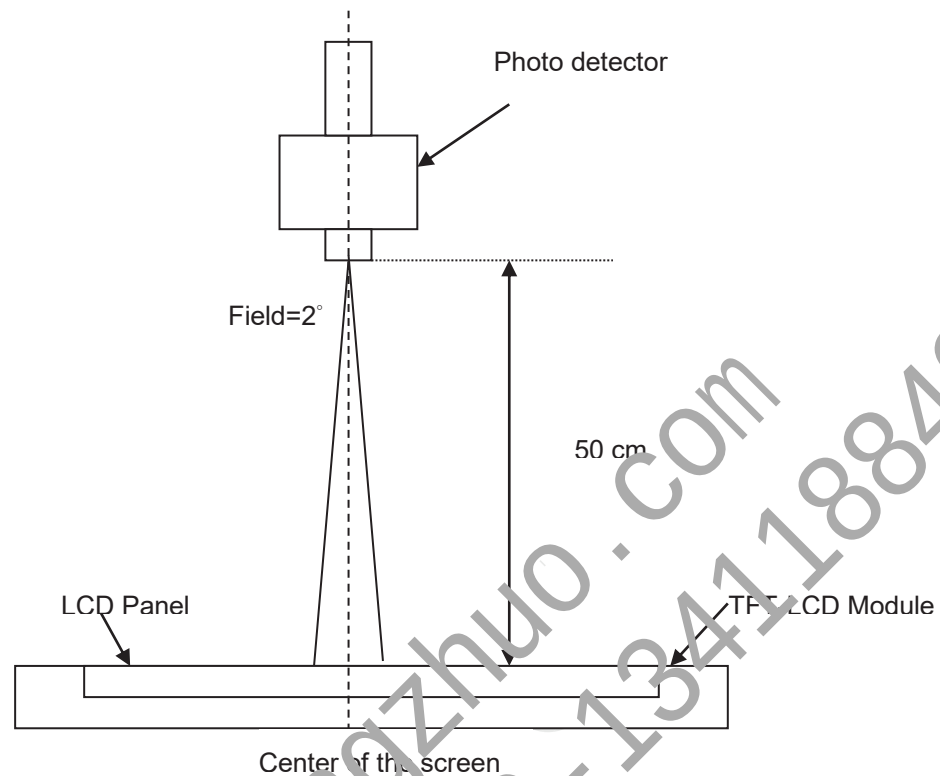
The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of



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screen.



Note 5 : Definition of Average Luminance of White (YL):

Measure the luminance of gray level 65 at 5 points , $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

Note 7 : Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



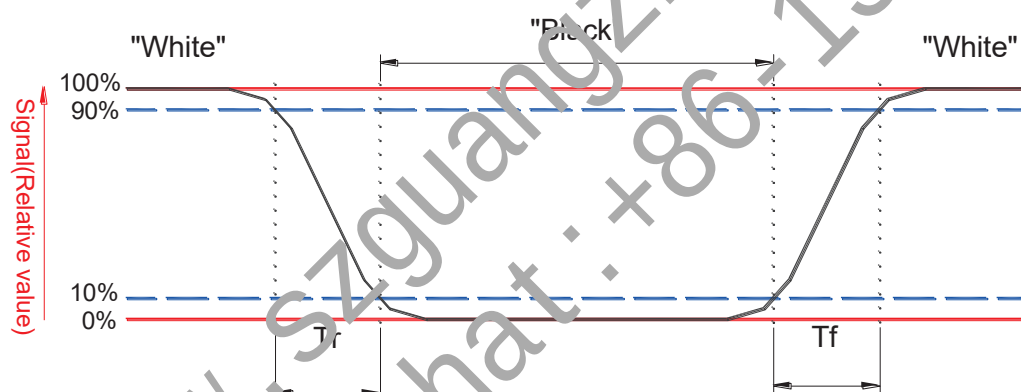
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Note 8: Definition of response time:

The output signals of SR-3 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



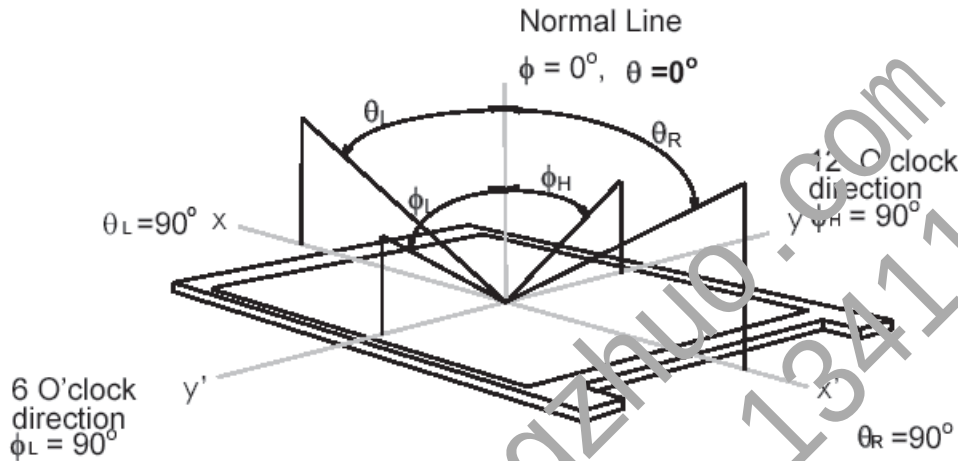


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Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



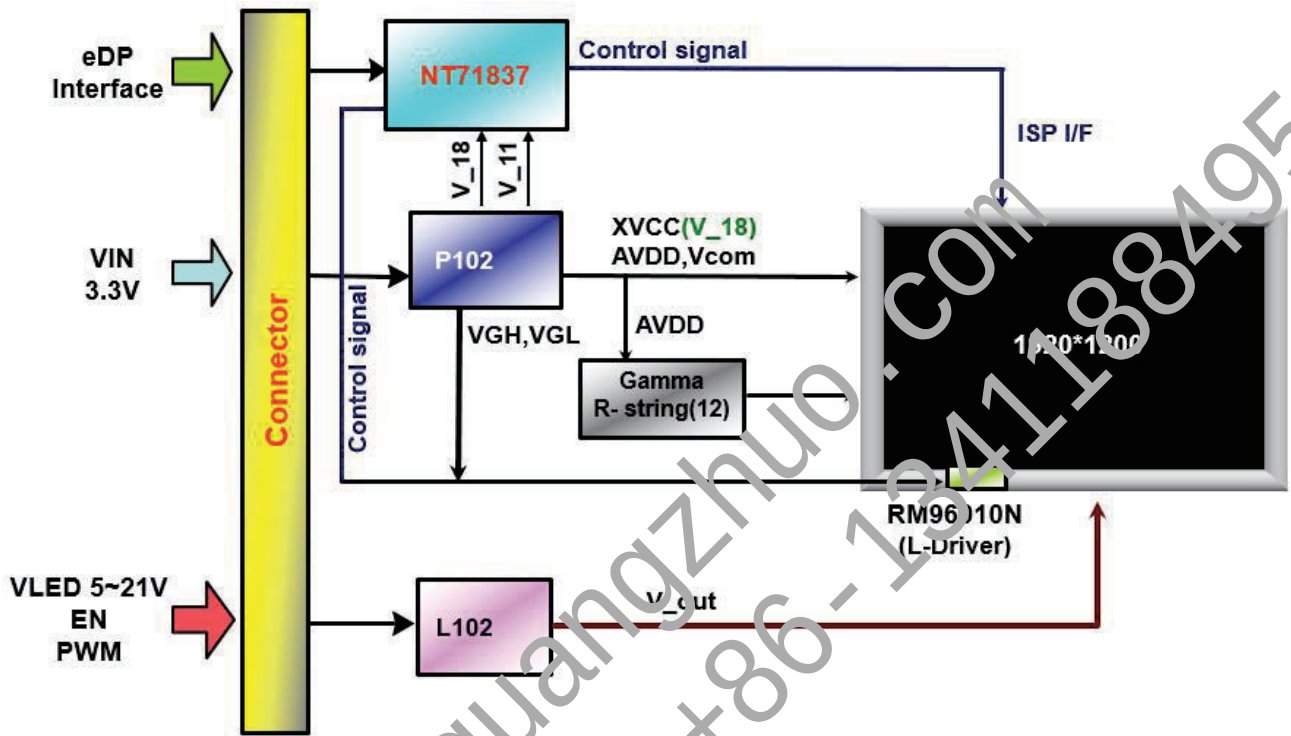


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3. Functional Block Diagram

The following diagram shows the functional block of the 13.3 inches wide Color TFT/LCD 30 Pin





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4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operating Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

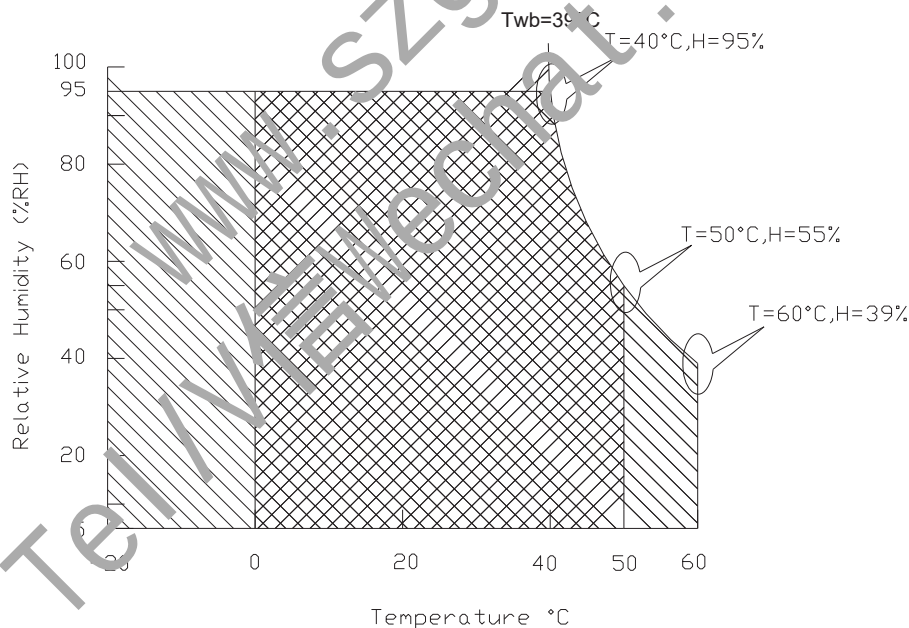
Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).

Note 5: The packing material of system forbid to involve ammonium component

Note 6: The reliability test conditions do not exceed the verified conditions of TFT module that refer to section 7.3

Note 7: Be sure the panel test condition do not exceed the component limitation of TFT module(TN Liquid crystal , for example)





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5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power @ mosaic pattern	-	-	0.6	[Watt]	Note 1
IDD	IDD Current(RMS) @ mosaic pattern	-	-	466	[mA]	Note 1
PDD	VDD Power @ Worst pattern	-	-	200	[Watt]	Note 1
IDD	IDD Current(RMS) @ Worst pattern	-	-	1.4	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
Ipeak	Peak Current	-	-	1500	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : PDD(Max)@ mosaic pattern Maximum Power

PDD(Max)@ Worst pattern Maximum Power

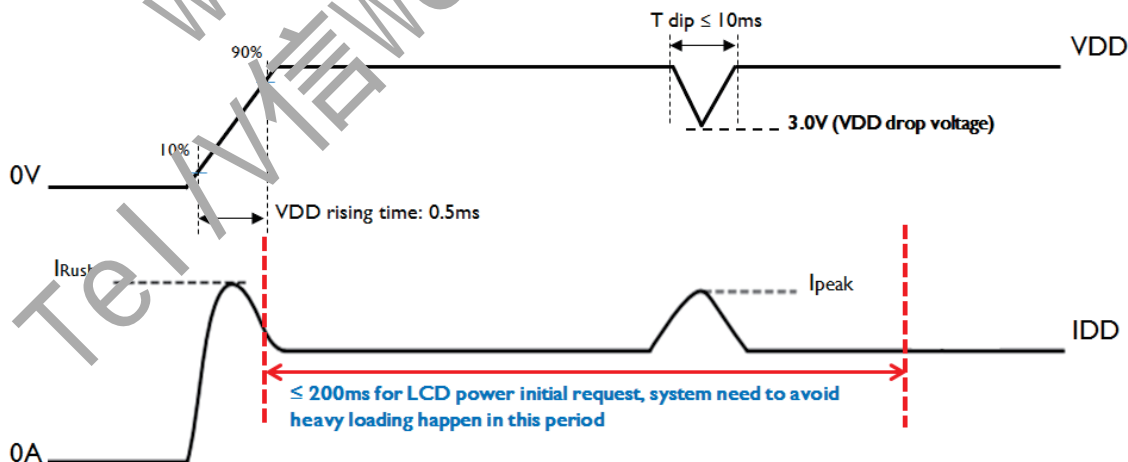
$IDD(Max) = PDD(Max) / VDD(Min)$

Worst pattern: sub-pixel checker pattern

Note 2 :

a. IRush: VDD measured rising timing @ 0.5ms

b. IPeak: VDD drop Voltage $\geq 3V$ at this Ipeak current

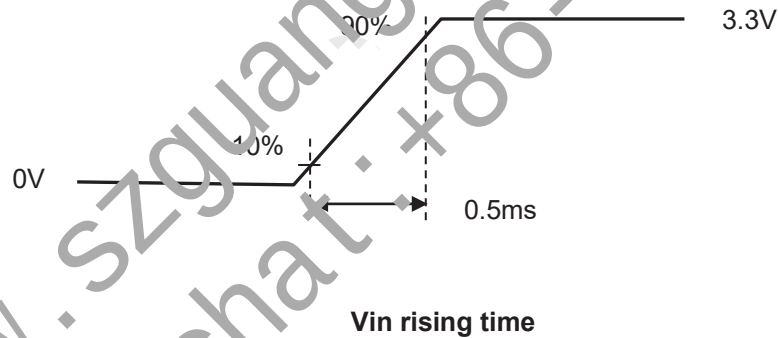
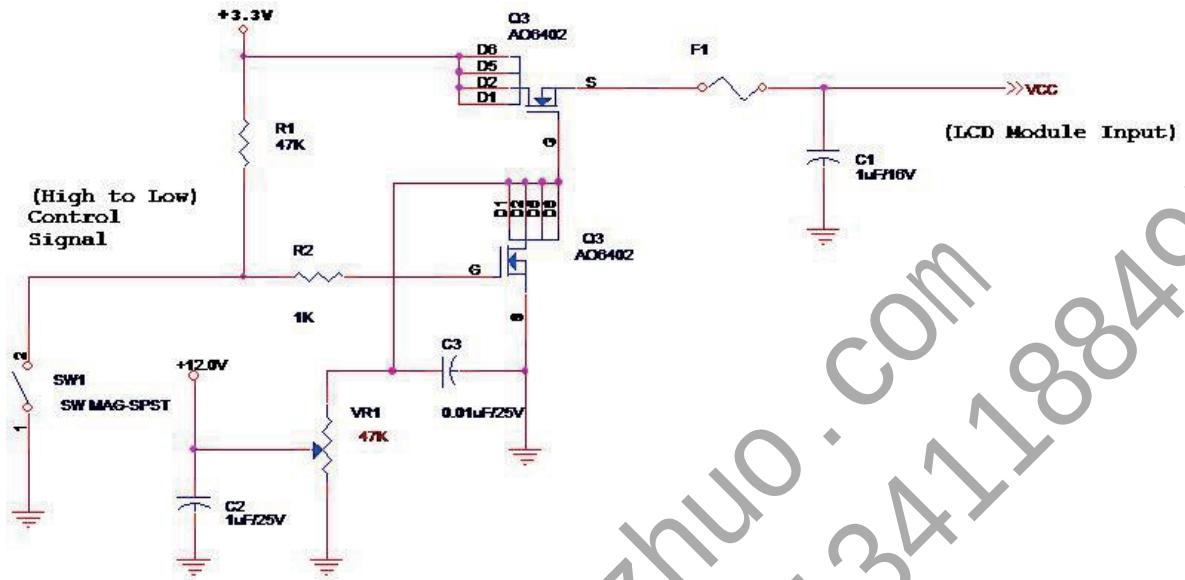




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c. IRush Measure Condition:





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5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

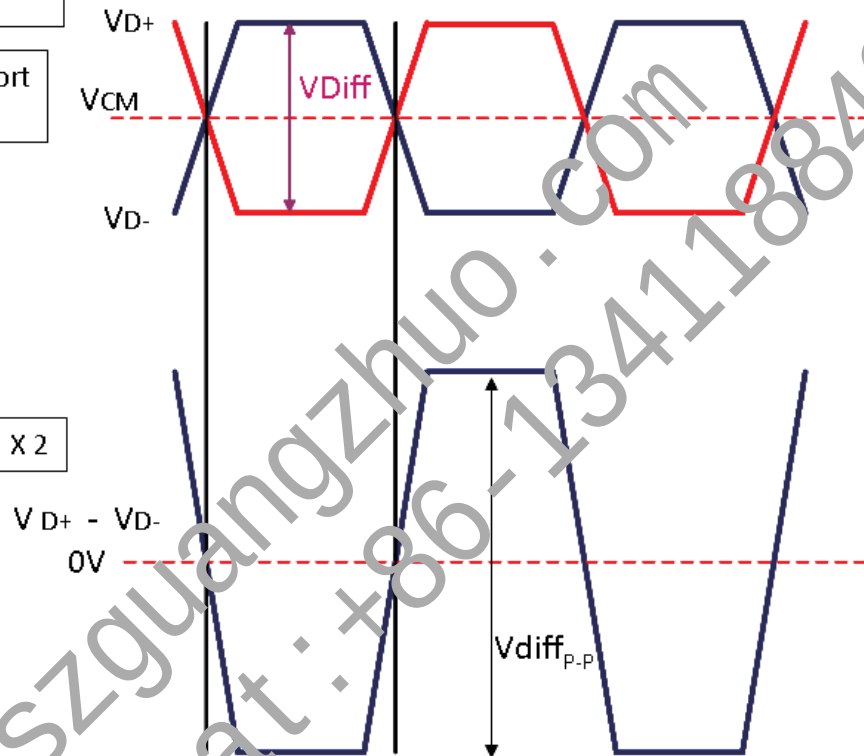
Signal electrical characteristics are as follows;

Display Port main link signal:

Differential pair VD+ , VD-
Which is one Display port
Main link

VCM of Display port
Main link

$$V_{diffP-P} = [(VD+) - (VD-)] \times 2$$



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
VDiff _{P-P}	Peak-to-peak Voltage at a receiving Device	150		1320	mV

Follow as VESA display port standard V1.4

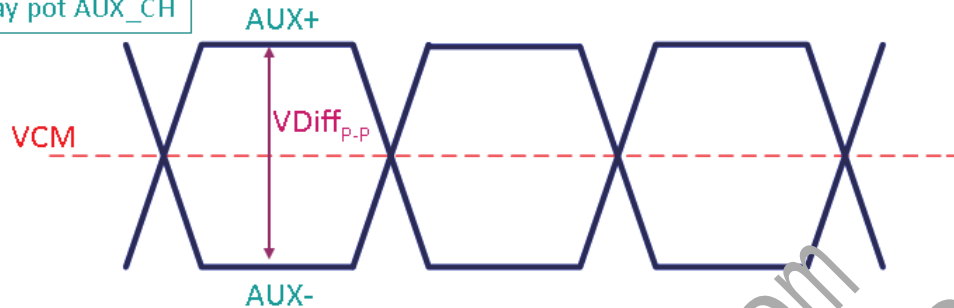


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Display Port AUX_CH signal:

Differential AUX+ , AUX-
Which is Display port AUX_CH



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff _{P-P}	AUX Peak-to-peak Voltage at TX package pins (TP1)	0.18	0.2	1.38	V
VDiff _{P-P}	AUX Peak-to-peak Voltage at TP3	0.14		1.36	V

Follow as VESA Embedded DisplayPort (eDP) Standard V1.4a

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25		3.6	V

Follow as VESA display port standard



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5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	P _{LED}	-	-	3.3	[Watt]	(Ta=25°C), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25°C), Note 2 If=22 mA
Inrush Current	VLED	-	-	200	mA	VLED : 6V/White pattern, Note 4

Note 1: Calculator value for reference $P_{LED} = V_F$ (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous

Note 4: VLED measured rising timing to BL enable load current (T13+T14+T15) / VLED input 6V / test pattern : White pattern / PWM 100%

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	5.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25°C) Note 3
LED Enable Input High Level	VLED_EN	2.5	-	3.6	[Volt]	
LED Enable Input Low Level		-	-	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	3.6	[Volt]	
PWM Logic Input Low Level		-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	1 * Note 2	--	100	%	

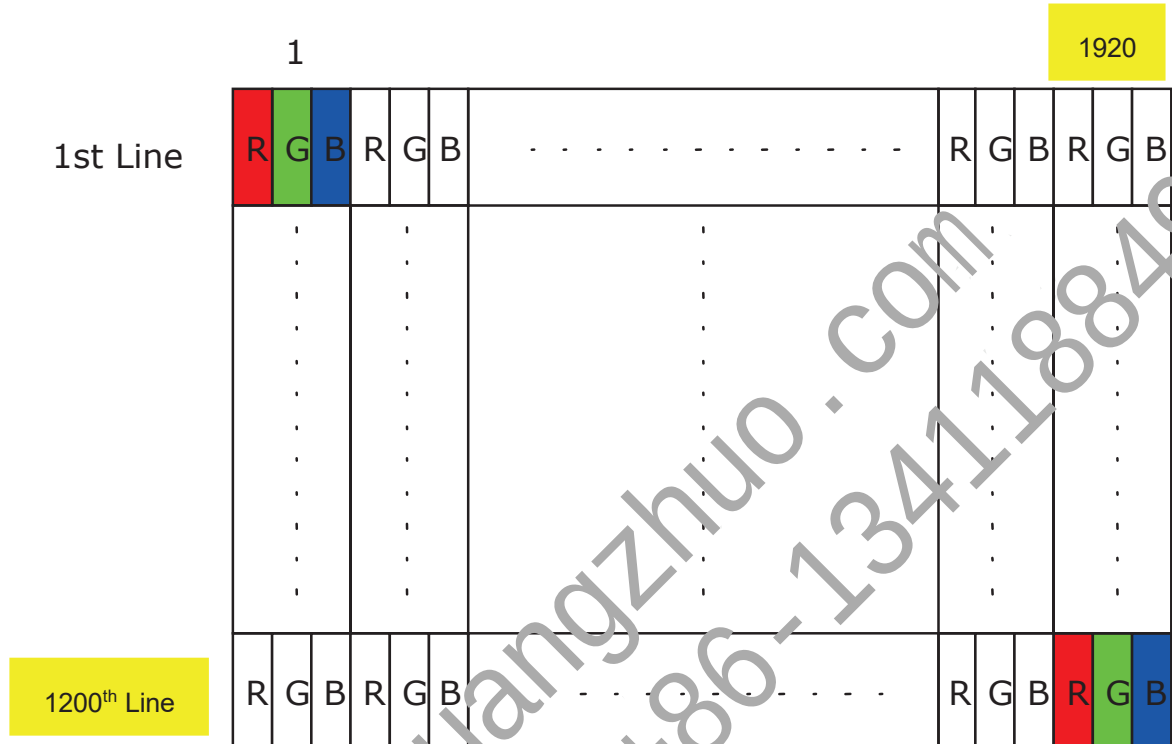
Note 2: If the PWM duty ratio(min) is set between 5% to 1%, the PWM input frequency should be set below 1KHz . The brightness-duty characteristic might not be able to keep in it's linearity if the dimming control is operated in 1% to 5% range.

Note 3: BL Control Mode is DC diming mode.

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.





6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	STC
Type / Part Number	STC 300E30-1010RA-G3
Mating Housing/Part Number	20453

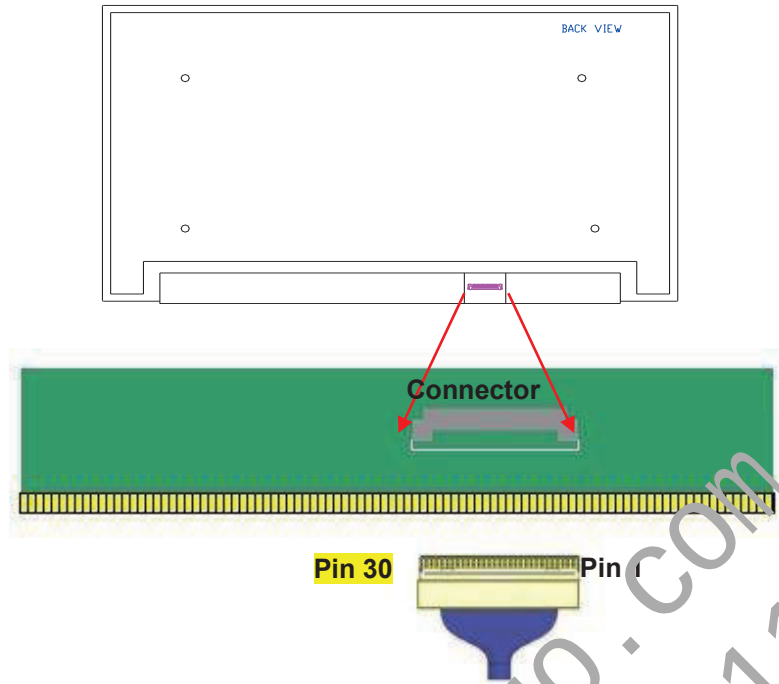
6.2.2 Pin Assignment (2 Lane)

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO.	Symbol	Function
1	NC	NC
2	H_GND	High Speed Ground
3	Lane1_N	Comp Signal Lane 1
4	Lane1_P	True Signal Link Lane 1
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver
14	LCD_Self_Test or NC	LCD Panel Self Test Enable (Optional)
15	LCD_GND	LCD logic and driver ground
16	LCD_GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	BL_GND	Backlight ground
19	BL_GND	Backlight ground
20	BL_GND	Backlight ground
21	BL_GND	Backlight ground
22	BL_Enable	Backlight On / Off
23	BL_PWM_DIM	System PWM signal Input
24	NC	EDID_CLK
25	NC	EDID_DATA
26	BL_PWR	Backlight power (5V~21V)
27	BL_PWR	Backlight power (5V~21V)
28	BL_PWR	Backlight power (5V~21V)
29	BL_PWR	Backlight power (5V~21V)
30	NC	NC

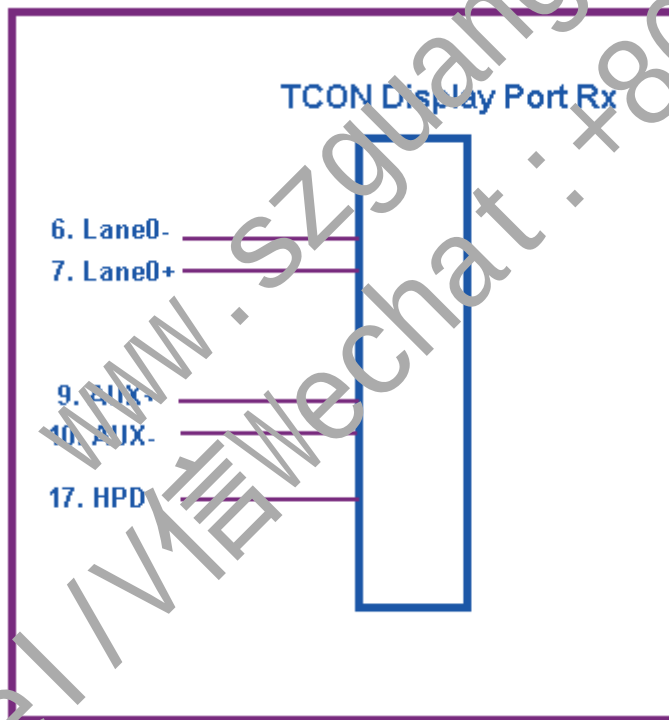
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Note1: Start from right side.

Note2: Input signals shall be low or High-impedance state when VDD is off.
Internal circuit of eDP inputs are as following.





6.3 Interface Timing

6.3.1 Timing Characteristics

For normal display, interface timings should match the 1920x1200 /60Hz manufacturing guide line timing.

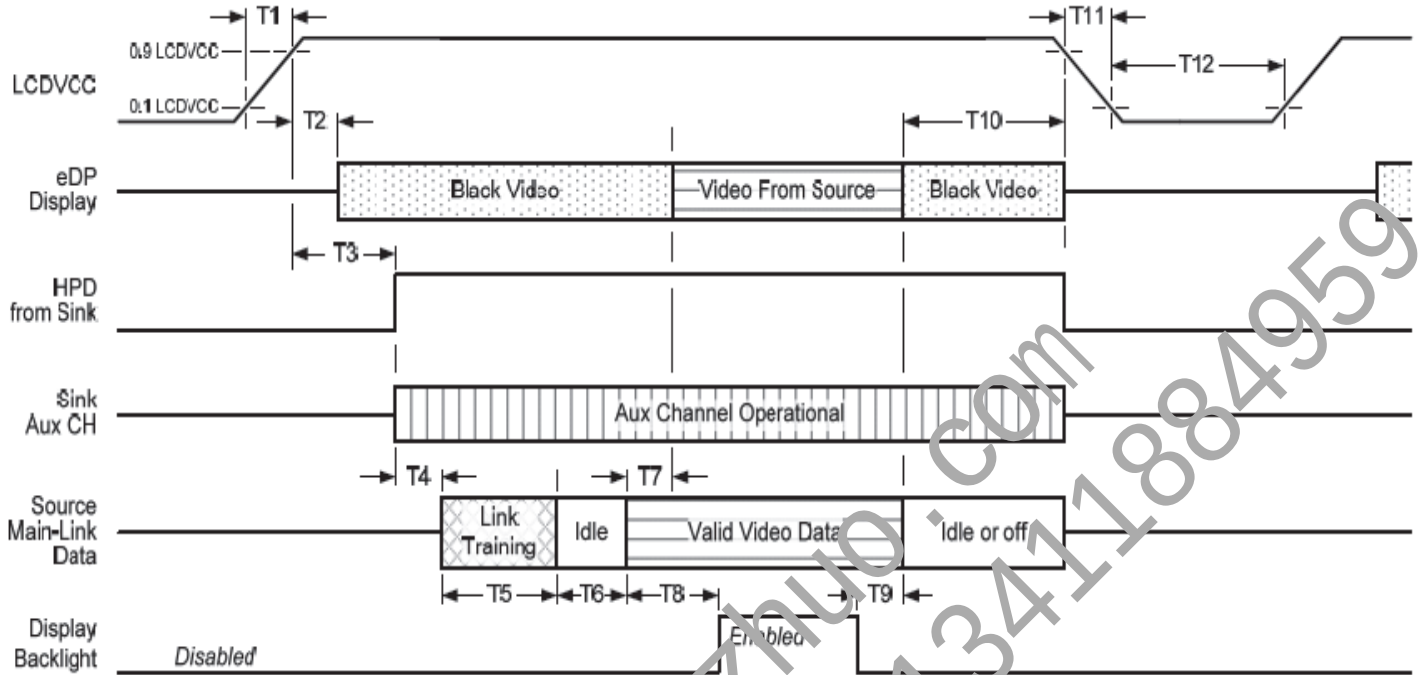
Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		1/ T _{Clock}	154.2	156.1	170	MHz
Vertical Section	Period	T _V	1235	1236	1200+A	T _{Line}
	Active	T _{VD}	1200			
	Blanking	T _{VB}	35	36	A	
Horizontal Section	Period	T _H	2080	2104	1920+B	T _{Clock}
	Active	T _{HD}	1920			
	Blanking	T _{HB}	160	184	B	

Note 1 : The above is as optimized setting

Note 2 : The maximum clock frequency = (1920+B)*(1200+A)*60<80MHz

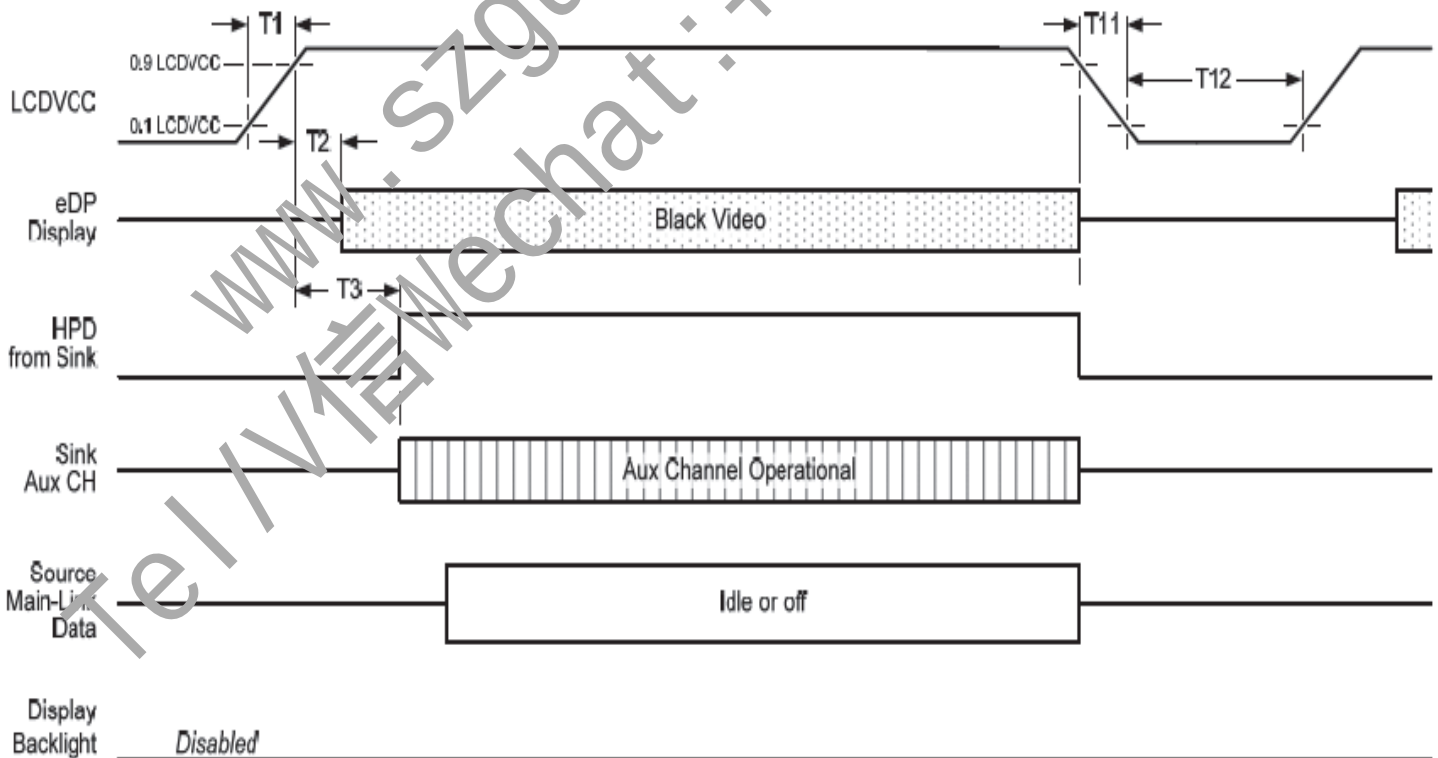
6.4 Power ON/OFF Sequence

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only.



Display port interface power up/down sequence, AUX_CH transaction only



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Display Port panel power sequence timing parameter:

Timing Parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	Power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	Delay from LCDVDD to black video generation	sink	0ms		eDP 1.2 =>200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		eDP 1.4 =>80ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize
T5	link training duration	source				dependent on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 90% to 10%	source			10ms	
T12	power off time	source	500ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:

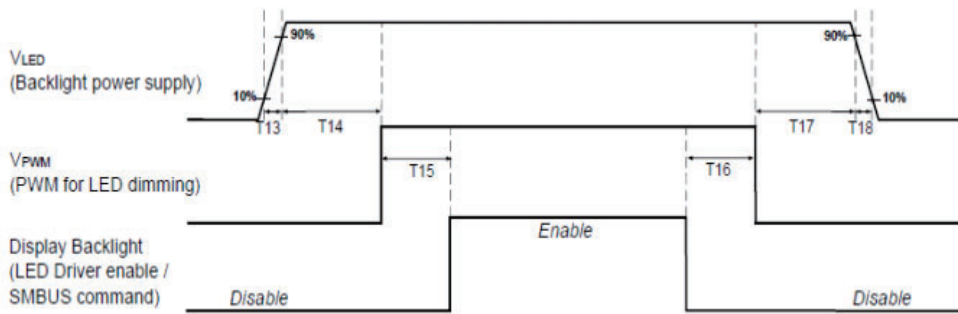
- upon LCDVDD power on (within T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
- When no valid link data or invalid video data is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

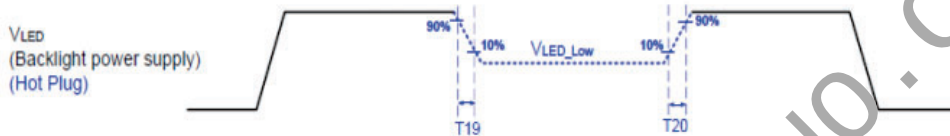
Note 4: T8>T7

Display Port panel B/L power sequence timing parameter:



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	0	-
T16	0	-
T17	10	-
T18	0.5	10
T19	-	-
T20	-	-

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



Seamless change: $T19/T20 = 5 \times T_{PWM}^*$
 $*T_{PWM} = 1/VPWM \text{ Frequency}$

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

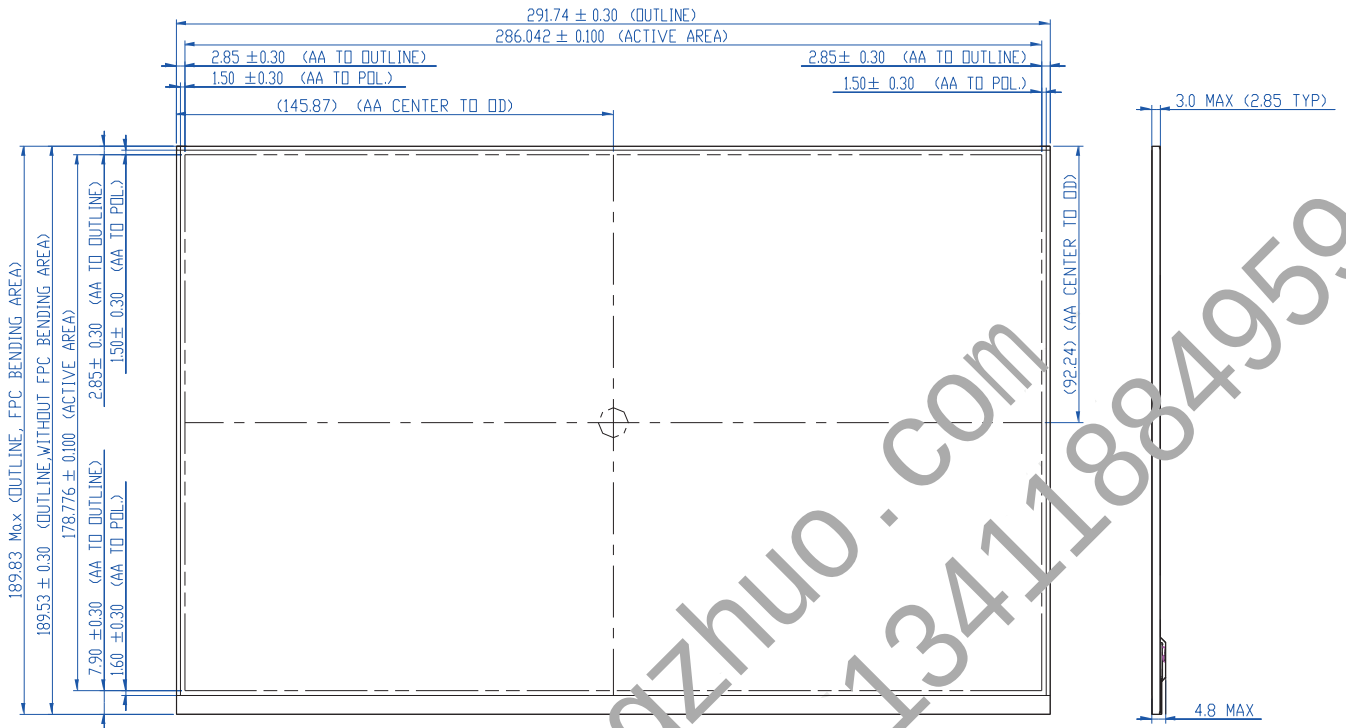
7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C, 90%RH, 300h	
High Temperature Operation	Ta= 50°C, Dry, 300h	
Low Temperature Operation	Ta= 0°C, 300h	
High Temperature Storage	Ta= 60°C, 300h	
Low Temperature Storage	Ta= -20°C, 250h	
Thermal Shock Test	Ta=-20°C to 60°C, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note 1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable, No data lost, No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

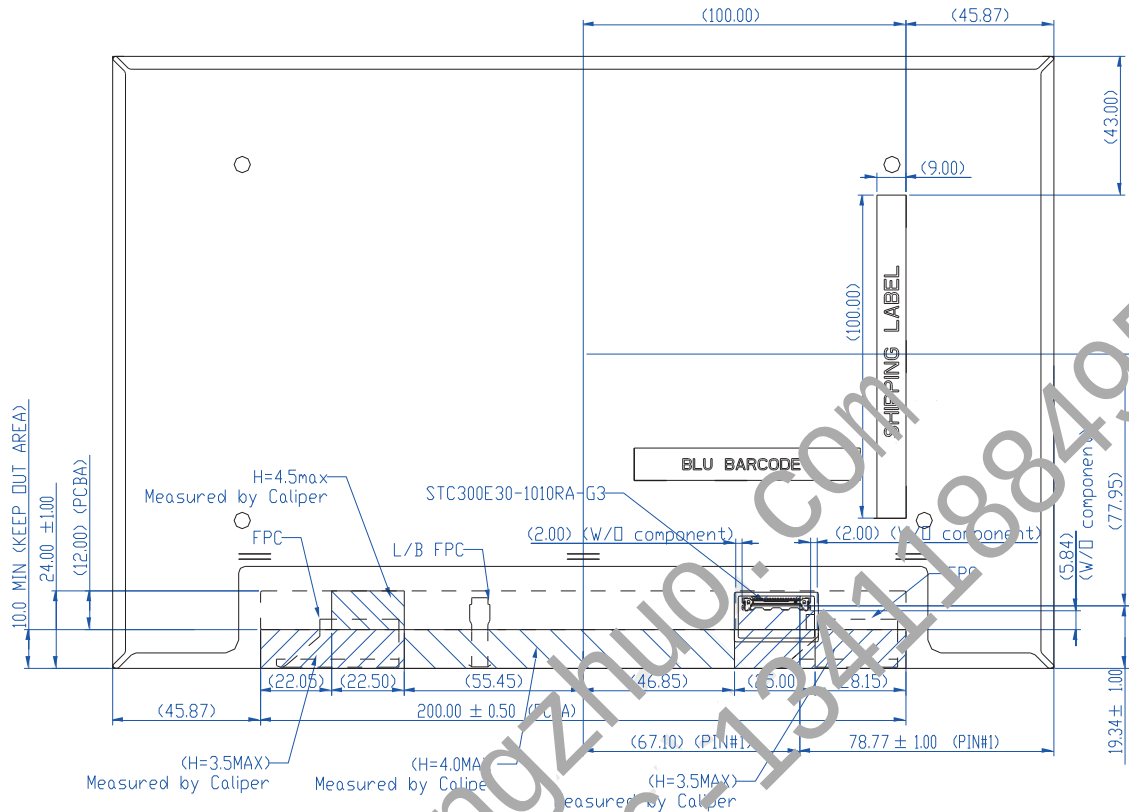




Product Specification

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8.1 LCM Outline Dimension



Note: Prevention IC damage, IC positions not allowed any overlap over these areas.



9. Shipping and Package

9.1 Shipping Label Format

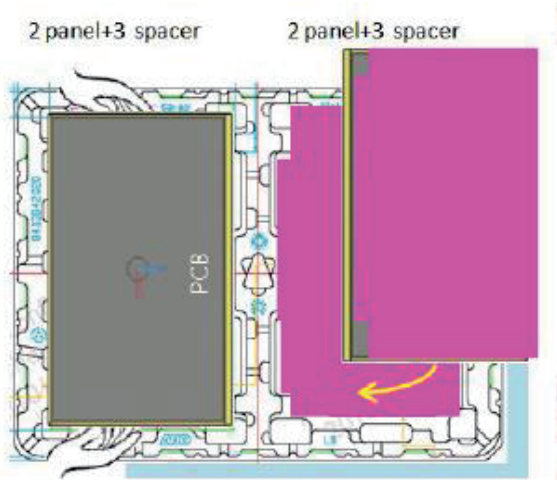
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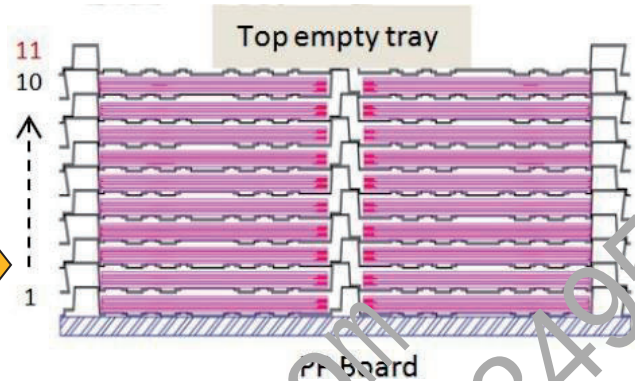
Product Specification

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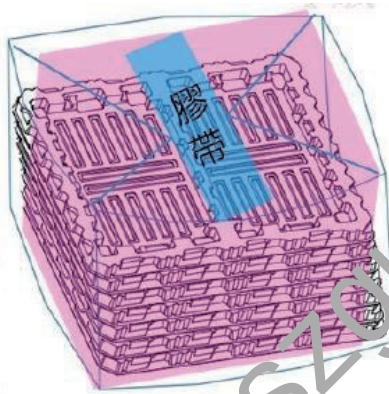
9.2 Carton Package



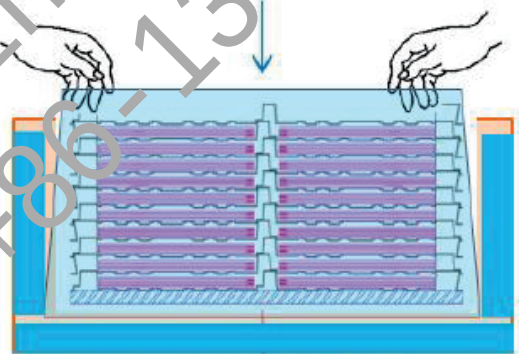
TRAY with 4 pcs Panel and 6 pcs spacer.



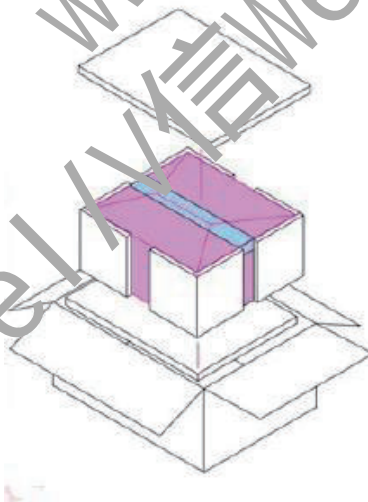
Following method packing 10 layer TRAY, each TRAY rotate 180 edge stack, Top stack empty TRAY, total 11 layer TRAY with 40 pcs Panels



All TRAY put into ESD bag, and close by tape.



Carton bottom be closed by tape, and then put EPE Cushion and esd bag into the carton.



Put top EPE pad



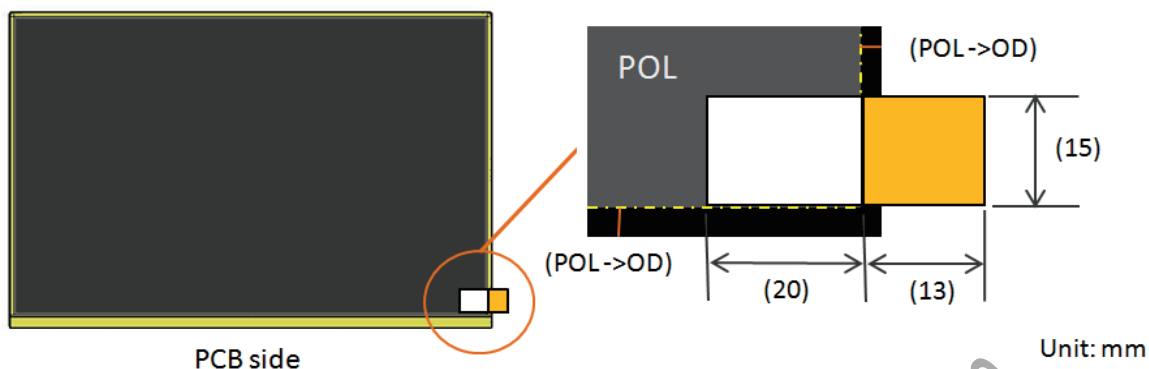
Carton be closed by tape, 40pcs/carton



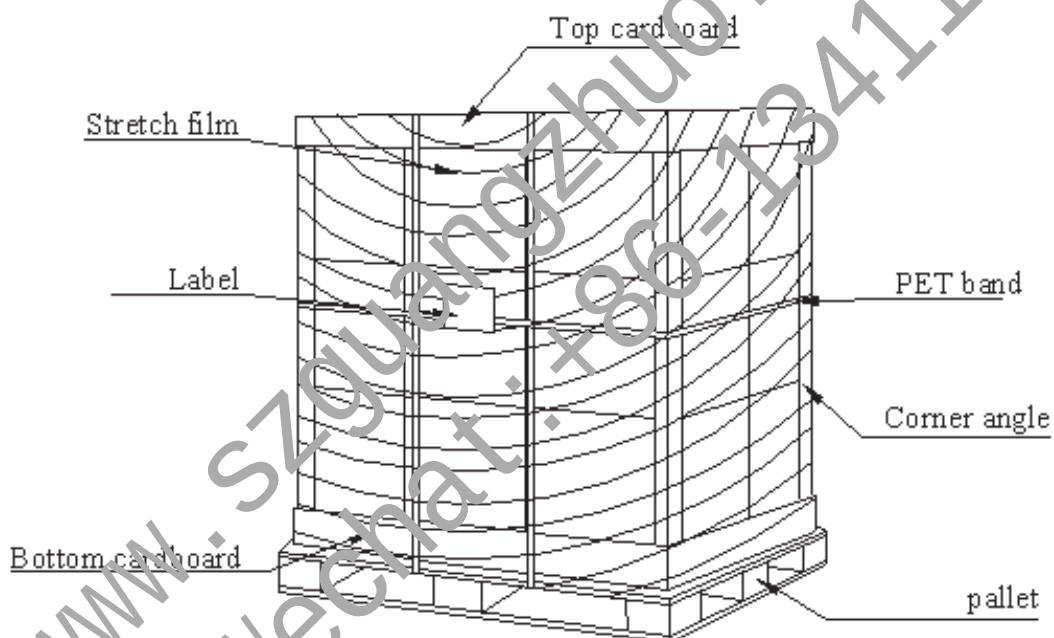
Product Specification

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Pull Bar Position:



9.3 Shipping Package of Palletizing Sequence





Product Specification

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10. Appendix:

10.1 EDID Description

TBD

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